Structure Silicon monolithic integrated circuit

Product Power management switch IC

Type **BD6528HFV**

Feature Single channel of low on resistance (Typ = 110mΩ) N-channel MOSFET built in

Reverse-current protection when power switch off

Output discharge circuit

◇Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	-0.3 ～ 6.0	V
VIN voltage	V_{IN}	-0.3 ～ 6.0	V
EN voltage	V_{EN}	-0.3 ～ V_{DD} + 0.3	V
VOUT voltage	V_{OUT}	-0.3 ～ 6.0	V
Storage temperature	T_{STG}	-55 ～ 150	℃
Power dissipation	Pd	849*1	mW

*1 Mounted on 70mm * 70mm * 1.6mm glass-epoxy PCB. Derating: 6.8mW/℃ above Ta = 25℃.

* This product is not designed for protection against radioactive rays.

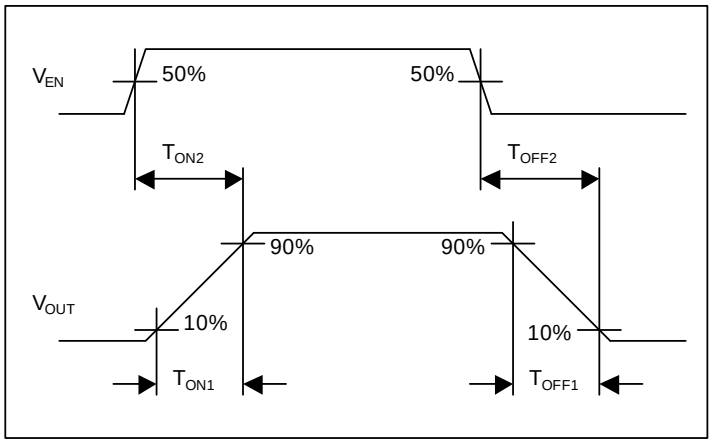
◇Operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating voltage	V_{DD}	2.7	-	4.5	V
Switch input voltage	V_{IN}	0	-	2.7	V
Operating temperature	T_{OPR}	-25	-	85	°C
Output current	I_{LO}	0	-	500	mA

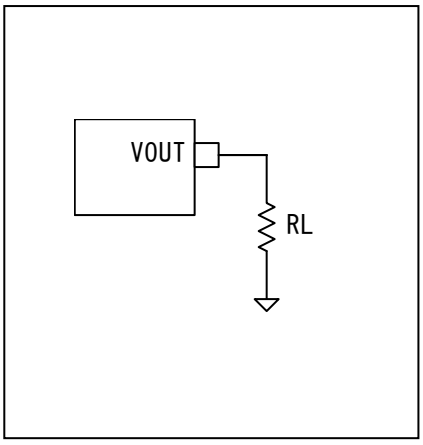
◇Electric characteristics (Unless otherwise specified, V_{DD} = 3.3V, V_{IN} = 1.2V, Ta = 25°C)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
Operating current	I_{DD}	-	20	30	μA	V_{EN} = 1.2V
Standby current	I_{STB}	-	0.01	1	μA	V_{EN} = 0V
EN input voltage	V_{ENH}	1.2	-	-	V	High level input
	V_{ENL}	-	-	0.4	V	Low level input
EN input current	I_{EN}	-1.0	-	1.0	μA	V_{EN} = 0V or V_{EN} = 1.2V
ON resistance	R_{ON}	-	110	-	mΩ	I_{OUT} = 500mA
Switch leakage current	I_{LEAK}	-	0.01	10	μA	V_{EN} = 0V, V_{OUT} = 0V
Output turn on rise time	T_{ON1}	-	0.5	1.0	ms	RL = 10Ω V_{OUT} :10% → 90%
Output turn on time	T_{ON2}	-	0.6	2.0	ms	RL = 10Ω V_{EN} High → V_{OUT} 90%
Output turn off fall time	T_{OFF1}	-	1	20	μs	RL = 10Ω V_{OUT} :90% → 10%
Output turn off time	T_{OFF2}	-	15	100	μs	RL = 10Ω V_{EN} Low → V_{OUT} 10%
Discharge ON resistance	R_{DISC}	-	70	110	Ω	I_{OUT} = -1mA, V_{EN} = 0V
Discharge current	I_{DISC}	-	15	20	mA	V_{OUT} = 3.3V, V_{EN} = 0V

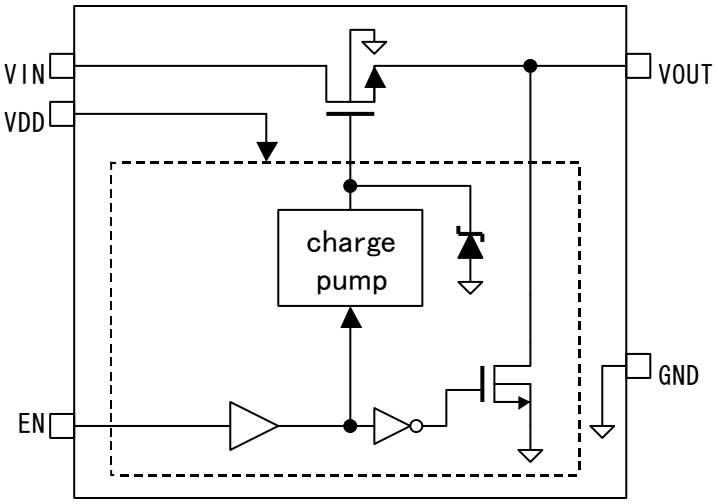
◇ Switch output turn ON/OFF timing



◇ Test circuit



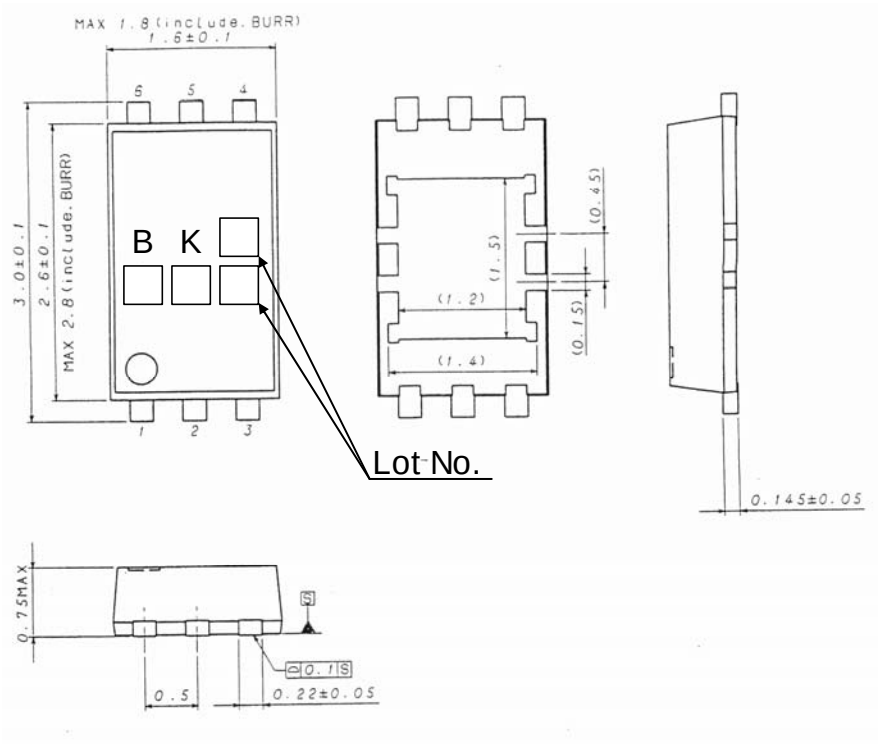
◇Block diagram



◇Pin number, Pin name

PIN number	Pin Name	Description
1	GND	Ground
2, 3	VOUT	Switch output
4	VIN	Switch input
5	VDD	Power supply
6	EN	Enable input

◇Package outline



HVSOF6 (Unit: mm)

○Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal design
Perform thermal design in which there are adequate margins by taking into account the power dissipation (PD) in actual states of use.

Notes

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