Rev 1; 1/09

MAXIM

Cache-Memory Battery-Backup Management IC

DS2731

General Description

The DS2731 is a complete power-management solution for modular backup applications. It is well-suited for 2.5V and below memory bus voltages, with an input voltage of 12V. The DS2731 includes an internal MOSFET switching power stage for charging a one-cell lithium chemistry battery. It has a fully integrated synchronous buck regulator capable of supplying up to 450mA of cache backup supply current, and the necessary logic and power devices for handling the switchover from system power to battery power. The battery charging method of the DS2731 is constant current/constant voltage (CCCV). Output voltage can be margined from 3.8V to 4.6V using a resistor-divider. Charge is terminated when the charging current falls below 5% of full charge current. Switchover to battery backup is initiated by an internal comparator and occurs automatically when a sensed-input voltage drops below 2.93V. At light loads, the 2MHz internal synchronous buck regulator operates in burst mode for maximum efficiency. All nonessential functions of the DS2731 are disabled while supplying holdup current to the cache memory, and the IC goes into very low-current dormant mode when the battery voltage drops below a user-settable threshold. The DS2731 keeps track of charge status and signals the user through open-drain I/O pins that can be used to drive LEDs.

Applications

RAID Controller Card

Features

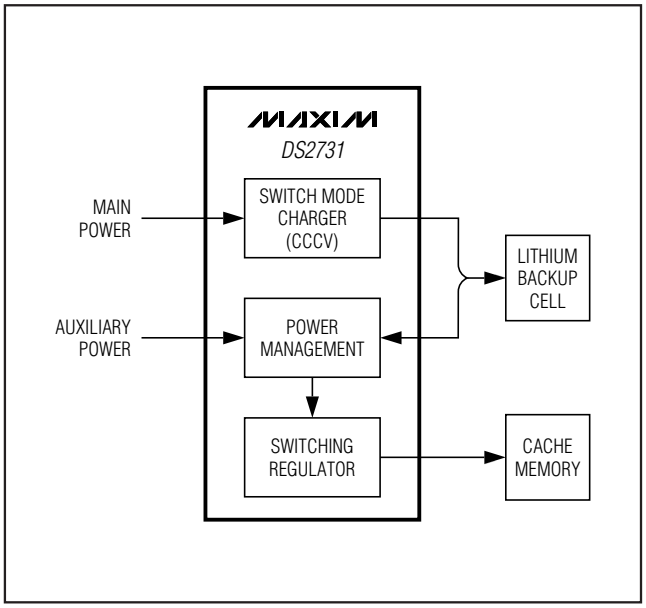
- ♦ **Lithium Chemistry CCCV Charger**
- ♦ **Adjustable Regulated Charging Up to 1.5A DC**
- ♦ **Adjustable Charge Voltage from 3.8V to 4.6V**
- ♦ **External and Internal Thermal Protection**
- ♦ **Safety Timer Secondary Termination**
- ♦ **LED Indicator Outputs**
- ♦ **Detects Power Outage and Switches Between Normal Power and Backup Battery**
- ♦ **Adjustable High-Efficiency Synchronous Buck Regulator with Skip Mode at Light Loads**
- ♦ **Low-Power Consumption in Discharge Mode**

Ordering Information

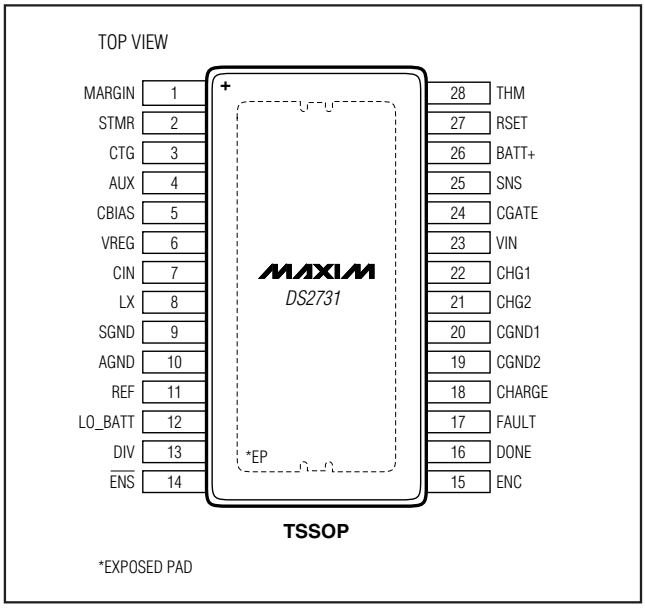
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS2731E+	-20°C to +70°C	28 TSSOP-EP* (173 mils)	DS2731
DS2731E+T&R	-20°C to +70°C	28 TSSOP-EP* (173 mils)	DS2731

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Typical Operating Circuit



Pin Configuration



Cache-Memory Battery-Backup Management IC

ABSOLUTE MAXIMUM RATINGS

Voltage Range on CGND1, CGND2, and SGND Pins Relative to AGND .....-0.3V to +0.3V
Voltage Range on VIN, CHG1, CHG2, and CGATE Pins Relative to AGND.....-0.3V to +16.0V
Voltage Range on CHARGE, FAULT, and DONE Pins Relative to AGND .....-0.3V to +16.0V
Voltage Range on Any Other Pin Relative to AGND .....-0.3V to +6.0V
Continuous Sink Current on VIN, CGND1, CGND2, SGND, AUX, BATT+ Pins .....750mA each
Continuous Source Current on CHG1, CHG2, and LX Pins.....750mA each
Continuous Sink Current on CHARGE, FAULT, and DONE Pins.....20mA each
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(V_{IN} = +10.8V to +13.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charger Supply Voltage	V_{IN}	(Note 1)	10.8	12.0	13.2	V
Auxiliary Supply Voltage	V_{AUX}	(Note 1)	3.0		3.6	V
Battery Voltage	V_{BATT+}	Operating as input (Note 1)	2.7		5.0	V
LED Voltage (CHARGE, FAULT, DONE Pins)		(Note 1)	0		V_{IN} + 0.3	V
Charger Enable (ENC)		(Notes 1, 2)	0		V_{CBIAS} + 0.3	V
Switcher Enable ($\overline{ENS}$)		(Notes 1, 2)	0		V_{CIN} + 0.3	V

CHARGER CIRCUIT ELECTRICAL CHARACTERISTICS

(V_{IN} = +10.8V to +13.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charger Idle Supply Current	I_{IN}	$V_{IN} > V_{UVLO-CHG}$ (Note 3), V_{AUX} = 3.3V		1		mA
Regulator Supply Current (Note 3)	I_{AUX}	$V_{AUX} > V_{TRIP}$		100		µA
	I_{BATT+}	$V_{AUX} < V_{TRIP}$, $V_{BATT+} > V_{SLEEP}$, $\overline{ENS}$ disabled		100	150	µA
	I_{SLEEP}	$V_{IN} = V_{AUX}$ = 0.0V, $V_{BATT+} < V_{SLEEP}$			10	µA
C_{BIAS} Regulator Voltage	V_{CBIAS}			3.3		V
C_{GATE} Regulator Voltage	V_{CGATE}			V_{IN} - 4.0		V
C_{GATE} Capacitance	C_{CGATE}		2.2			µF
C_{BIAS} Capacitance	C_{CBIAS}		0.22			µF
Enable Logic-Low ($\overline{ENS}$, ENC)	V_{IL}	(Notes 4, 5)			0.4	V
Enable Logic-High ($\overline{ENS}$, ENC)	V_{IH}	(Notes 5, 6)	1.6			V

CHARGER CIRCUIT ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +10.8V to +13.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable Hysteresis ($\overline{ENS}$, ENC)	V_{HYS-EN}		35	70	140	mV
Pulldown Resistance ($\overline{ENS}$, ENC)	R_{PD}		100	200	300	kΩ
LED Outputs Low (CHARGE, DONE, FAULT)	V_{OL}	I_{OL} = 10mA			1.0	V
Fault LED Flash Rate	f_{FAULT}			4		Hz
Preconditioning Charge Threshold	V_{MIN}	(Note 1)	2.55	2.60	2.70	V
Preconditioning Hysteresis	V_{HYS}		50	100		mV
Preconditioning Charge Current	I_{PRE}	$V_{BATT+} < V_{MIN}$	5.0	10.0	15.0	% of I_{CHG}
Precondition Timeout	t_{PRE}		27	30	33	min
Charge-Current Range (RSET Resistance)	I_{CHG}	Charge current determined by RSET (Note 7)	0.5		1.5	A
			5.0		1.6	kΩ
Charge-Current Accuracy	$I_{ERR-CHG}$	RSET resistor tolerance 0.1%, R_{SNS} = 0.050Ω	-5		+5	%
Overcurrent Clamp	$I_{OVERCURRENT}$	RSET = 0 or R_{SNS} = 0	1.7		2.5	A
Constant-Voltage Threshold Range	V_{CV}	Charge voltage determined by MARGIN pin voltage	3.6	4.2	4.6	V
MARGIN Pin Leakage	$I_{LEAKAGE}$		-2		+2	µA
Constant-Voltage Charge Accuracy	V_{ERR-CV}		-25.0		+25.0	mV
Charge Termination (CV) Current	$I_{TERMINATE}$	In constant-voltage mode	4.0	5.0	6.0	% of I_{CHG}
Charge-Restart Threshold	V_{DELTA}	(Note 8)	94	95	96	% of V_{CV}
Safety Timeout Range (STMR Resistance)	t_{SAFETY}		1		10	hr
			22		220	kΩ
Safety Timeout Error	$t_{ERR-SAFETY}$	R_{STMR} = 22,000Ω	-5		+5	%
Battery Charger Switching Period	t_{SW-CHG}	Full load (1.5A) (Note 9)	0.83	1.00		µs
Charger Undervoltage Lockout	$V_{UVLO-CHG}$		8		10	V
High-Side MOSFET On-Resistance	$R_{DSON-CP}$	I_{CHG} = 1A, V_{IN} = 10.8V (Note 10)			0.4	Ω
Low-Side MOSFET On-Resistance	$R_{DSON-CN}$	I_{CHG} = 1A, V_{IN} = 10.8V (Note 10)			0.15	Ω
Reverse Leakage of Charge FET (CHG1, CHG2)	$I_{REVERSE}$	V_{IN} = 0V, V_{CV} = 4.2V, ENC = 0V			10	µA
Forward Leakage of Charge FET (CHG1, CHG2)	$I_{FORWARD}$	V_{IN} = 12V, V_{CV} = 4.2V, ENC = 0V			10	µA
SNS Leakage Current	$I_{LKG-CHG}$	No charge current, V_{IN} = 12V	-2		+2	µA
Startup Time	t_{START}	Using typical application components		1		ms

BUCK REGULATOR AND POWER MUX CIRCUIT ELECTRICAL CHARACTERISTICS

(V_{IN} = +10.8V to +13.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Input Trip Threshold	V_{TRIP}	(Note 1)	2.85	2.93	3.00	V
Auxiliary Input Trip Hysteresis	$V_{HYS-TRIP}$	Relative to actual V_{TRIP}	50	80	150	mV
Multiplexer Delay Break-Before-Make	t_{BREAK}	Switching to/from BATT+ (Note 11)			1	µs
Power Multiplexer On-Resistance	R_{MUX}	I_{MUX} = 10mA, BATT+ or AUX source		0.6	1.0	Ω
Regulator Output Voltage Range	V_{REG}	Set by V_{DIV} pin voltage	0.9		2.5	V
DIV Pin Voltage Range	V_{DIV}		0.4		V_{REF}	V
Regulator Output Voltage Error	$V_{ERR-REG}$	(Note 9)	-5.0		+5.0	%
Low-Battery Threshold Adjustment Range	V_{SLEEP}		2.75		3.00	V
LO_BATT Pin Voltage Range	$V_{LO-BATT}$		0.6		V_{REF}	V
V_{REF} Voltage	V_{REF}		1.220	1.238	1.260	V
V_{REF} Load Range (Equivalent Resistance)	I_{REF}		1.22		126.00	µA
			1000		10	kΩ
Buck Regulator Switching Period	t_{SW-REG}	50mA (Note 9)		500		ns
Regulator Undervoltage Lockout	$V_{UVLO-REG}$		2.45		2.70	V
Switching Power pFET Resistance	$R_{DSON-SP}$	I_{OUT} = 100mADC BATT+ = 3.0V, V_{AUX} = 0 (Note 10)			0.6	Ω
Switching Power nFET Resistance	$R_{DSON-SN}$	I_{OUT} = 100mADC BATT+ = 3.0V, V_{AUX} = 0 (Note 10)			1.2	Ω
nFET Off Threshold	I_{OFFN}		0	40	80	mA
Switching Power pFET Overcurrent Limit	I_{OCLP}		500	750	1000	mA
Switching Power nFET Overcurrent Limit	I_{OCLN}		400	650	900	mA
VREG Pin Leakage	$I_{LKG-REG}$		-2		+2	µA

THERMAL PROTECTION CHARACTERISTICS

(V_{IN} = +10.8V to +13.2V, T_A = -20°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THM Pin Internal Pullup Voltage	V_{THM}	(Notes 1, 12)		V_{CBIAS}		V
THM Pin Internal Resistance	R_{THM}	THM to C_{BIAS} (Note 12)	9.8	10.0	10.2	kΩ
Thermistor Overtemperature HALT Threshold	V_{HOT}	(Notes 12, 13)	0.271	0.283	0.292	Ratio to V_{CBIAS}
Thermistor Overtemperature Resume Threshold	$V_{HYS-HOT}$	(Notes 12, 13)		0.3055		Ratio to V_{CBIAS}
Thermistor Undertemperature HALT Threshold	V_{COLD}	(Notes 12, 13)	0.727	0.739	0.748	Ratio to V_{CBIAS}
Thermistor Undertemperature Resume Threshold	$V_{HYS-COLD}$	(Notes 12, 13)		0.714		Ratio to V_{CBIAS}
Thermistor Disable Threshold	$V_{DISABLE}$	(Notes 12, 13)	0.02	0.03	0.04	Ratio to V_{CBIAS}
Internal Overtemperature Protection Threshold CCCV	$T_{PROTECT\_CCCV}$	(Note 12)		160		°C
Internal Overtemperature Hysteresis CCCV	$T_{HYS-PROTECT\_CCCV}$	(Note 12)		-20		°C
Internal Overtemperature Protection Threshold MEM_REG	$T_{PROTECT\_MEMREG}$	(Note 14)		165		°C
Internal Overtemperature Hysteresis MEM_REG	$T_{HYS-PROTECT\_MEMREG}$	(Note 14)		-15		°C
Charging Current Reduction Threshold	T_{CHOKE}	(Note 12)		100		°C
Charging Current Reduction Rate	T_{CHOKE_RATE}	(Note 12)		133		mA/°C

Note 1: All voltages referenced to AGND pin.

Note 2: V_{CIN} is equivalent to V_{AUX} when V_{AUX} is greater than V_{TRIP}, otherwise V_{CIN} is equivalent to V_{BATT+}.

Note 3: Supply-current specification is only for current drain of the IC and does not include cell-charge current, load-supply current, or any external resistor bias currents. The only exception is I_{SLEEP}, which does account for complete current drain of the lithium cell during low-battery conditions.

Note 4: Below this voltage, the input is guaranteed to be logic-low.

Note 5: Operating from 3.3V ±10%.

Note 6: Above this voltage, the input is guaranteed to be logic-high.

Note 7: Assumes an R_{SNS} value of 0.05Ω.

Note 8: Relative to V_{CV}.

Note 9: With recommended application circuit.

Note 10: Includes complete package resistance.

Note 11: This specification is from the rising or falling edge of $\overline{ENS}$ to the closure of the switch and includes whatever delay is in the internal logic and FET drivers.

Note 12: Applies to charger.

Note 13: Multiply these values by C_{BIAS} voltage to get value in volts. Recommended value of resistor in divider network is 10kΩ ±1%. Tolerance includes tolerances of internal resistance and C_{BIAS} voltage.

Note 14: Applies to memory buck regulator.

Cache-Memory Battery-Backup Management IC

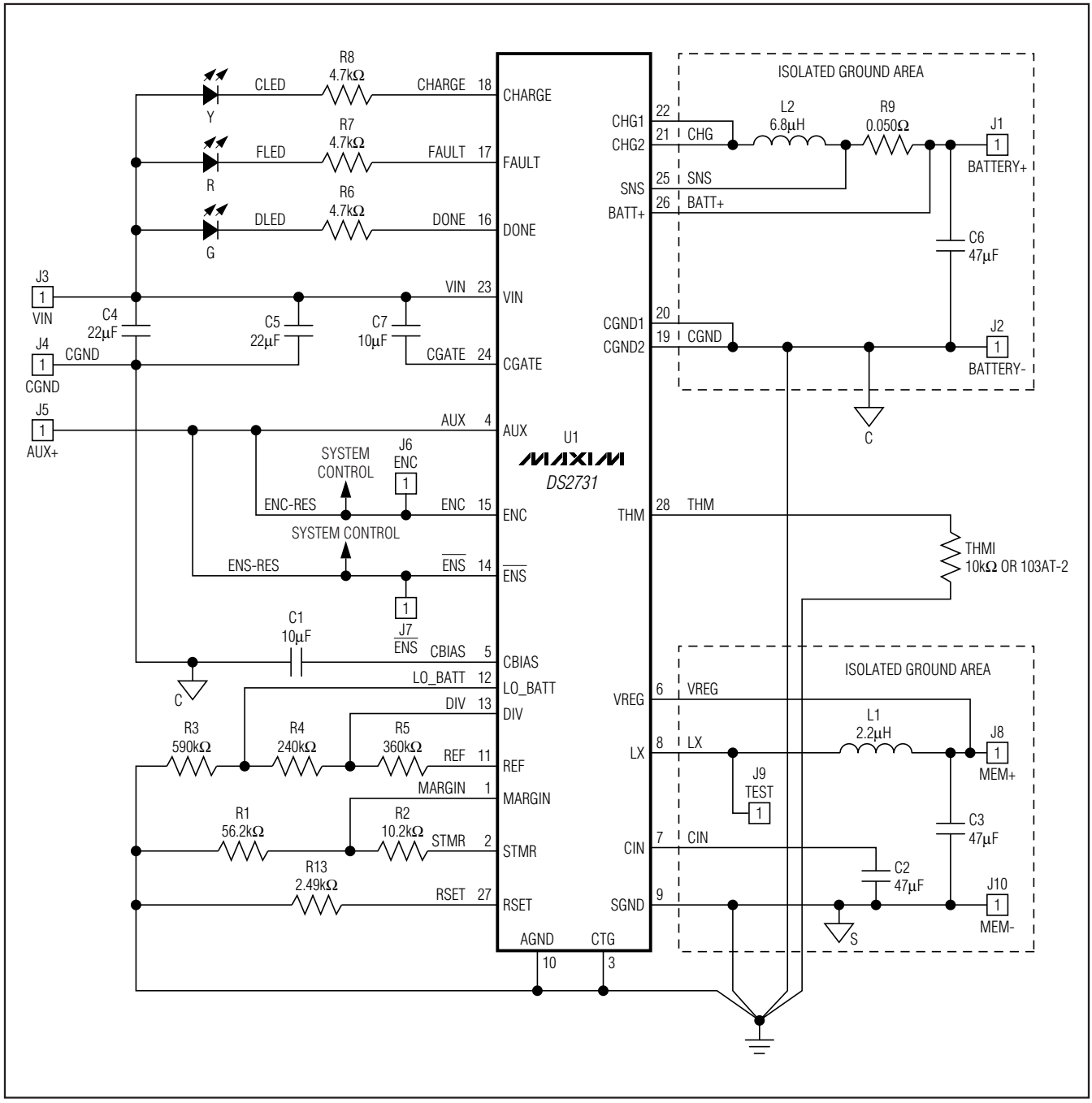


Figure 1. Typical Application Diagram

Pin Description

PIN	NAME	FUNCTION
1	MARGIN	Voltage-Margining Input. Selects regulation voltage of charging circuit. Connect to the STMR pin through a resistor-divider.
2	STMR	Voltage Safety-Timer Input. Sets timeout period for a charge cycle based on external resistance to AGND.
3	CTG	Connect To Ground. Must be connected to AGND externally.
4	AUX	Auxiliary. External supply input to switching supply. Connect to system 3.3V supply.
5	CBIAS	Internal Regulator Output. Internal supply for the charging circuit generated from the V_{IN} input. Bypass with a capacitor to AGND.
6	VREG	Cache Voltage-Sense Input. Feedback for regulation of the switching circuit voltage. Connect to the positive side of the switching output load.
7	CIN	Holdup/Bypass Capacitor. Internal supply for the switching regulator. Bypass with a 4.7µF capacitor to AGND.
8	LX	Switching Node, Backup Supply. Output from the switching regulator. Connect to the switching regulator's external coil.
9	SGND	Switcher Ground. Ground reference for the switching regulator. Connect to the negative side of the load.
10	AGND	Analog Ground. Ground reference for the charging circuit. Connect to the negative side of the battery.
11	REF	Voltage Reference for Backup. 1.238V voltage reference used to set regulation voltage and low-battery-detection threshold. Connect to AGND through a resistor network.
12	LO_BATT	Low-Battery Detection. Selects the low-battery shutdown threshold of the switching regulator. Connect to the REF pin through a resistor-divider.
13	DIV	Voltage Divider for Backup. Controls the voltage output level of the switching regulator. Connect to the REF pin through a resistor-divider.
14	$\overline{ENS}$	Enable Switcher. Active-low enable for the switching regulator.
15	ENC	Enable Charger. Active-high enable for the charging circuit.
16	DONE	Charge-Done Indicator. Open-drain active-low output indicating successful charge completion of the external cell.
17	FAULT	Charger-Fault Indicator. Open-drain active-low output indicating failure during charge of the external cell.
18	CHARGE	Charge Indicator. Open-drain active-low output indicating charge of the external cell in progress.
19	CGND2	Charger Ground 2. Ground reference for battery-charging circuit. Connect to negative side of external cell.
20	CGND1	Charger Ground 1. Ground reference for battery-charging circuit. Connect to negative side of external cell.
21	CHG2	High-Current Charger Output 2. Output from the charging circuit. Connect to charging circuit's external coil.
22	CHG1	High-Current Charger Output 1. Output from the charging circuit. Connect to charging circuit's external coil.
23	VIN	Charge-Supply Input. Connect to 10.8V to 13.2V system supply.
24	CGATE	Floating Gate Drive Bypass. Internal supply for the charger gate control. Bypass with a 2.2µF capacitor to VIN.
25	SNS	Current-Sense Input. Feedback for regulator of charger current. Connect a 0.050Ω sense resistor between SNS and BATT+.
26	BATT+	Battery Terminal Voltage. Feedback for regulation of charger voltage and supply to switching regulator during power loss.
27	RSET	Charge-Setting Resistor Intput. Selects CC charge rate for external lithium cell. Connect to AGND through an external resistor.
28	THM	Thermistor Input. Connect to 10kΩ NTC thermistor with good thermal contact to the external lithium cell.
—	EP	Exposed Paddle. It is recommended the exposed pad be connected to system ground.

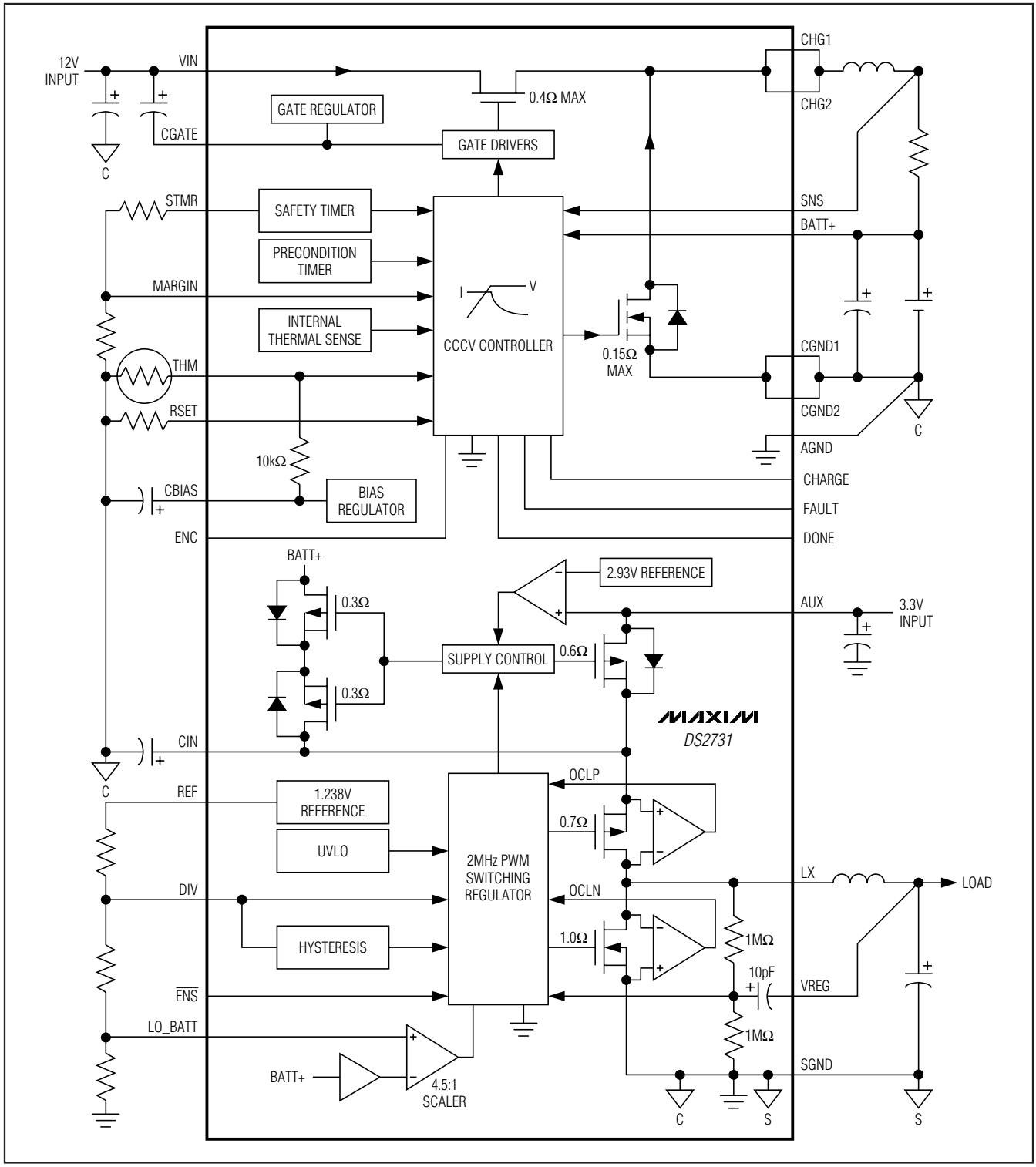


Figure 2. Block Diagram

Detailed Description

The DS2731 is a complete power-management solution for modular backup applications. It is well suited for 2.5V and below memory bus voltages. It has a 12V supply input for battery charging and a 3.3V aux supply input for power failure circuitry and memory voltage regulation. The DS2731 includes an internal MOSFET-switching power stage for charging a lithium-ion (Li+) cell. It has a fully integrated synchronous-buck regulator capable of supplying up to 450mA of cache-backup supply current. It also handles switching from system power to battery power.

The battery-charging method is CCCV. Charging can be broken into three different modes: precondition, constant-current (CC) charge, and constant-voltage (CV) charge. Precondition mode charges at a reduced rate for a severely depleted cell. CC mode charge rate is user selectable from 0.5A to 1.5A. In CV mode, charge is terminated when the charging current falls below 5% of CC mode charge rate. The CV mode output is also user selectable from 3.8V to 4.6V. Charge status is signaled to the user through three open-drain pins that can be used to drive LEDs. A thermistor input is provided to prevent charging outside of temperature specifications and a safety timer prevents the continued charging of a damaged cell.

Switchover to battery backup is initiated by an internal comparator and occurs automatically when a sensed input voltage drops below 2.93V. The power failure switching circuitry can be disabled by the user. Memory voltage is user selectable from 0.9V to 2.5V. At light loads, the 2MHz internal synchronous buck regulator operates in burst mode for maximum efficiency. All nonessential functions of the DS2731 are disabled during a power failure while supplying holdup current to the cache memory. To prevent damaging the battery, the regulator shuts down and the IC goes into a very low-current dormant mode when the battery voltage drops below a user-settable threshold (LO_BATT).

Li+ Charger

The CCCV charger circuitry is powered by the 12V input supply. When the charger circuitry is enabled, battery voltage is continuously monitored at the BATT+ pin. Charging begins when the battery voltage drops below the charge restart threshold. Accurate charge current measurements are achieved by the Kelvin remote-sense connections at the SNS and BATT+ pins. Measuring the voltage through a Kelvin remote-sense connection eliminates offset error caused by small trace resistances at high current.

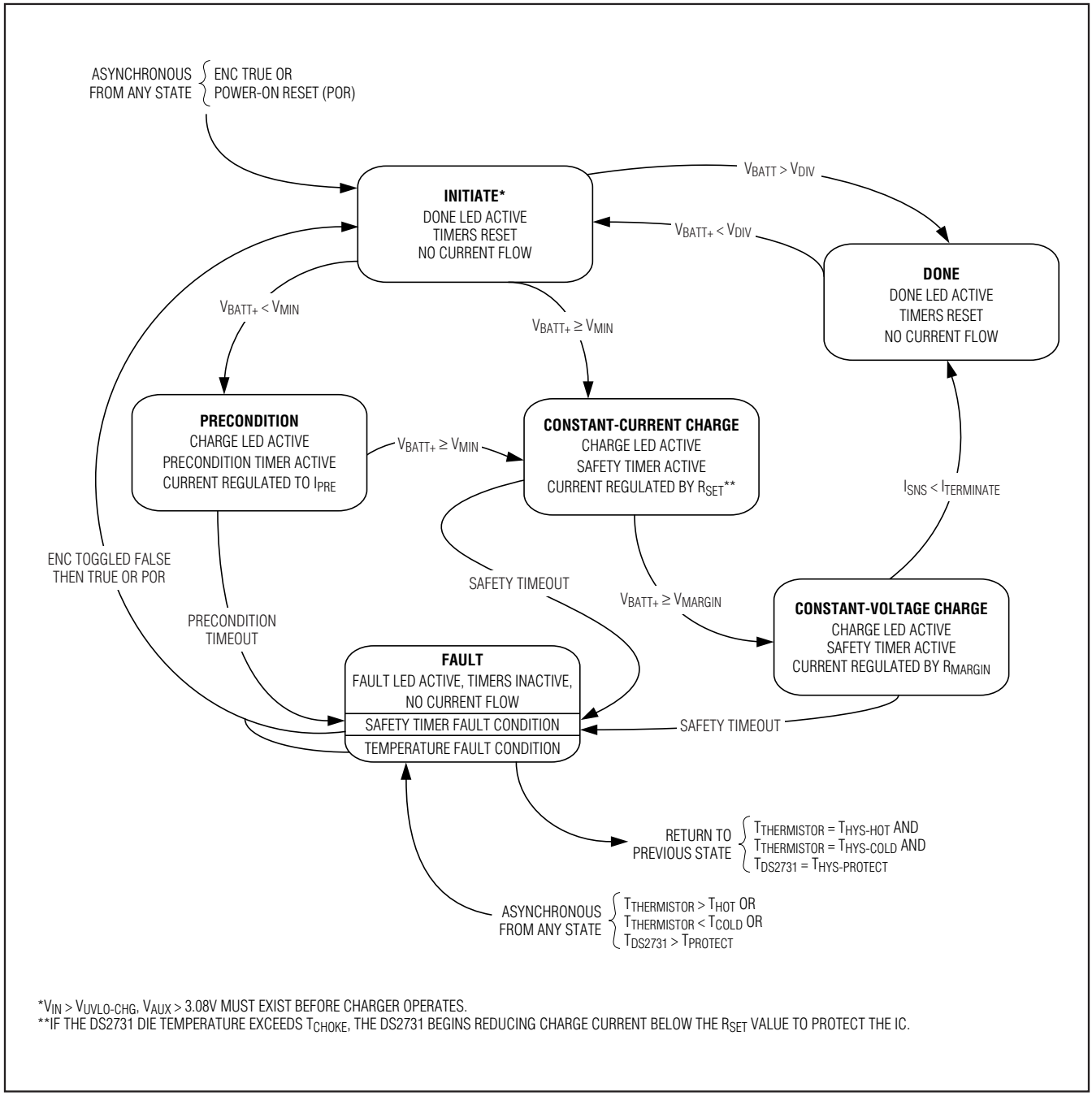
Charging Algorithm

From initiate, CC charging proceeds if ENC is high, the UVLO-CHG is false, the die temperature is below $T_{PROTECT\_CCCV}$, and the battery is above the minimum voltage. If the battery is below the minimum voltage, the charger goes into preconditioning charge. Once the battery voltage exceeds V_{MIN}, the charger proceeds to CC mode. Precondition charge has a default 30-minute timer. If the timer expires before the battery voltage exceeds V_{MIN}, the charger goes to fault. For CC charging, the charge safety timer starts. CC charging proceeds until the output voltage reaches the CV set point. The charger then proceeds to CV mode. Charging terminates when the current drops below 5% of the CC charge rate. The charge-safety timer duration is the sum of the CC and CV charge times and should be set to about 15% above the expected maximum charge time. If the charge-safety timer expires, the charger goes to fault. After charge termination, the charger monitors the battery voltage for self-discharge. When it drops 200mV below the CV charge threshold, the charger enters Initiate and a new charge cycle begins.

Note: V_{AUX} must be above 3.08V for the charger to operate.

Precharge Mode

Precharge mode is intended to restore severely depleted cells. Batteries with a voltage < V_{MIN} charge at a reduced rate, 10% x I_{CHG}, to prevent damaging the cell. Precharge mode has a fixed safety timer of 30 minutes. This timer is independent of the STMR pin. If the battery voltage has not exceeded V_{MIN} within 30 minutes, the charger goes to the fault state. The charge pin is active during precharge mode.



*V_{IN} > $V_{UVLO-CHG}$, V_{AUX} > 3.08V MUST EXIST BEFORE CHARGER OPERATES.
**IF THE DS2731 DIE TEMPERATURE EXCEEDS T_{CHOKE}, THE DS2731 BEGINS REDUCING CHARGE CURRENT BELOW THE R_{SET} VALUE TO PROTECT THE IC.

Figure 3. Charger State Diagram

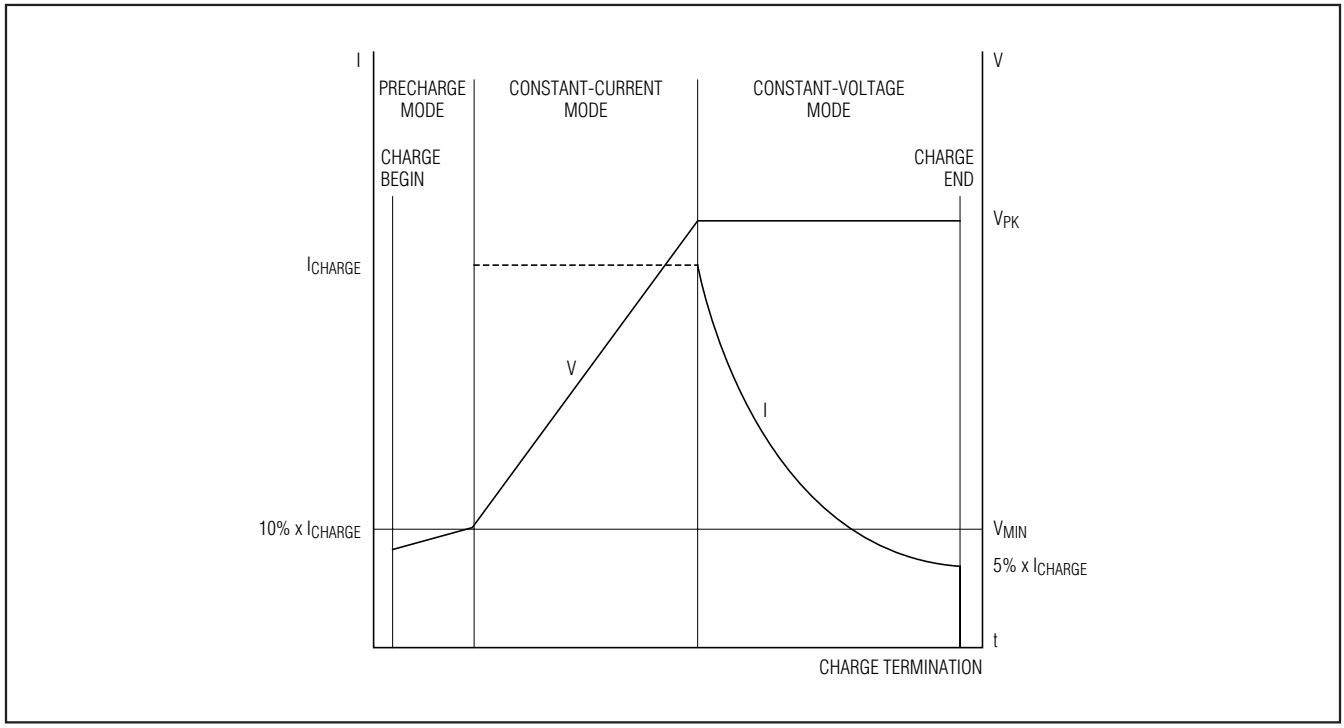


Figure 4. Li+ Battery Charging Characteristics

Constant-Current (CC) Mode

CC mode is entered either directly from initiate or after precharge. Current is regulated based on the voltage drop across an external 50mΩ sense resistor and an internal feedback circuit. The CC charge rate is set by the RSET pin. It can be calculated by the following formula:

$$I_{CHARGE} = 2500/R$$

Where R is the value of the resistor connected to RSET. The charge current can range from 0.5A to 1.5A.

The safety timer begins when CC mode is entered. If it expires during CC mode, the charger enters a fault state. If the current-sense feedback or RSET resistor is shorted, the charger clamps current at $I_{OVERCURRENT}$.

Li+ Charger CC Operation Detailed Description

In CC mode, the CCCV charger regulates current by monitoring the voltage drop across the SNS resistor. The differential voltage measurement provides feedback that controls the switching of the high-side and low-side FETs. Inside the DS2731 CHG1 and CHG2 pins are a high-side p-channel MOSFET (Q1) and a low-side n-channel MOSFET (Q2). Q1 and Q2 alternate on and off, either supplying current to the load and inductor or providing a current loop for the inductor to supply the load. The inductor charges during Q1 ON and discharges during Q2 ON. The Q1 and Q2 switching is controlled by the voltage across R_{SNS}.

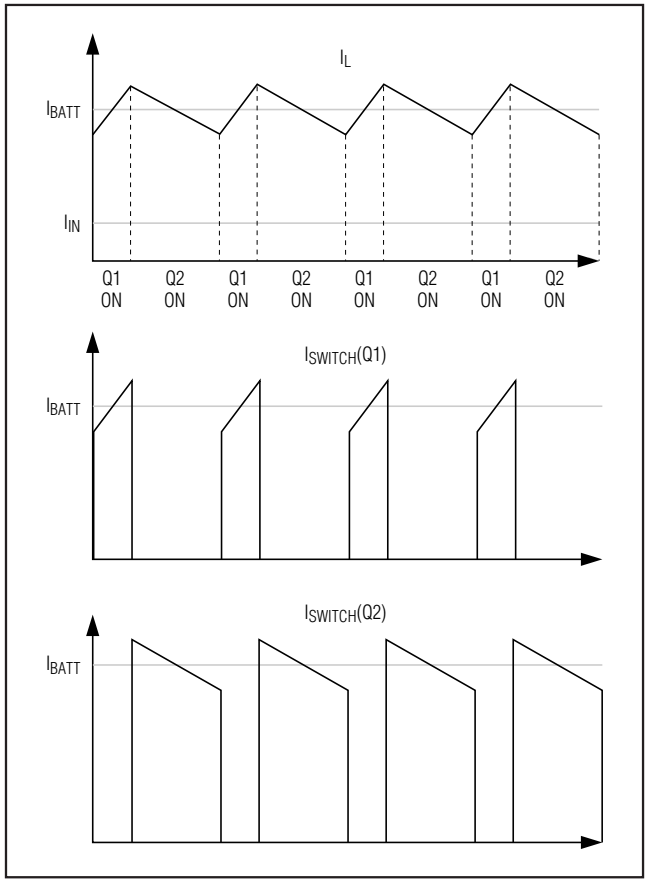


Figure 5. Li+ Battery Charger CC Operation Characteristics

The current in the inductor is a combination of the current in Q1 and Q2. The voltage on the inductor is higher during Q1 ON than Q2 ON. This allows the current in the inductor to remain continuous because the *power-in* approximately equals the *power-out*.

Constant-Voltage (CV) Mode

CV mode is entered after CC mode when the battery voltage reaches the CV output threshold. Battery voltage is measured at the BATT+ pin. When the voltage reaches the CV threshold set by the MARGIN pin, regulation goes from CC mode to CV mode. Charge termination occurs when the current drops below 5% of the CC charge rate.

The MARGIN pin sets the CV threshold according to the following formula:

$$V_{PK}\ (\text{CV Set Point}) = 4.97V \times R1/(R2 + R1)$$

Where R2 is the resistor between STMR and MARGIN, and R1 is the resistor between MARGIN and ground. Voltage regulation can be set from 3.8V to 4.6V. If the safety timer expires during CV mode the charger enters the fault state. A fault that occurs in CV mode, once cleared, causes the charger to transition to done. Charge resumes if/when the battery voltage collapses to 95% (V_{DELTA}) of the CV threshold.

Fault Conditions

There are several types of fault conditions that can occur. The precondition timer or safety timer can expire and the charger enters the fault state. This fault condition must be cleared by power cycling the part or toggling ENC. If the temperate exceeds the hot or cold limits, the charger enters fault. In the case of a temperature fault, charging resumes once the temperature returns to the normal operation range unless the fault occurs in CV mode. If a fault occurs in CV mode, the charger sees a charge termination condition because the current has dropped below 5% x I_{CHG}. Once the fault condition is removed the charger transitions to done. The charger remains in the done state unless the cell voltage collapses below 95% (V_{DELTA}) of the CV threshold.

Thermal Protection

The charger circuitry has a shutdown feature that pauses charging if the internal die temperature exceeds 160°C. Charging resumes after the temperature has cooled 20°C below 160°C. The charger circuitry is also equipped with a temperature choke point. If the die temperature reaches 100°C, the CCCV charger begins to choke the current 133mA/°C above 100°C. The choke continues down to 0mA if the temperature continues to increase. These thermal-regulation features operate independent of the thermistor input.

Enable Charger

The ENC pin is an active-high input that enables the charger. When enabled, the DS2731 performs battery qualification and begins charging using the CCCV algorithm. Toggling ENC resets charge timers and clears fault conditions. Any time ENC is low, the DS2731 charging circuitry is disabled and the high-side switch is guaranteed to be off. No current can flow from the battery to the VIN pin when the charger is off.

Safety Timer

The charger has a safety timer that controls the maximum length of time for a charge cycle. It is user selectable from 1 to 10 hours. If this timer expires and the battery has failed to reach the termination current, the charger enters the fault state and is latched off. Charging does not continue until either power is cycled or the ENC pin is strobed low and then high again. The timer does not start until CC mode is entered and continues through CV mode. Precharge mode is not included in the STMR.

Timing Equation:

$0.1647 \times R_{STMR} = t$ (in seconds); $R_{STMR} = R1 + R2$

Where R1 is the resistor from MARGIN to ground and R2 is the resistor from STMR to MARGIN.

Thermistor Input

Battery temperature can be monitored using an external thermistor. The THM input goes to a comparator and is pulled up internally by a 10kΩ resistor. The voltage on this pin must be above $V_{HYS-HOT}$ and below $V_{HYS-COLD}$ in order to start charging. Thermistor functionality can be disabled by grounding the THM pin and charging is independent of temperature. During charging, if the voltage on the THM pin goes below V_{HOT} volts, the charger pauses until the voltage rises above $V_{HYS-HOT}$ volts. Also, if the voltage on the THM pin goes above V_{COLD} volts, the charger pauses until the voltage falls below $V_{HYS-COLD}$ volts. All timers pause while charging is interrupted and resume when the temperature returns to the valid range. The charger enters the fault state when an overtemperature or undertemperature condition occurs. A 10kΩ NTC thermistor is recommended for this pin.

Charge Status Indicators

The CHARGE, FAULT, and DONE pins can be used as digital discretes or as LED drivers; they are open drain. When charging, the CHARGE pin is held low. When the charger detects a full battery/termination condition, $I_{TERMINATE}$, the DONE pin goes low and the CHARGE pin goes high impedance. Any charging fault (overtemperature or expiration of the safety timer) causes the FAULT pin to flash at a 4Hz rate and the CHARGE and DONE pins go high impedance. The FAULT pin stays on solid, not flash, if the fault occurs in CV mode.

Table 1. Thermistor Threshold

THM THRESHOLD	RATIO OF C_{BIAS}	THERMISTOR RESISTANCE (kΩ)	TEMPERATURE (°C)	
			SEMITEC 103AT-2	FENWAL 197-103LAG-A01 173-103LAF-301
COLD	0.739	27.040	0	4
HOT	0.283	4.925	45	42
DISABLE	0.030	—	—	—

Table 2. Charge Status Indicator Description

CONDITION	CHARGE PIN	DONE PIN	FAULT PIN	COMMENT
Precharge	Low	High-Z	High-Z	—
Battery Charged	High-Z	Low	High-Z	(Done)
Fault	High-Z	High-Z	Blinking	50% DF, 4Hz rate; low if fault occurs during CV mode.
Charger Disabled	High-Z	High-Z	High-Z	—

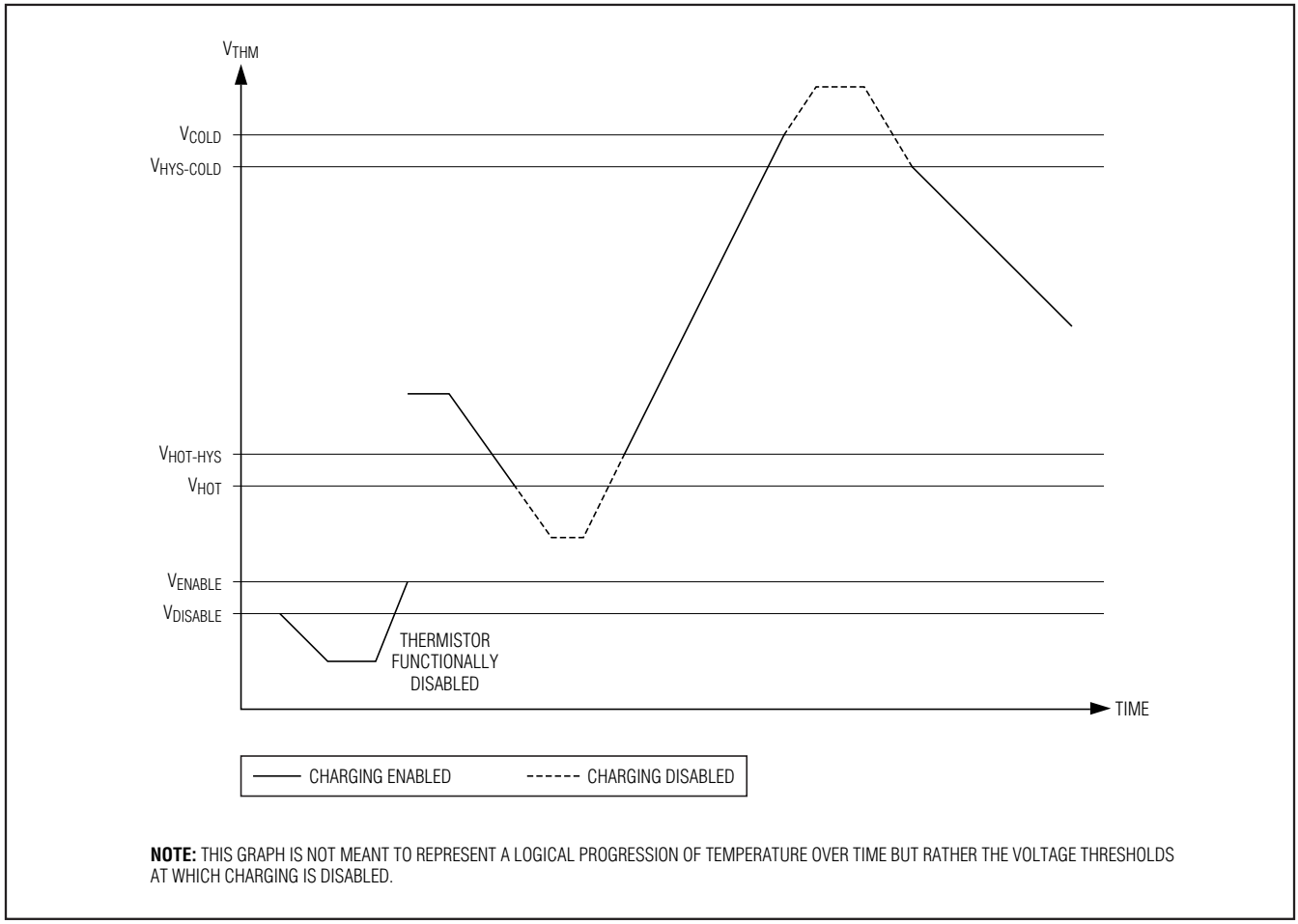


Figure 6. Temperature Operation

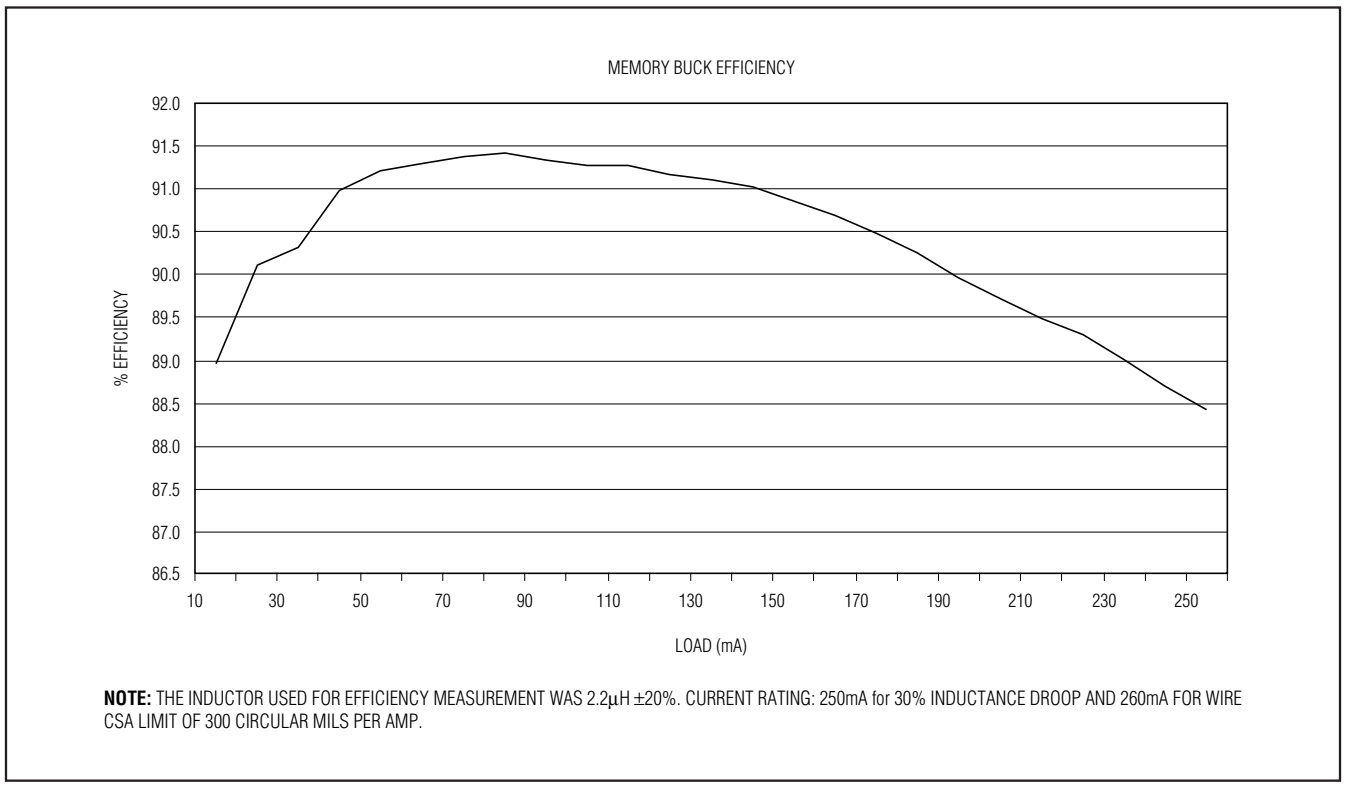
____Cache-Memory Battery-Backup Buck-Regulator Supply (2MHz PWM)

A 2MHz internal synchronous buck regulator is used to generate the appropriate cache-memory supply voltage. With careful inductor selection, high efficiencies can be achieved with this type of supply (see Figures 7a and 7b). The regulator has a user-selectable voltage range of 0.9V to 2.5V, and can supply up to 450mA. There is also a user-selectable LO_BATT threshold with a range of 2.5V to 3V. If the battery voltage drops below this threshold, the regulator shuts down and the IC goes into a low-power state until system power is restored. The regulator can be disabled by the $\overline{ENS}$ pin during normal power conditions. The buck regulator is designed to supply enough current to power the cache memory during data retention/refresh mode. The regulator can be enabled during normal system power, but it cannot supply power to the cache memory during normal operating conditions.

Note: The buck regulator and the charger should not run simultaneously.

Buck-Regulator Operation Overview

VREG is the feedback pin for the 2MHz PWM switching regulator cache-memory supply. The switching node uses this voltage reference feedback to regulate the output voltage to the value specified by DIV. The switching power-supply high-side and low-side FETs drive LX. The output inductor is connected to this node. During normal operation, the switching frequency observed on the LX pin is approximately 2MHz. The exact switching frequency and duty factor varies based on load and inductor selection. The SGND pin connects to the source of the internal low-side switch. This pin should be routed from the DS2731 to the negative terminal of the output capacitor. There are fast transient currents in this connection caused by the commutation of the body-drain diode of the low-side switch when the high-side switch turns on. Considerations should be taken during layout to minimize EMI. The buck regulator is equipped with an internal temperature-shutdown circuit that turns off the regulator if the circuit temperature reaches 165°C. Regulation resumes once the temperature has cooled 15°C below 165°C.



NOTE: THE INDUCTOR USED FOR EFFICIENCY MEASUREMENT WAS 2.2µH ±20%. CURRENT RATING: 250mA for 30% INDUCTANCE DROOP AND 260mA FOR WIRE CSA LIMIT OF 300 CIRCULAR MILS PER AMP.

Figure 7a. Memory Buck Regulator Efficiency with 2.2µH Inductor

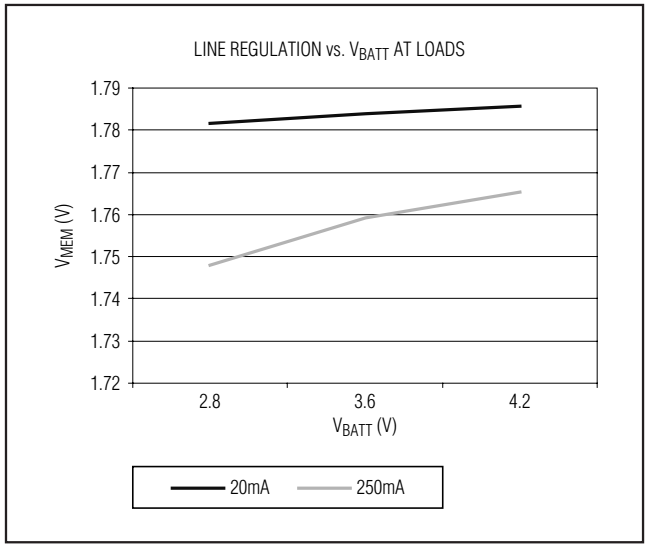


Figure 7b. Memory Buck Regulator Line Regulation vs. Battery Voltage at Loads

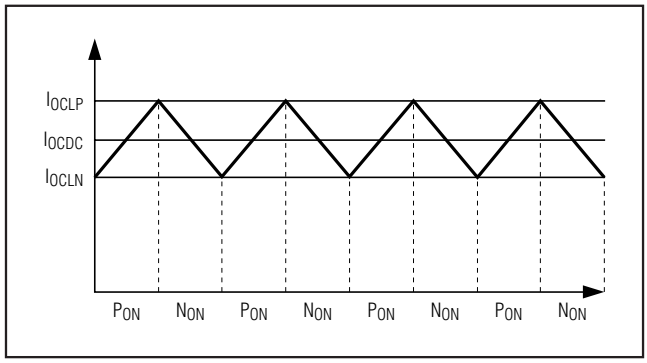


Figure 8. Buck Regulator Overcurrent Switching

Setting Memory Voltage and Low-Battery Shutdown

The cache-memory and low-battery shutdown voltages are set using a 1.25V reference and resistor-divider. The 1.25V reference is supplied at the REF pin. This pin cannot supply power for any system loads. In order to ensure that the voltage reference is not overloaded, a 1MΩ total resistor-divider network is recommended.

Memory Voltage

The voltage on the DIV pin is the average DC voltage set point to which the cache-memory supply regulates. The cache-memory supply voltage can range from 0.9V to 2.5V and is set by the following formula:

$$V_{DIV} \times 25/12 = V_{VREG}$$

Low-Battery Shutdown

The voltage on the LO_BATT pin is compared to the prescaled battery voltage. The scale factor is 4.5:1. When the scaled battery voltage drops below the voltage on LO_BATT, the IC goes into quiescent-power mode. All circuitry is shut off and does not turn on again until the V_{BIAS} voltage is stable and UVLO-REG is off. The low-battery voltage set point can be determined by the following formula:

$$V_{LO\_BATT} \times 4.5 = \text{Low-Battery Voltage Set Point}$$

Layout

Due to high-frequency switching, high-current loops, and large-voltage switching, special consideration should be taken for layout of the DS2731 board in order to reduce EMI.

CCCV Charger

The CCCV charger generates a high-current loop from VIN to CHG1 and CHG2 to CGND1 and CGND2. Also, large dV/dT is generated at CHG1 and CHG2 from the switching on and off of the 12V supply. These combine to generate magnetic and electric fields. To reduce these fields, the high-current loop should be made as small as possible. Traces should be routed point-to-point, as straight as possible, and a ground plane/shield should be used to isolate the noise from nearby components. Also, the trace width of the charge path should be sufficiently large enough to accommodate the high current. SNS and BATT+ should be connected as close as possible to the SNS resistor and BATT+ terminal for accurate current regulation and battery voltage measurements.

The AGND pin is the analog reference connection. No charge current flows into AGND. It should be connected as close as possible to the negative terminal of the battery. This allows for a more accurate battery voltage measurement by avoiding any voltage drops caused by stray resistance in the high-current charge path.

Cache-Memory Buck Regulator

Even though the voltages and currents are not as high as the CCCV charger, care still needs to be taken during layout of the memory buck regulator. There are fast-transient voltages at LX. The fast-transient current loop is from CIN to LX to SGND. Again, the current loop should be routed as small as possible and ground shielding should be used to isolate the circuit.

Power-Failure Switchover

During a power-failure event, the DS2731 can assume responsibility for supplying power to the cache memory using the backup battery. As long as the 2MHz internal synchronous buck regulator is enabled and the battery voltage is above LO_BATT, the buck regulator supplies power to the memory. During normal power the buck regulator runs off of the aux input voltage. The DS2731 monitors the aux input voltage for power failure. During a power-failure event, the DS2731 internally switches the buck-regulator supply to the battery backup. The battery is connected internally by a break-before-make switching mux. The break-before-make circuitry ensures that the battery is never connected to the 3.3V aux supply. The capacitor on the CIN pin provides power to the IC during switchover. If the buck regulator is disabled during normal power conditions, $\overline{ENS}$ must be driven low by the system when a loss of power is detected.

Auxiliary Voltage

The aux switch monitors the aux power supply. In the system, this supply fails before the cache-memory power supply. When it crosses 2.93V, a comparator in the DS2731 activates the power multiplexer and switches the power source for the buck regulator from the aux power to the battery. This occurs as a break-before-make operation to prevent current from flowing out of the battery into the aux supply.

Bypass/Holdup Capacitor

The bypass/holdup capacitor, connected to pin CIN, is sized to be able to support full input current to the switcher in the case where the $\overline{ENS}$ pin is low when the aux voltage falls below 2.93V. Since the power mux is break-before-make, the capacitor supplies power during the handover operation. Prior to the event, the capacitor is charged to 2.93V, and immediately afterwards it is connected to the battery voltage through the 1Ω mux switch. If power is restored, the conduction path between the battery and holdup capacitor is opened before the capacitor is connected to the 3.3V aux supply.

Enable Switcher

The buck regulator is enabled by the $\overline{ENS}$ pin. If the pin is low, the regulator turns on supplying power to the cache memory. The $\overline{ENS}$ pin should be driven low by the system when the cache memory has halted active processing and is in its data-retention/refresh mode.

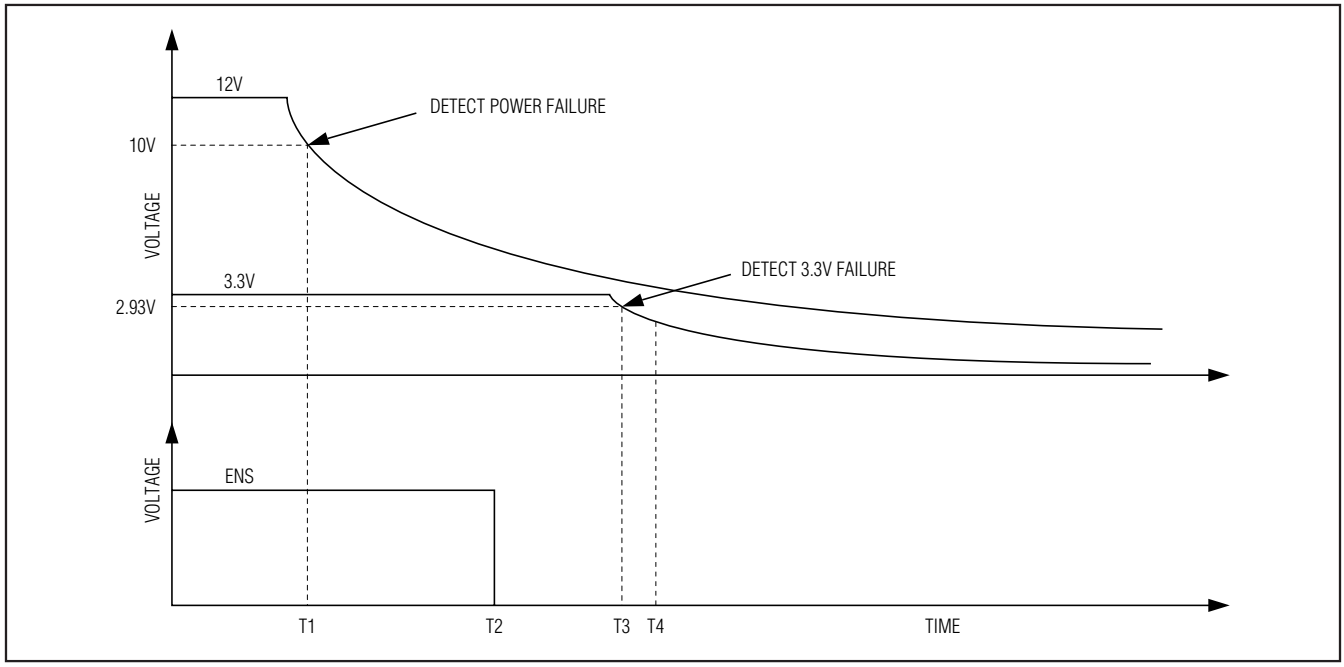


Figure 9. Expected Scenario for Multiplex Switchover from Aux to Battery

Actions Occurring During Time Intervals

From T1 to T2: At T1, the power-failure signal occurs and the system must put the cache memory into its self-refresh mode. Then it must shut off the system cache supply. Between the time the system power supply is shut off and the $\overline{ENS}$ pin is driven low, the cache memory is powered from its local bypass capacitance.

From T2 to T3: When the $\overline{ENS}$ pin goes low, the DS2731 buck regulator turns on and takes over regulation of the cache-memory voltage. The power source for the DS2731's switcher during this interval is the 3.3V aux voltage.

From T3 to T4: At time T3, the DS2731 detects that the 3.3V aux supply is about to fail and activates the multiplexer. However, to prevent cross-connections between the 3.3V aux and the battery, the multiplexer is designed as break-before-make. The interval T3–T4 is t_{BRK}. During this interval the DS2731 switching supply uses the holdup capacitor on CIN as its power source. CIN must be sized so that it has enough capacity to hold up the regulator for t_{BRK}.

After T4: At T4, the multiplexer connects CIN to the battery's positive terminal. The regulator operates from the battery.

Reapplication of Power

This is essentially the reverse process from the power-loss sequence. Power is applied to the RAID card; the 12V and 3.3V buses turn on and become stable. The main cache-memory power supply turns on but the power MOSFET that connects the cache to the cache-power supply remains off. The cache-backup supply in the DS2731 automatically switches from the battery source to the 3.3V bus when the 3.3V bus goes above 2.93V. The system then disables $\overline{ENS}$ and enables the cache's power MOSFET, connecting the cache to the main cache power supply. Enough bulk storage capacitance must be available at the cache to hold up during this switchover time. The memory is now ready to exit from autorefresh mode (IDD6 for DDR2 memory) and resume full operation.

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	—	**21-0108**

Cache-Memory Battery-Backup Management IC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/07	Initial release.	—
1	1/09	Corrected part numbers in the *Ordering Information* table.	1