Features

- **Advanced Processor for Dual-mode Digital Still Cameras and Video Recorders**
- **Supports Personal Video Recording Applications**
- **ARM946E-S™ Core with Enhanced DSP Capability for A/V Processing and System Control Functions, 8 KBytes Each for Instruction/Data Cache, Runs up to 96 MHz**
- **Supports Progressive and Interlaced CCD Imagers (up to 4 Fields)**
- **Image Processing Functions for CCD/CMOS Imagers**
- **Image Scaling and Rotation Hardware**
- **Video Encoder with Two DACs and Line Drivers for Composite or S-Video NTSC/PAL TV**
- **Digital Video Outputs Include: Composite, 16/8-bit YC (CCIR-656), RGB 565, 24-bit RGB, Component (Y/Pr/Pb), VESA up to XGA Resolutions**
- **Direct Interface to Casio, Epson, AU, and Toppoly LCDs**
- **Encodes/Decodes Images and Video: Baseline JPEG, MPEG-1 at 24 fps VGA, MPEG-4 at 30 fps VGA (Performance Figures are for Half Duplex)**
- **DDR SDRAM Interface Supports from 128 Mbits to 1 Gbit**
- **Unified Memory Architecture (Entire Program and Data Stored in DDR SDRAM)**
- **Support for All Flash Card Interfaces (MMC/SD, Memory Stick Pro™, SSFDC/SmartMedia, CompactFlash®)**
- **ATA/IDE Controller**
- **Static Memory Controller (Flash/SRAM) Supports up to Eight 16 MB Devices**
- **One DAC for Camera Control Functions and Audio Output**
- **Four ADC Channels for Monitoring Camera Analog Inputs (Audio, Switches, etc.)**
- **Audio Data Interface for Connection to External Stereo ADC/DAC**
- **USB 2.0 High-speed Slave and Full-speed Host Controllers for PC Camera and Printing Applications**
- **IEEE 1394 Link Layer Interface**
- **Two USART Interfaces and a Serial Peripheral Interface (SPI) for Loading Boot Code and Controlling Camera Components**
- **Six General-purpose Timers for Waveform Generation (PWM, etc.) and Event Monitoring**
- **Programmable Watchdog Timer and Real-time Clock**
- **Keyboard Interface Supports up to 25 Buttons**
- **Up to 8 External Interrupts and up to 130 Pins Configurable as General-purpose I/Os**
- **280-ball BGA Package, 1.8V Core, and 1.8 to 3.3V I/O Operation**

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High-Performance Digital/Video Camera Processor

IS-5114

09/04/07

1. Description

The IS-5114 is a highly integrated solution for dual-mode digital still-image and video cameras. It combines a number of functions that are required in such devices, including the following:

- The device is based on an ARM946ES microprocessor whose function is to control the entire system, to capture and play back audio, and to multiplex compressed video and audio into a single bit stream that can be delivered to the main CPU. Most computationally-intensive functions are implemented in hardware which can be programmed according to user specifications, thus allowing the ARM® processor to be free for other user-defined functions such as advanced image and multimedia processing. The processor has 8 KB + 8 KB of internal instruction/data cache which helps it to operate efficiently and use minimal DDR SDRAM bandwidth.

- The device supports imager sizes of up to 16 megapixels. It accepts both Bayer RGB and CCIR-656 interfaces, which cover all possible CCD and CMOS sensors. It supports progressive as well as interlaced (up to 4 fields) imagers, including the special readout modes of progressive VGA CCD imagers. The device also supports a programmable delay on the external imager clock so that the highest quality images can be captured.

- The device has a high-performance still-image and video image processing block that performs all the necessary functions to convert the image/video data to a format that can be compressed in either JPEG or MPEG formats, as well as deliver image data to the LCD controller for a live view. This block performs gain control, color recovery, Gamma correction, image enhancement, image correction, scaling, rotation, and conversion to the YC format. All those functions have been implemented in the hardware to achieve the required performance at very low power consumption figures. In addition, there is a hardware block that collects statistics on the imager for auto-exposure (AE) and auto-white balancing (AWB) algorithms. Those AE/AWB algorithms are performed in the embedded ARM9 CPU to allow customization of the application. The current architecture also has the appropriate interfaces and sufficient performance to support a strobe-type flash light, as well as dark frame subtraction for low-level light conditions.

- The device has numerous display capabilities. It has an integrated video encoder (double sampling) and two 10-bit video DACs running at up to 27 MHz to support direct display to high-definition TVs and projectors. The device also has a 24-bit RGB output to interface to flat-panel TVs (LCDs and Plasma) at different VESA rates up to XGA (1024 x 768) resolution. It supports both square pixel and CCIR-type formats and can display in NTSC or PAL mode with the same crystal. It also has an integrated LCD controller which can interface directly to various LCDs. It directly supports a variety of LCD panels from Epson, Casio, AU, and Toppoly without the need for external ICs. Finally, it has a digital video output interface which can supply composite, 8-bit YC (CCIR-656), 16-bit YC, RGB 565, or component (Y/Pr/Pb) formats.

- The device has a high-performance image scaler that can perform up and down scaling at floating point resolutions.

- For video applications, a hardware video codec is included that supports MPEG-4 Simple Profile (encode and decode) and Advanced Simple Profile (encode only) communication at up to 30 fps VGA resolution. The hardware video engine is a pipelined architecture which is also flexible enough to support JPEG compression/decompression, H.263, MPEG-2 encode(I/P frames) at 30 fps VGA, and MPEG-1 encode/decode at 24 fps VGA (I frames only). The video codec can also be used to record and play back video clips including those taken from other digital cameras and mobile phones. All performance figures are for half duplex operation. Full duplex is possible, but the performance has not been characterized.

- The device utilizes a unified memory architecture using the DDR-SDRAM to capture, process, and play back images and video as well as to store program code and variables. It supports SDRAM configurations of up to 1 gigabit.

- The device supports all Flash cards, including Multimedia Card (MMC), Secure Digital (SD), Memory Stick Pro, SSFDC/SmartMedia/NAND Flash, and CompactFlash. The Flash card interfaces can support read/write operations at the maximum speeds specified by the Flash cards.

- The device has an ATA/IDE controller with UDMA capability to stream video directly to hard drives or CompactFlash devices.

- A static memory controller is included that supports up to eight 16 MB devices such as Flash, SRAM, or other memory-mapped peripherals. Both 8-bit and16-bit data buses are supported, with data accesses of up to 32 bits. The number of wait states, and setup, hold, and data float times are programmable on a per device (chip select) basis.

- A general-purpose 10-bit 96 kHz DAC is available. It can be used to control camera components such as the iris, shutter motor, lens motor, flash bulb, or AGC gain. It can also be used to drive audio output.

- A general-purpose 10-bit, 96 kHz ADC is available. This ADC has four input channels, which can be used for such things as battery level checking, photo detection, focus sensing, or audio capture.

- The I^2S- and AC'97-compatible audio data interface allows the device to connect with an external stereo ADC/DAC to capture or play back voice or audio. The device can encode captured audio in various popular formats, and can package it in the same bit stream as the video or inside compressed JPEG pictures. It can also play back stand-alone audio such as MP3 files, or audio embedded in MPEG bit streams.

- The USB 2.0 high-speed slave controller can be used to connect to a PC for efficient downloading of captured images to the PC. The USB 2.0 full-speed host controller allows the device to connect directly to printers and other slave devices.

- An IEEE 1394 link layer interface allows the device to stream video (compressed or uncompressed) to other devices.

- Two USART interfaces are included for serial communication. They support standard baud rates of up to 460.8 kbps or non-standard rates of up to 4.875 Mbps in asynchronous mode. They support rates of up to 19.5 Mbps in synchronous mode.

- The Serial Peripheral Interface (SPI) is used to boot from an external EEPROM. Once the boot code is loaded inside the program memory, the CPU can download its code from any peripheral supported by the device, including non-volatile storage media. With four chip select pins, the SPI can also be used to control other external devices at speeds of up to 24 Mbps.

- Three 16-bit and three 32-bit general-purpose timers are included which can be used to generate interrupts to the internal CPU. The 16-bit timers can also generate waveforms on their associated pins via pulse-width modulation (PWM) or other techniques. They can also monitor and count external events on these pins.

- A dedicated watchdog timer is available which can provide an interrupt, an event on an external pin, or a reset to the internal CPU in the event that software is not responding as expected. Write access to the watchdog is protected by control access keys to prevent corruption of the watchdog should an error condition occur.

- A real-time clock is provided to keep track of the time. It operates on its own power supplies, so the clock can keep running with very low power consumption even if the rest of the chip is unpowered. Two pins are provided to control system power switching.
- The device provides a keyboard interface that can monitor up to 25 buttons.
- The device provides up to 8 external interrupt pins, depending on the system configuration, which can be handled by the interrupt controller as either edge or level sensitive.
- Up to 130 pins can also be configured as GPIOs, depending on the system application.
- During normal operation, the power consumption may be minimized by disabling the clock of any internal module that is not in use. In order to further reduce power consumption, the main CPU clock can be divided to run at a slower speed. In order to minimize power consumption when the device is not in use, a "sleep mode" is available that halts the operation of all logic and shuts down the oscillators and PLLs. Recovery from the sleep mode occurs via the WKP ("wake-up") pin, at which time the device begins execution from its previous state.

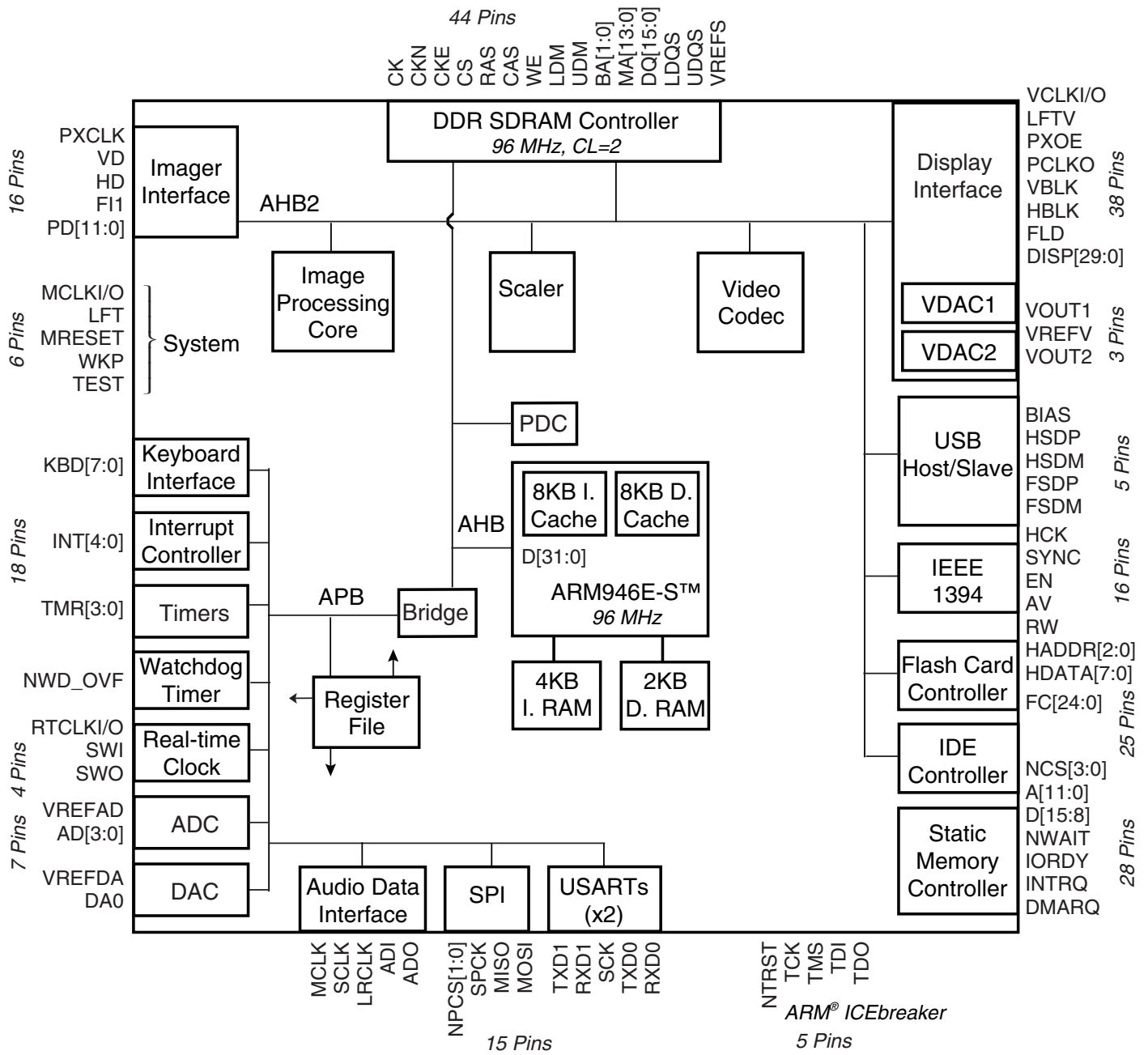**Figure 1-1.** Typical DSC Application Using the IS-5114
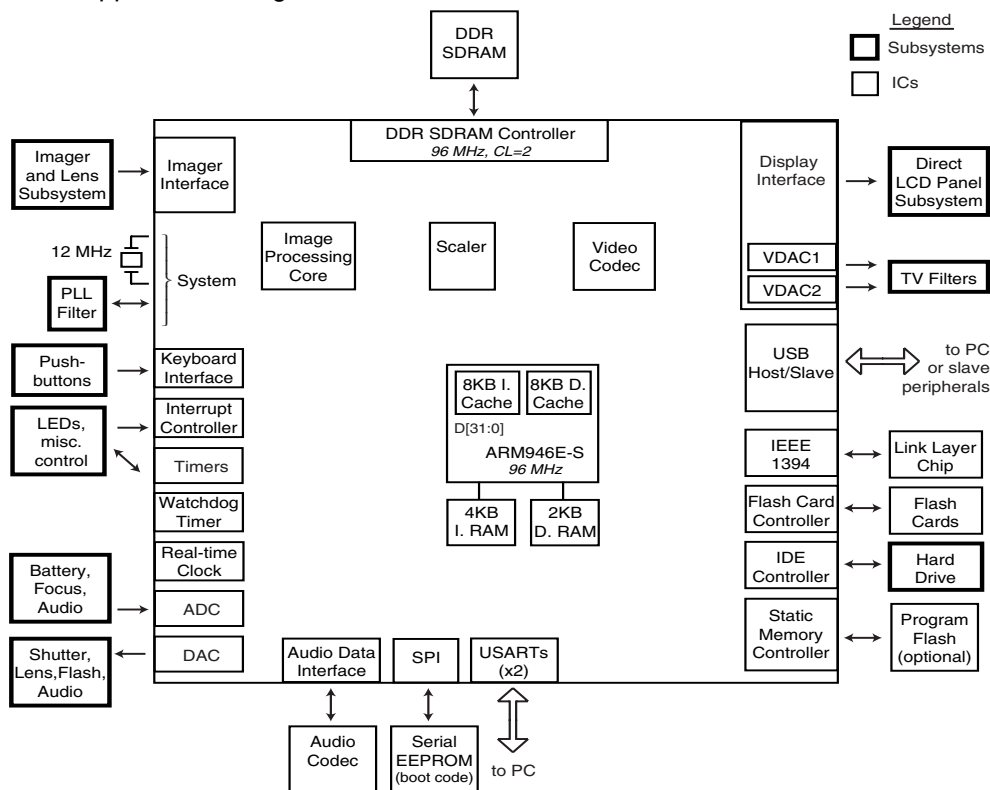
1.1 Technology

- The device is fabricated in a 0.18 micron process.
- The core logic requires a 1.8V power supply. Most I/O pads require 3.3V supplies, a few interfaces use 1.8V supplies, and the DDR interface requires a 2.5V supply.
- The package is a 280-ball BGA.

2. Block Diagram

Figure 2-1. The IS-5114 Top-level Architecture

3. Device I/O

The IS-5114 has 230 I/O signals, 46 digital power/grounds, and 4 analog power/grounds. All digital signal pads have 3.3V TTL-compatible output drivers and CMOS inputs, except for SWI, SWO, and INT[1:0], which have 1.8V TTL-compatible output drivers and CMOS inputs, the crystal and PLL signals, which also run at 1.8V, and the DDR SDRAM Interface, which has SSTL_2 (2.5V) drivers. Table 3-1 provides a description of the I/Os. A package pin map is provided in "Packaging Information" on page 14.

Note that some pins have more than one possible function. For example, the IDE Controller chip selects are shared with the Static Memory Controller (SMC) chip select pins (NCS[1:0]). The pin_sel register is used to control the function of the multi-purpose pins.

3.1 I/O Table Definitions

- I = input, O = output, T = tri-state output, B = bi-directional
- H = logic high, L = logic low
- pd = pad includes a pull-down resistor
- st = pad has Schmitt-triggered input
- * = pad has a drive strength customized for its application

Table 3-1. I/O Signal Descriptions

Pin Name	Direction	Drive Strength	Reset State	Function
DDR SDRAM Interface (All pads are SSTL_2 compatible)				
CK	T	*	H	SDRAM clock
CKN	T	*	L	SDRAM clock inverted (clocks are differential)
CKE	T	*	L	Clock enable
CS	T	*	H	Chip select (active low)
RAS	T	*	H	Row address select (active low)
CAS	T	*	H	Column address select (active low)
WE	T	*	H	Write enable (active low)
LDM	T	*	L	Input data mask, lower byte
UDM	T	*	L	Input data mask, upper byte
BA[1:0]	T	*	all bits L	Bank address
MA[13:0]	T	*	all bits L	Memory address
DQ[15:0]	B	*	Input	Data
LDQS	B	*	Input	Data strobe, lower byte
UDQS	B	*	Input	Data strobe, upper byte
VREFS	I	N/A	Input	Reference voltage for SSTL_2 pads (analog, 1.25V nominal)
Imager Interface				
PXCLK	I	N/A	Input	Pixel clock
VD	B	2 mA	Input	Vertical synchronization
HD	B	2 mA	Input	Horizontal synchronization

IS-5114

Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
FI1	I	N/A	Input	Field identification signal (for interlaced output imagers)
PD[11:0]	B	2 mA	Input	Pixel data - use MSBs in case of data less than 12 bits (PD[1:0] also programmable as Keyboard: KBD[9:8]) (PD[3:0] also programmable as GPIO)
Display Interface				
VCLKI	I	N/A	Input	Video crystal connection 1 (up to 27 MHz, depending on display type)
VCLKO	O	*	X [1]	Video crystal connection 2
LFTV	O	*	X [2]	External low-pass filter for video PLL
PXOE	I	N/A	Input	Pixel output enable (active low)
PCLKO	B	8 mA	L	Pixel clock output
VBLK	B	4 mA	PXOE = 0: L 1: Input	Video, Casio LCD: Vertical blanking reference AU LCD: VSY Toppoly LCD: XVD
HBLK	B	4 mA	PXOE = 0: L 1: Input	Video, Casio LCD: Horizontal blanking reference AU LCD: HSY Toppoly LCD: XHD
FLD	B	4 mA	PXOE = 0: L 1: Input	Field select
DISP[29:24]	B	2 mA	Input	Display data component: PR[1:0], PB[1:0], Y[1:0] VESA: B[1:0], G[1:0], R[1:0] (DISP[29:27] also programmable as INT[7:5]) (also programmable as SMC: A[19:14]) (also programmable as GPIO)
DISP[23:16]	B	2 mA	Input	RGB24b: B[2:0], G[1:0], R[2:0] CVBS: NoConnect[7:2], CVBS[1:0] Separate: NoConnect[7:4], CV_C[1:0], CV_Y[1:0] Component: PR[4:2], PB[3:2], Y[4:2] VESA: B[4:2], G[3:2], R[4:2] Epson LCD: FV, FRYP, NoConnect[5:0] (also programmable as SMC: A[23:20], Chip Select [7:4] (NCS [7:4], active low) (also programmable as GPIO)

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Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
DISP[15:8]	B	2 mA	PXOE = 0: 0x80 1: Input	YC16b: C[7:0] (display or capture) ITU-656: YC[7:0] (display or capture) RGB565: B[4:0], G[5:3] RGB24b: B[7:3], G[7:5] Separate: CV_C[9:2] Component: PR[9:5], PB[9:7] VESA: B[9:5], G[9:7] Epson LCD: XSCL, GCP, D[5:0] Casio LCD (1G): POL, STBYB, D[5:0] Casio LCD (2G): D[7:0] AU LCD: D[07:00] Toppoly LCD: DIN[7:0] (also programmable as GPIO)
DISP[7:0]	B	2 mA	PXOE = 0: 0x00 1: Input	YC16b: Y[7:0] (display or capture) RGB565: G[2:0], R[4:0] RGB24b: G[4:2], R[7:3] CVBS: CVBS[9:2] Separate: CV_Y[9:2] Component: PB[6:4], Y[9:5] VESA: G[6:4], R[9:5] Epson LCD: DY, FRYS, YSCLD, YSCL, XINH, FRX, LP, RES Casio LCD (1G): CP, STB, RIT, GRES, GSRT, GPCK, RIT, STH, CLK Casio LCD (2G): DI, CS, SCK, NoConnect[4], VSYNC, HSYNC, NoConnect[1], CLK AU LCD (A015BL01): DITH, H_DIR, STB, SHDB, SEL0, GRB, V_DIR, DCLK AU LCD (A015AN04): ISDA, CS, ISCL, NoConnect[4], SEL0, GRB, NoConnect[1], DCLK Toppoly LCD: SDATA, SLOAD, SCLK, NoConnect[4:1], MCLK
VREFV	I	N/A	Input	Positive reference voltage for video DACs (analog) (typically AVDD1/2) [3]
VOUT1	T	*	Hi-Z	Video DAC 1 output (analog, VOUT1 full range = (16/11)*VEXT1) Drives S-Video Y or Composite Video (CVBS) signal
VOUT2	T	*	Hi-Z	Video DAC 2 output (analog, VOUT2 full range = (16/11)*VEXT2) Drives S-Video C signal
USB Interface				
BIAS	T	*	Hi-Z	Bias (analog)
HSDP	B	*	Input	High-speed transceiver data, positive polarity (analog)
HSDM	B	*	Hi-Z	High-speed transceiver data, negative polarity (analog)
FSDP	B	*	Hi-Z	Full-speed transceiver data, positive polarity
FSDM	B	*	Input	Full-speed transceiver data, negative polarity
IEEE1394 Interface (Also Programmable as GPIO)				
HCK	B	2 mA	L	Clock

Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
SYNC	B	2 mA	Input	Synchronization pulse
EN	B	2 mA	L	Buffer data valid
AV	B	2 mA	Input	Data available
RW	B	2 mA	H	Read/Write (1 = read, 0 = write)
HADDR[2:0]	B	2 mA	all bits L	Transport address
HDATA[7:0]	B	2 mA	Input	Transport data
Flash Card Interfaces (Shared with Static Memory Controller and IDE Controller, Also Programmable as GPIO)				
FC0	B	4 mA	Input	SD: DAT[0] (bi-directional) SSFDC: D[0] (bi-directional) SMC: D[0] (bi-directional) IDE: DD[0] (bi-directional)
FC1	B	4 mA	Input	SD: DAT[1] (bi-directional) MS: SDIO[1] (bi-directional) SSFDC: D[1] (bi-directional) SMC: D[1] (bi-directional) IDE: DD[1] (bi-directional)
FC2	B	4 mA	Input	SD: DAT[2] (bi-directional) MS: SDIO[2] (bi-directional) SSFDC: D[2] (bi-directional) SMC: D[2] (bi-directional) IDE: DD[2] (bi-directional)
FC3	B	4 mA	Input	SD: DAT[3] (bi-directional) MS: SDIO[3] (bi-directional) SSFDC: D[3] (bi-directional) SMC: D[3] (bi-directional) IDE: DD[3] (bi-directional)
FC4	B	4 mA	Input	SD: CMD (bi-directional) SSFDC: D[4] (bi-directional) SMC: D[4] (bi-directional) IDE: DD[4] (bi-directional)
FC5	B	4 mA	Input	SSFDC: D[5] (bi-directional) SMC: D[5] (bi-directional) IDE: DD[5] (bi-directional)
FC6	B	4 mA	Input	SSFDC: D[6] (bi-directional) SMC: D[6] (bi-directional) IDE: DD[6] (bi-directional)
FC7	B	4 mA	Input	SSFDC: D[7] (bi-directional) SMC: D[7] (bi-directional) IDE: DD[7] (bi-directional)

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Table 3-1.   I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
FC8	B	4 mA	L	SSFDC: ALE (output) SMC: A[12] (output) IDE: NRESET (active low output)
FC9	B	4 mA	L	SSFDC: CLE (output) SMC: A[13] (output) IDE: NDMACK (active low output)
FC10	B	4 mA	H	SSFDC: WE (active low output) SMC: NWR0 (active low output) IDE: NDIOW (active low output)
FC11	B	4 mA	H	SSFDC: RE (active low output) SMC: NRD (active low output) IDE: NDIOR (active low output)
FC12	B	4 mA	L	SSFDC: WP (active low output) SMC: NWR1 (active low output) IDE: NLED (active low output)
FC13	B	2 mA	H	SSFDC: CE1 (active low output)
FC14	B	2 mA	H	SSFDC: CE0 (active low output)
FC15	B	2 mA	Input	SSFDC: R/$\overline{B}$ (input)
FC16	B	2 mA	Input	SSFDC: CD (active low input)
FC17	B	2 mA	Input	SSFDC: WPZU (input)
FC18	B	4 mA	H	SD: DDIR (active low output) MS: BS (active low output)
FC19	B	4 mA	H	SD: CDIR (active low output) MS: SDIR (active low output)
FC20	B	4 mA	L	SD: CLK (output) MS: SCLK (output)
FC21	B	2 mA	Input	SD: CD (input)
FC22	B	2 mA	Input	MS: INS (input)
FC23	B	4 mA	Input	MS: SDIO[0] (bi-directional)
FC24	B	2 mA	Input	IDE: CompactFlash CD (active low input)
Static Memory Controller/IDE Controller (Also Programmable as GPIO)				
NCS[3:0]	B	2 mA	all bits H	SMC: Chip selects (active low) (NCS[7:4] is shared with DISP[19:16]) IDE: Shares NCS[1:0] only (if an IDE device is present, these pins cannot be used by SMC) (NCS[3:2] also programmable as timers: TMR[5:4])
A[11:0]	B	4 mA	all bits L	SMC: Address (A[23:20] is shared with DISP[23:20], A[19:14] is shared with DISP[29:24], A[13:12] is shared with FC[9:8]) IDE: shares A[2:0] only (maps to DA[2:0])
D[15:8]	B	4 mA	Input	SMC: Data (D[7:0] is implemented on the FC[7:0] pins) IDE: Shares all bits (maps to DD[15:8])

Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
NWAIT	B	2 mA	Input	SMC: Access stall (active low)
IORDY	B	2 mA	Input	IDE: I/O path ready
INTRQ	B	2 mA	Input	IDE: Interrupt request
DMARQ	B	2 mA	Input	IDE: DMA request (active low)
USART1 (Also Programmable as GPIO)				
TXD1	B	2 mA	Input	USART1: Transmit data SPI: Peripheral chip select 3 (active low)
RXD1	B	2 mA	Input	USART1: Receive data SPI: Peripheral chip select 2 (active low)
USART0 (Also Programmable as GPIO)				
SCK	B	2 mA	Input	USART serial clock (can be used for USART0 or USART1)
TXD0	B	2 mA	Input	USART0 transmit data
RXD0	B	2 mA	Input	USART0 receive data
Serial Peripheral Interface (Also Programmable as GPIO)				
NPCS[1:0]	B	2 mA	Input	Peripheral chip selects (active low) (NPCS[3:2] is shared with TXD1, RXD1)
SPCK	B	4 mA	Input	Serial peripheral clock
MISO	B	4 mA	Input	Master in, slave out
MOSI	B	4 mA	Input	Master out, Slave in
Audio Data Interface (Also Programmable as GPIO)				
MCLK	B	2 mA	Input	I^2S: Oversampling clock AC '97: BIT_CLK
SCLK	B	2 mA	Input	I^2S: Serial bitrate clock AC '97: RESET
LRCLK	B	2 mA	Input	I^2S: Left/right channel clock AC '97: SYNC
ADI	B	2 mA	Input	I^2S: Audio data input (from ADC) AC '97: SDATA_IN
ADO	B	2 mA	Input	I^2S: Audio data output (to DAC) AC '97: SDATA_OUT
Keyboard Interface (Also Programmable as GPIO)				
KBD[7:0]	B	2 mA	Input	Keyboard I/O (KBD[9:8] is shared with PD[1:0])
Interrupt Controller (Also Programmable as GPIO)				
INT[4:0]	B	2 mA	Input	External interrupt sources (INT[7:5] is shared with DISP[29:27]) (INT4 also programmable as Imager Interface: PXCLK2)
General-purpose Timers (Also Programmable as GPIO)				
TMR[3:1]	B	2 mA	Input	Timer I/O (programmable function) (TMR[5:4] is shared with NCS[3:2])

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Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
TMR[0]	B	2 mA	L	Timer I/O (programmable function) (Resets as ARM ICEbreaker RTCK)
Watchdog Timer (Also Programmable as GPIO)				
NWD_OVF	B	2 mA	H	Watchdog timer overflow (active low)
Real-time Clock and Power Management				
RTCLKI	I	N/A	Input	Real-time clock crystal connection 1 (32.768 kHz)
RTCLKO	O	*	X [1]	Real-time clock crystal connection 2
SWI	B	2 mA	Input	Power switch input (rising edge causes SWO=1) (also programmable as GPIO)
SWO	B	2 mA	L	Power switch output (1 = on, 0 = off) (also programmable as GPIO)
A/D & D/A Converters (All analog connections)				
VREFDA	I	N/A	Input	Positive reference voltage for DAC (2.4V to 3.3V, DA0 output = VREFDA * data/1024)
DA0	T	* [4]	Hi-Z	Output from DAC
VREFAD	I	N/A	Input	Positive reference voltage for ADCs (2.4V to 3.3V, full scale output when AD input = VREFAD)
AD[3:0]	I	N/A	Input	Inputs to ADC
System Control				
MCLKI	I	N/A	Input	Logic crystal connection 1 (12.0 MHz)
MCLKO	O	*	X [1]	Logic crystal connection 2
LFT	O	*	X [2]	External low-pass flter for main logic PLL
MRESET	I (st)	N/A	Input	System reset (active low)
WKP	I (st)	N/A	Input	Wake-up from sleep mode
TEST	I (st)	N/A	Input	Production test mode (normally tie to GNDP)
ARM ICEbreaker				
NTRST	I	N/A	Input	Test reset (active low)
TCK	I	N/A	Input	Test clock
TMS	I	N/A	Input	Test mode set
TDI	I	N/A	Input	Test data In
TDO	T	1	Hi-Z	Test data output
Power				
VDDP[6:0]	I	N/A	Input	3.3V I/O power (±0.3V)
GNDP[6:0]	I	N/A	Input	0V I/O ground
VDDS[7:0]	I	N/A	Input	2.5V I/O power for DDR interface (±0.25V)
GNDS[7:0]	I	N/A	Input	0V I/O ground for DDR interface

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Table 3-1. I/O Signal Descriptions (Continued)

Pin Name	Direction	Drive Strength	Reset State	Function
VDDC[7:4]	I	N/A	Input	1.8V core power (±0.15V)
GNDC[7:4]	I	N/A	Input	0V core ground
VDDC[3]	I	N/A	Input	1.8V power for video oscillator and PLL (±0.15V)
GNDC[3]	I	N/A	Input	0V ground for video oscillator and PLL
VDDC[2]	I	N/A	Input	1.8V power for peripheral PLL (±0.15V)
GNDC[2]	I	N/A	Input	0V ground for peripheral PLL
VDDC[1]	I	N/A	Input	1.8V power for main oscillator and PLL (±0.15V)
GNDC[1]	I	N/A	Input	0V ground for main oscillator and PLL
VDDC[0]	I	N/A	Input	1.8V power for real-time clock (±0.15V)
GNDC[0]	I	N/A	Input	0V ground for real-time clock
AVDD[1]	I	N/A	Input	3.3V power for video DACs (±0.15V)
AGND[1]	I	N/A	Input	0V ground for video DACs
AVDD[0]	I	N/A	Input	3.3V power for low-speed ADC/DAC (±0.3V)
AGND[0]	I	N/A	Input	0V ground for low-speed ADC/DAC

Notes: 1. The oscillator output pins toggle as they are driven by external crystals.

2. The PLLs are enabled at reset, so their charge pumps begin driving the LFT pins to some voltage between 0 and 1.8V. If the video PLL is not used, tie the LFTV pin to the GNDC3 supply.

3. If the video DACs are not used, tie the VREFV pin to the AGND1 supply and leave the VOUT1/VOUT2 pins unconnected.

4. The low-speed DAC is designed to drive a maximum load of 50pF.

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4.   Packaging Information

The IS-5114 is packaged in a 280-ball BGA. Table 4-1 shows how the device I/O signals map to package pins. Figure 4-1 shows a physical view of the pins. Figure 4-2 contains mechanical drawings of the package.

Table 4-1.   Package Pin List

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
GNDC1	C3	AD0	U3	GNDP2	U17	GNDC0	C17
MCLKI	C2	VREFAD	V3	A3	U18	INT0	B17
MCLKO	B1	DA0	W2	A0	V19	SWI	A18
VDDC1	C1	VREFDA	W3	A1	U19	SWO	A17
DQ15	D4	AGND0	T4	A7	T16	INT1	D16
DQ0	D3	TMS	U4	A5	T17	VDDC0	C16
VDDS0	D2	TDI	V4	A4	T18	PD10	B16
GNDS0	D1	TDO	W4	A2	T19	PD11	A16
DQ14	E5	INT2	R5	A10	R15	FI1	E15
DQ1	E3	TCK	U5	A11	R17	PD3	C15
DQ2	E2	NPCS0	V5	NCS1	R18	PD8	B15
DQ13	E4	NTRST	T5	NCS2	R16	VD	D15
DQ3	E1	SPCK	W5	IORDY	R19	PD9	A15
DQ12	F5	TMR0	R6	INT3	P15	TMR3	E14
VDDS1	F3	NPCS1	U6	DMARQ	P17	PD2	C14
GNDS1	F2	MOSI	V6	INTRQ	P18	PD6	B14
DQ11	F4	TMR1	T6	NCS3	P16	HD	D14
DQ4	F1	MISO	W6	DISP0	P19	PD7	A14
DQ10	G5	WKP	R7	VBLK	N15	VDDP4	E13
DQ5	G3	RXD0	U7	DISP28	N17	GNDP4	C13
DQ6	G2	TXD0	V7	DISP2	N18	PD4	B13
VDDS2	G1	SCK	W7	DISP1	N19	PD5	A13
GNDS2	G4	RXD1	T7	DISP29	N16	PD1	D13
LDQS	H1	FC20	W8	DISP3	M19	PXCLK	A12
DQ7	H3	TXD1	U8	DISP26	M17	KBD7	C12
UDQS	H2	FC19	V8	DISP4	M18	PD0	B12
DQ8	H4	VDDP0	T8	DISP27	M16	KBD6	D12
DQ9	H5	GNDP0	R8	HBLK	M15	KBD5	E12
LDM	J1	FC23	W9	DISP5	L19	SCLK	A11
VDDS3	J2	FC18	V9	DISP6	L18	ADO	B11
GNDS3	J3	FC17	U9	DISP25	L17	KBD4	C11
UDM	J4	FC22	T9	VDDC6	L16	KBD3	D11
CS	J5	FC21	R9	GNDC6	L15	KBD2	E11
RAS	K1	FC13	W10	DISP7	K19	MCLK	A10

Table 4-1. Package Pin List (Continued)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
CAS	K2	FC14	V10	DISP8	K18	ADI	B10
WE	K3	FC15	U10	DISP24	K17	AV	C10
VDDS4	K4	VDDC5	T10	VDDP3	K16	KBD1	D10
GNDS4	K5	GNDC5	R10	GNDP3	K15	KBD0	E10
CK	L1	FC0	W11	PCLKO	J19	LRCLK	A9
BA1	L2	FC1	V11	DISP9	J18	HDATA0	B9
CKE	L3	FC11	U11	DISP22	J17	HADDR0	C9
VDDC4	L4	FC12	T11	DISP23	J16	EN	D9
GNDC4	L5	FC16	R11	FLD	J15	NWD_OVF	E9
CKN	M1	FC2	W12	DISP10	H19	HDATA1	A8
BA0	M2	FC3	V12	DISP11	H18	HDATA2	B8
MA13	M3	FC9	U12	DISP20	H17	HCK	C8
VDDS5	M4	FC10	T12	DISP21	H16	VDDC7	D8
GNDS5	M5	FC24	R12	PXOE	H15	GNDC7	E8
MA0	N1	FC4	W13	DISP12	G19	HDATA3	A7
MA1	N2	FC5	V13	DISP13	G18	HDATA4	B7
MA12	N3	FC8	U13	DISP18	G17	HADDR1	C7
MA11	N4	VDDP1	T13	DISP19	G16	VDDP5	D7
MA10	N5	GNDP1	R13	TEST	G15	GNDP5	E7
VDDS6	P1	FC6	W14	DISP14	F19	HDATA5	A6
GNDS6	P2	FC7	V14	DISP15	F18	HDATA6	B6
MA9	P3	NCS0	U14	DISP16	F17	HADDR2	C6
MA8	P4	NWAIT	T14	DISP17	F16	SYNC	D6
MA7	P5	MRESET	R14	TMR2	F15	INT4	E6
MA2	R1	D8	W15	VOUT1	E19	HDATA7	A5
MA6	R3	A8	U15	AVDD1	E17	RW	C5
MA3	R2	D9	V15	VREFV	E18	VDDP6	B5
VDDS7	R4	A9	T15	AGND1	E16	FSDP	D5
GNDS7	T1	D10	W16	VOUT2	D19	FSDM	A4
MA4	T2	D11	V16	VDDC3	D18	GNDP6	B4
MA5	T3	A6	U16	GNDC3	D17	HSDP	C4
AVDD0	U1	D12	W17	LFTV	C19	HSDM	A3
VREFS	V1	D14	W18	VCLKI	B19	BIAS	A2
AD3	U2	D13	V17	VCLKO	C18	VDDC2	B3
AD2	V2	D15	V18	RTCLKI	B18	GNDC2	B2
AD1	W1	VDDP2	W19	RTCLKO	A19	LFT	A1

Figure 4-1.   Package Pin Diagram

TOP VIEW

VDDP: Periphery Power (3.3V)
GNDP: Periphery Ground (0V)

VDDS: Periphery Power (2.5V)
GNDS: Periphery Ground (0V)

VDDC: Core Power (1.8V)
GNDC: Core Ground (0V)

    0: Real-Time Clock (RTCLKI/O, SWI/O, INT[1:0])
    1: Main oscillator and PLL (MCLKI/O, LFT)
    2: Peripheral PLL
    3: Video oscillator and PLL (VCLKI/O, LFTV)
    4-7: Other core logic

AVDD: Analog Power
AGND: Analog Ground

    0: 3.3V Power for Low Speed ADC/DAC
    1: 3.3V Power for Video DACs

Pin assignments:

- Row A: A1 LFT, A2 BIAS, A3 HSDM, A4 FSDM, A5 HDATA7, A6 HDATA5, A7 HDATA3, A8 HDATA1, A9 LRCLK, A10 MCLK, A11 SCLK, A12 PXCLK, A13 PD5, A14 PD7, A15 PD9, A16 PD11, A17 SWO, A18 SWI, A19 RTCLKO
- Row B: B1 MCLKO, B2 GNDC2, B3 VDDC2, B4 GNDP6, B5 VDDP6, B6 HDATA6, B7 HDATA4, B8 HDATA2, B9 HDATA0, B10 ADI, B11 ADO, B12 PD0, B13 PD4, B14 PD6, B15 PD8, B16 PD10, B17 INT0, B18 RTCLKI, B19 VCLKI
- Row C: C1 VDDC1, C2 MCLKI, C3 GNDC1, C4 HSDP, C5 RW, C6 HADDR2, C7 HADDR1, C8 HCK, C9 HADDR0, C10 AV, C11 KBD4, C12 KBD7, C13 GNDP4, C14 PD2, C15 PD3, C16 VDDC0, C17 GNDC0, C18 VCLKO, C19 LFTV
- Row D: D1 GNDS0, D2 VDDS0, D3 DQ0, D4 DQ15, D5 FSDP, D6 SYNC, D7 VDDP5, D8 VDDC7, D9 EN, D10 KBD1, D11 KBD3, D12 KBD6, D13 PD1, D14 HD, D15 VD, D16 INT1, D17 GNDC3, D18 VDDC3, D19 VOUT2
- Row E: E1 DQ3, E2 DQ2, E3 DQ1, E4 DQ13, E5 DQ14, E6 INT4, E7 GNDP5, E8 GNDC7, E9 NWD_OVF, E10 KBD0, E11 KBD2, E12 KBD5, E13 VDDP4, E14 TMR3, E15 FI1, E16 AGND1, E17 AVDD1, E18 VREFV, E19 VOUT1
- Row F: F1 DQ4, F2 GNDS1, F3 VDDS1, F4 DQ11, F5 DQ12, F15 TMR2, F16 DISP17, F17 DISP16, F18 DISP15, F19 DISP14
- Row G: G1 VDDS2, G2 DQ6, G3 DQ5, G4 GNDS2, G5 DQ10, G15 TEST, G16 DISP19, G17 DISP18, G18 DISP13, G19 DISP12
- Row H: H1 LDQS, H2 UDQS, H3 DQ7, H4 DQ8, H5 DQ9, H15 PXOE, H16 DISP21, H17 DISP20, H18 DISP11, H19 DISP10
- Row J: J1 LDM, J2 VDDS3, J3 GNDS3, J4 UDM, J5 CS, J15 FLD, J16 DISP23, J17 DISP22, J18 DISP9, J19 PCLKO
- Row K: K1 RAS, K2 CAS, K3 WE, K4 VDDS4, K5 GNDS4, K15 GNDP3, K16 VDDP3, K17 DISP24, K18 DISP8, K19 DISP7
- Row L: L1 CK, L2 BA1, L3 CKE, L4 VDDC4, L5 GNDC4, L15 GNDC6, L16 VDDC6, L17 DISP25, L18 DISP6, L19 DISP5
- Row M: M1 CKN, M2 BA0, M3 MA13, M4 VDDS5, M5 GNDS5, M15 HBLK, M16 DISP27, M17 DISP26, M18 DISP4, M19 DISP3
- Row N: N1 MA0, N2 MA1, N3 MA12, N4 MA11, N5 MA10, N15 VBLK, N16 DISP29, N17 DISP28, N18 DISP2, N19 DISP1
- Row P: P1 VDDS6, P2 GNDS6, P3 MA9, P4 MA8, P5 MA7, P15 INT3, P16 NCS3, P17 DMARQ, P18 INTRQ, P19 DISP0
- Row R: R1 MA2, R2 MA3, R3 MA6, R4 VDDS7, R5 INT2, R6 TMR0, R7 WKP, R8 GNDP0, R9 FC21, R10 GNDC5, R11 FC16, R12 FC24, R13 GNDP1, R14 MRESET, R15 A10, R16 NCS2, R17 A11, R18 NCS1, R19 IORDY
- Row T: T1 GNDS7, T2 MA4, T3 MA5, T4 AGND0, T5 NTRST, T6 TMR1, T7 RXD1, T8 VDDP0, T9 FC22, T10 VDDC5, T11 FC12, T12 FC10, T13 VDDP1, T14 NWAIT, T15 A9, T16 A7, T17 A5, T18 A4, T19 A2
- Row U: U1 AVDD0, U2 AD3, U3 AD0, U4 TMS, U5 TCK, U6 NPCS1, U7 RXD0, U8 TXD1, U9 FC17, U10 FC15, U11 FC11, U12 FC9, U13 FC8, U14 NCS0, U15 A8, U16 A6, U17 GNDP2, U18 A3, U19 A1
- Row V: V1 VREFS, V2 AD2, V3 VREFAD, V4 TDI, V5 NPCS0, V6 MOSI, V7 TXD0, V8 FC19, V9 FC18, V10 FC14, V11 FC1, V12 FC3, V13 FC5, V14 FC7, V15 D9, V16 D11, V17 D13, V18 D15, V19 A0
- Row W: W1 AD1, W2 DA0, W3 VREFDA, W4 TDO, W5 SPCK, W6 MISO, W7 SCK, W8 FC20, W9 FC23, W10 FC13, W11 FC0, W12 FC2, W13 FC4, W14 FC6, W15 D8, W16 D10, W17 D12, W18 D14, W19 VDDP2

IS-5114

Figure 4-2. Package Mechanical Drawings

TOP VIEW

BOTTOM VIEW

TFBGA280

Ball Pitch :		Substrate Thickness :	
	0.80		0.21
Ball Diameter :		Mold Thickness :	
	0.45		0.53

all dimensions are in mm