406596354

	PA241CE PA241CEA	PA241DF PA241DFA
SUPPLY VOLTAGE, $+V_S$ to V_S	7	7
OUTPUT CURRENT, continuous within SOA	60 mA	60 mA
OUTPUT CURRENT, peak	120 mA	120 mA
POWER DISSIPATION, continuous @ T_C $ 8		8
INPUT VOLTAGE, differential	–16 V	–16 V
INPUT VOLTAGE, common mode	$–V_S$	$–V_S$
5L8633QJOTPMEFSmTFD	$	$
TEMPERATURE, junction[2]	$	$
5L8633UPSBHF	mUP$ mUP$	
5L8633(QPXSFEDBTF	mUP$ mUP$	

4184

PARAMETER	TEST CONDITIONS[1]	PA241CE, PA241DF MIN	TYP	MAX	PA241CEA MIN	TYP	MAX	UNITS
INPUT								
0"4[illegible]BM								N7
OFFSET VOLTAGE, vs. temperature[3]	UP$							7$
OFFSET VOLTAGE, vs. temperature[3]	UP$							7$
0"4[illegible]WTTVQQMZ								77
0"4[illegible]WTUJNF								7LI
BIAS CURRENT, initial[6]								Q"
4[illegible]WTTVQQMZ								Q7
OFFSET CURRENT, initial[6]								Q"
INPUT IMPEDANCE, DC			10^{11}					
16[illegible]								Q'
COMMON MODE, voltage range		$+V_S$m						7
COMMON MODE, voltage range		$-V_S$						7
COMMON MODE REJECTION, DC	V_{CM} 7%$							E#
NOISE, broad band	10kHz BW, R_S ,							73.4
0"4[illegible]SFRVFODZ	)[							7QQ
GAIN								
01[illegible]01BU[illegible]	3_L = ,							E#
[illegible]HBJOCBOEXEUIQSPEVDU								.)[
108[illegible]	7QQ							L)[
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$–V_S$ 12	$–V_S$ 10		$–V_S$ 10	$–V_S$m		V
CURRENT, peak[4]								N"
6[illegible]POUJOVPVT								N"
SETTLING TIME to .1%	10V step, A_V m							T
SLEW RATE	C_C Q'							7T
RESISTANCE , 1mA	R_{CL} =							æ
RESISTANCE , 40 mA	R_{CL}							æ
POWER SUPPLY								
7[illegible]								7
[illegible]TDFOU								N"
THERMAL								
PA241CE RESISTANCE, AC junction to case	F > 6)[							8
PA241DF RESISTANCE, AC junction to case	F > 6)[							8
PA241CE RESISTANCE, DC junction to case	F < 6)[							8
PA241DF RESISTANCE, DC junction to case	F < 6)[							8
1[illegible]VODUJPOUPBJS	'VMMUFNQFSBUVSFSBOHF							8
PA241DF RESISTANCE, junction to air[7]	'VMMUFNQFSBUVSFSBOHF							8
5L8633(QBTF	.FFUTGVMMSBOHFTQFDhT m							$

0[illegible] TQFDJBBUJPOJTUIFTBNFBTUIFOPOTQFDJBBUJPO

1. Unless otherwise noted T_C $ $_C$ = 6.8pF. DC input speci cations are – value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
   4BNQMFUFTUFECZXGFSUP
4. Guaranteed but not tested.
   5FTFMFDUFEWBMVFPG3must be added to the values given for total output resistance.
   4QFDJBBUJPOTTFQBSBUFECZJOEJDBUFWBMVFTGPSUIF18OE1%'SFTQFDUJWFMZ
7. Rating applies with solder connection of heatslug to a minimum 1 square inch foil area of the printed circuit board.

The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

ABSOLUTE MAXIMUM RATINGS

	PA241DW PA241DWA
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	7
OUTPUT CURRENT, continuous within SOA	60 mA
OUTPUT CURRENT, peak	120 mA
POWER DISSIPATION, continuous @ T_C = 25°C	8
INPUT VOLTAGE, differential	–16 V
INPUT VOLTAGE, common mode	$–V_S$
[illegible]	25°C
TEMPERATURE, junction[2]	25°C
[illegible]	mUP25°C
[illegible]	mUP25°C

ELECTRICAL CHARACTERISTICS

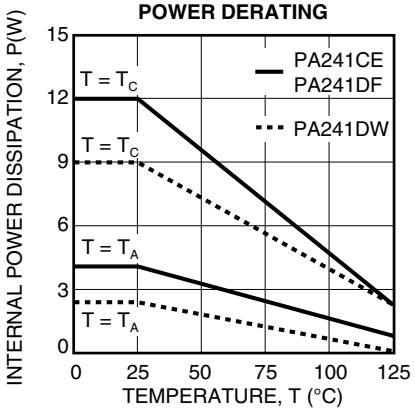
PARAMETER	TEST CONDITIONS[1]	PA241DW MIN	PA241DW TYP	PA241DW MAX	PA241DWA MIN	PA241DWA TYP	PA241DWA MAX	UNITS
INPUT								
[illegible]								N7
OFFSET VOLTAGE, vs. temperature[3]	UP25°C							7.5
OFFSET VOLTAGE, vs. temperature[3]	UP25°C							7.5
[illegible]								77
[illegible]								7LI
BIAS CURRENT, initial			100	2000				Q"
[illegible]								Q7
[illegible]								Q"
INPUT IMPEDANCE, DC			10^{11}					
[illegible]								Q’
COMMON MODE, voltage range		$+V_S$m						7
COMMON MODE, voltage range		$-V_S$						7
COMMON MODE REJECTION, DC	V_{CM} 7%25°C							E#
NOISE, broad band	10kHz BW, R_S ,							73.4
[illegible]	)[							7QQ
GAIN								
[illegible]	3_L = ,							E#
[illegible]								.)[
[illegible]	7QQ							L)[
OUTPUT								
VOLTAGE SWING	I_O = 40mA	$–V_S$ 12	$–V_S$ 10		$–V_S$ 10	$–V_S$m		V
CURRENT, peak[4]								N"
[illegible]								N"
SETTLING TIME to .1%	10V step, A_V m							T
SLEW RATE	C_C Q’							7T
RESISTANCE , 1mA	R_{CL} =							æ
RESISTANCE , 40 mA	R_{CL}							æ
POWER SUPPLY								
[illegible]								7
[illegible]								N"
THERMAL								
PA241DW RESISTANCE, AC junction to case	F > 6)[							[illegible]
PA241DW RESISTANCE, DC junction to case	F < 6)[							[illegible]
[illegible]	'VMMUFNQFSBUVSFSBOHF							[illegible]
[illegible]	.FFUTGVMMSBOHFTQFDhT m							$

NOTES:

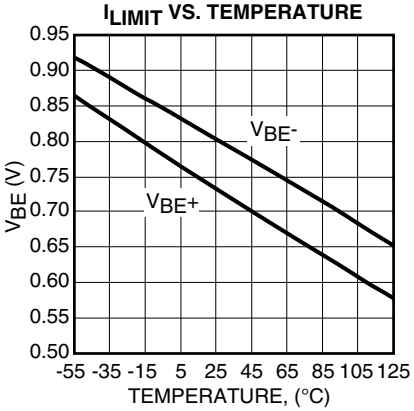
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are – value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. [illegible]
4. Guaranteed but not tested.
5. [illegible] must be added to the values given for total output resistance.

The PA241 is constructed from MOSFET transistors. ESD handling procedures must be observed.

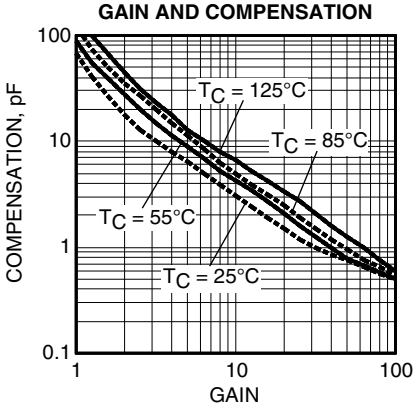
POWER DERATING



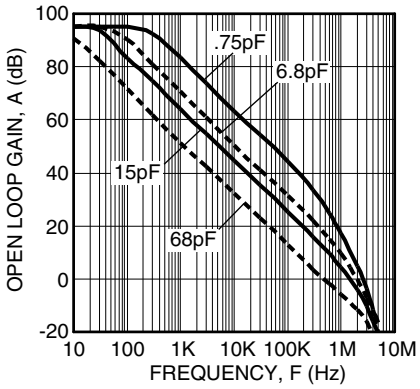
I_{LIMIT} VS. TEMPERATURE



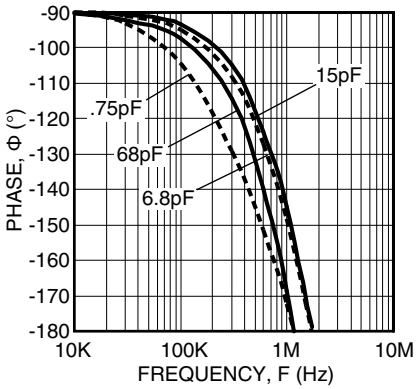
GAIN AND COMPENSATION



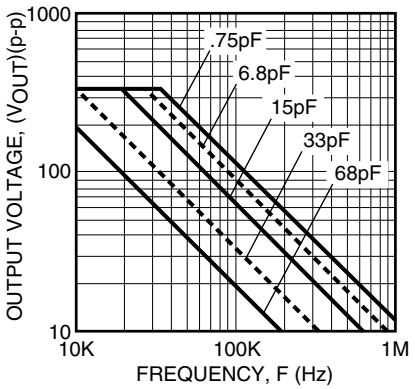
SMALL SIGNAL RESPONSE



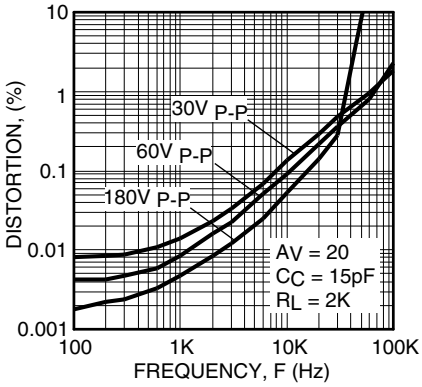
PHASE RESPONSE



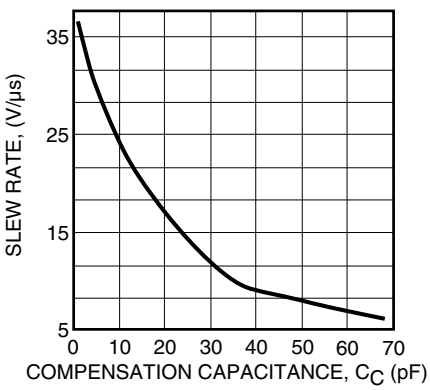
POWER RESPONSE



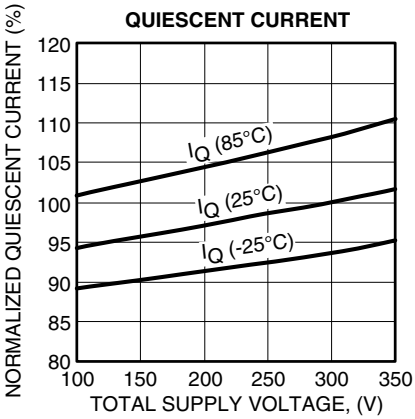
HARMONIC DISTORTION



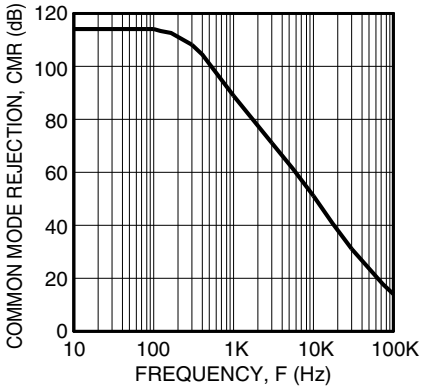
SLEW RATE



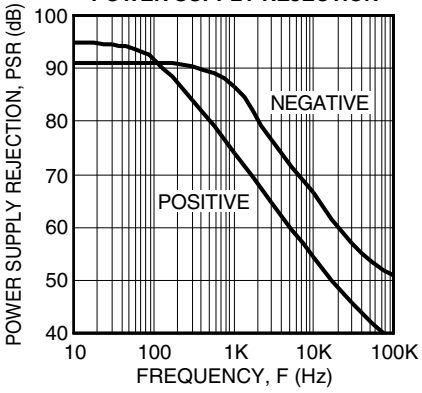
QUIESCENT CURRENT



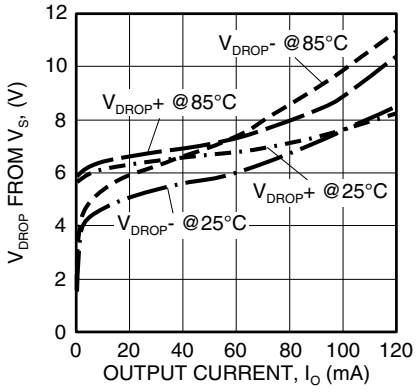
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



3

1MTSEMUPOPUOSM0SUOHPOTE-
FSBUJPOTXJDIDPWFSTTUBCJMJUZQPXFSTVQQMJFTIFBUTJOLJOH mounting, current limit, SOA interpretation, and speci cation interpretation. Visit www.Cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

1)'48.145/

Open loop gain and phase shift both increase with increasing temperature. The PHASE COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are CBTFEPOBDIJFWJOHBQIBTFNBSHJOPGBMDVMBUFUIFIJHIest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the nished circuit. The compensation capacitor must be rated for at least the total voltage applied to the ampli er and should be a temperature stable type such as NPO or COG.

0)5&4'5'8&4

There are two important concepts about closed loop gain when choosing compensation. They stem from the fact that XJMFHBJOJTUIFNPTUDPNNPOMZVTFEUFSβN (the feedback factor) is really what counts when designing for stability.

1. Gain must be calculated as a non-inverting circuit (equal input and feedback resistors can provide a signal gain of -1, but for calculating offset errors, noise, and stability, this is a gain of 2).
2. Including a feedback capacitor changes the feedback factor or gain of the circuit. Consider Rin=4.7k, Rf=47k for a gain of 11. Compensation of 4.7 to 6.8pF would be reasonable. Adding 33pF parallel to the 47k rolls off the circuit at 103kHz, BOEBU.)[BTSFEVDFEHBJOGSPNUPSPVHIMZBOE the circuit is likely to oscillate.

As a general rule the DC summing junction impedance (parallel combination of the feedback resistor and all input SFTJTUPSTTIPVMECFMJNJUFEUPLPINTPSMFTTFBNQMJFS input capacitance of about 6pF, plus capacitance of connecting traces or wires and (if used) a socket will cause undesirable circuit performance and even oscillation if these resistances are too high. In circuits requiring high resistances, measure or FTUJNBUFUIFUPUBMTVNQPJOUDBQBDJUBODFNVMUJQMZCZ3JO3CBOE parallel Rf with this value. Capacitors included for this purpose are usually in the single digit pF range. This technique results in equal feedback factor calculations for AC and DC cases. It does not produce a roll off, but merely keeps β constant over BXEFGSFRVFODZSBOHF1BSBHSBQIPG'QQMJDBUJPOPUF details suitable stability tests for the nished circuit.

6)33&5

For proper operation, the current limit resistor, Rcl, must be connected as shown in the external connection diagram. The NJOJNVNWBMVFJTPINTIPXFWFSGPSPQUJNVNSFMJBCJMJUZ the resistor should be set as high as possible. The maximum practical value is 110 ohms. Current limit values can be predicted as follows:

$$Ilimit = \frac{Vbe}{Rcl}$$

Where Vbe is shown in the CURRENT LIMIT typical graph.

Note that +Vbe should be used to predict current through the +Vs pin, -Vbe for current through the -Vs pin, and that they vary with case temperature. Value of the current limit resistor BUBDBTFUFNQFSBUVSFPGDBOCFFTUJNBUFEBTGPMMPX

$$Rcl = \frac{0.7}{Ilimit}$$

When the ampli er is current limiting, there may be spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the ampli er, value of the current limit resistor, and the load. The oscillation will cease as the ampli er comes out of current limit.

4'&1&3&

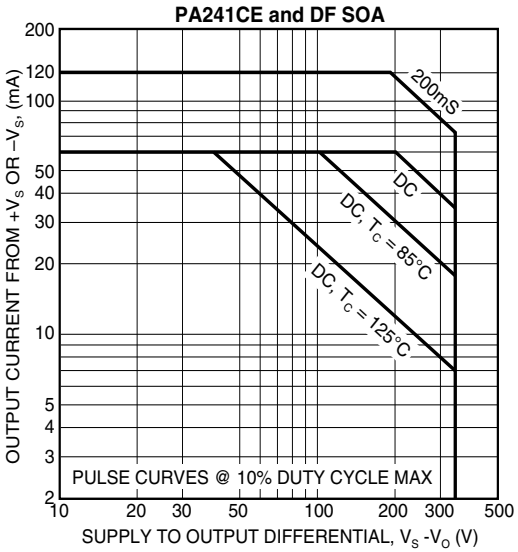
The MOSFET output stage of the PA241 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

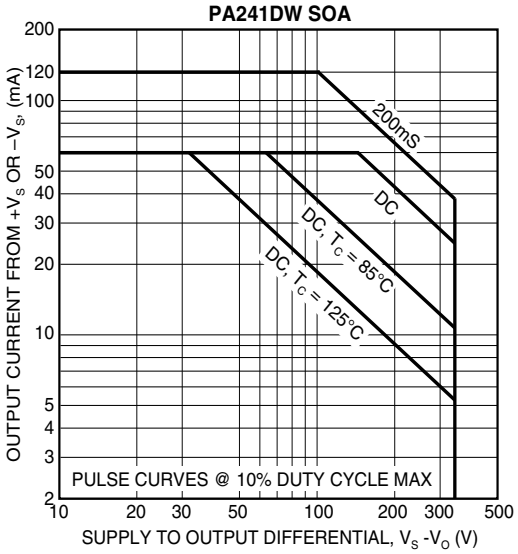
1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metalization.
3. Temperature of the output MOSFETS.

These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown GPS B DBTF UFNQFSBUVSF PG $BOE DPSSFTQPOE UP UIFSNBM SFTJTUBODFTPG$GPSUIF$BOE%'BOE$ for the PA241DW respectively. Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient yback by the parasitic diodes of the output stage MOSFET structure. However, for protection against sustained high energy yback external fast-recovery diodes must be used.

)&(

The PA241DF package has a large exposed integrated copper heatslug to which the monolithic ampli er is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area on the printed circuit board will result JOUIFSNBMQFSGPSNBODFPG$KVODUJPOUPBJSSBUJOHPGUIF PA241DF. Solder connection to an area of 1 to 2 square inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow UIFUFNQFSBUVSFUPFYDFFE$





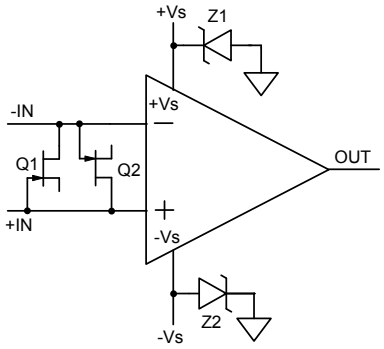


FIGURE 1

0[illegible]

Although the PA241 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

11-[illegible]

For additional technical information please refer to the following Application Notes:
AN1: General Operating Considerations
AN3: Bridge Circuit Drives
[illegible]
AN38: Loop Stability with Reactive Loads

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