

# Single-chip Type with Built-in FET Switching Regulator Series

## Output 1.5A or Less High-efficiency Step-down Switching Regulator with Built-in Power MOSFET


**BD8312HFN**

No.10027ECT04

### ● Description

BD8312HFN produces step-down output including 1.2, 1.8, 3.3, or 5 V from 4 batteries, batteries such as Li2cell or Li3cell, etc. or a 5V/12V fixed power supply line.

This IC allows easy production of small power supply by a wide range of external constants, and is equipped with an external coil/capacitor downsized by high frequency operation of 1.5 MHz, built-in synchronous rectification SW capable of withstanding 15 V, and flexible phase compensation system on board.

### ● Features

- 1) Incorporates Pch/Nch synchronous rectification SW capable of withstanding 1.0 A/15V.
- 2) Incorporates phase compensation device between input and output of Error AMP.
- 3) Small coils and capacitors to be used by high frequency operation of 1.5MHz
- 4) Input voltage 3.5 V – 14 V  
Output current 1.2A(7.4V input, 3.3V output)  
0.8A(4.5V input, 3.3V output)
- 5) Incorporates soft-start function.
- 6) Incorporates timer latch system short protecting function.
- 7) As small as 2.9mm×3 mm, SON 8-pin package HSON8

### ● Application

For portable equipment like DSC/DVC powered by 4 dry batteries or Li2cell and Li3cell, or general consumer-equipment with 5 V/12 V lines

### ● Operating Conditions (Ta = 25°C)

Parameter	Symbol	Voltage circuit	Unit
Power supply voltage	VCC	3.5 to 14	V
Output voltage	VOUT	1.2 to 12	V

### ● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Maximum applied power voltage	VCC, PVCC	15	V
Maximum input current	Iinmax	1.0	A
Power dissipation	Pd	630	mW
Operating temperature range	Topr	−25 to +85	°C
Storage temperature range	Tstg	−55 to +150	°C
Junction temperature	Tjmax	+150	°C

\*1 When used at Ta = 25°C or more installed on a 70×70×1.6mm board, the rating is reduced by 5.04mW/°C.

\* These specifications are subject to change without advance notice for modifications and other reasons.

## ●Electrical Characteristics

(Unless otherwise specified, Ta = 25 °C, VCC = 7.4 V)

Parameter	Symbol	Target Value			Unit	Conditions	
		Min	Typ	Max			
[Low voltage input malfunction preventing circuit]							
Detection threshold voltage	VUV	-	2.9	3.2	V	VREG monitor	
Hysteresis range	$\Delta VUV_{hy}$	100	200	300	mV		
[Oscillator]							
Oscillation frequency	Fosc	1.38	1.5	1.62	MHz		
[Regulator]							
Output voltage	VREG	4.65	5.0	5.35	V		
[Error AMP]							
INV threshold voltage	VINV	0.99	1.00	1.01	V		
Input bias current	IINV	-50	0	50	nA	VCC=12.0V, VINV=6.0V	
Soft-start time	Tss	3.2	5.3	7.4	msec		
[PWM comparator]							
LX Max Duty	Dmax	-	-	(※)100	%		
[Output]							
PMOS ON resistance	RONP	-	450	600	m $\Omega$		
NMOS ON resistance	RONN	-	300	420	m $\Omega$		
Leak current	Ileak	-1	0	1	$\mu$ A		
[STB]							
STB pin control voltage	Operation	VSTBH	2.5	-	11	V	
	No-operation	VSTBL	-0.3	-	0.3	V	
STB pin pull-down resistance		250	400	700	k $\Omega$		
[Circuit current]							
Standby current	VCC pin	ISTB1	-	-	1	$\mu$ A	
	PVCC pin	ISTB2	-	-	1	$\mu$ A	
Circuit current at operation VCC		-	600	900	$\mu$ A	VINV=1.2V	
Circuit current at operation PVCC		-	30	50	$\mu$ A	VINV=1.2V	

(※)100% is MAX Duty as behavior of a PWM comparator.

Using in region where High side PMOS is 100% on state as application circuit causes detection of SCP then DC/DC converter stops.

© Not designed to be resistant to radiation

●Description of Pins

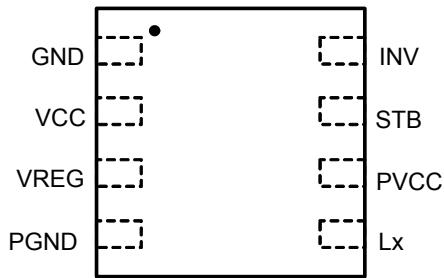


Fig.1 Terminal layout

Pin No.	Pin Name	Function
1	GND	Ground terminal
2	VCC	Control part power input terminal
3	VREG	5 V output terminal of regulator for internal circuit
4	PGND	Power transistor ground terminal
5	Lx	Coil connecting terminal
6	PVCC	DC/DC converter input terminal
7	STB	ON/OFF terminal
8	INV	Error AMP input terminal

●Block Diagram

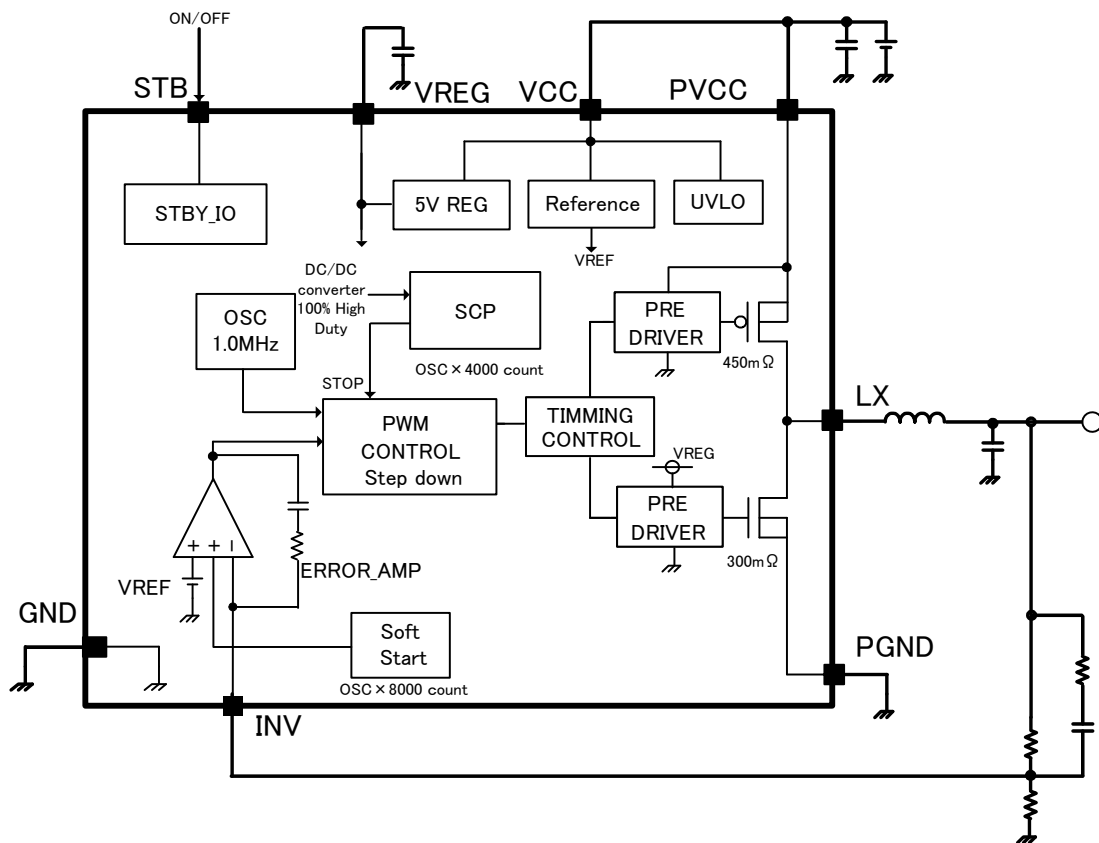


Fig.2 Block diagram

**●Description of Blocks**

1. Reference  
This block produces ERROR AMP standard voltage.  
The standard voltage is 1.0 V.
2. 5 V Reg  
5 V low saturation regulator for internal analog circuit  
BD8312HFN is equipped with this regulator for the purpose of protecting the internal circuit from high voltage. Therefore, this output is reduced when VCC is less than 5 V, then PMOS ON resistance increases and Power efficiency and Maximum output current of DC/DC converter decreases in this region. Please see attached data (fig14,15,16,17) about increasing of PMOS ON resistance in this region.
3. UVLO  
Circuit for preventing low voltage malfunction  
Prevents malfunction of the internal circuit at activation of the power supply voltage or at low power supply voltage.  
Monitors VCC pin voltage to turn off all output FET and DC/DC converter output when VCC voltage is lower than 2.9 V, and reset the timer latch of the internal SCP circuit and soft-start circuit. This threshold contains 200 mV hysteresis.
4. SCP  
Timer latch system short-circuit protection circuit  
When DC/DC converter is 100% High Duty, the internal SCP circuit starts counting.  
The internal counter is in synch with OSC, the latch circuit is activated about 2.7 msec after the counter counts about 4000 oscillations to turn off DC/DC converter output.  
To reset the latch circuit, turn off the STB pin once. Then, turn it on again or turn on the power supply voltage again.
5. OSC  
Circuit for oscillating sawtooth waves with an operation frequency fixed at 1.5 MHz
6. ERROR AMP  
Error amplifier for detecting output signals and output PWM control signals  
The internal standard voltage is set at 1.0 V.  
A primary phase compensation device of 200 pF, 62 kΩ is built in-between the inverting input terminal and the output terminal of this ERROR AMP.
7. PWM COMP  
Voltage-pulse width converter for controlling output voltage corresponding to input voltage  
Comparing the internal SLOPE waveform with the ERROR AMP output voltage, PWM COMP controls the pulse width to the output to the driver.
8. SOFT START  
Circuit for preventing in-rush current at startup by bringing the output voltage of the DC/DC converter into a soft-start  
Soft-start time is in synch with the internal OSC, and the output voltage of the DC/DC converter reaches the set voltage after about 8000 oscillations.
9. PRE DRIVER/TIMING CONTROL  
CMOS inverter circuit for driving the built-in synchronous rectification SW  
The synchronous rectification OFF time for preventing feedthrough is about 25 nsec.
10. STBY\_IO  
Voltage applied on STB pin (7 pin) to control ON/OFF of IC  
Turned ON when a voltage of 2.5 V or higher is applied and turned OFF when the terminal is open or 0 V is applied.  
Incorporates approximately 400 kΩ pull-down resistance.
11. Pch/Nch FET SW  
Built-in synchronous rectification SW for switching the coil current of the DC/DC converter  
Incorporates a 450 mΩ PchFET SW capable of withstanding 15 V. and 300 mΩ SW capable of withstanding 15 V.  
Since the current rating of this FET is 1.0A, it should be used within 1.0A including the DC current and ripple current of the coil.

●Reference data

(Unless otherwise specified, Ta = 25°C, VCC = 7.4 V)

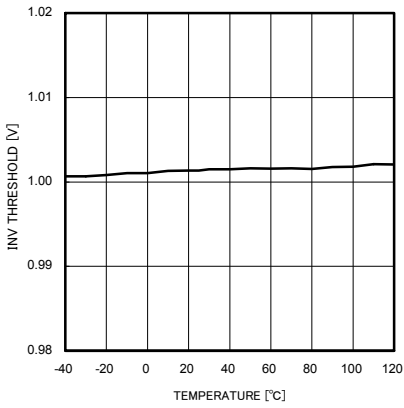


Fig.3. INV threshold temperature property

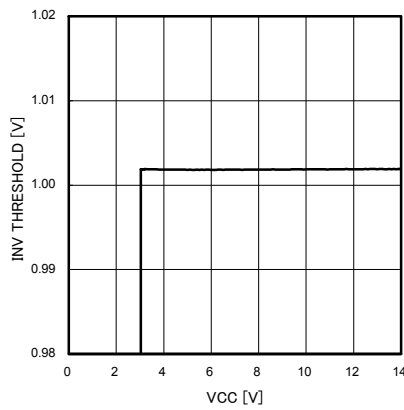


Fig.4. INV threshold power supply property

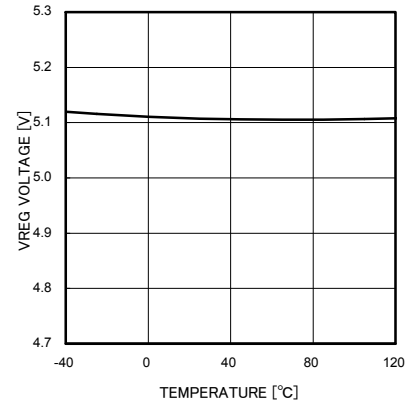


Fig.5. VREG output temperature property

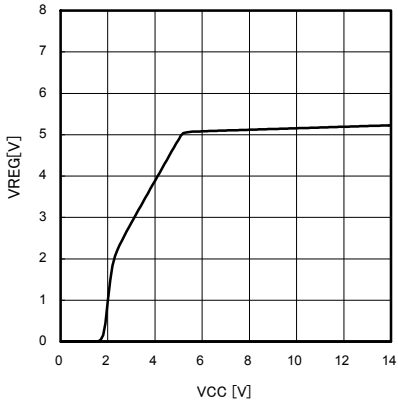


Fig.6. VREG output power supply property

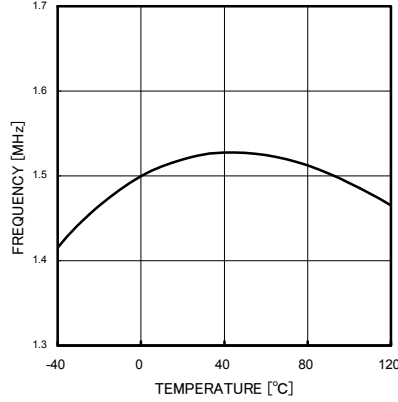


Fig.7. fosc temperature property

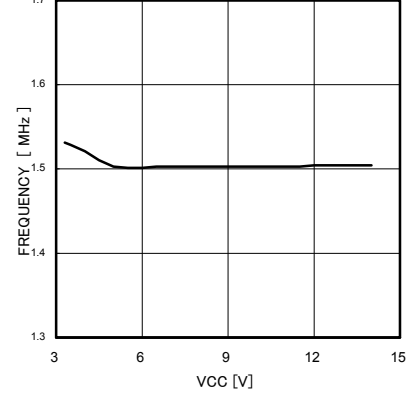


Fig.8. fosc voltage property

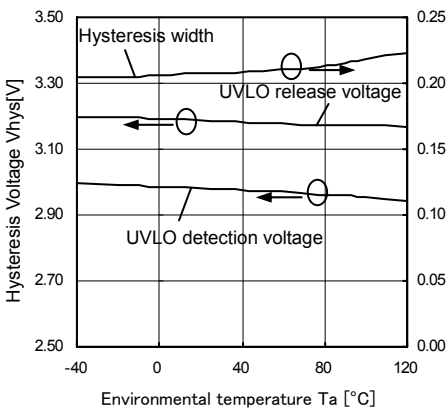


Fig.9. UVLO threshold temperature property

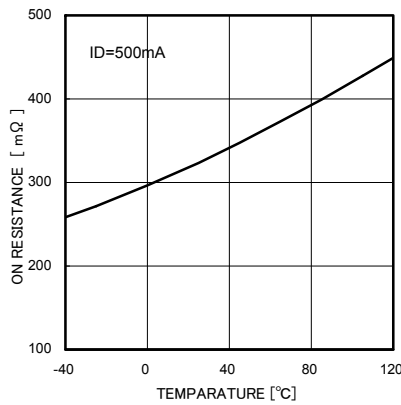


Fig.10. Nch FET ON resistance temperature property

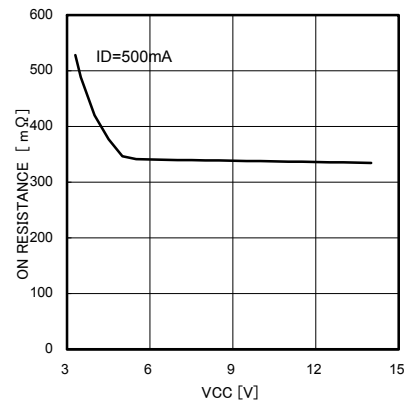


Fig.11. Nch FET ON resistance power supply property

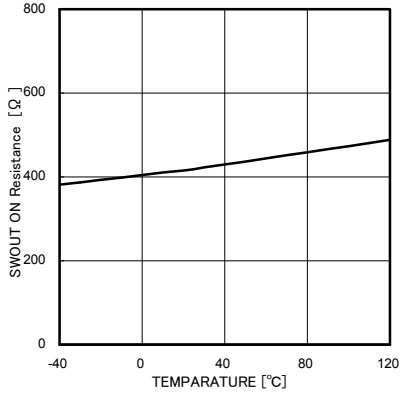


Fig.12. Pch FET ON resistance temperature property

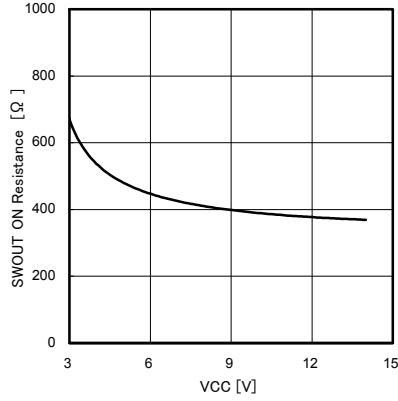


Fig.13. Pch FET ON resistance power supply property

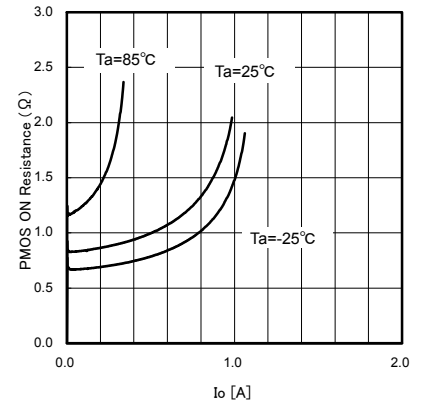


Fig.14. PchFET ON resistance Io property [VCC=3.5V]

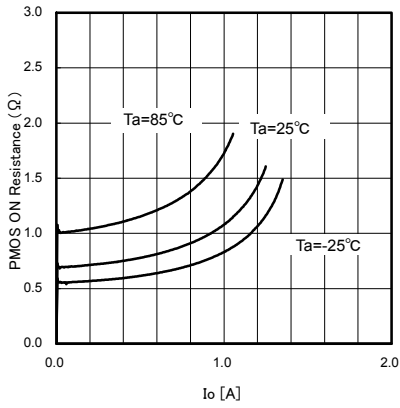


Fig.15. PchFET ON resistance Io property [VCC=4.0V]

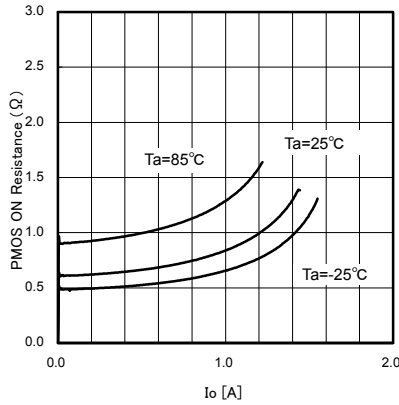


Fig.16. PchFET ON resistance Io property [VCC=4.5V]

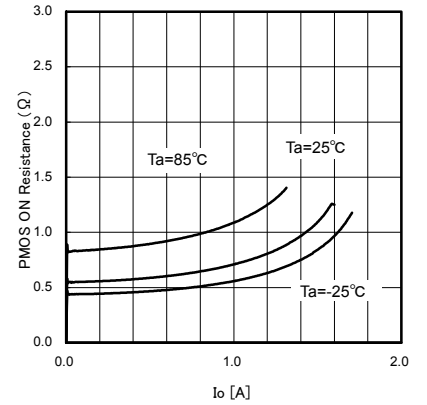


Fig.17. PchFET ON resistance Io property [VCC=5.0V]

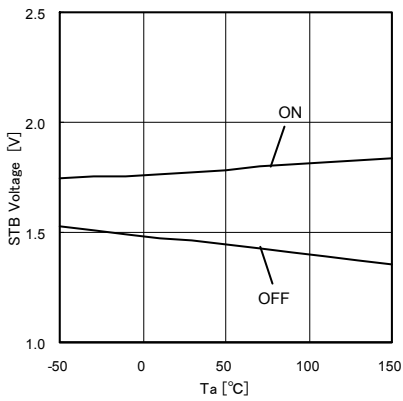


Fig.18. STB threshold temperature property

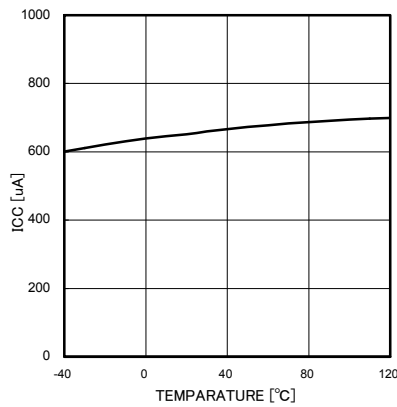


Fig.19. Circuit current temperature property

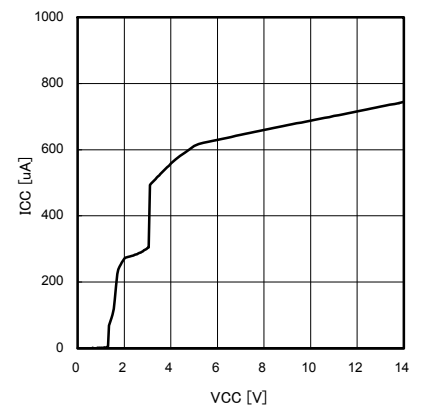


Fig.20. Circuit current voltage property

●Example of Application Input: 4.5 to 10 V, output: 3.3 V / 500mA

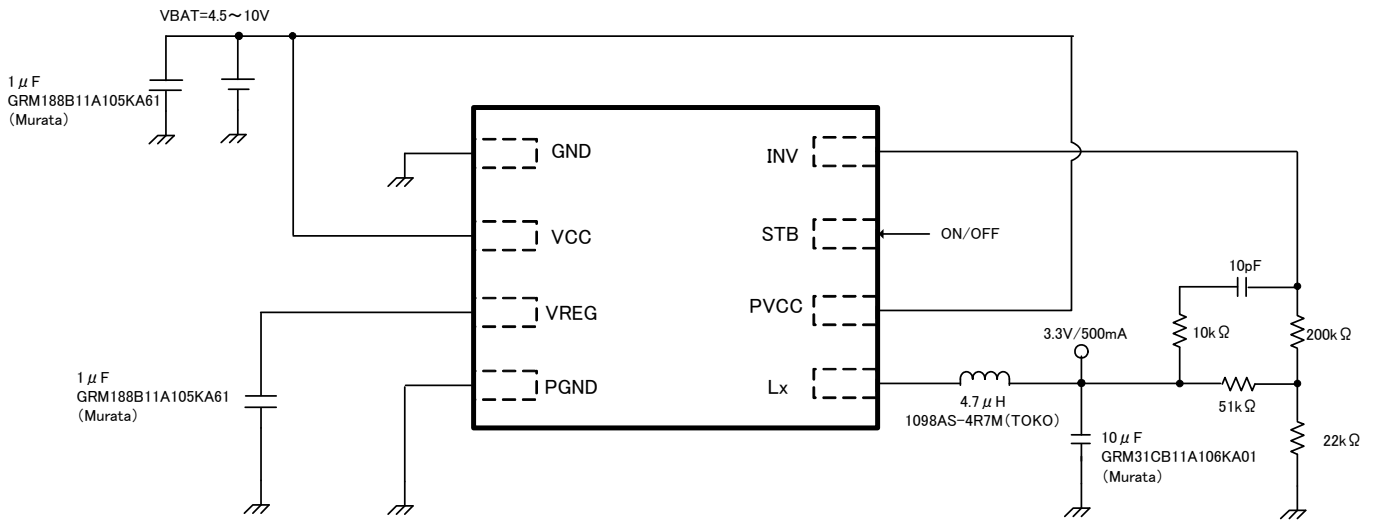


Fig.21 Reference application diagram

●Reference application data 1

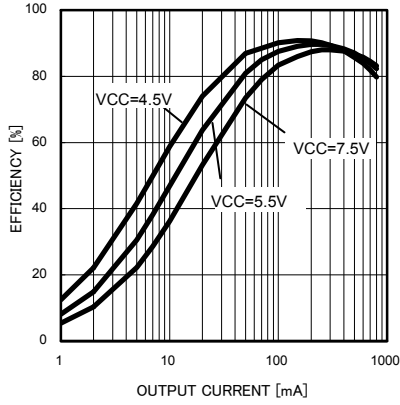


Fig.22 Power conversion efficiency (VOUT = 3.3 V)

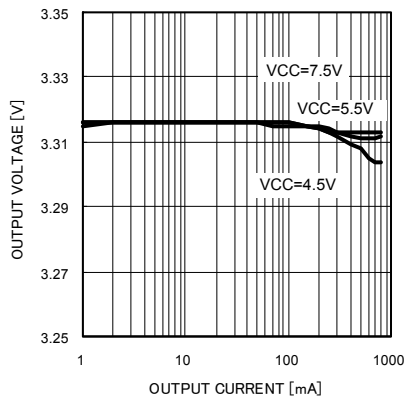


Fig.23 Load regulation (VOUT = 3.3 V)

●Reference application data 2 (Input 4.5 V, 6.0 V, 8.4 V, 10 V, output 3.3 V )

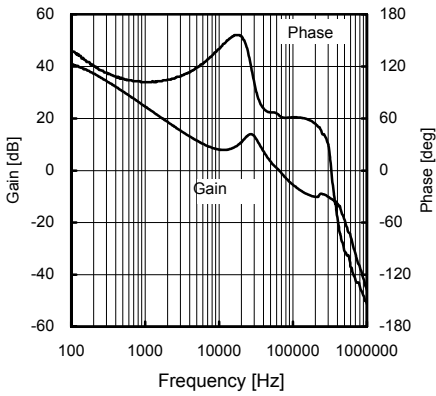


Fig.24 Frequency response 1 (VCC=4.5V, Io=250mA)

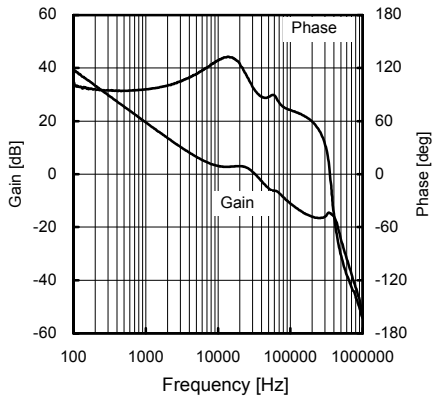


Fig.25 Frequency response 2 (VCC=6.0V, Io=250mA)

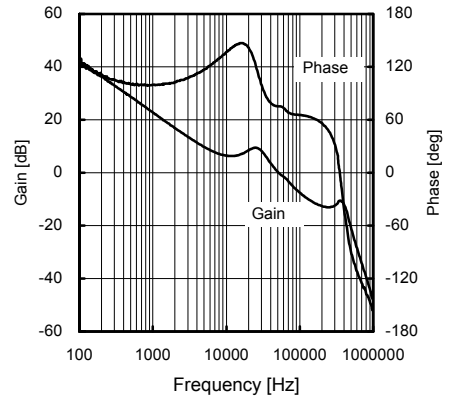


Fig.26 Frequency response 3 (VCC=8.4V, Io=250mA)

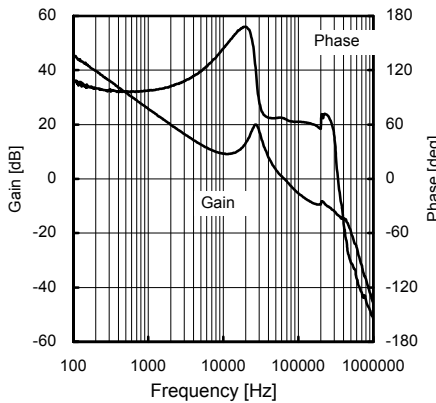


Fig.27 Frequency response 4 (VCC=10V, Io=250mA)

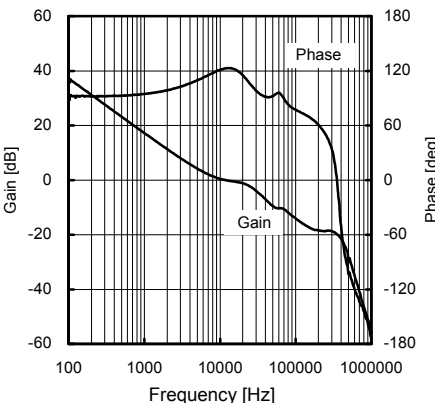


Fig.28 Frequency response 5 (VCC=4.5V, Io=500mA)

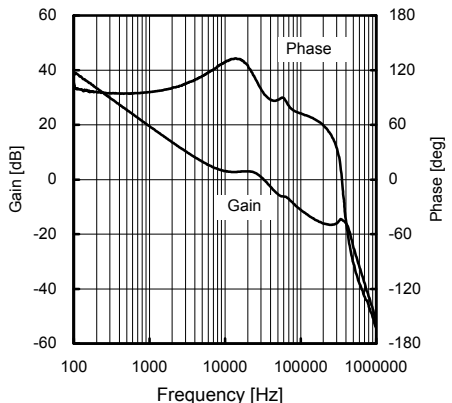


Fig.29 Frequency response 6 (VCC=6.0V, Io=500mA)

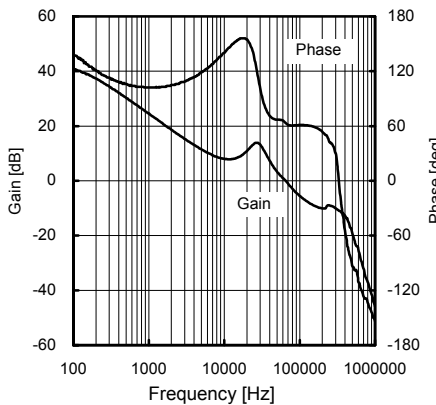


Fig.30 Frequency response 7 (VCC=8.4V, Io=500mA)

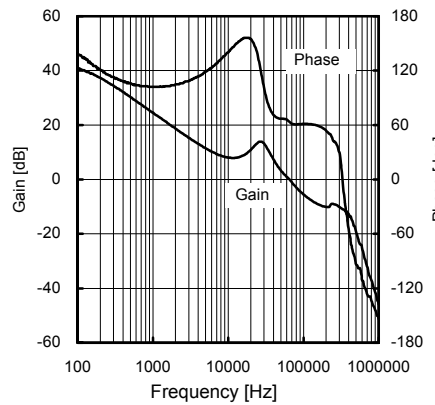
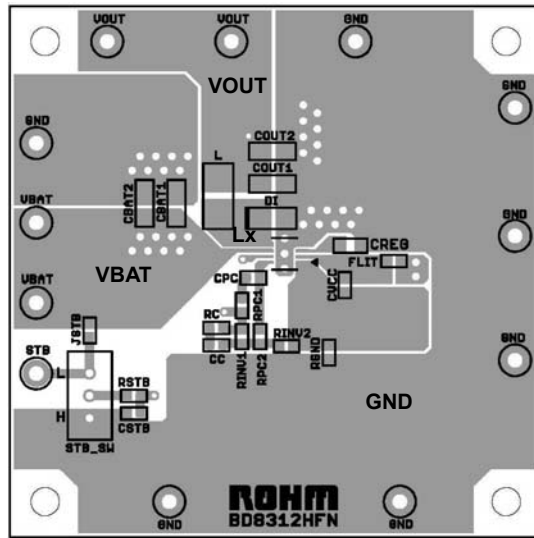


Fig.31 Frequency response 8 (VCC=10V, Io=500mA)



●Reference board pattern



- The radiation plate on the rear should be a GND flat surface of low impedance in common with the PGND flat surface.
- It is recommended to install a GND pin in another system as shown in the drawing without connecting it directly to this PNGD.
- Produce as wide a pattern as possible for the VBAT, Lx and PGND lines in which large current flows.

●Selection of Part for Applications

(1) Inductor

A shielded inductor that satisfies the current rating (current value, I<sub>pecac</sub> as shown in the drawing below) and has a low DCR (direct resistance component) is recommended. Inductor values affect inductor ripple current, which will cause output ripple. Ripple current can be reduced as the coil L value becomes larger and the switching frequency becomes higher.

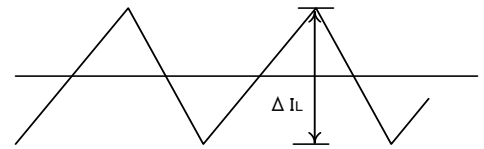


Fig.32 Inductor current

$$I_{peak} = I_{out} + \Delta I_L / 2 \text{ [A]} \tag{1}$$

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} \times \frac{V_{out}}{V_{in}} \times \frac{1}{f} \text{ [A]} \tag{2}$$

(η: Efficiency, ΔIL: Output ripple current, f: Switching frequency)

As a guide, inductor ripple current should be set at about 20 to 50% of the maximum input current.

\*Current over the coil rating flowing in the coil brings the coil into magnetic saturation, which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

(2) Output capacitor

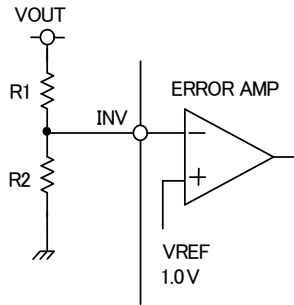
A ceramic capacitor with low ESR is recommended for output in order to reduce output ripple. There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration. Output ripple voltage is acquired by the following equation.

$$V_{pp} = \Delta I_L \times \frac{1}{2\pi \times f \times C_o} + \Delta I_L \times R_{ESR} \text{ [V]} \dots \tag{3}$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

(3) Output voltage setting

The internal standard voltage of the ERROR AMP is 1.0 V. Output voltage is acquired by Equation (4).



$$V_o = \frac{(R_1 + R_2)}{R_2} \times 1.0 \text{ [V]} \dots (4)$$

Fig.33 Setting of voltage feedback resistance

(4) DC/DC converter frequency response adjustment system

Condition for stable application

The condition for feedback system stability under negative feedback is that the phase delay is 135° or less when gain is 1 (0dB).

Since DC/DC converter application is sampled according to the switching frequency, the bandwidth GBW of the whole system (frequency at which gain is 0 dB) must be controlled to be equal to or lower than 1/10 of the switching frequency. In summary, the conditions necessary for the DC/DC converter are:

- Phase delay must be 135° or lower when gain is 1 (0 dB).
- Bandwidth GBW (frequency when gain is 0 dB) must be equal to or lower than 1/10 of the switching frequency.

To satisfy those two points, R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>, D<sub>s</sub> and R<sub>s</sub> in Fig. 34 should be set as follows.

[1] R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>

BD8313HFN incorporates phase compensation devices of R<sub>4</sub>=62kΩ and C<sub>2</sub>=200pF. These C<sub>2</sub> and R<sub>1</sub>, R<sub>2</sub>, and R<sub>3</sub> values decide the primary pole that determines the bandwidth of DC/DC converter.

Primary pole point frequency

$$f_p = \frac{1}{2\pi \left\{ A \times \left( \frac{R_1 \times R_2}{R_1 + R_2} + R_3 \right) \times C_2 \right\}} \dots (1)$$

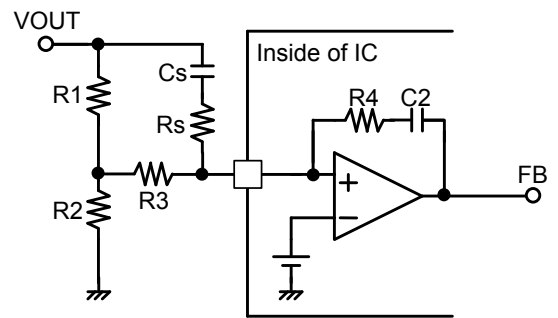


Fig.34 Example of phase compensation setting

DC/DC converter DC Gain

$$\text{DC Gain} = A \times \frac{1}{B} \times \frac{V_{IN}}{V_O} \dots (2)$$

- A: Error AMP Gain  
About 100dB = 10<sup>5</sup>
- B: Oscillator amplification = 0.5
- V<sub>IN</sub>: Input voltage
- V<sub>OUT</sub>: Output voltage

By Equations (1) and (2), the frequency f<sub>sw</sub> of point 0 dB under limitation of the bandwidth of the DC gain at the primary pole point is as shown below.

$$f_{sw} = f_p \times \text{DC Gain} = \frac{1}{2\pi C_2 \times \left( \frac{R_1 \cdot R_2}{R_1 + R_2} + R_3 \right)} \times \frac{1}{B} \times \frac{V_{IN}}{V_O} \dots (3)$$

It is recommended that f<sub>sw</sub> should be approx. 10 kHz. When load response is difficult, it may be set at approx. 20 kHz. By Equation (3), R<sub>1</sub> and R<sub>2</sub>, which determine the voltage value, will be in the order of several hundred kΩ. If an appropriate resistance value is not available since the resistance is so high and routing may cause noise, the use of R<sub>3</sub> enables easy setting.

[2] Cs and Rs setting

For DC/DC converter, the 2nd dimension pole point is caused by the coil and capacitor as expressed by the following equation.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad \dots \dots (4)$$

This secondary pole causes a phase rotation of 180°. To secure the stability of the system, put a zero point in 2 places to perform compensation.

Zero point by built-in CR  $f_{z1} = \frac{1}{2\pi R_4 C_2} = 13\text{kHz} \quad \dots \dots (5)$

Zero point by Cs  $f_{z1} = \frac{1}{2\pi(R_1+R_3)C_s} \quad \dots \dots (6)$

Setting  $f_{z2}$  to be half to 2 times a frequency as large as  $f_{LC}$  provides an appropriate phase margin. It is desirable to set  $R_s$  at about 1/20 of  $(R_1+R_3)$  to cancel any phase boosting at high frequencies.

Those pole points are summarized in the figure below. The actual frequency property is different from the ideal calculation because of part constants. If possible, check the phase margin with a frequency analyzer or network analyzer. Otherwise, check for the presence or absence of ringing by load response waveform and also check for the presence or absence of oscillation under a load of an adequate margin.

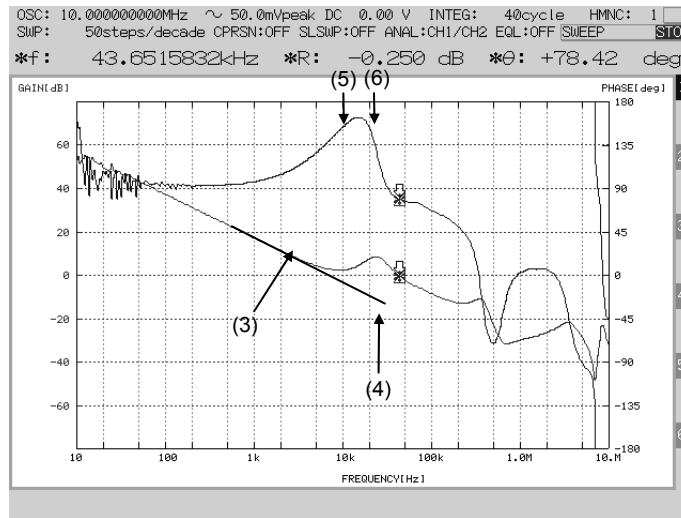
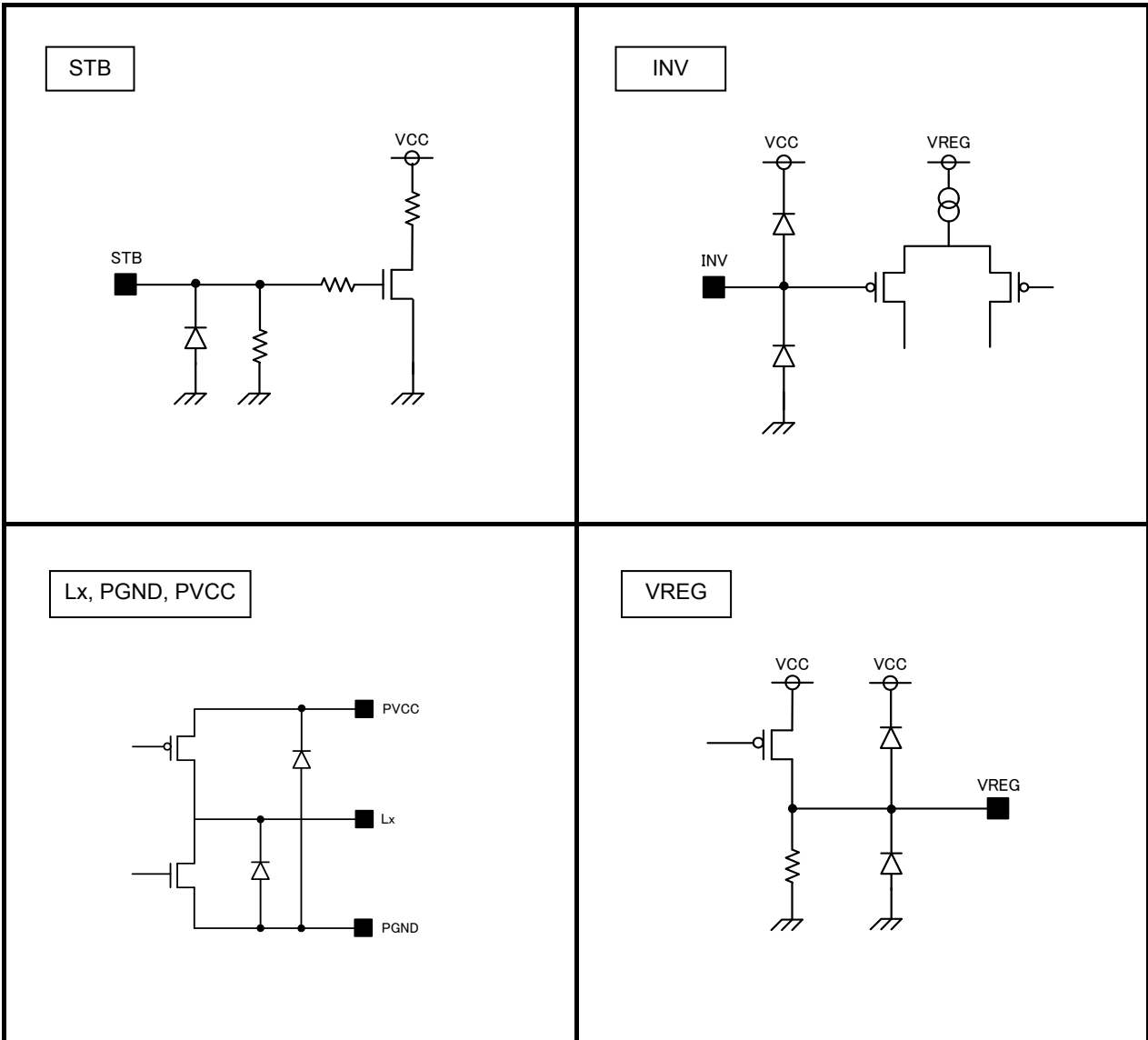


Fig.35 Example of DC/DC converter frequency property (Measured with FRA5097 by NF Corporation)

●I/O Equivalence Circuit



### ●Notes for use

#### 1) Absolute Maximum Rating

We dedicate much attention to the quality control of these products, however the possibility of deterioration or destruction exists if the impressed voltage, operating temperature range, etc., exceed the absolute maximum ratings. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. If a special mode exceeding the absolute maximum rating is expected, please review matters and provide physical safety means such as fuses, etc.

#### 2) GND Potential

Keep the potential of the GND pin below the minimum potential at all times.

#### 3) Thermal Design

Work out the thermal design with sufficient margin taking power dissipation (Pd) in the actual operation condition into account.

#### 4) Short Circuit between Pins and Incorrect Mounting

Attention to IC direction or displacement is required when installing the IC on a PCB. If the IC is installed in the wrong way, it may break. Also, the threat of destruction from short-circuits exists if foreign matter invades between outputs or the output and GND of the power supply.

#### 5) Operation under Strong Electromagnetic Field

Be careful of possible malfunctions under strong electromagnetic fields.

#### 6) Common Impedance

When providing a power supply and GND wirings, show sufficient consideration for lowering common impedance and reducing ripple (i.e., using thick short wiring, cutting ripple down by LC, etc.) as much as you can.

#### 7) Thermal Protection Circuit (TSD Circuit)

This IC contains a thermal protection circuit (TSD circuit). The TSD circuit serves to shut off the IC from thermal runaway and does not aim to protect or assure operation of the IC itself. Therefore, do not use the TSD circuit for continuous use or operation after the circuit has tripped.

#### 8) Rush Current at the Time of Power Activation

Be careful of the power supply coupling capacity and the width of the power supply and GND pattern wiring and routing since rush current flows instantaneously at the time of power activation in the case of CMOS IC or ICs with multiple power supplies.

#### 9) IC Terminal Input

This is a monolithic IC and has P+ isolation and a P substrate for element isolation between each element. P-N junctions are formed and various parasitic elements are configured using these P layers and N layers of the individual elements.

For example, if a resistor and transistor are connected to a terminal as shown on Fig.36:

- The P-N junction operates as a parasitic diode when  $GND > (\text{Terminal A})$  in the case of a resistor or when  $GND > (\text{Pin B})$  in the case of a transistor (NPN)
- Also, a parasitic NPN transistor operates using the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when  $GND > (\text{Pin B})$ .

The parasitic element consequently rises under the potential relationship because of the IC's structure. The parasitic element pulls interference that could cause malfunctions or destruction out of the circuit. Therefore, use caution to avoid the operation of parasitic elements caused by applying voltage to an input terminal lower than the GND (P board), etc.

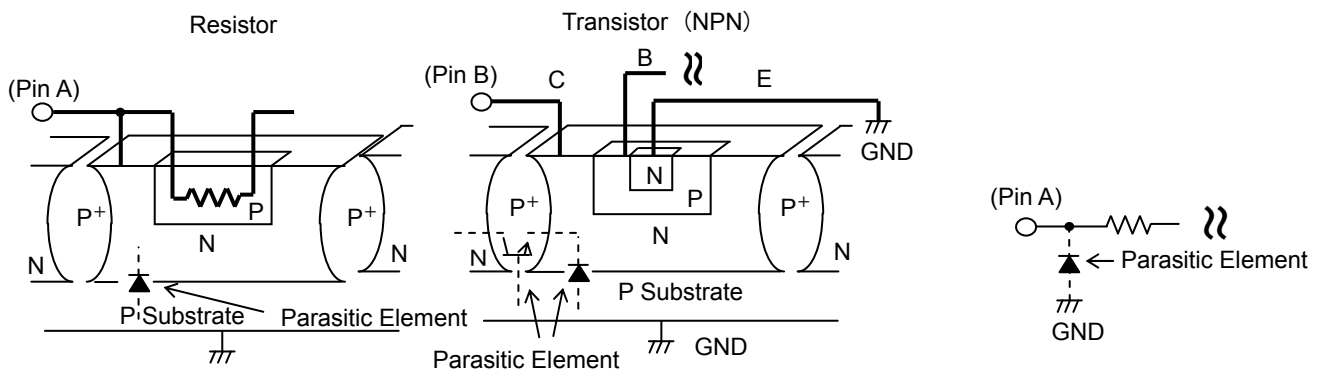


Fig.36 Example of simple structure of Bipolar IC

● Ordering part number

B	D
---	---

Part No.

8	3	1	2
---	---	---	---

Part No.

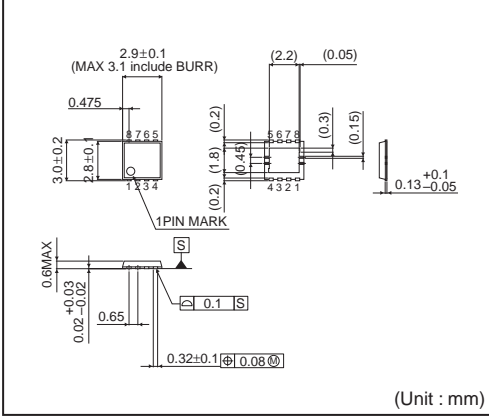
H	F	N
---	---	---

Package  
HFN:HS0N8

T	R
---	---

Packaging and forming specification  
TR: Embossed tape and reel

HS0N8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR ( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand )

\* Order quantity needs to be multiple of the minimum quantity.

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