

# RNA51958A, B

REJ03D0915-0302

Rev.3.02

## Voltage Detecting, System Resetting IC Series

Apr 01, 2010

### Description

RNA51958A,B are semiconductor integrated circuits for resetting of all types of logic circuits such as CPUs, and has the feature of setting the detection voltage by adding external resistance.

They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor.

They find extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

### Features

- Few external parts
- Large delay time with a capacitor of small capacitance ( $t_d \approx 100$  ms, at  $0.33 \mu\text{F}$ )
- Wide supply voltage range: 2 V to 17 V
- Wide application range
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA51958AFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51958APT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Reel)	0 (Ni/Pd/Au)
RNA51958BFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51958BPT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Reel)	0 (Ni/Pd/Au)

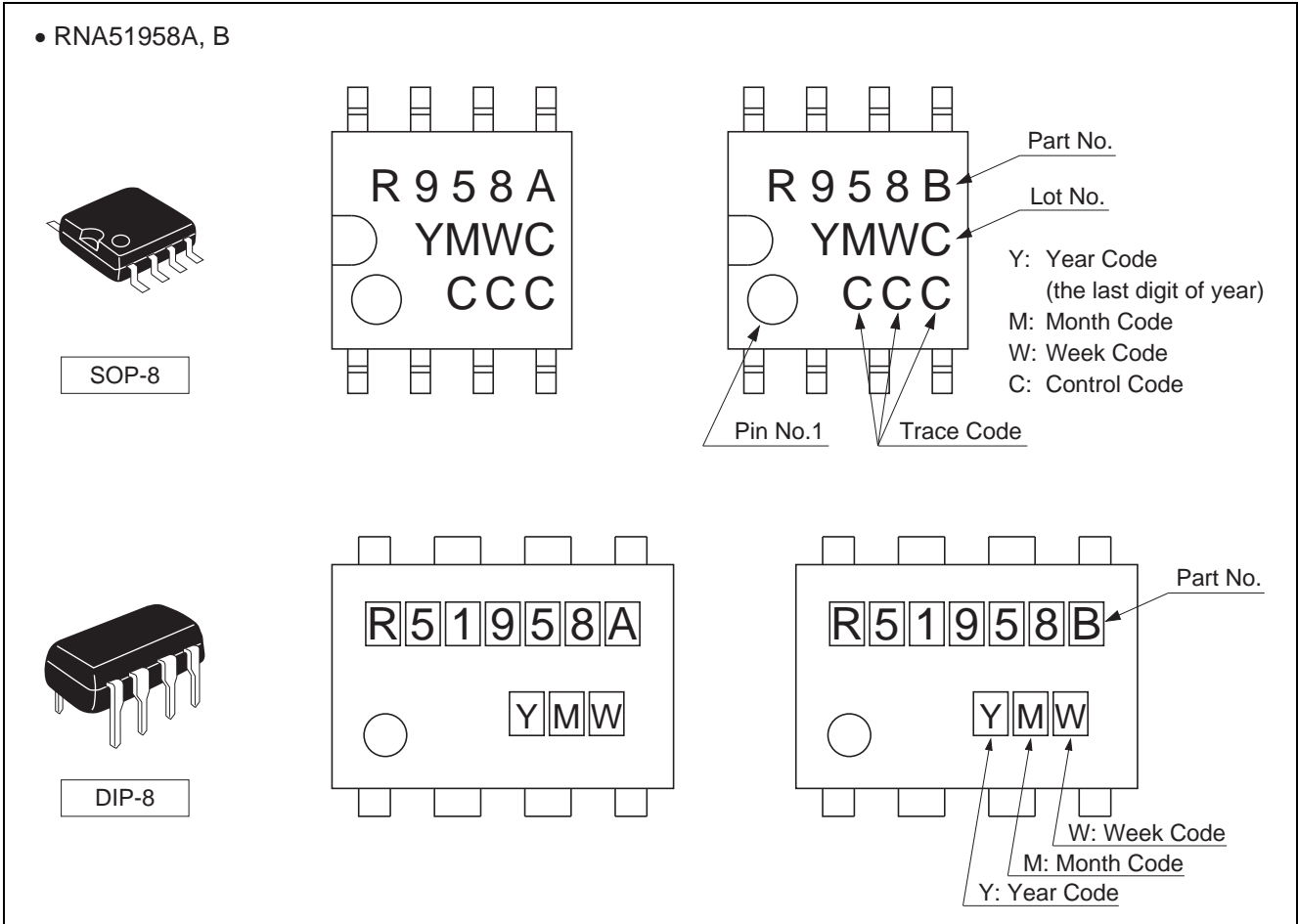
### Application

- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit

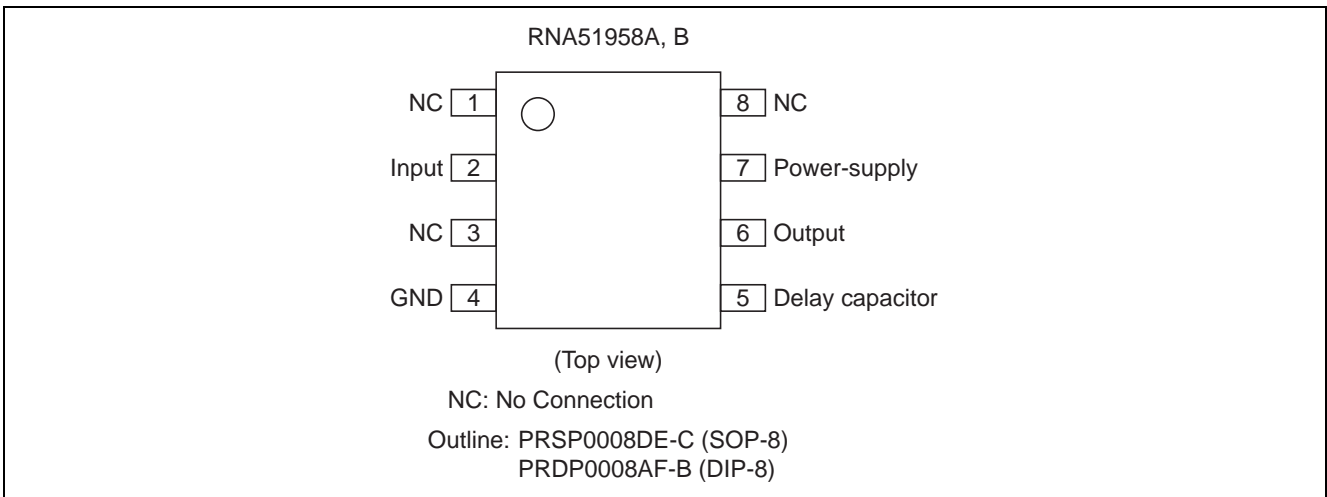
### Recommended Operating Condition

- Supply voltage range: 2 V to 17 V

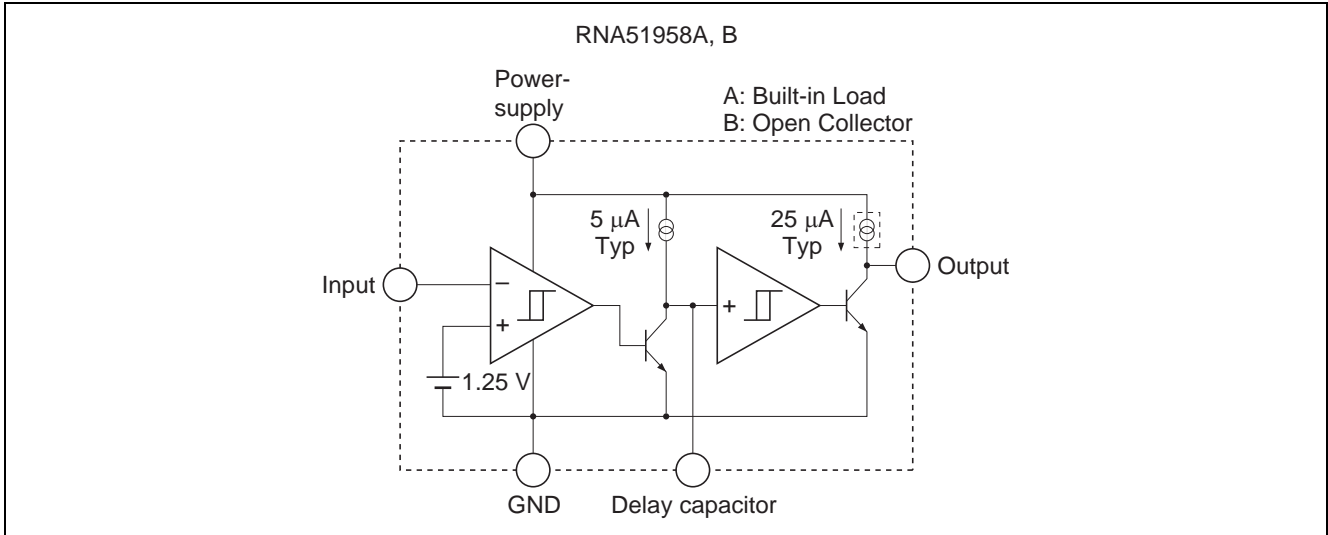
Outline and Article Indication



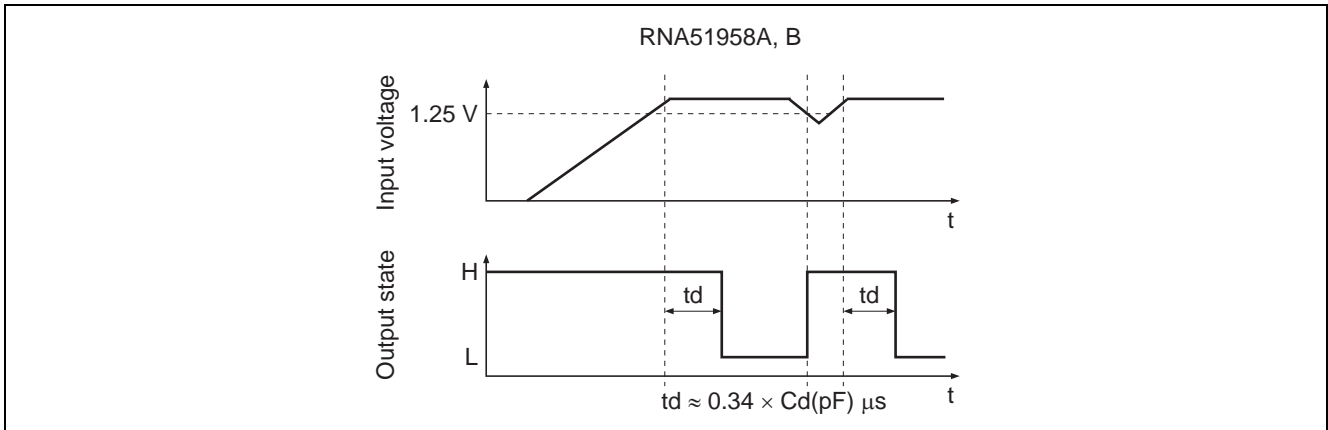
Pin Arrangement



### Block Diagram



### Operating Waveform



## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	18	V	
Output sink current	I <sub>sink</sub>	6	mA	
Output voltage	V <sub>O</sub>	V <sub>CC</sub>	V	Type A (output with constant current load)
		18		Type B (open collector output)
Power dissipation	P <sub>d</sub>	400	mW	8-pin SOP (PRSP0008DE-C)
		570		8-pin DIP (PRDP0008AF-B)
Thermal derating	K <sub>θ</sub>	4.4	mW/°C	8-pin SOP (PRSP0008DE-C)
		8.3		8-pin DIP (PRDP0008AF-B)
Operating temperature	T <sub>opr</sub>	-40 to +85	°C	Refer to the thermal derating curve.
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	
Input voltage range	V <sub>IN</sub>	-0.3 to V <sub>CC</sub>	V	V <sub>CC</sub> ≤ 7 V
		-0.3 to +7		V <sub>CC</sub> > 7 V

## Electrical Characteristics

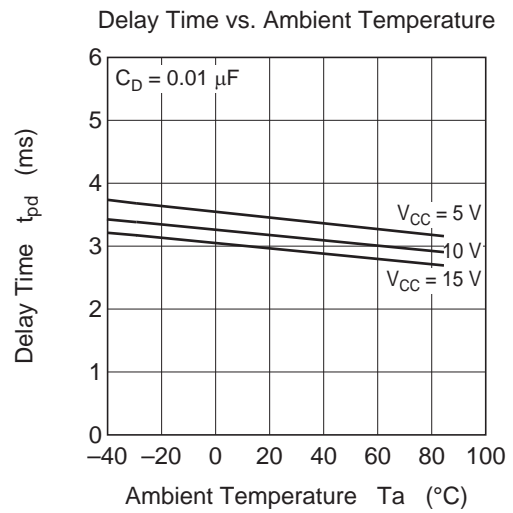
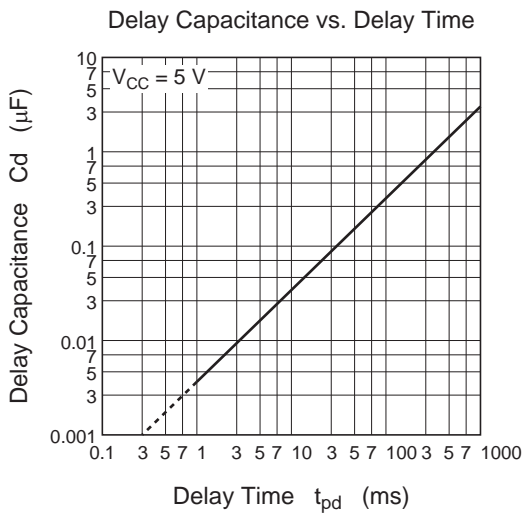
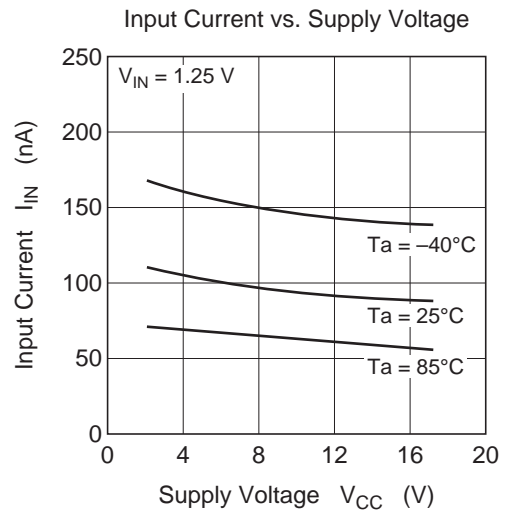
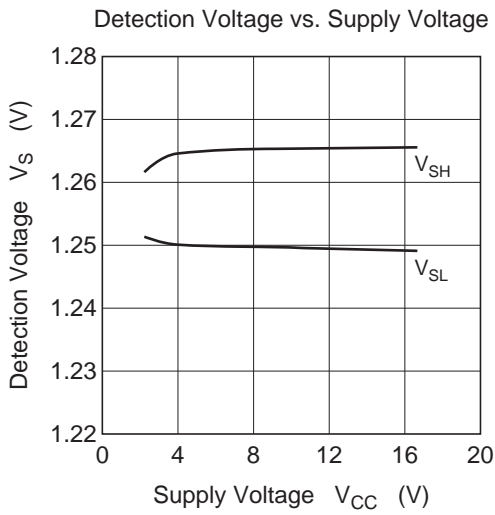
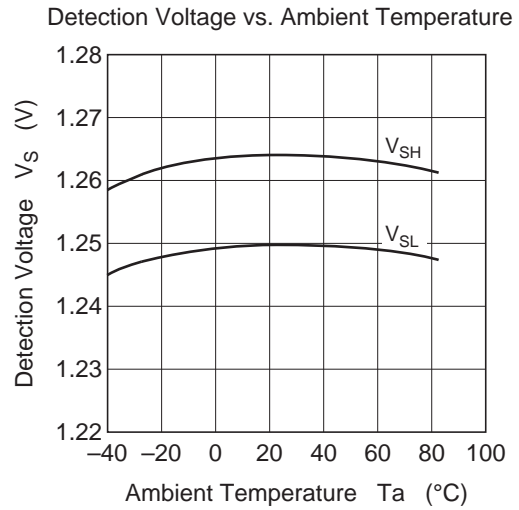
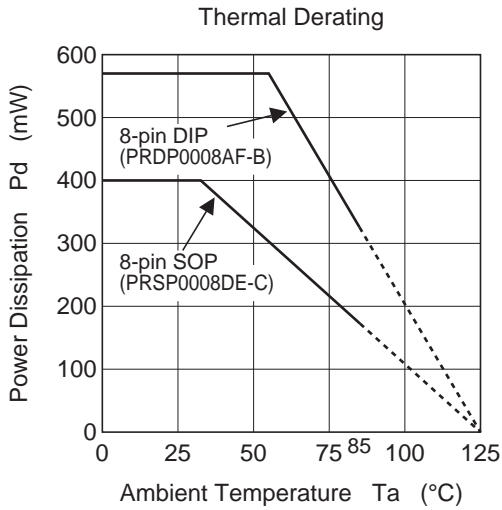
(Ta = 25°C, unless otherwise noted)

- “H” reset type

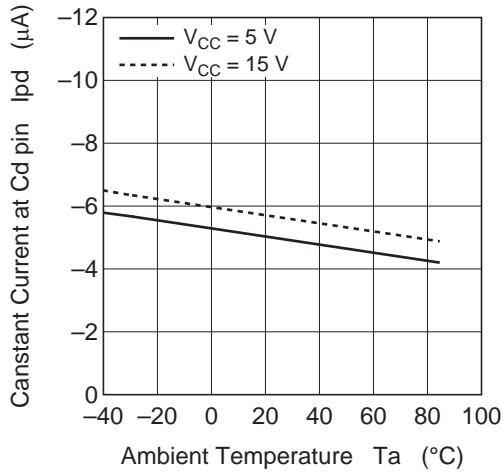
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detecting voltage	V <sub>s</sub>	1.20	1.25	1.30	V	
Hysteresis voltage	ΔV <sub>s</sub>	9	15	23	mV	V <sub>CC</sub> = 5V
Detecting voltage temperature coefficient	V <sub>s</sub> /ΔT	—	0.01	—	%/°C	
Supply voltage range	V <sub>CC</sub>	2	—	17	V	
Input voltage range	V <sub>in</sub>	-0.3	—	V <sub>CC</sub>	V	V <sub>CC</sub> ≤ 7V
		-0.3	—	7.0		V <sub>CC</sub> > 7V
Input current	I <sub>in</sub>	—	100	500	nA	V <sub>in</sub> = 1.25V
Circuit current	I <sub>CC</sub>	—	390	590	μA	Type A, V <sub>CC</sub> = 5V
		—	360	540		Type B, V <sub>CC</sub> = 5V
Delay time	t <sub>pd</sub>	1.6	3.4	7.0	ms	C <sub>d</sub> = 0.01 μF *
Constant current	I <sub>pd</sub>	-8	-5	-3	μA	V <sub>CC</sub> = 5V
Output saturation voltage	V <sub>sat</sub>	—	0.2	0.4	V	V <sub>CC</sub> = 5V, V <sub>in</sub> < 1.35V, I <sub>sink</sub> = 4mA
Output leakage current	I <sub>OH</sub>	—	—	30	nA	Type B
Output load current	I <sub>OC</sub>	-40	-25	-17	μA	Type A, V <sub>CC</sub> = 5V, V <sub>O</sub> = 1/2 × V <sub>CC</sub>
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.2	V <sub>CC</sub> -0.06	—	V	Type A

Note: Please set the desired delay time by attaching capacitor of the range between 4700 pF and 10 μF.

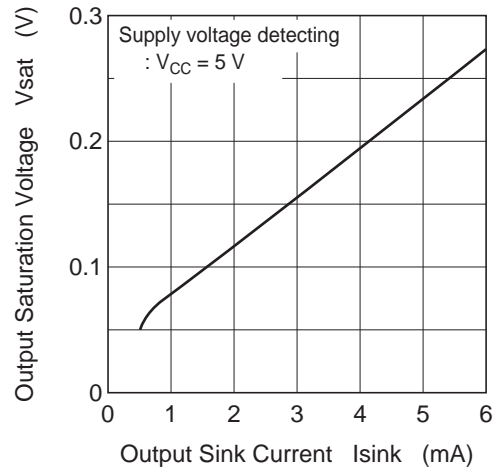
Typical Characteristics



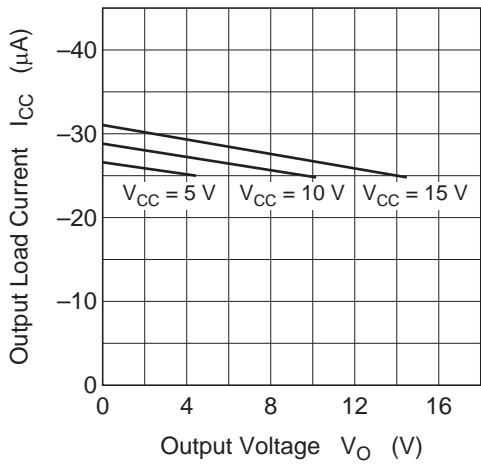
Constant Current at Cd pin vs. Ambient Temperature



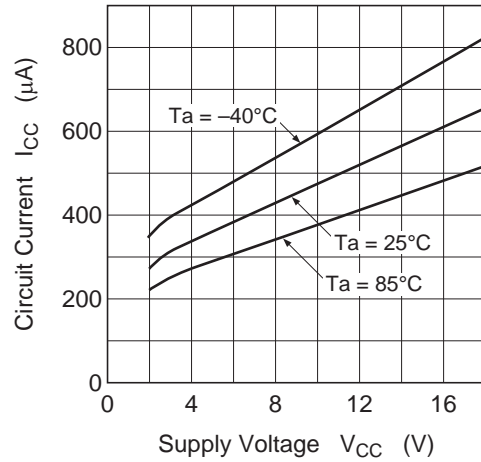
Output Saturation Voltage vs. Output Sink Current



Output Load Current vs. Output Voltage (RNA51958A)

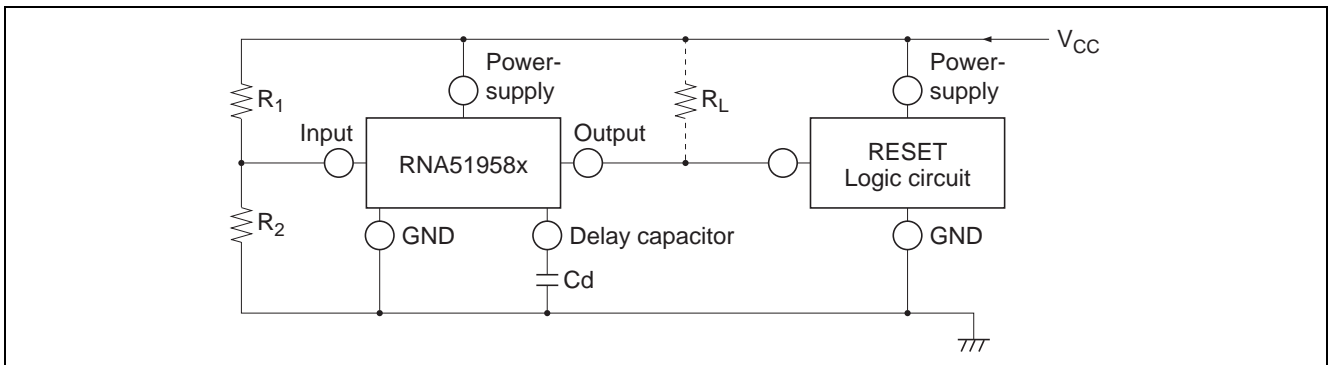


Circuit Current vs. Supply Voltage (RNA51958B)



## Example of Application Circuit

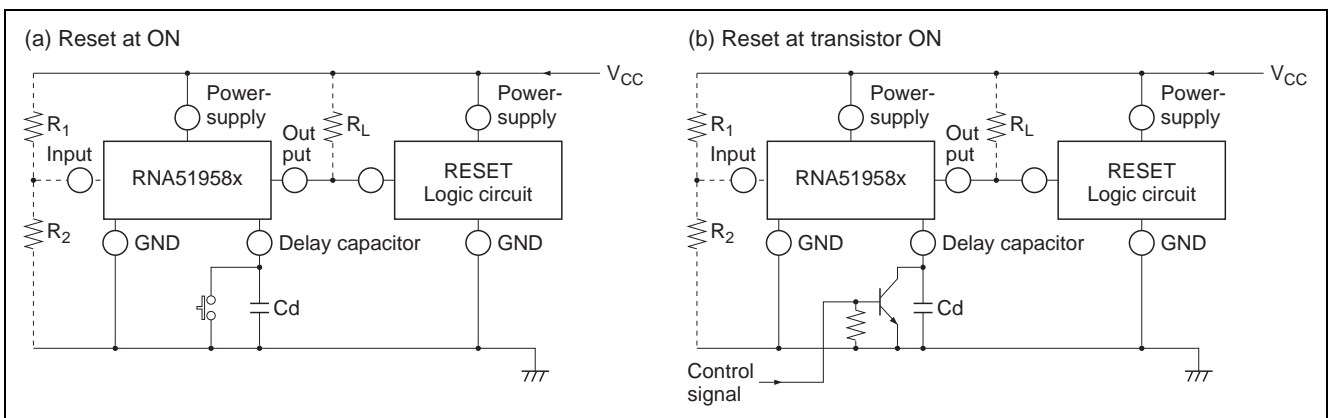
### Reset Circuit of RNA51958



**Figure 1 Reset Circuit of RNA51958**

- Notes:
1. When the detecting supply voltage is 4.25 V, RNA51953 are used. In this case,  $R_1$  and  $R_2$  are not necessary. When the voltage is anything except 4.25 V, RNA51957 and RNA51958 are used. In this case, the detecting supply voltage is  $1.25 \times (R_1 + R_2) / R_2$  (V) approximately. The detecting supply voltage can be set between 2 V and 15 V.
  2. If a longer delay time is necessary, RNA51953, RNA51957, RNA51958 are used. In this case, the delay time is about  $0.34 \times C_d$  (pF)  $\mu$ s.
  3. If the RNA51958 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
  4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor  $R_L$  to overcome the pull-down resistor.
  5. When the reset terminal in the logic circuit is of the low reset type, RNA51953 and RNA51957 are used and when the terminal is of the high reset type, RNA51958 are used.
  6. When a negative supply voltage is used, the supply voltage side of RNA51958 and the GND side are connected to negative supply voltage respectively.

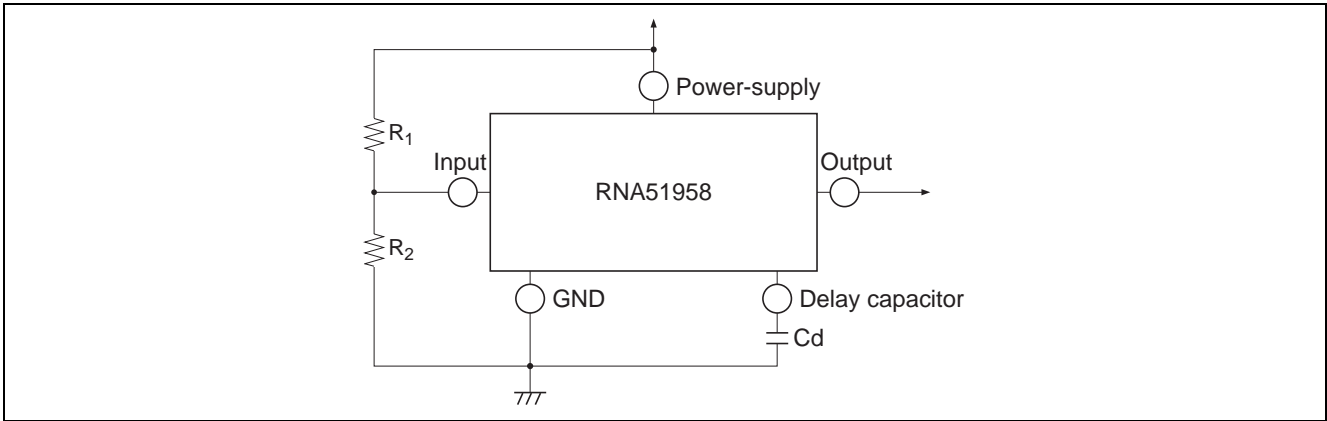
### Case of Using Reset Signal except Supply Voltage in the RNA51958



**Figure 2 Case of Using Reset Signal except Supply Voltage in the RNA51958**

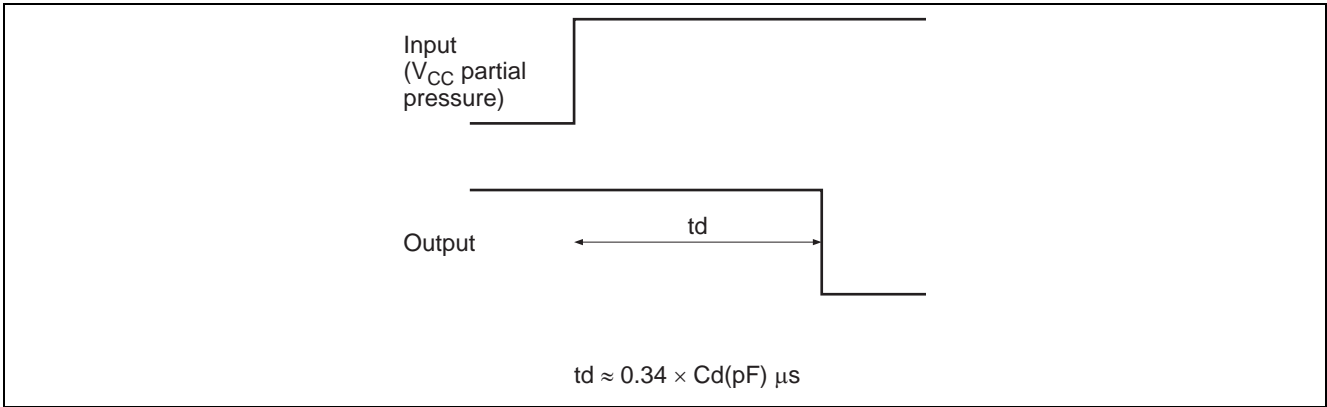
**Delay Waveform Generating Circuit**

When RNA51958 are used, a waveform with a large delay time can generate only by adding a small capacitor.



**Figure 3 Delay Waveform Generating Circuit**

**Operating Waveform**



**Figure 4 Operating Waveform**



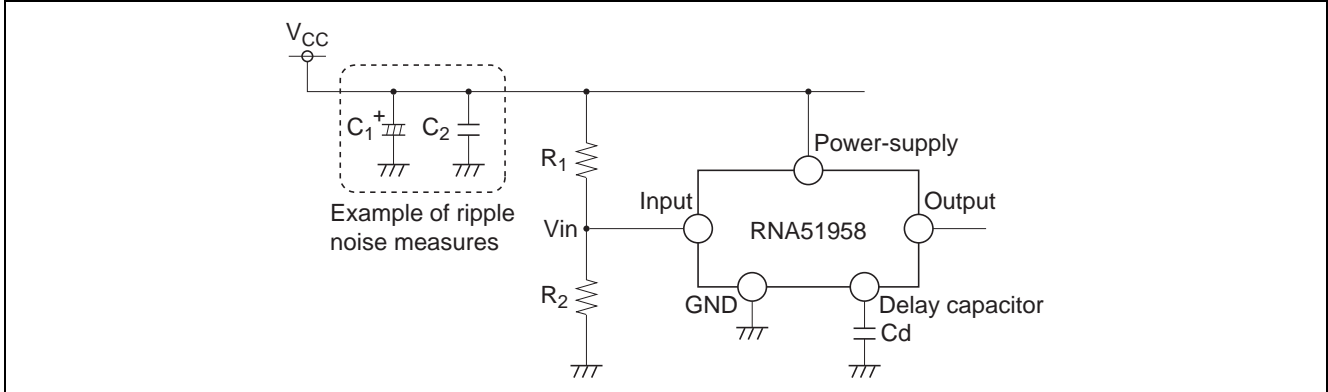
## Notice for use

### About the Power Supply Line

1. About bypass capacitor

Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.

Therefore, please install  $C_1$  and  $C_2$  for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 5.



**Figure 5 Example of Ripple Noise Measures**

2. The sequence of voltage impression

Please do not impress the voltages to the input terminals earlier than the power supply terminal. Moreover, please do not open the power supply terminal with the voltage impressed to the input terminal.

(The setting of the bias of an internal circuit collapses, and a parasitic element might operate.)

### About the Input Terminal

1. Setting range of input voltage

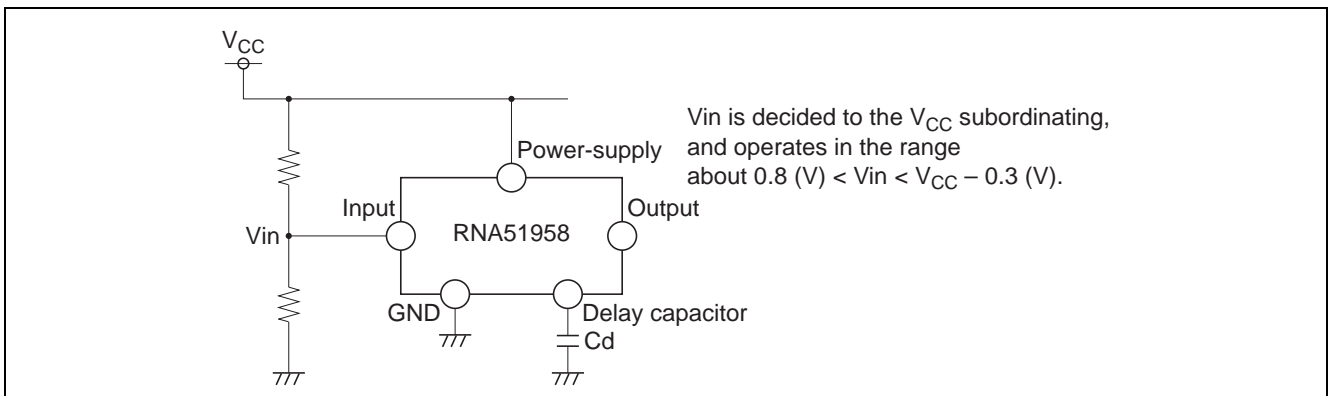
The following voltage is recommended to be input to the input terminal (pin 2).

$$\text{about } 0.8 \text{ (V)} < V_{in} < V_{CC} - 0.3 \text{ (V)} \dots \text{ at } V_{CC} \leq 7 \text{ V}$$

$$\text{about } 0.8 \text{ (V)} < V_{in} < 6.7 \text{ (V)} \dots \text{ at } V_{CC} > 7 \text{ V}$$

2. About using input terminal

Please do an enough verification to the transition characteristic etc. of the power supply when using independent power supply to input terminal (pin 2).



**Figure 6 Recommended Example**

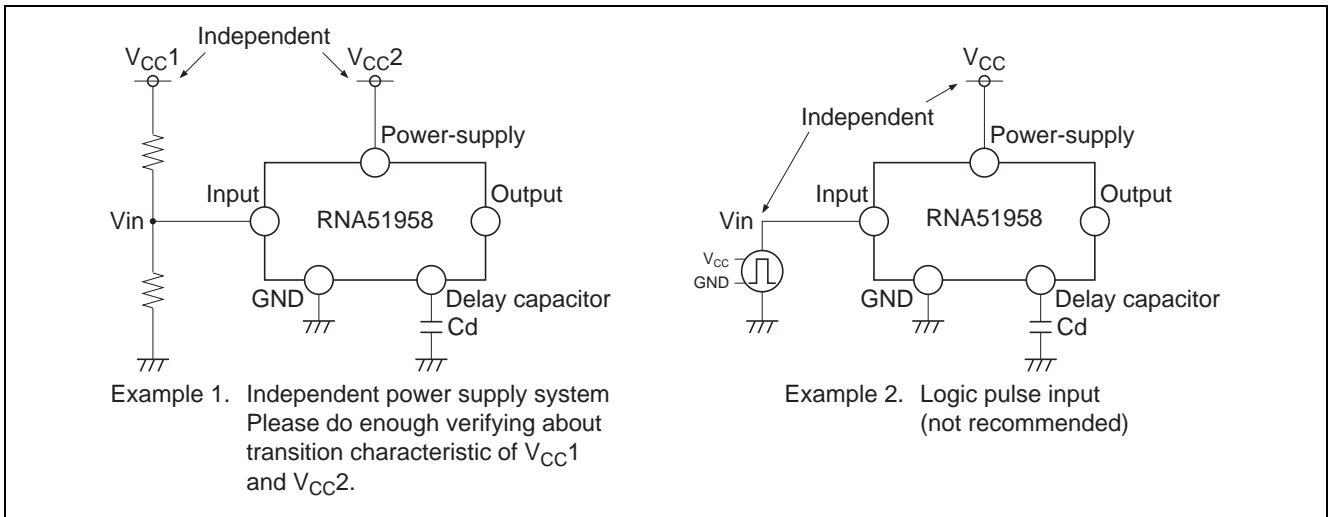


Figure 7

3. Calculation of detecting voltage

Detecting voltage V<sub>S</sub> can be calculated by the following expression.

However, the error margin is caused in the detecting voltage because input current I<sub>in</sub> (standard 100 nA) exists if it sets too big resistance.

Please set the constant to disregard this error margin.

$$V_S = 1.25 \times \left( \frac{R_1 + R_2}{R_2} \right) + \frac{I_{in} \times R_1}{\text{error margin}}$$

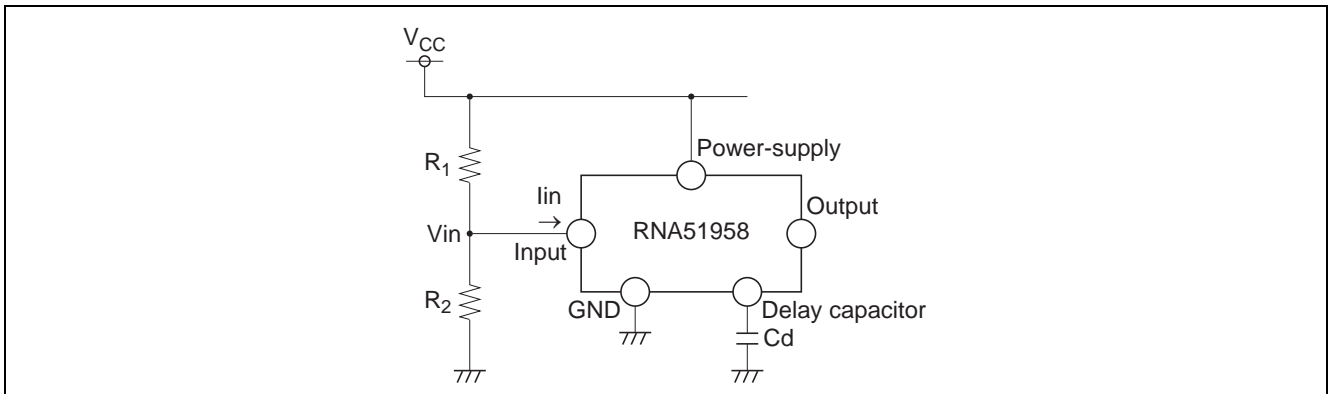


Figure 8 Influence of Input Current

4. About the voltage input outside ratings

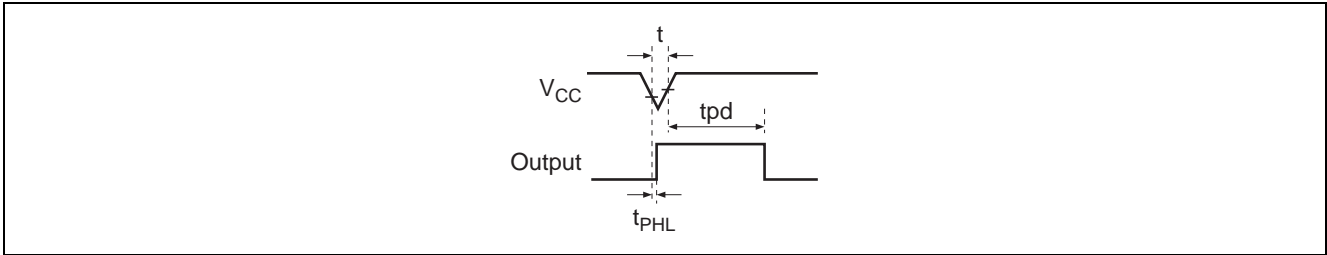
Please do not input the voltage outside ratings to the input terminal.

An internal protection diode becomes order bias, and a large current flows.

### Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 μF or less.

When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.



**Figure 9 Time Chart at Momentary Voltage-Decrease**

(1) The difference at delay time becomes remarkable.

A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be 'tpd', the difference occurs in the range from  $0.47 \times tpd$  to  $2.05 \times tpd$ . For instance, 34 seconds can be calculated at 100 μF. However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.

For example, the reaction time  $t_{PHL}$  is 10 μs when delay capacitor  $C_d = 0.1 \mu F$ .

The momentary voltage-decrease that is longer than such  $t_{PHL}$  are occurs, the detection becomes possible. When the delay capacitance is enlarged,  $t_{PHL}$  also becomes long. For instance, it becomes about 100 to 200 μs in case of circuit constant  $C1 = 100 \mu F$ .

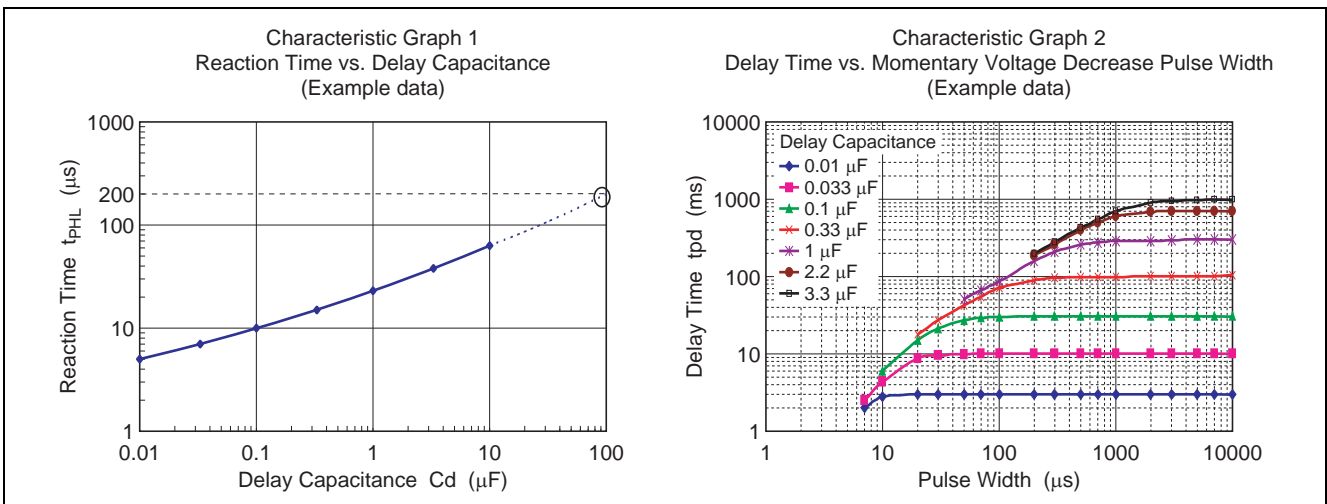
(Characteristic graph 1 is used and extrapolation in case of  $C_d = 100 \mu F$ .)

Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

(3) Original delay time is not obtained.

When the momentary voltage-decrease time 't' is equivalent to  $t_{PHL}$ , the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.

Please refer to characteristic graph 2. (Delay time versus input pulse width)



**Figure 10 Characteristic Graph**

### Setting of Output Load Resistance (RNA51958B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance)  $R_L$  so that the output current (output inflow current  $I_L$ ) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).

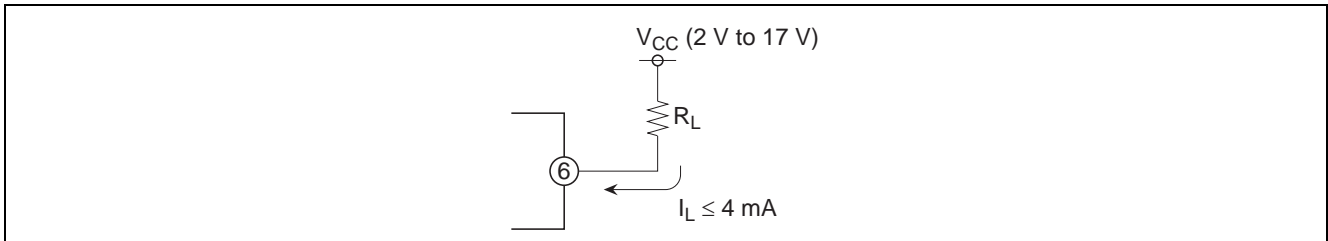


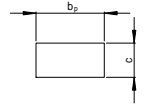
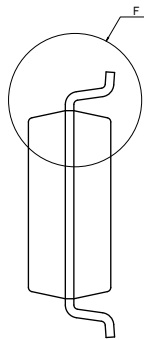
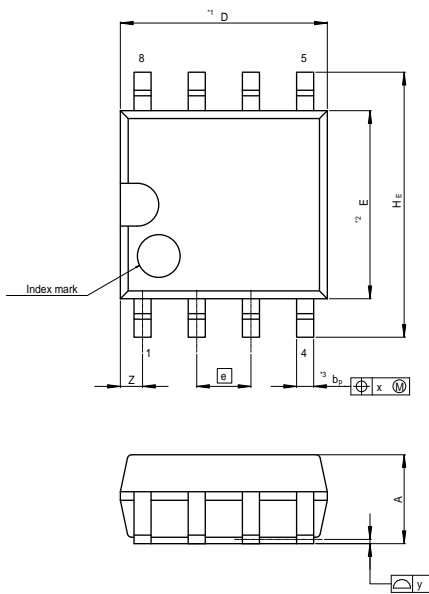
Figure 11 Output Load Resistance  $R_L$

### Others

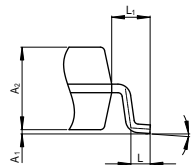
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2. Additionally, please inquire of our company when there is an uncertain point on use.

### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



Terminal cross section  
(Ni/Pd/Au plating)

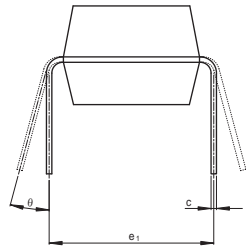
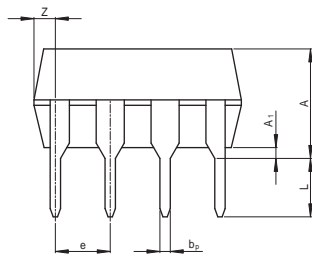
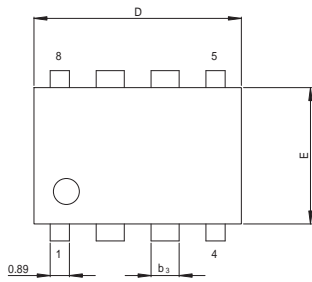


Detail F

NOTE)  
1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION\*\*3\*DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A <sub>2</sub>	—	1.85	—
A <sub>1</sub>	0.00	0.1	0.20
A	—	—	2.03
b <sub>p</sub>	0.34	0.4	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.7	6.2	6.5
Ⓧ	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L <sub>1</sub>	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x9.6-2.54	PRDP0008AF-B	DP-8FV	0.54g



(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e <sub>1</sub>	—	7.62	—
D	—	9.60	10.6
E	—	6.30	7.4
A	—	—	5.06
A <sub>1</sub>	0.5	—	—
b <sub>p</sub>	0.40	0.48	0.56
b <sub>3</sub>	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—

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