CY2X014

Low Jitter LVPECL Crystal Oscillator

Features

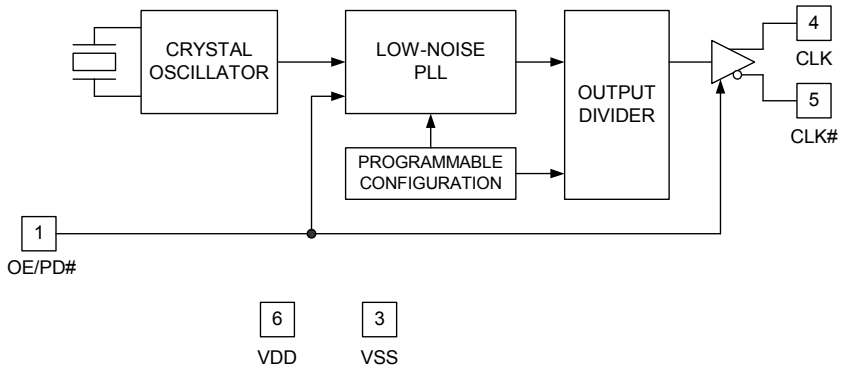
- Low Jitter Crystal Oscillator (XO)
- Less than 1 ps Typical RMS Phase Jitter
- Differential LVPECL Output
- Output Frequency from 50 MHz to 690 MHz
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Output Enable or Power Down Function
- Supply Voltage: 3.3V or 2.5V
- Pb-Free Package: 5.0 x 3.2 mm LCC
- Commercial and Industrial Temperature Ranges

Functional Description

The CY2X014 is a high performance and high frequency Crystal Oscillator (XO). The device uses a Cypress proprietary low noise PLL to synthesize the frequency from an embedded crystal.

The CY2X014 is available as a factory configured device or as a field programmable device.

Logic Block Diagram



Pinout

Figure 1. Pin Diagram - 6 Pin Ceramic LCC

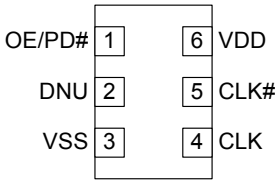


Table 1. Pin Definitions - 6 Pin Ceramic LCC

Pin	Name	I/O Type	Description
1	OE/PD#	CMOS Input	Output Enable Pin: Active HIGH. If OE = 1, CLK is enabled. Power Down Pin: Active LOW. If PD# = 0, the device is powered down and the clock is disabled. The functionality of this pin is programmable.
4, 5	CLK, CLK#	LVPECL Output	Differential Output Clock
2	DNU	–	Do Not Use: DNU pins are electrically connected, but perform no function
6	VDD	Power	Supply Voltage: 2.5V or 3.3V
3	VSS	Power	Ground

Programming Description

The CY2X014 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described in the following sections.

Field Programmable CY2X014F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks™ Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction.

The software is located at www.cyberclocksonline.com.

Factory Configured CY2X014

For ready-to-use devices, the CY2X014 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders. The CY2X014 is one time programmable (OTP).

Programming Variables

Output Frequency

The CY2X014 can synthesize a frequency to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

The CY2X014 has an output frequency range of 50 MHz to 690 MHz, but the range is not continuous. The CY2X014 cannot generate frequencies in the ranges of 521 MHz to 529 MHz and 596 MHz to 617 MHz.

Pin 1: Output Enable or Power Down (OE/PD#)

Pin 1 is programmed as either Output Enable (OE) or Power Down (PD#). The OE function is used to enable or disable the CLK output quickly, but it does not reduce core power consumption. The PD# function puts the device into a low power state, but the wake up takes longer because the PLL must reacquire lock.

Industrial vs. Commercial Device Performance

Industrial and Commercial devices have different internal crystals. They have a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Phase Noise vs. Jitter Performance

In most cases, the device configuration for optimal phase noise performance is different from the device configuration for optimal cycle to cycle or period jitter. CyberClocks Online Software includes algorithms to optimize performance for either parameter.

Table 2. Device Programming Variables

Variable
Output Frequency
Pin 1 Function (OE or PD#)
Optimization (Phase Noise or Jitter)
Temperature Range (Commercial or Industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, Storage	Non operating	–55	135	°C
T_J	Temperature, Junction		–40	135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000		V
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3V Supply Voltage Range	3.0	3.3	3.6	V
	2.5V Supply Voltage Range	2.375	2.5	2.625	V
T_{PU}	Power Up Time for V_{DD} to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	–	500	ms
T_A	Ambient Temperature (Commercial)	0	–	70	°C
	Ambient Temperature (Industrial)	–40	–	85	°C

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[3]	Operating Supply Current	V_{DD} = 3.6V, CLK = 150 MHz, OE/PD# = V_{DD}, output terminated	–	–	150	mA
		V_{DD} = 2.625V, CLK = 150 MHz, OE/PD# = V_{DD}, output terminated	–	–	145	mA
I_{SB}	Standby Supply Current	PD# = V_{SS}	–	–	200	µA
V_{OH}	LVPECL High Output Voltage	V_{DD} = 3.3V or 2.5V, R_{TERM} = 50Ω to V_{DD} – 2.0V	V_{DD} – 1.15	–	V_{DD} – 0.75	V
V_{OL}	LVPECL Low Output Voltage	V_{DD} = 3.3V or 2.5V, R_{TERM} = 50Ω to V_{DD} – 2.0V	V_{DD} – 2.0	–	V_{DD} – 1.625	V
V_{OD1}	LVPECL Output Voltage Swing (V_{OH} - V_{OL})	V_{DD} = 3.3V or 2.5V, R_{TERM} = 50Ω to V_{DD} – 2.0V	600	–	1000	mV
V_{OD2}	LVPECL Output Voltage Swing (V_{OH} - V_{OL})	V_{DD} = 2.5V, R_{TERM} = 50Ω to V_{DD} – 1.5V	500	–	1000	mV
V_{OCM}	LVPECL Output Common Mode Voltage (V_{OH} + V_{OL})/2	V_{DD} = 2.5V, R_{TERM} = 50Ω to V_{DD} – 1.5V	1.2	–	–	V
I_{OZ}	LVPECL Output Leakage Current	PD#/OE = V_{SS}	–35	–	35	µA
V_{IH}	Input High Voltage		0.7*V_{DD}	–	–	V
V_{IL}	Input Low Voltage		–	–	0.3*V_{DD}	V
I_{IH}	Input High Current	Input = V_{DD}	–	–	115	µA
I_{IL}	Input Low Current	Input = V_{SS}	–	–	50	µA
C_{IN}	Input Capacitance		–	15	–	pF

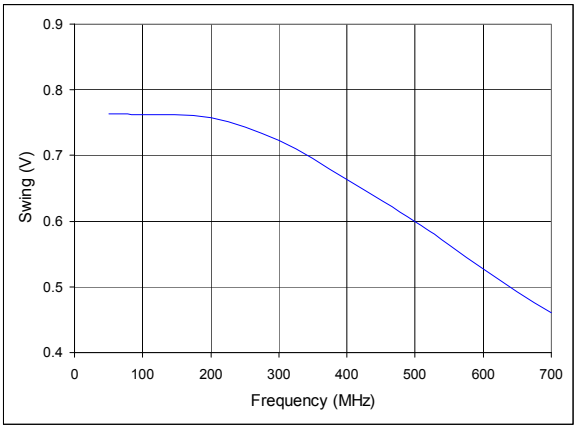
Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. I_{DD} includes ~24 mA of current that is dissipated externally in the output termination resistors.

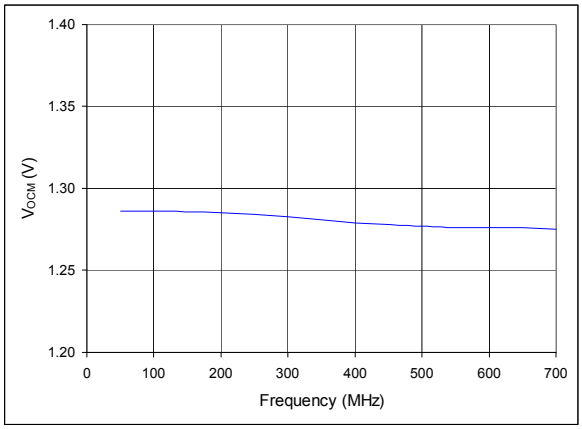
AC Electrical Characteristics[4]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output Frequency[6]		50	–	690	MHz
FSC	Frequency Stability, Commercial Devices[5]	V_{DD} = min to max, T_A = 0°C to 70°C	–	–	±35	ppm
FSI	Frequency Stability, Industrial Devices[5]	V_{DD} = min to max, T_A = –40° to 85°C	–	–	±55	ppm
AG	Aging, 10 Years		–	–	±15	ppm
T_{DC}	Output Duty Cycle	F <= 450 MHz, measured at zero crossing	45	50	55	%
		F > 450 MHz, measured at zero crossing	40	50	60	%
T_R, T_F	Output Rise and Fall Time	20% and 80% of full output swing	200	400	600	ps
T_{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.) or from PD# rising edge	–	–	10	ms
$T_{Jitter(\phi)}$	RMS Phase Jitter (Random)	F_{OUT} = 106.25 MHz (12 kHz to 20 MHz)	–	1	–	ps

Typical Output Characteristics

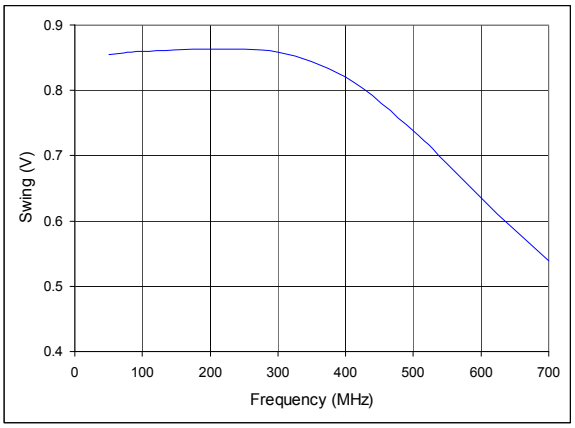
Figure 2. 2.5V Supply and Termination to V_{DD}–1.5V, Minimum V_{DD} and Maximum T_A





Notes
4. Not 100% tested, guaranteed by design and characterization.
5. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, and variation from temperature and supply voltage.
6. This parameter is specified in CyberClocks Online software

Figure 3. 2.5V Supply and Termination to V_{DD}–2V, Minimum V_{DD} and Maximum T_A



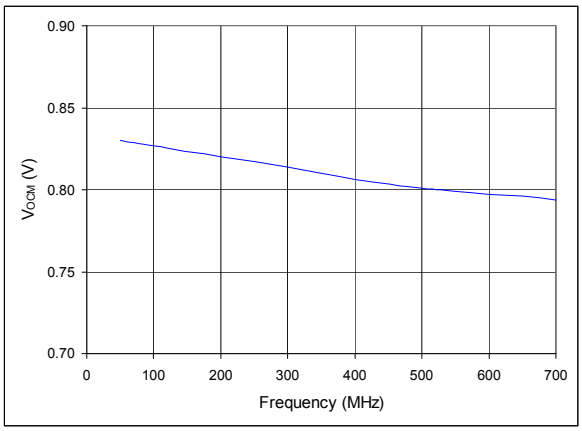
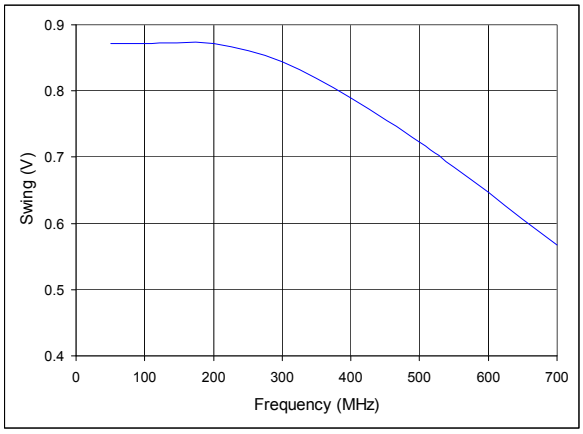
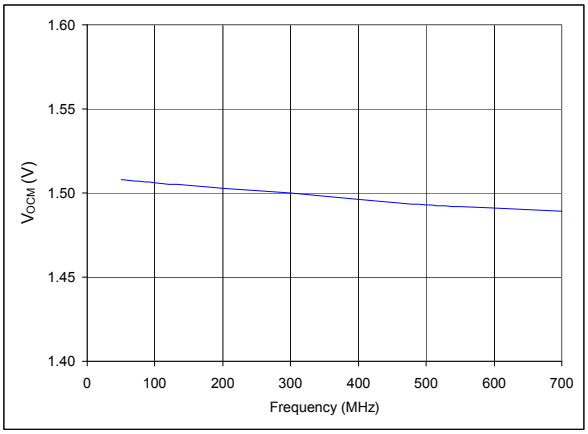


Figure 4. 3.3V Supply and Termination to V_{DD}–2V, Minimum V_{DD} and Maximum T_A





Switching Waveforms

Figure 5. Output DC Parameters

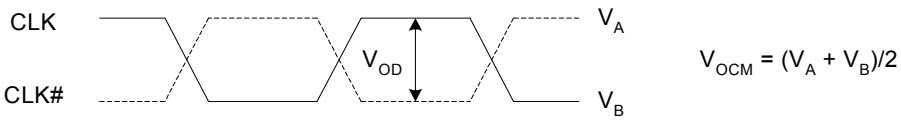


Figure 6. Duty Cycle Timing

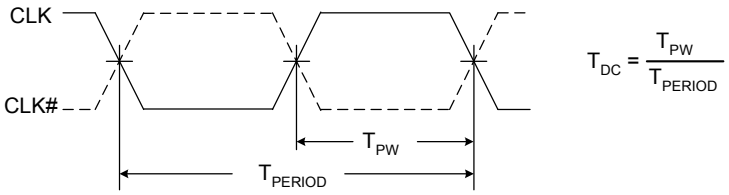


Figure 7. Output Rise and Fall Time

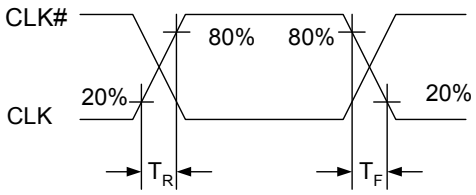
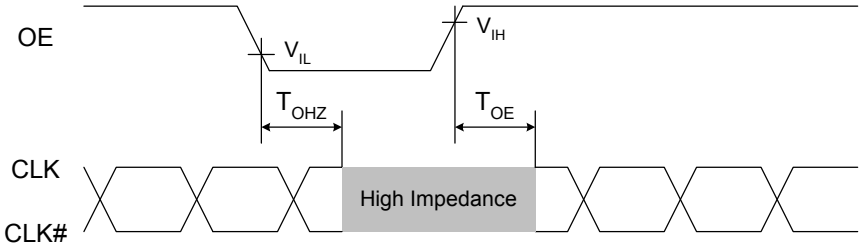
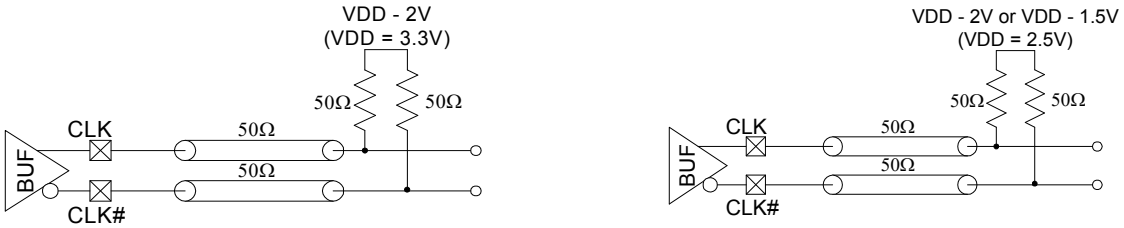


Figure 8. Output Enable and Disable Timing



Termination Circuits

Figure 9. LVPECL Termination

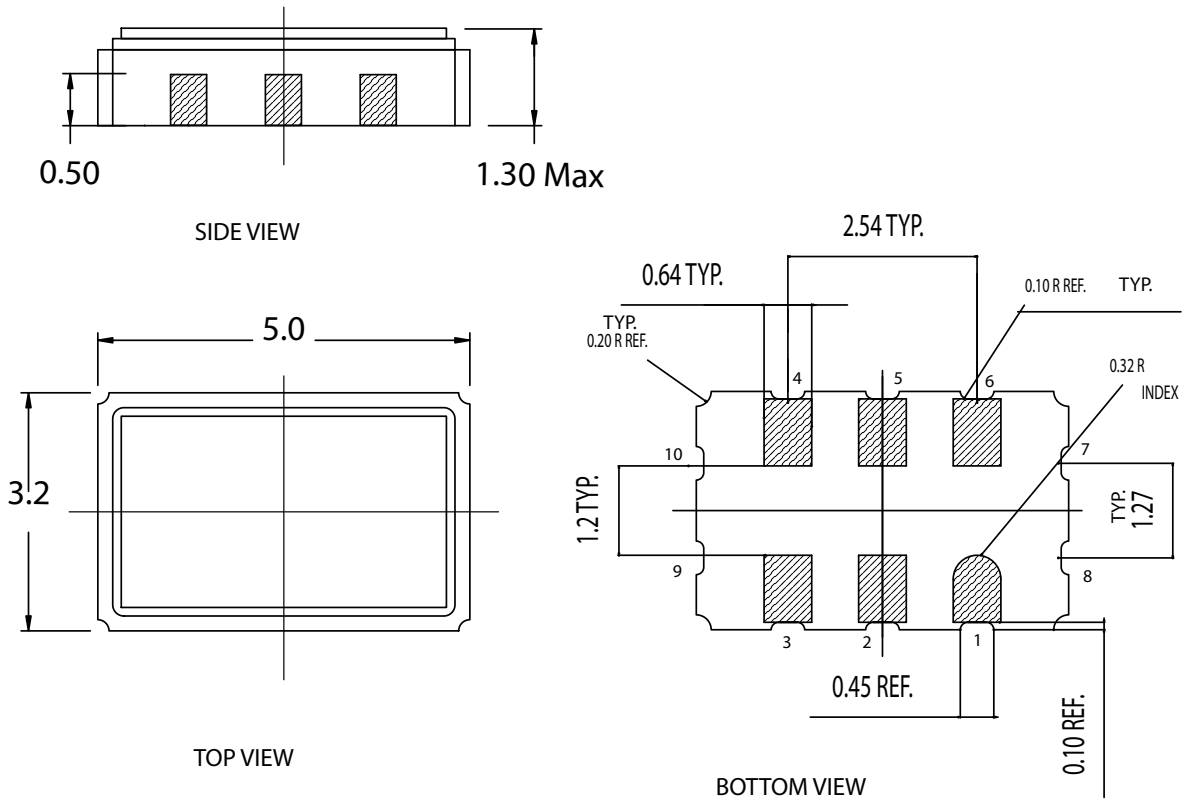


Ordering Information

Part Number[7]	Configuration	Package Description	Product Flow
Pb-Free			
CY2X014FLXCT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2X014FLXIT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C
CY2X014LXCxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2X014LXIxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C

Package Diagram

Figure 10. 6-Pin 3.2x5.0 mm Ceramic LCC LZ06A



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Note
7. "xxx" is a factory assigned code that identifies the programming option.

Document History Page

Document Title: CY2X014 Low Jitter LVPECL Crystal Oscillator Document Number: 001-10179				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	504478	RGL	See ECN	New data sheet
*A	1428603	JWK/SFV	See ECM	Removed pull up on pin 1 and related specifications, Added items to Programming Variables section, Added C_{IN} specification, Modified t_{J2}, I_{IH}, I_{IL}, I_{DD} and I_{SB} specifications, Changed to a single Frequency Stability specification, Removed Peak-to-peak Period Jitter specification, Changed pin 2 from NC to DNU, Changed max storage temperature, Title change, 2.5V supply tightened from ±10% to ±5%, 2.5V termination option changed from VDD-1.4V to VDD-1.5V, Added typical output characteristic curves
*B	2669117	KVM/AESA	03/05/09	Revised frequency stability and aging specs and conditions, Max frequency changed from 700 MHz to 690 MHz, Duty cycle changed from 45/55 to 40/60 for freq > 450 MHz, Removed reference to CY3672 programmer, Junction and storage temperatures changed from 125 to 135°C, IIH changed from 20µA to 115µA, IIL changed from 20µA to 50µA, Rise and fall times changed from 350 ps to 500 ps, Removed MSL spec, Changed Data Sheet Status to Final.
*C	2701663	KVM/PYRS	05/06/09	General clean up Added explanation of gaps in the frequency range Added URL for software Removed frequency stability paragraph under Programming Variables Added programming variables table Added separate IDD spec for 2.5V supply Changed the amount of load current in IDD footnote Changed phase jitter parameter name Removed supply voltage as a programming variable Changed conditions for ESD spec Changed rise & fall times from 500 ps to 400 ps typ, added min and max
*D	2718433	WWZ/HMT	06/12/09	No change. Submit to ECN for product launch.

Sales, Solutions, and Legal Information

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