1. *Basic Specifications*

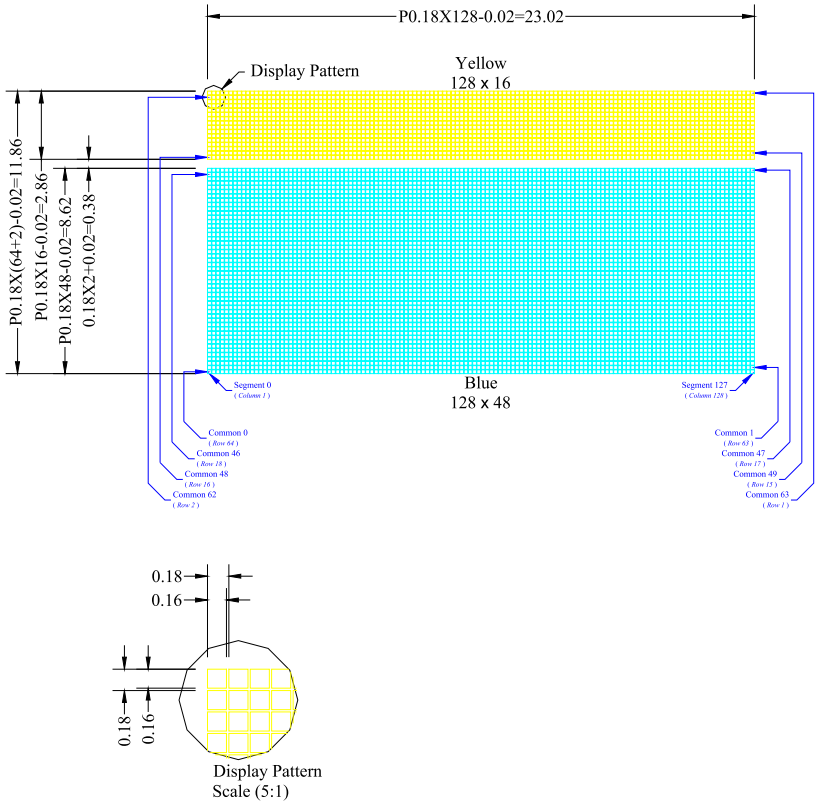
1.1 Display Specifications

1) Display Mode: Passive Matrix
2) Display Color: Area Color (Light Blue, Yellow)
3) Drive Duty: 1/64 Duty

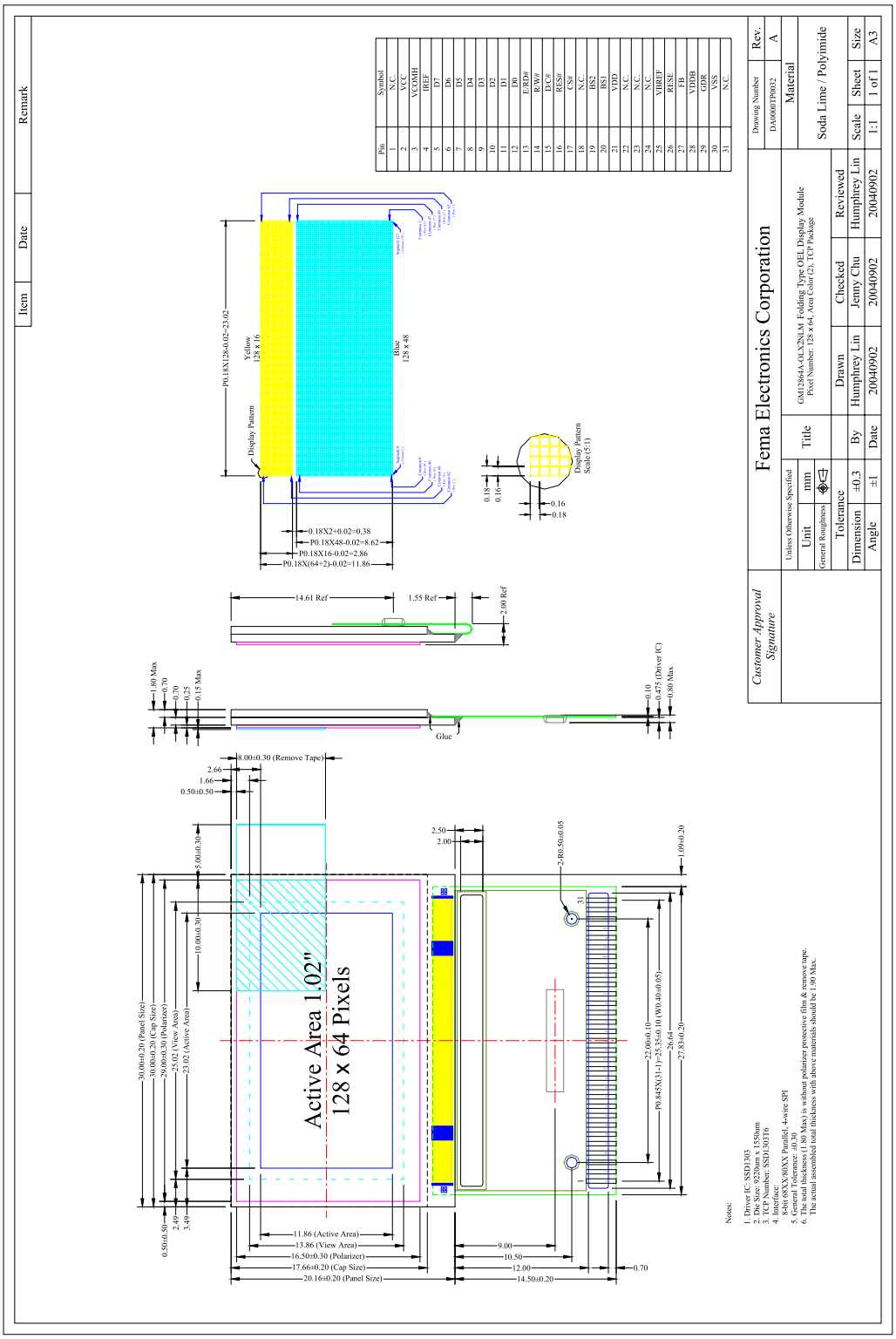
1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 128 × 64
3) Panel Size: 30.00 × 20.16 × 1.80 (mm)
4) Active Area: 23.02 × 11.86 (mm)
5) Pixel Pitch: 0.18 × 0.18 (mm)
6) Pixel Size: 0.16 × 0.16 (mm)
7) Weight: 2.0 (g)

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



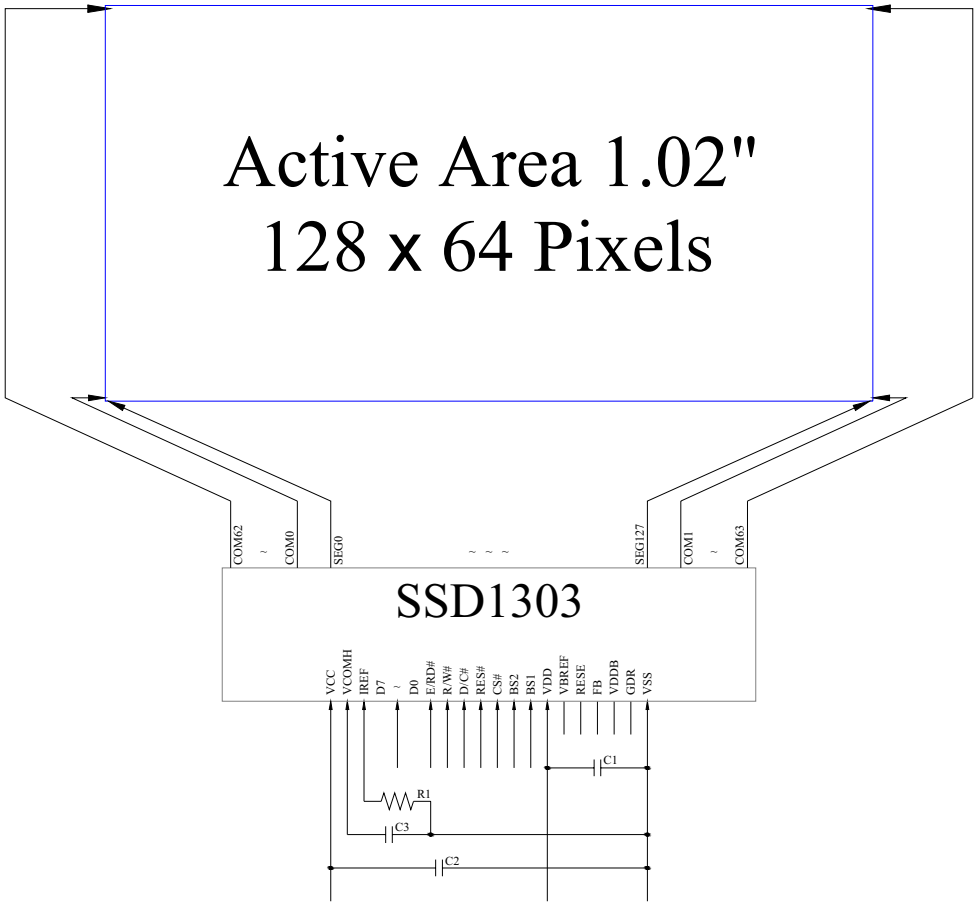
1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>21</td><td>VDD</td><td>I</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>30</td><td>VSS</td><td>I</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>2</td><td>VCC</td><td>I/O</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter.</td></tr>
<tr><td>4</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>I/O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>28</td><td>VDDB</td><td>I</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to VDD when the converter is used. It must be floated when the converter is not used.</td></tr>
<tr><td>29</td><td>GDR</td><td>O</td><td>Output for Connected External NMOS
This output pin drives the gate of the external NMOS of the booster circuit.</td></tr>
<tr><td>26</td><td>RESE</td><td>I</td><td>Input for Connected External NMOS
This pin connects to the source current pin of the external NMOS of the booster circuit.</td></tr>
<tr><td>25</td><td>VBREF</td><td>I/O</td><td>Voltage Reference for DC/DC Converter Circuit
This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1uF, should be connected to VSS.</td></tr>
<tr><td>27</td><td>FB</td><td>I</td><td>Feedback Input for DC/DC Converter Circuit
This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (VCC).</td></tr>
<tr><td>20
19</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>6800-parallel</td><td>8080-parallel</td><td>Serial</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>16</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
13	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
14	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
5~12	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
1, 31	N.C.	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins.
18, 22~24	N.C.	-	*Reserved Pin* The N.C. pins between function pins are reserved for compatible and flexible design.

1.6 Block Diagram



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES#, and CS#
* VBREF, RESE, FB, VDDB, GDR, and VSSB should be left float.

C1, C3: 4.7µF
C2: 10µF
R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4	V	1, 2
Driver Supply Voltage	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. Electrical Characteristics

3.1 DC Characteristics

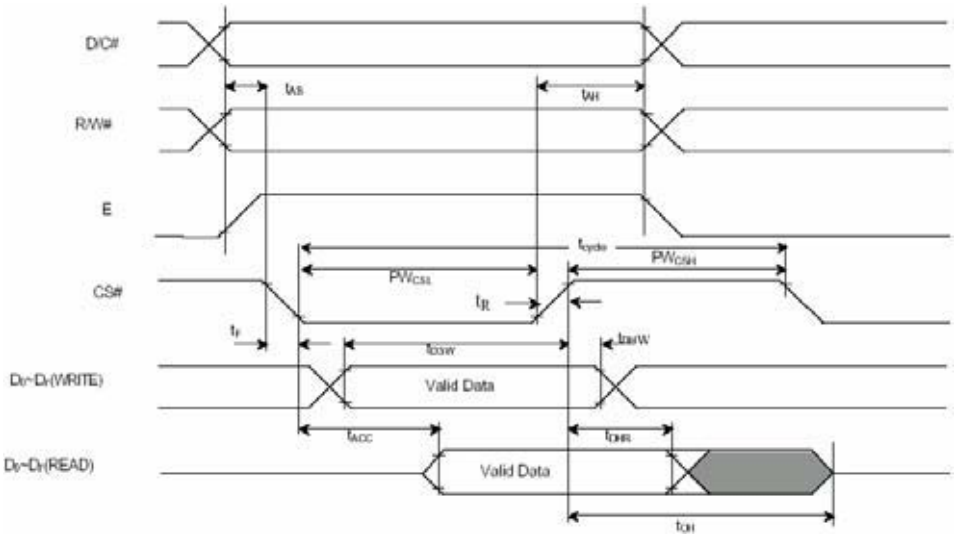
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.6	2.8	3.5	V
Driver Supply Voltage	V_{CC}		-	9	-	V
High Level Input	V_{IH}		$0.8 \times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}		0	-	$0.2 \times V_{DD}$	V
High Level Output	V_{OH}		$0.9 \times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}		0	-	$0.1 \times V_{DD}$	V

3.2 AC Characteristics

3.2.1 6800-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

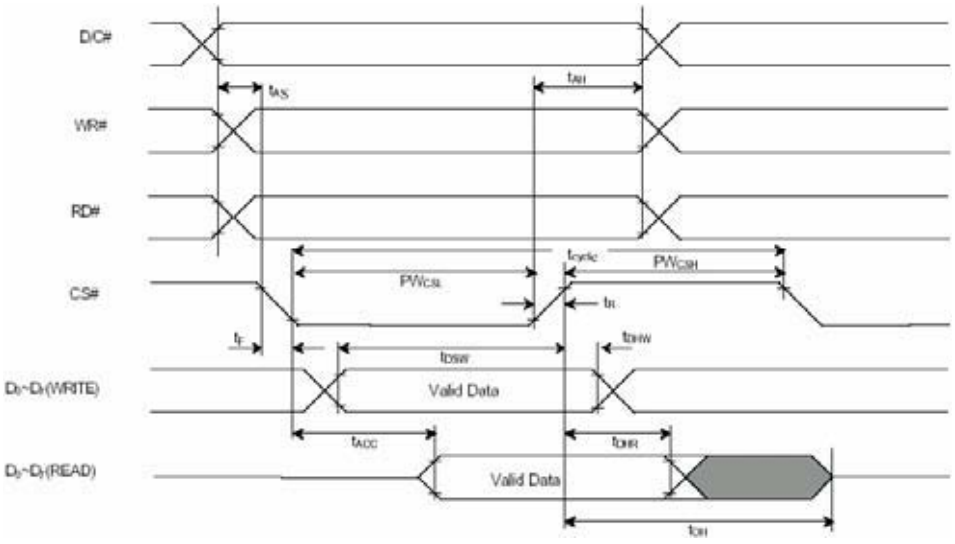
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.2 8080-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

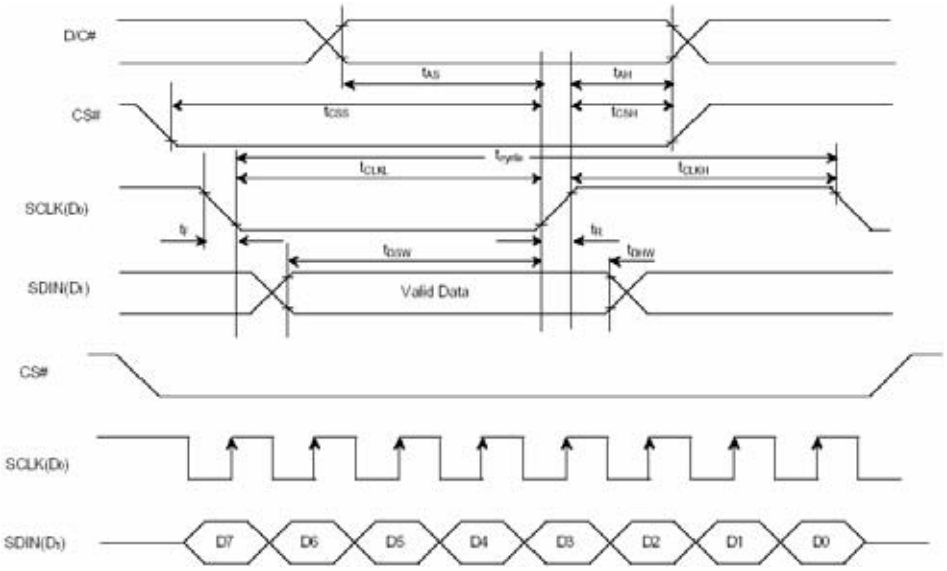
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	100	-	ns
t_{DHW}	Write Data Hold Time	100	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer	35	60	-	cd/m^2
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.24	0.16 0.28	0.20 0.32	
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.43 0.46	0.47 0.50	0.51 0.54	
Dark Room Contrast	CR	Shown as below	-	>1:100	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at 1/64 duty, 100Hz Frame Rate, 0xFF Contrast Setting.

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.6	2.8	3.5	V
Driver Supply Voltage	V_{CC}		8	9	10	V
Operating Current for V_{DD}	I_{DD}	Note 4	-	TBD	TBD	mA
		Note 5	-	TBD	TBD	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	TBD	TBD	mA
		Note 5	-	TBD	TBD	mA

Note 4: V_{DD} = 2.8V, V_{CC} = 9V, Frame Rate = 100Hz, Contrast Setting = 0xFF, 50% Display Area Turn on.

Note 5: V_{DD} = 2.8V, V_{CC} = 9V, Frame Rate = 100Hz, Contrast Setting = 0xFF, 100% Display Area Turn on.

4. *Functional Specification*

4.1. Commands

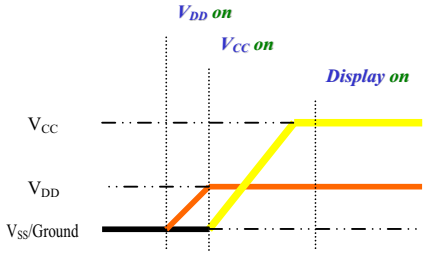
Refer to the Technical Manual for the SSD1303

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

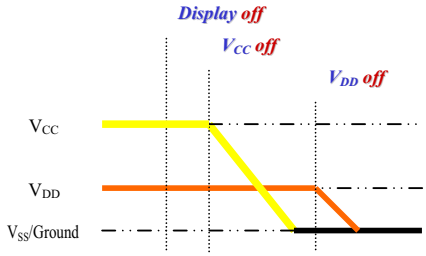
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{CC}
5. Delay 100ms
   (when V_{DD} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 132×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00H and COM0 mapped to row address 00H)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80H
9. Internal booster is selected

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization Setting>
Set Display Clock Divide Ratio / Oscillator Frequency
(11010101 with XXXXXXXX)

Set Display Offset
(11010011 with **XXXXXX)
* XXXXXX = 64 - Dummy Lines from Common 0
Set Multiplex Ratio
(10101000 with **XXXXXX)

Set DC/DC On/Off
(10101101 with 1000101X)
10001010 => 0x8A (Off)
Set Area Color Mode & Low Power Display Mode
(11011000 with 00XX0X0X)
00000101 => 0x05 (Mono & Low Power Save Mode)

Set Display Start Line
(01XXXXXX)
Set Segment Re-map
(1010000X)
Set COM Output Scan Direction
(1100X***)
Set COM Pins Hardware Configuration
(11011010 with 000X0010)
00010010 => 0x12 (Alternative Mode)

Set Contrast Control Register
(10000001 with XXXXXXXX)

Set Entire Display On/Off (1010010X)
10100100 => 0xA4 (Normal)
Set Normal/Inverse Display (1010011X)
10100110 => 0xA6 (Normal)
Set Display On/Off (1010111X)
10101111 => 0xAF (Turns On)

<Display Boundary Setting>
Set Page Address (1011XXXX)
10110000 => 0xB0
Set Lower Column Address
(0000XXXX)
Set Higher Column Address
(0001XXXX)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-20°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-30°C, 240 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 240 hrs	
Thermal Shock	-30°C ⇔ 80°C, 10 cycles 30 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.
An average operating lifetime of more than 10,000 hrs at room temperature is approached by 240 hrs @ 70°C operating.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Inspection Method:

6.1.1 Applicable Standard

MIL-STD-105E, Level II, Normal Inspection, Single Sampling

6.1.2 AQL

Partition	AQL	Definition
Major	0.65	Defects may lead to the failure of display function or the failure of passing the reliability criteria.
Minor	1.0	Defects do not affect all of the display functions, and have no impact to the reliability.

6.1.3 Inspection Condition

Test and measurement were conducted under the following conditions:

Temperature: 23 ± 5°C

Humidity: 55 ± 15 %RH

Distance between the Panel & Eyes of the Inspector: ≥ 30 cm

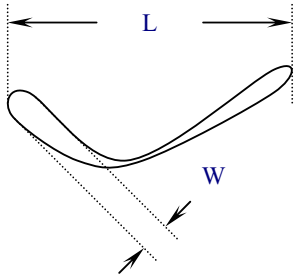
6.2 Inspection Criterion

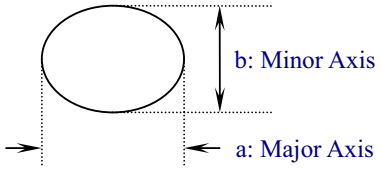
Check Item	Classification	Criteria	
Non Operation/Display	Major	Not Allowable	
Flicker			
Missing Line or Pixel			
Wrong Display			
Cross Talk *			
Scratches, Fiber **	Minor	$W \le 0.05$ $W \le 0.1, L \le 2$ $2 < L$	Ignore $n \le 3$ $n = 0$
Dirt, Black Spot, White Spot, Greasy Dirt, Foreign Material, Dent, Bubbles **	Minor	$\Phi \le 0.1$ $0.1 < \Phi \le 0.2$ $0.2 < \Phi \le 0.25$ $0.25 < \Phi$	Ignore $n \le 3$ $n \le 1$ $n = 0$
Fingerprint, Flow Mark	Minor	Not Allowable	

* In displays which manifests itself has the other shadowing, ghosting or streaking.

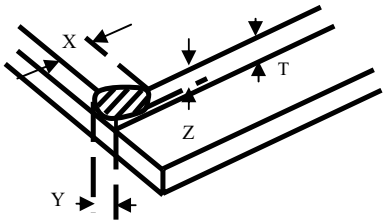
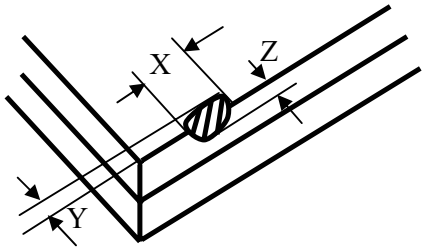
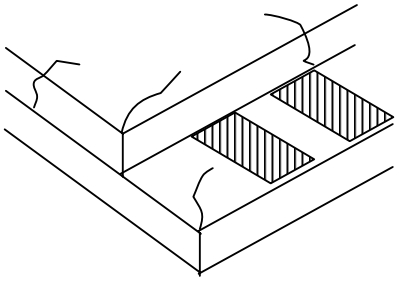
** Distance between any 2 defects should over 10mm.

*** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





Visual Check in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Major	X ≤ 1/6 Panel Length Y ≤ 1 Z ≤ T  
Panel Crack	Minor	Any crack is not allowable. 
Terminal Cable: Twist, Scar, Split, Scratch	Minor	Not Allowable

7. Precautions When Using These OEL Display Modules

7.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0?C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1303
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

7.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the TCP
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.