

**192MHz – 400MHz Low Phase Noise LVDS VCXO (12 – 25MHz Crystal)**

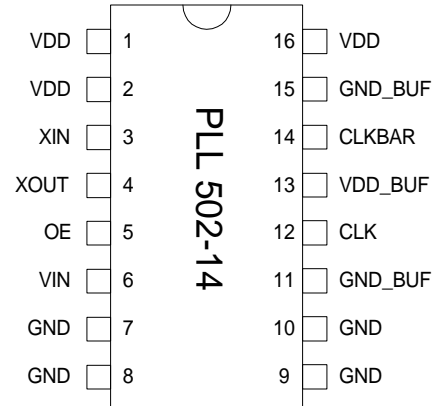
**FEATURES**

- Low phase noise output for the 192MHz to 400MHz range (-132 dBc at 10kHz offset).
- LVDS output.
- 12 to 25MHz crystal input.
- Integrated crystal load capacitor: no external load capacitor required.
- Output Enable selector.
- Wide pull range (min. +/-190 ppm)
- 3.3V operation.
- Available in 16 Pin TSSOP or SOIC.

**DESCRIPTION**

The PLL502-14 is a monolithic low jitter and low phase noise (-115dBc/Hz @ 10kHz offset) VCXO IC with LVDS output, for 192MHz to 400MHz output range. It allows the control of the output frequency with an input voltage (VIN), using a low cost crystal. The chip provides a pullable output at a frequency of  $F_{XIN} \times 16$ . This makes the PLL502-14 ideal for a wide range of applications.

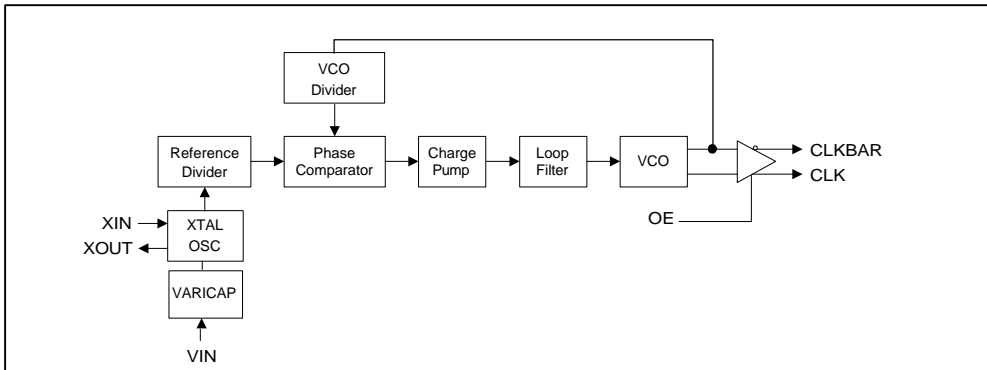
**PIN CONFIGURATION**



$$F_{OUT} = F_{XIN} \times 16$$

OE (Pin 5)	Output State
0	Tri-state
1 (Default)	Output enabled

**BLOCK DIAGRAM**



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**PIN DESCRIPTIONS**

Name	Number	Type	Description
VDD	1,2,16	P	+3.3V Power supply connectors.
XIN	3	I	Crystal input pin.
XOUT	4	I	Crystal output pin.
OE	5	I	Output enable input pin. Disables (tri-state) output when low. Internal pull-up enables output by default if pin is not connected to low.
VIN	6	I	Frequency control voltage input pin.
GND	7,8,9,10	P	GND Power connectors.
GND_BUF	11,15	P	GND connector for output buffers.
CLK	12	O	True clock output pin.
VDD_BUF	13	P	+3.3V Power supply connector for output buffers.
CLKB	14	O	Complementary clock output pin.

**ELECTRICAL SPECIFICATIONS**
**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature*	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

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**2. Crystal Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	12		25	MHz
Crystal Loading Rating	$C_L$ (xtal)	At $V_{IN} = 1.65V$		9.5		pF
Crystal Pullability	$C_0/C_1$ (xtal)	AT cut			250	-
Recommended ESR	$R_E$	AT cut			30	$\Omega$

**Note:** Crystal Loading rating: 9.5pF is the loading the crystal sees from the VCXO chip at  $V_{IN} = 1.65V$ . It is assumed that the crystal will be at nominal frequency at this load. If the crystal requires more load to be at nominal frequency, the additional load must be added externally. This however may reduce the pull range.

**3. Voltage Control Crystal Oscillator**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range		$F_{XIN} = 12 - 25MHz$ ; XTAL $C_0/C_1 < 250$	380			ppm
CLK output pullability		$0V \leq V_{CON} \leq 3.3V$	$\pm 190$			ppm
Linearity				5	10	%
VCXO Tuning Characteristic				115		ppm/V
VCON pin input impedance			2000			$k\Omega$
VCON modulation BW		$0V \leq V_{CON} \leq 3.3V, -3dB$	25			kHz

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

**4. General Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	$I_{DD}$	LVDS			60	mA
Operating Voltage	$V_{DD}$		3.13		3.47	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				$\pm 50$		mA

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**5. Jitter and Phase Noise specification**

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 311MHz	With capacitive decoupling between VDD and GND.		9		ps
Accumulated jitter RMS at 311MHz	With capacitive decoupling between VDD and GND. Over 10,000 cycles.		TBM		ps
Integrated jitter RMS at 311MHz	Integrated 12 kHz to 20 MHz		4		ps
Phase Noise relative to carrier	311MHz @10Hz offset		-60		dBc/Hz
Phase Noise relative to carrier	311MHz @100Hz offset		-90		dBc/Hz
Phase Noise relative to carrier	311MHz @1kHz offset		-111		dBc/Hz
Phase Noise relative to carrier	311MHz @10kHz offset		-115		dBc/Hz
Phase Noise relative to carrier	311MHz @100kHz offset		-110		dBc/Hz

Note: Phase Noise measured at VIN = 0V

**6. LVDS Electrical Characteristics**

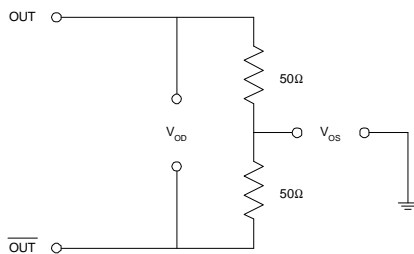
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

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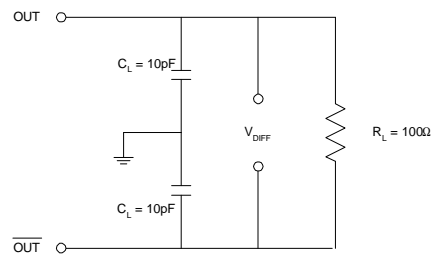
**7. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

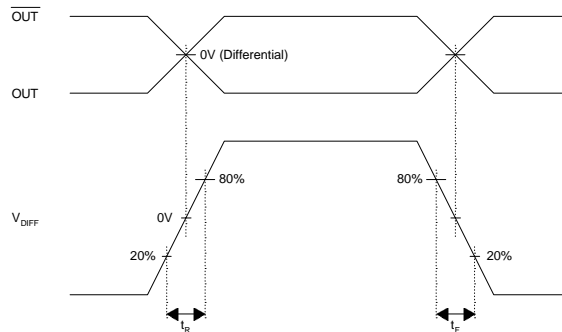
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



**192MHz – 400MHz Low Phase Noise LVDS VCXO (12 – 25MHz Crystal)**

**PACKAGE INFORMATION**

16 PIN Narrow SOIC, TSSOP ( mm )				
Symbol	SOIC		TSSOP	
	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	

**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**  
 47745 Fremont Blvd., Fremont, CA 94538, USA  
 Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
 Device number, Package type and Operating temperature range

**PLL502-14 S C XX**

PART NUMBER \_\_\_\_\_

- \_\_\_\_\_ REVISION CODE (when applicable)
- \_\_\_\_\_ TEMPERATURE  
 C=COMMERCIAL  
 M=MILITARY  
 I=INDUSTRIAL
- \_\_\_\_\_ PACKAGE TYPE  
 S=SOIC. O=TSSOP

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