

# RD74LVC74B

## Dual D-type Flip Flops with Preset and Clear

REJ03D0324-0100Z

Rev.1.00

Jun. 22, 2004

### Description

The RD74LVC74B has independent data, preset, clear, and clock inputs Q and  $\bar{Q}$  outputs in a 14 pin package. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$
- All inputs  $V_{IH} (\text{Max.}) = 5.5 \text{ V} (@V_{CC} = 0 \text{ V to } 5.5 \text{ V})$
- Typical  $V_{OL}$  ground bounce  $< 0.8 \text{ V} (@V_{CC} = 3.3 \text{ V}, T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0 \text{ V} (@V_{CC} = 3.3 \text{ V}, T_a = 25^\circ\text{C})$
- High output current
  - $\pm 4 \text{ mA} (@V_{CC} = 1.65 \text{ V})$
  - $\pm 8 \text{ mA} (@V_{CC} = 2.3 \text{ V})$
  - $\pm 12 \text{ mA} (@V_{CC} = 2.7 \text{ V})$
  - $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 5.5 \text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
RD74LVC74BFPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs / reel)
RD74LVC74BTELL	TSSOP-14 pin	TTP-14DV	T	ELL (2,000 pcs / reel)

### Function Table

Inputs				Outputs	
PR	CLR	CK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	$H^{\uparrow}$	$H^{\uparrow}$
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	$Q_0$	$\bar{Q}_0$
H	H	H	X	$Q_0$	$\bar{Q}_0$
H	H	$\downarrow$	X	$Q_0$	$\bar{Q}_0$

H: High level

L: Low level

X: Immaterial

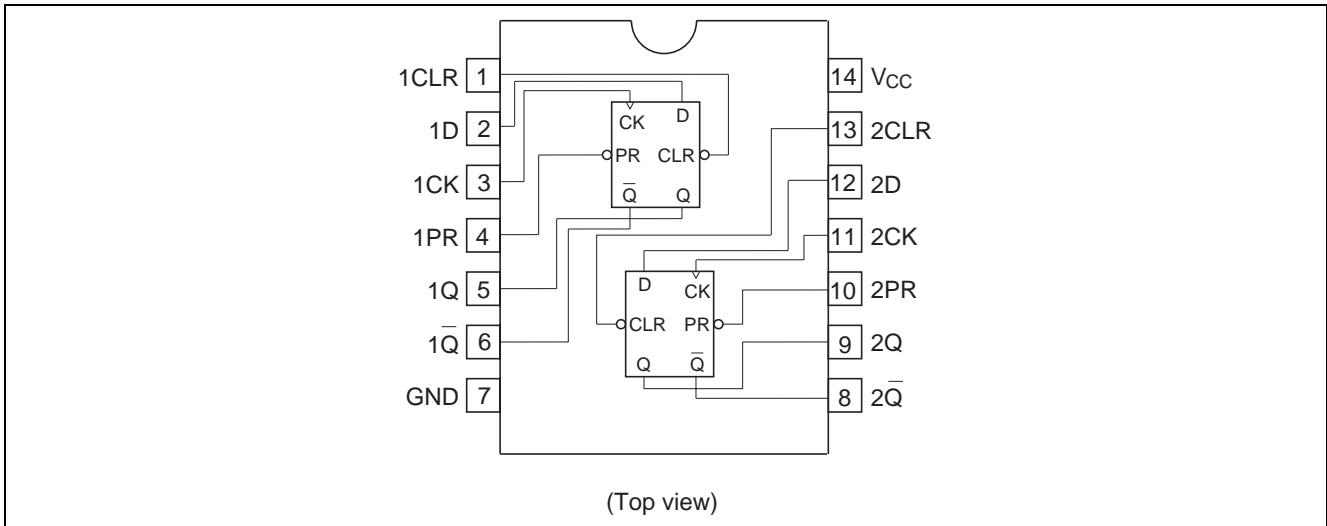
$\downarrow$ : High to Low transition

$\uparrow$ : Low to high transition

$Q_0$ : Level to Q before the indicated steady input conditions were established.

Note: 1. Q and  $\bar{Q}$  will remain high as long as preset and clear are low, but Q and  $\bar{Q}$  are unpredictable, if preset and clear go high simultaneously.

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 7.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5\text{ V}$
Input voltage	$V_I$	-0.5 to 7.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5\text{ V}$
		50		$V_O = V_{CC} + 0.5\text{ V}$
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	100	mA	
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}\text{C}$	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.5 to 5.5	V	Data retention
		1.65 to 5.5		At operation
Input / output voltage	$V_I$	0 to 5.5	V	PR, CLR, CK, D
	$V_O$	0 to $V_{CC}$		$Q, \bar{Q}$
Operating temperature	$T_a$	-40 to 85	°C	
Output current	$I_{OH}$	-4	mA	$V_{CC} = 1.65\text{ V}$
		-8		$V_{CC} = 2.3\text{ V}$
		-12		$V_{CC} = 2.7\text{ V}$
		-24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
	$I_{OL}$	4	mA	$V_{CC} = 1.65\text{ V}$
		8		$V_{CC} = 2.3\text{ V}$
		12		$V_{CC} = 2.7\text{ V}$
		24		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	20	ns/V	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$
		10		$V_{CC} = 3.0\text{ V to }5.5\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	1.65 to 1.95	V <sub>CC</sub> ×0.65	—	V	
		2.3 to 2.7	1.7	—		
		2.7 to 3.6	2.0	—		
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—		
	V <sub>IL</sub>	1.65 to 1.95	—	V <sub>CC</sub> ×0.35	V	
		2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3		
Output voltage	V <sub>OH</sub>	1.65 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		1.65	1.2	—		I <sub>OH</sub> = -4 mA
		2.3	1.7	—		I <sub>OH</sub> = -8 mA
		2.7	2.2	—		I <sub>OH</sub> = -12 mA
		3.0	2.4	—		
		3.0	2.2	—		I <sub>OH</sub> = -24 mA
		4.5	3.8	—		
		V <sub>OL</sub>	1.65 to 5.5	—		0.2
	1.65		—	0.45	I <sub>OL</sub> = 4 mA	
	2.3		—	0.7	I <sub>OL</sub> = 8 mA	
	2.7		—	0.4	I <sub>OL</sub> = 12 mA	
	3.0		—	0.55		
	4.5		—	0.55	I <sub>OL</sub> = 24 mA	
	Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±5.0	μA	V <sub>IN</sub> = 3.6 V to 5.5 V
		2.7 to 5.5	—	5.0		V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	2.7 to 3.6	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND

## Switching Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Maximum clock frequency	f <sub>max</sub>	1.8±0.15	—	—	83	MHz		
		2.5±0.2	—	—	83			
		2.7	—	—	150			
		3.3±0.3	—	—	150			
		5.0±0.5	—	—	150			
Propagation delay time	t <sub>PLH</sub> t <sub>PHL</sub>	1.8±0.15	1.0	—	13.4	ns	CK	Q
		2.5±0.2	1.0	—	7.1			
		2.7	1.0	—	6.0			
		3.3±0.3	1.0	—	5.2			
		5.0±0.5	1.0	—	4.1			
	t <sub>PLH</sub> t <sub>PHL</sub>	1.8±0.15	1.0	—	14.4	ns	CK	Q̄
		2.5±0.2	1.0	—	7.7			
		2.7	1.0	—	6.0			
		3.3±0.3	1.0	—	5.2			
		5.0±0.5	1.0	—	4.4			
	t <sub>PLH</sub> t <sub>PHL</sub>	1.8±0.15	1.0	—	12.9	ns	PR or CLR	Q, Q̄
		2.5±0.2	1.0	—	7.0			
		2.7	1.0	—	6.0			
		3.3±0.3	1.0	—	5.4			
		5.0±0.5	1.0	—	4.1			
Setup time	t <sub>su</sub>	1.8±0.15	3.6	—	—	ns	Data	
		2.5±0.2	2.3	—	—			
		2.7	3.4	—	—			
		3.3±0.3	3.0	—	—			
		5.0±0.5	3.0	—	—			
	t <sub>su</sub>	1.8±0.15	2.7	—	—	ns	PR or CLR	
		2.5±0.2	1.9	—	—			
		2.7	2.2	—	—			
		3.3±0.3	2.0	—	—			
		5.0±0.5	2.0	—	—			
Hold time	t <sub>h</sub>	1.8±0.15	1.0	—	—	ns		
		2.5±0.2	1.0	—	—			
		2.7	1.0	—	—			
		3.3±0.3	0.0	—	—			
		5.0±0.5	0.0	—	—			
Pulse width	t <sub>w</sub>	1.8±0.15	4.1	—	—	ns	CK, PR, CLR	
		2.5±0.2	3.3	—	—			
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
		5.0±0.5	3.3	—	—			
Output skew between pins*1	t <sub>OSLH</sub> t <sub>OSSL</sub>	1.8±0.15	—	—	—	ns		
		2.5±0.2	—	—	—			
		2.7	—	—	—			
		3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			
Input capacitance	C <sub>IN</sub>	3.3	—	4.0	—	pF		

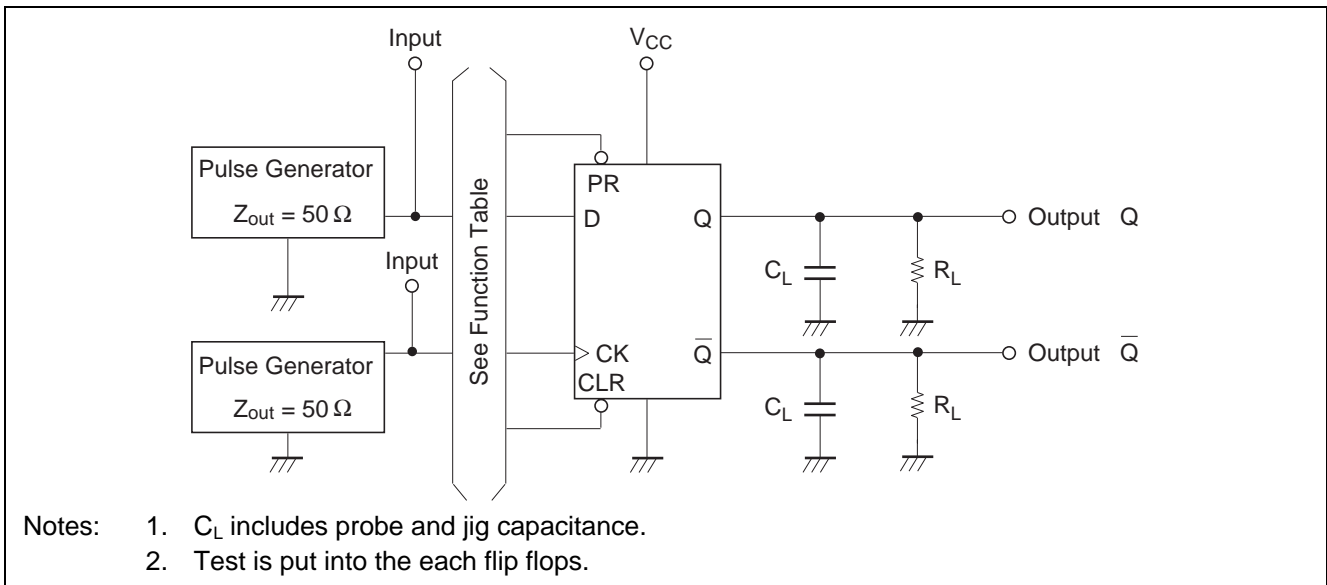
Note: 1. This parameter is characterized but not tested.

$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSSL} = |t_{PHLm} - t_{PHLn}|$$

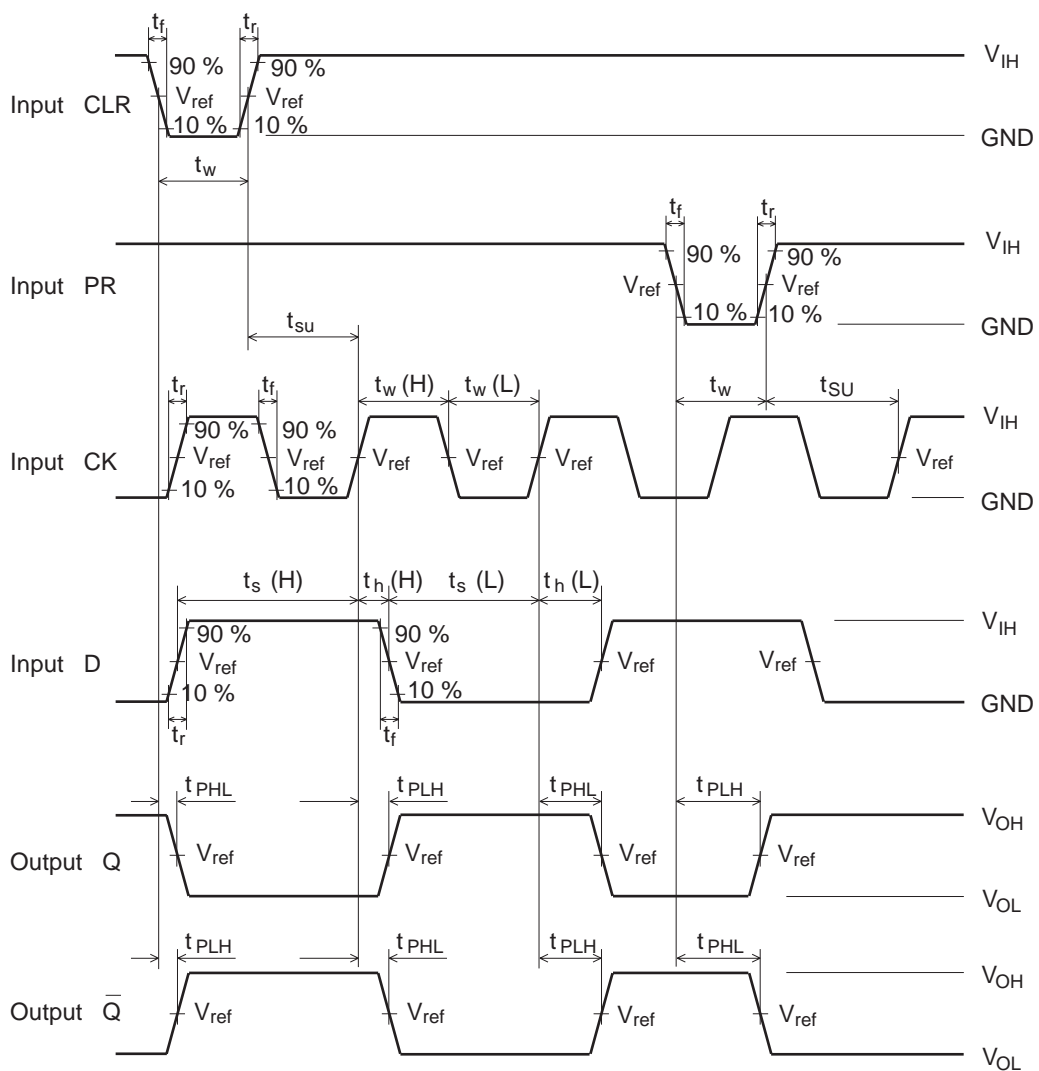
## Operating Characteristics

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^{\circ}C$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	$C_{PD}$	1.8	—	34	—	pF	$f = 10 \text{ MHz}$
		2.5	—	34	—		
		3.3	—	36	—		
		5.0	—	40	—		

## Test Circuit



## Waveforms

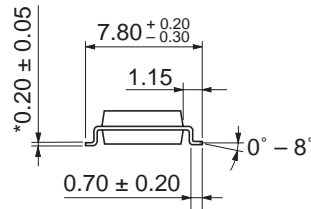
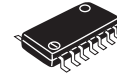
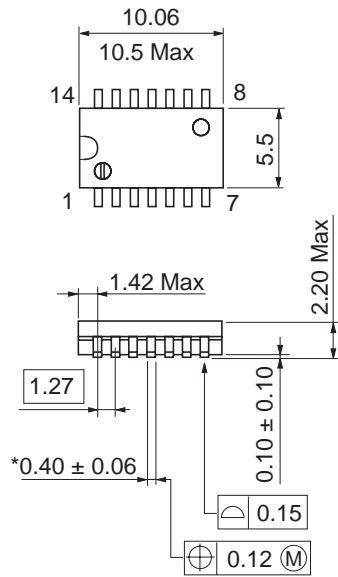


V <sub>cc</sub> (V)	INPUTS		V <sub>ref</sub>	C <sub>L</sub>	R <sub>L</sub>
	V <sub>IH</sub>	t <sub>r</sub> / t <sub>f</sub>			
V <sub>cc</sub> = 1.8±0.15 V	V <sub>cc</sub>	≤ 2 ns	1/2 V <sub>cc</sub>	30 pF	1.0 kΩ
V <sub>cc</sub> = 2.5±0.2 V	V <sub>cc</sub>	≤ 2 ns	1/2 V <sub>cc</sub>	30 pF	500 Ω
V <sub>cc</sub> = 2.7 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
V <sub>cc</sub> = 3.3±0.3 V	2.7 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
V <sub>cc</sub> = 5.0±0.5 V	V <sub>cc</sub>	≤ 2.5 ns	1/2 V <sub>cc</sub>	50 pF	500 Ω

- Notes: 1. Clock pulse Input waveform: PRR = 10 MHz, duty cycle 50%.  
 2. Data input waveform: PRR = 5 MHz, duty cycle 50%.

Package Dimensions

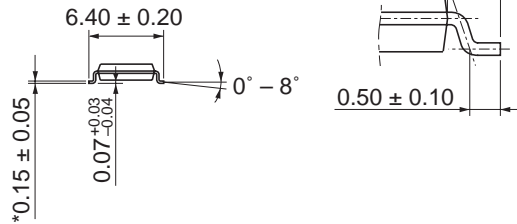
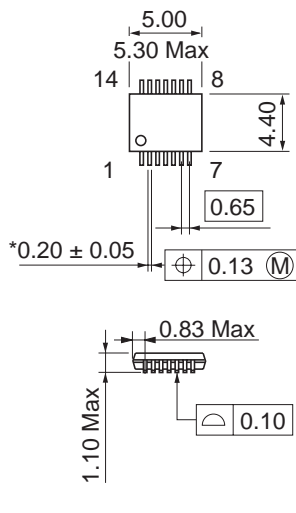
As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	TTP-14DV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g



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