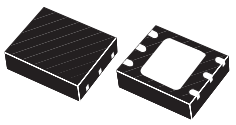
ST1S09

2 A, 1.5 MHz PWM step-down switching regulator with synchronous rectification

Features

- 1.5 MHz fixed frequency PWM with current control mode
- 2 A output current capability
- Typical efficiency: > 90%
- 2 % DC output voltage tolerance
- Two versions available: power good or inhibit
- Integrated output over-voltage protection
- Non switching quiescent current: (typ) 1.5 mA over temperature range
- R_{DSON} (typ) 100 mΩ
- Utilizes tiny capacitors and inductors
- Operating junction temp. -30 °C to 125 °C
- Available in DFN6 (3x3 mm) exposed pad



DFN6 (3x3mm)

Description

The ST1S09 is a step-down DC-DC converter optimized for powering low output voltage applications. It supplies a current in excess of 2 A over an input voltage range from 2.7 V to 6 V.

A high PWM switching frequency (1.5 MHz) allows the use of tiny surface-mount components.

Moreover, since the required synchronous rectifier is integrated, the number of the external components is reduced to minimum: a resistor divider, an inductor and two capacitors. The power good function continuously monitors the output voltage. An open drain power good flag is released when the output voltage is within regulation. In addition, a low output ripple is guaranteed by the current mode PWM topology and by the use of low E.S.R. SMD ceramic capacitors. The device is thermally protected and the output current limited to prevent damages due to accidental short circuit. The ST1S09 is available in the DFN6 3x3 mm package.

Table 1. Device summary

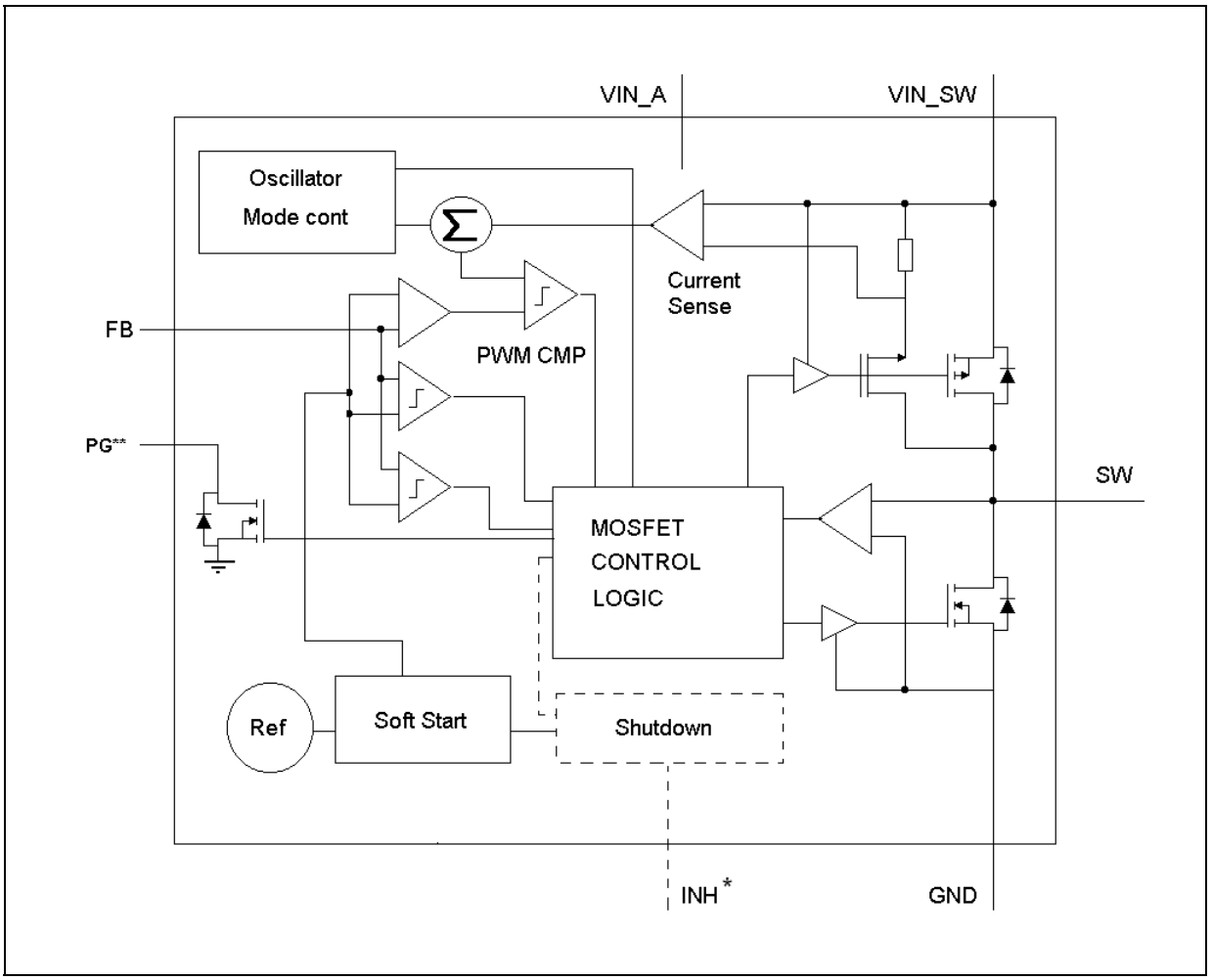
Order codes	Packaging	Package
ST1S09PU	ST1S09PUR	DFN6D (3x3 mm)
ST1S09APU (1)	ST1S09APUR	DFN6D (3x3 mm)
ST1S09IPU	ST1S09IPUR	DFN6D (3x3 mm)

1. Available on request.

Contents

1 Diagram

Figure 1. Schematic diagram

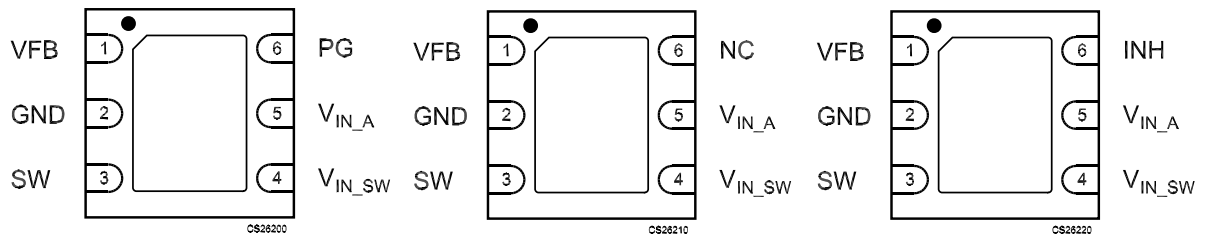


(*) Only for ST1S09IPU

(**) Only for ST1S09PU

2 Pin configuration

Figure 2. Pin connections (top view)



ST1S09 **ST1S09A** **ST1S09I**

Table 2. Pin description

Pin n°	Symbol	Name and function
1	FB	Feedback voltage
2	GND	System ground
3	SW	Switching pin
4	V_{IN_SW}	Power supply for the MOSFET switch
5	V_{IN_A}	Power supply for analog circuit
6	INH/PG/NC	Inhibit (to turn off the device) / Power Good / Not Connected.
Exposed Pad	GND	To be connected to PCB ground plane for optimal electrical and thermal performance.

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Inhibit voltage (I version)	-0.3 to V_I + 0.3	V
SWITCH Voltage	Max. voltage of output pin	-0.3 to 7	V
V_{FB}	Feedback voltage	-0.3 to 3	V
PG	Power Good open drain	-0.3 to 7	V
T_J	Max junction temperature	-40 to 150	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec	260	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	55	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	KV
ESD	ESD protection voltage	MM	500	V

4 Electrical characteristics

Table 6. Electrical characteristics for ST1S09PU Refer to *Figure 21* application circuit $V_{IN\_SW} = V_{IN\_A} = 5$ V, $V_O = 1.2$ V, C1 = 4.7 µF, C2 = 22 µF, L1 = 2.7 µH, T_J = -30 to 125 °C (unless otherwise specified. Typical values are referred to 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage		784	800	816	mV
I_{FB}	V_{FB} pin bias current				600	nA
V_I	Input voltage	I_O = 10mA to 2A	4.5		5.5	V
UV_{LO}	Under voltage lock out threshold	V_I Rising	3.5	3.7	3.9	V
		Hysteresis		150		mV
OVP	Over voltage protection threshold	V_O rising	1.05 V_O	1.1 V_O		V
	Over voltage protection hysteresis	V_O falling		5		%
I_{OVP}	Overvoltage clamping current	V_O = 1.2V		300		mA
I_Q	Quiescent current	Not switching		1.5	2.5	mA
I_O	Output current	V_I = 4.5 to 5.5V *Note 1*	2			A
$\%V_O/\Delta V_I$	Output line regulation	V_I = 4.5V to 5.5V, I_O = 100mA *Note 1*		0.16		$\%V_O/\Delta V_I$
$\%V_O/\Delta I_O$	Output load regulation	I_O = 10mA to 2A *Note 1*		0.2	0.6	%
$PWMf_S$	PWM switching frequency	V_{FB} = 0.65V	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle		80	87		%
PG	Power good output threshold			0.92 V_O		V
	Power good output voltage low	I_{SINK} = 6mA open drain output			0.4	V
R_{DSON}-N	NMOS switch on resistance	I_{SW} = 750 mA		0.1		Ω
R_{DSON}-P	PMOS switch on resistance	I_{SW} = 750 mA		0.1		Ω
I_{SWL}	Switching current limitation	*Note 1*	2.5	2.9	3.5	A
ν	Efficiency *Note 1*	I_O = 10mA to 100mA, V_O = 3.3V	65			%
		I_O = 100mA to 2A, V_O = 3.3V	82	87		
T_{SHDN}	Thermal shutdown			150		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
$\%V_O/\Delta I_O$	Load transient response	I_O = 100mA to 1A, T_A = 25°C $t_R = t_F \geq$ 200ns, *Note 1*	-10		+10	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	I_O = 10mA to I_O = short, T_A = 25°C *Note 1*	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production.

Table 7. Electrical characteristics for ST1S09IPU Refer to *Figure 22* application circuit
$V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5$ V, $V_O = 1.2$ V, C1 = 4.7 µF, C2 = 22 µF, L1 = 2.7 µH,
T_J = -30 to 125 °C (unless otherwise specified. Typical values are referred to 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
FB	Feedback voltage		784	800	816	mV
I_{FB}	V_{FB} pin bias current				600	nA
V_I	Minimum input voltage	I_O = 10mA to 2A	2.7			V
OVP	Over voltage protection threshold	V_O rising	1.05 V_O	1.1 V_O		V
	Over voltage protection hysteresis	V_O falling		5		%
I_Q	Quiescent current	V_{INH} > 1.2V, not switching		1.5	2.5	mA
		V_{INH} < 0.4V, T = - 30°C to 85°C			1	µA
I_O	Output current	V_I = 2.7 to 5.5V *Note 1*	2			A
V_{INH}	Inhibit threshold	Device ON, V_I = 2.7 to 5.5V	1.3			V
		Device ON, V_I = 2.7 to 5V	1.2			
		Device OFF			0.4	
I_{INH}	Inhibit pin current				2	µA
$\%V_O/\Delta V_I$	Output line regulation	V_I = 2.7V to 5.5V, I_O = 100mA *Note 1*		0.16		$\%V_O/\Delta V_I$
$\%V_O/\Delta I_O$	Output load regulation	I_O = 10mA to 2A *Note 1*		0.2	0.6	$\%V_O/\Delta I_O$
PWMf_S	PWM switching frequency	V_{FB} = 0.65V	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle		80	87		%
R_{DSON}-N	NMOS switch on resistance	I_{SW} = 750 mA		0.1		Ω
R_{DSON}-P	PMOS switch on resistance	I_{SW} = 750 mA		0.1		Ω
I_{SWL}	Switching current limitation	*Note 1*	2.5	2.9	3.5	A
ν	Efficiency *Note 1*	I_O = 10mA to 100mA, V_O = 3.3V	65			%
		I_O = 100mA to 2A, V_O = 3.3V	82	87		
T_{SHDN}	Thermal shutdown			150		°C
T_{HYS}	Thermal shutdown hysteresis			20		°C
$\%V_O/\Delta I_O$	Load transient response	I_O = 100mA to 1A, T_A = 25°C $t_R = t_F \geq$ 200ns, *Note 1*	-10		+10	$\%V_O$
$\%V_O/\Delta I_O$	Short circuit removal response	I_O = 10mA to I_O = short, T_A = 25°C *Note 1*	-10		+10	$\%V_O$

Note: 1 Guaranteed by design, but not tested in production.

5 Typical performance characteristics

($L = 3.3\ \mu H$, $C_I = 4.7\ \mu F$, $C_O = 22\ \mu F$, unless otherwise specified)

Figure 3. Voltage feedback vs temperature

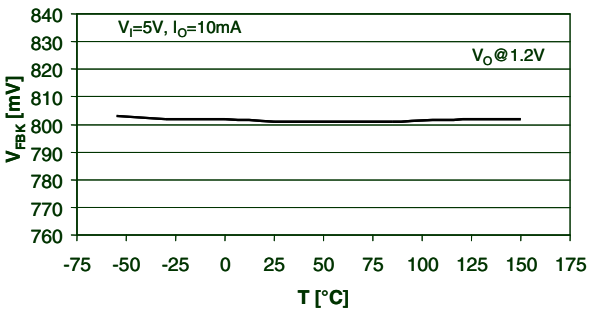


Figure 4. Feedback pin bias current vs temp.

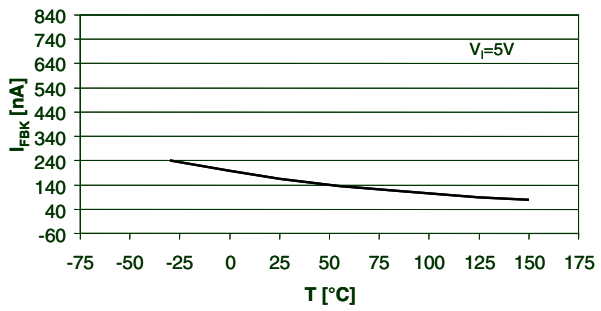


Figure 5. Quiescent current non switching vs temperature

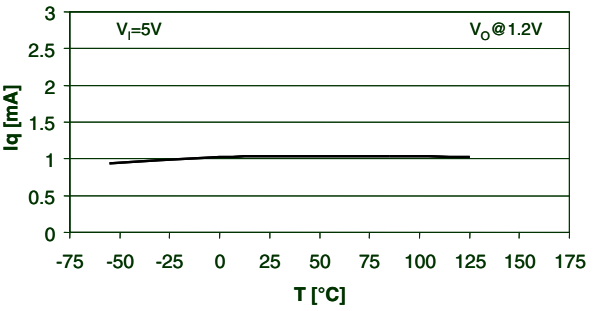


Figure 6. Inhibit voltage vs temperature

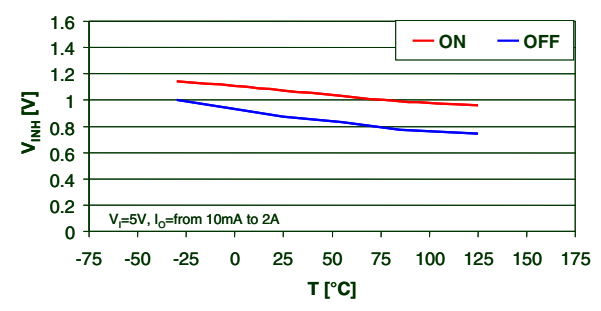


Figure 7. Inhibit voltage vs input voltage

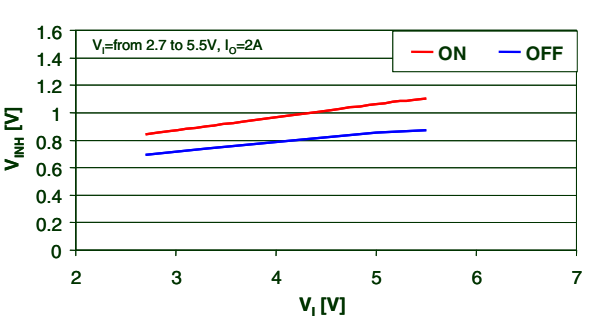


Figure 8. Output voltage vs input voltage

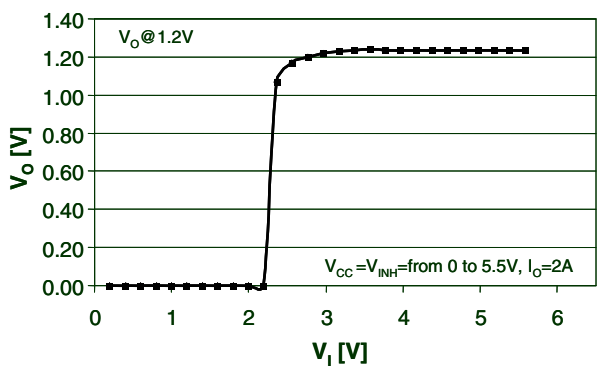


Figure 9. Line regulation vs temperature

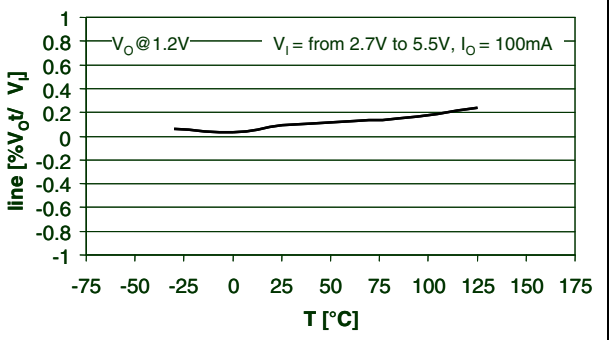


Figure 10. Load regulation vs temperature

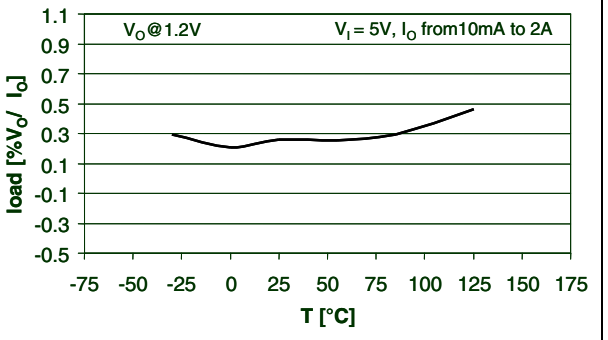


Figure 11. PWM Switching frequency vs temperature

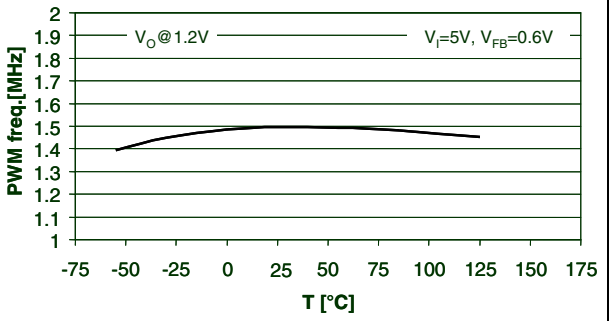


Figure 12. Maximum duty cycle vs temperature

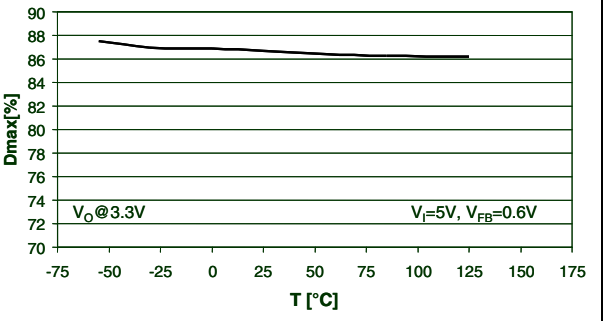


Figure 13. Under voltage lock out threshold vs temperature

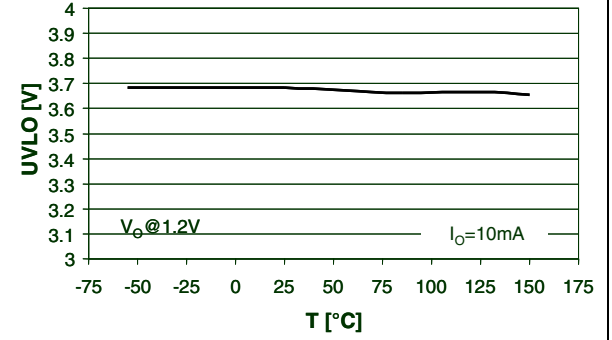


Figure 14. Efficiency vs output current

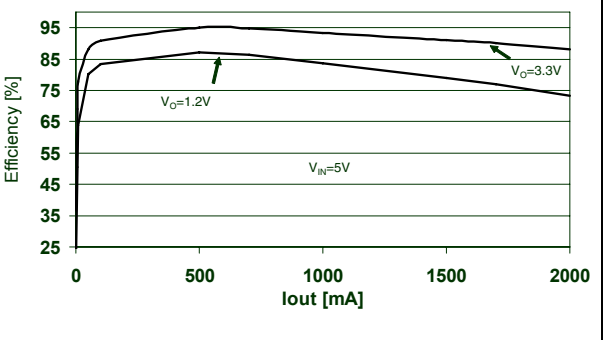


Figure 15. Efficiency vs temperature

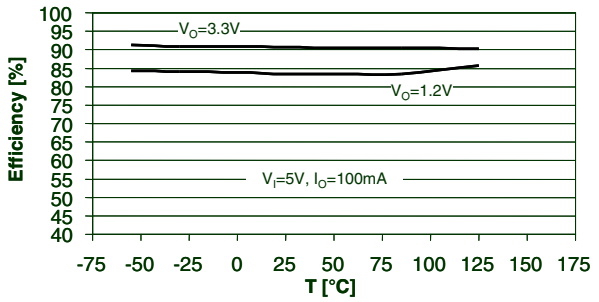


Figure 16. Over voltage protection vs temperature

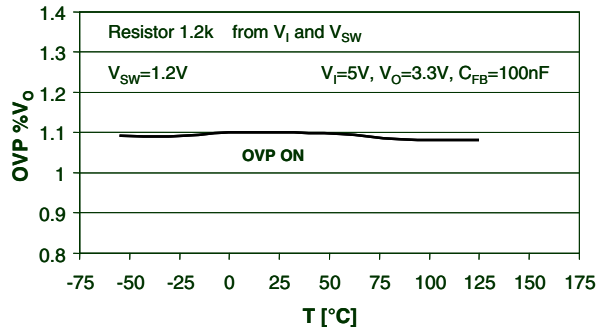


Figure 17. Over voltage protection vs temperature

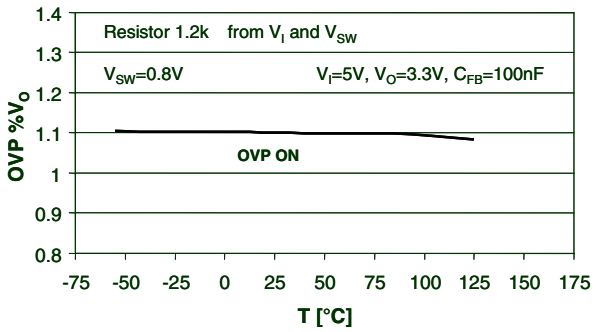


Figure 18. Over voltage protection hyst. vs temperature

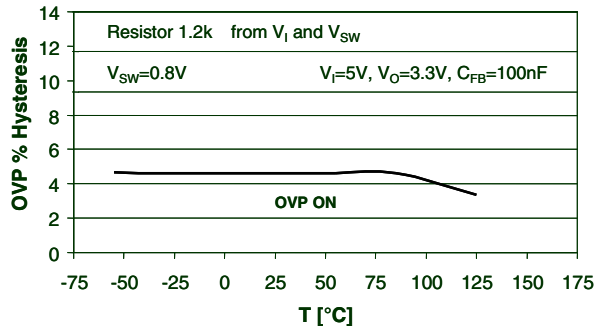
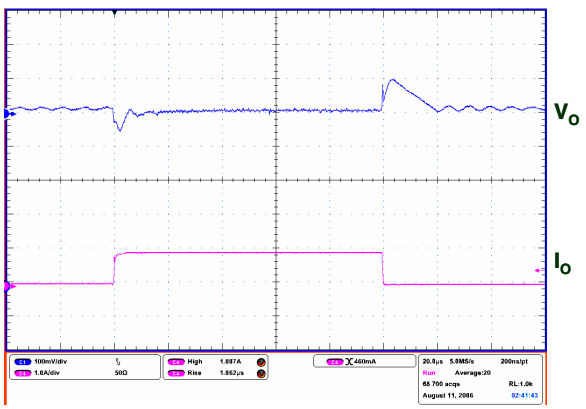
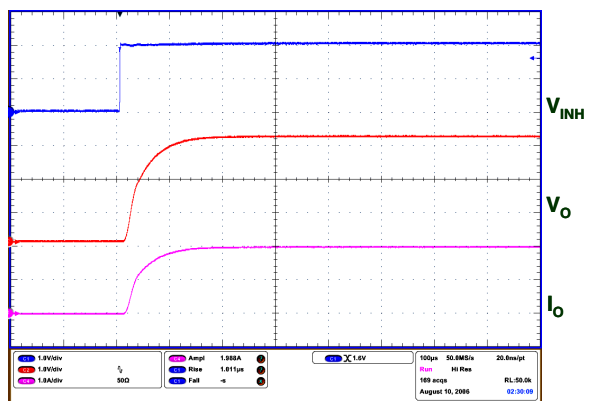


Figure 19. Load transient



V_I=5V, V_O=1.2V, I_O=100mA to1A, L=3.3µH, C_I=4.7µF, C_O=22µF

Figure 20. Inhibit transient



V_I=5V, V_{INH}=0 to 2V, I_O=2A, L=3.3µH, C_I=4.7µF, C_O=22µF, V_O=3.3V

6 Typical application

Figure 21. Application circuits

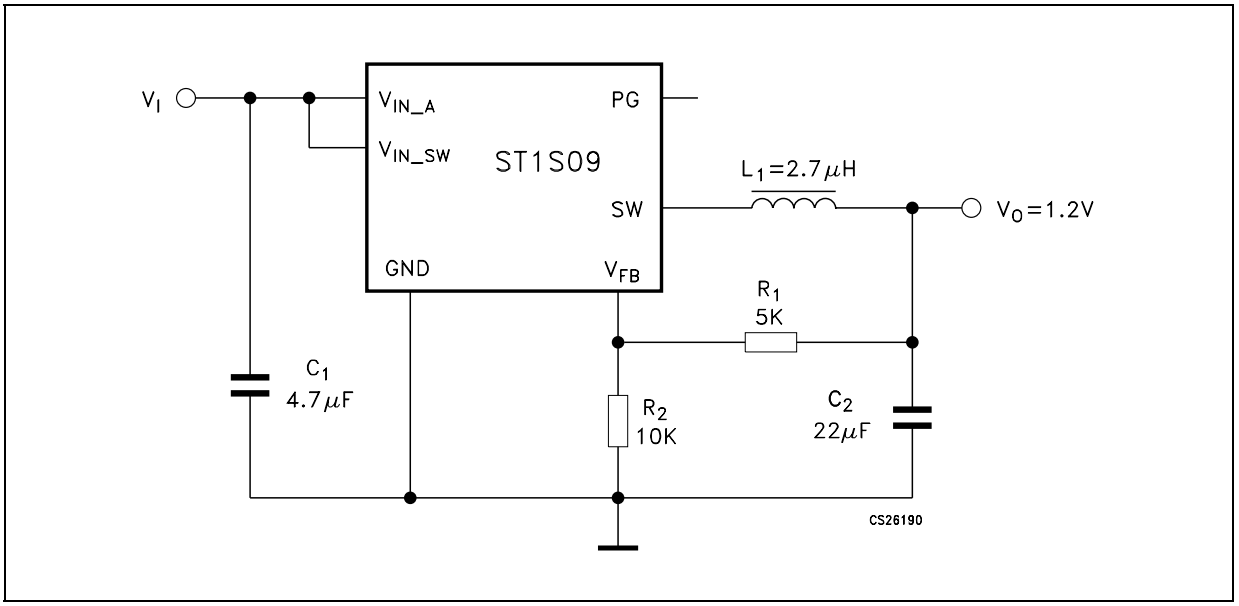
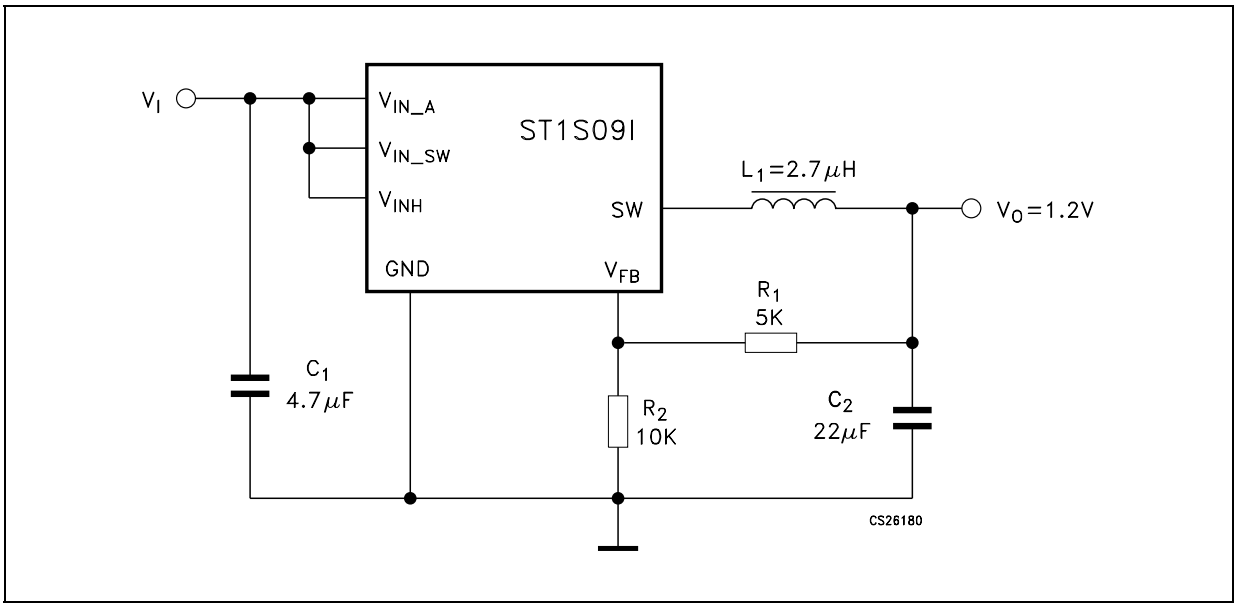


Figure 22. Application circuits



7 Application information

The ST1S09 is an adjustable current mode PWM step-down DC/DC converter with internal 2 A power switch, packaged in a DFN6 3x3 mm.

The device is a complete 2 A switching regulator with its internal compensation eliminating the need for additional components.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors results in low, predictable output ripple.

The over-voltage protection circuit acts when the output voltage is over 10 % of the rated voltage and within 200 ns the low side MOSFET will be turned on to clamp the output transient. The current limit for clamping is about 400 mA. When the output voltage drops to about 5 % above the nominal level, the device returns to nominal closed loop switching operation.

The open drain Power Good (PG) pin is released when the output voltage is higher than 0.92 x V_{O_NOM}. If the output voltage is below 0.92 x V_O, the PG pin goes to low impedance.

Other circuits fitted to the device protection are the Thermal Shut-down block, which turns off the regulator when the junction temperature exceeds 150 °C (typ), and the cycle-by-cycle Current Limiting, which provides protection against shorted outputs.

As an adjustable regulator, the ST1S09's output voltage is determined by an external resistor divider. The desired value is given by the following equation:

$V_O = V_{FB}[1+R1/R2]$

To utilize the device, only a few components are required: an inductor, two capacitors and the resistor divider. The inductor chosen must be able to reach peak current level without saturating. Its value can be selected while taking into account that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce package size and the total cost of the application. Finally, the ST1S09 has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These types of capacitors, due to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the correct functioning of the device.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

DFN6D (3x3) Mechanical Data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.00	0.031		0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23		0.45	0.009		0.018
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23		2.50	0.088		0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.75	0.059		0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020

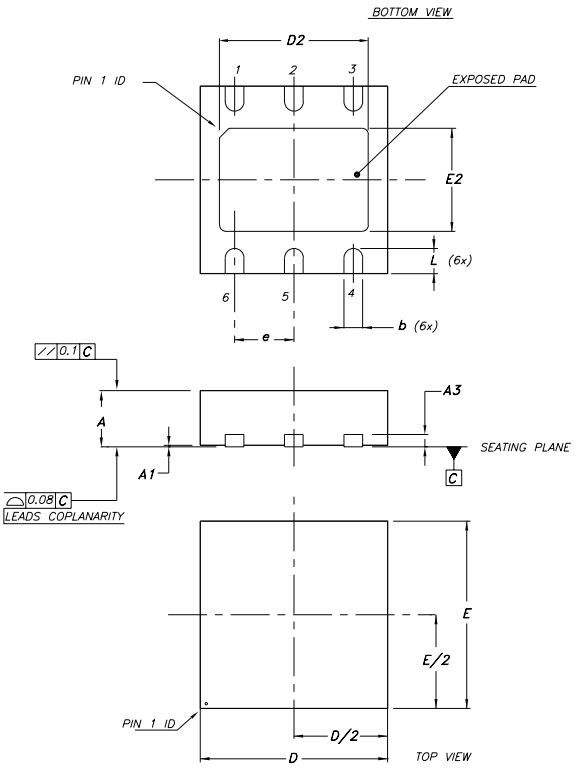


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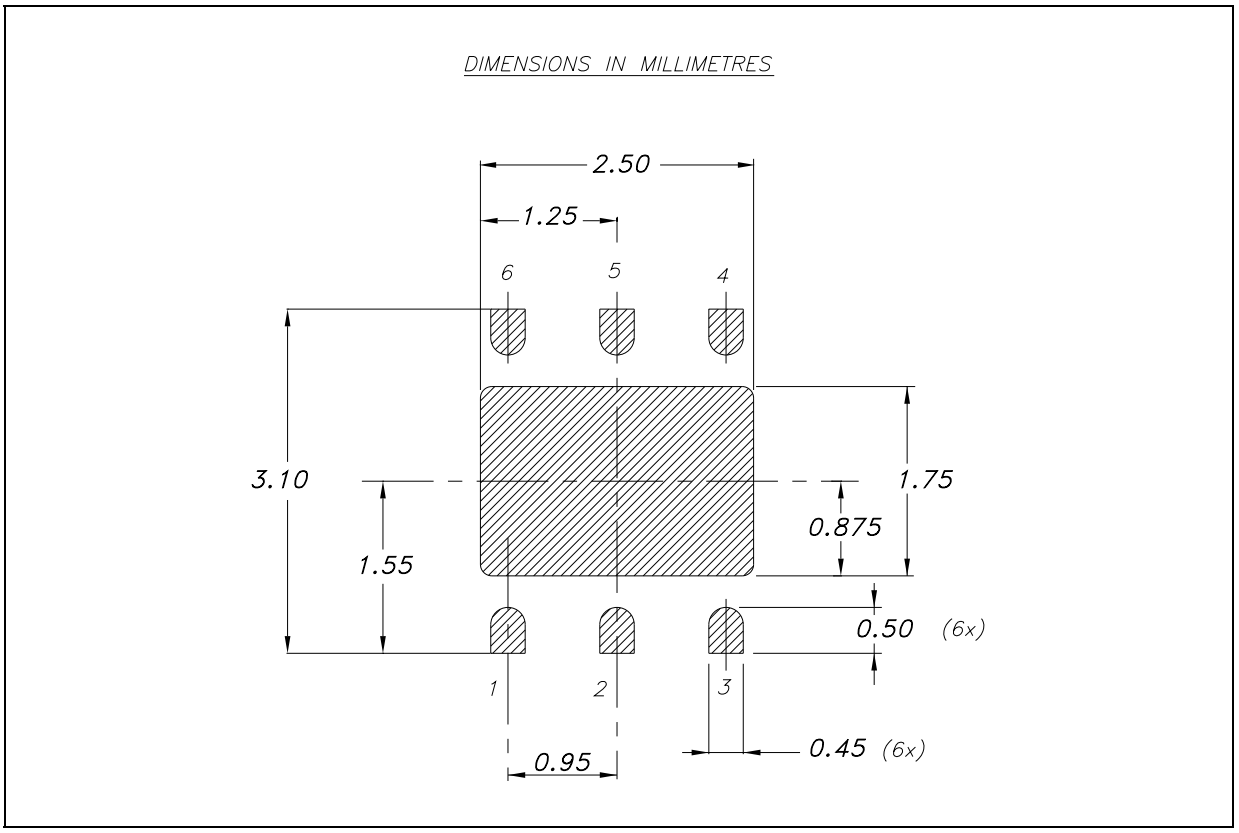
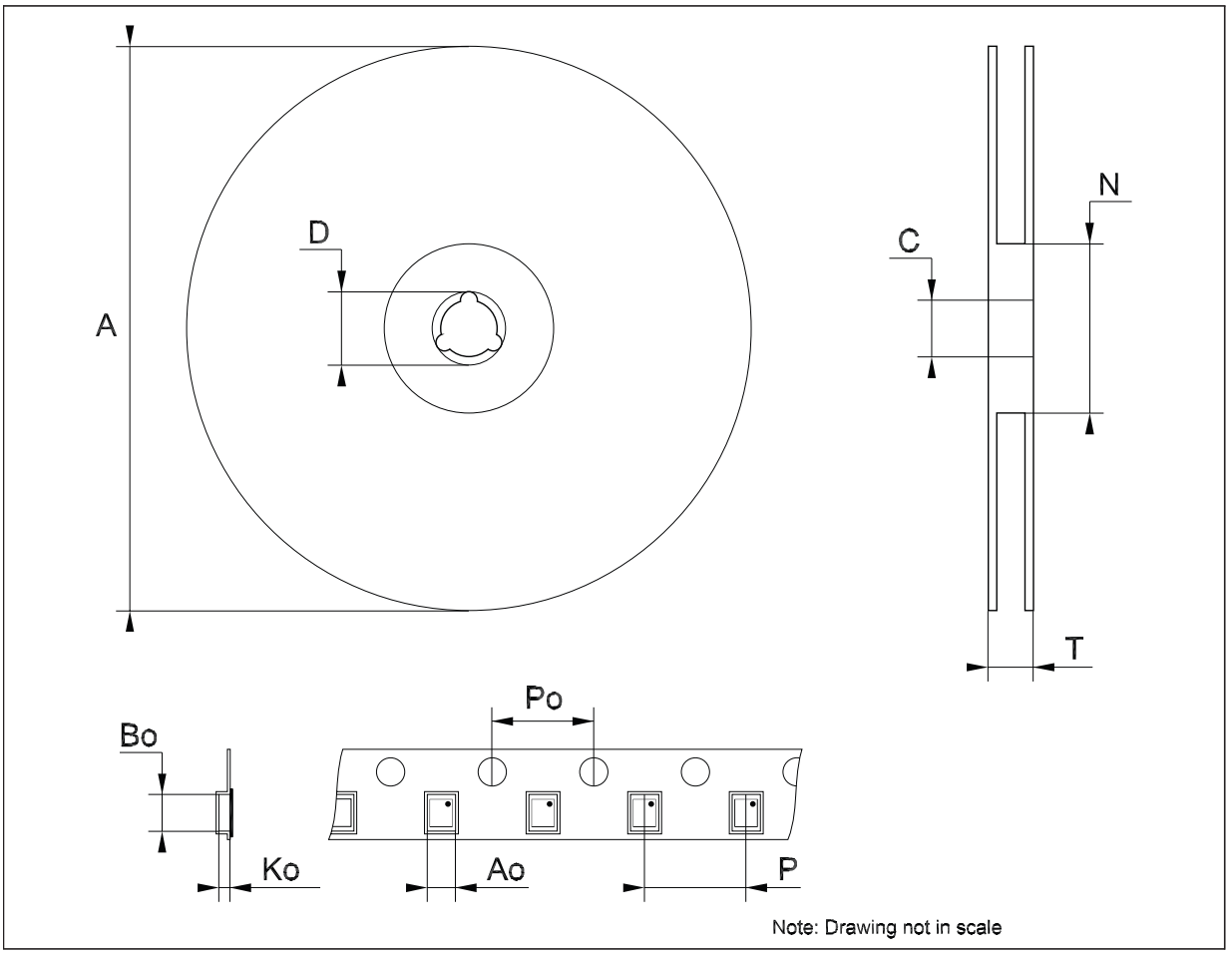
Figure 23. DFN6 (3x3 mm) footprint recommended data



Tape & Reel QFNxx/DFNxx (3x3) Mechanical Data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			18.4			0.724
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
18-Jun-2007	1	First Issue.
05-Jul-2007	2	Removed incorrect watermark.
31-Jan-2008	3	Modified: *Table 6 on page 6*.

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