ZXMC3F31DN8
30V SO8 Complementary dual enhancement mode MOSFET

Summary

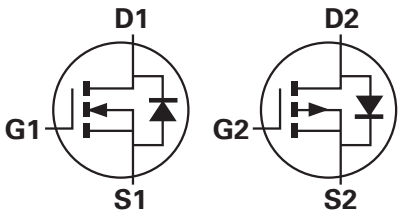
Device	$V_{(BR)DSS}$ (V)	Q_G (nC)	$R_{DS(on)}$ (Ω)	I_D (A)
Q1	30	12.9	0.024 @ V_{GS}= 10V	7.3
			0.039 @ V_{GS}= 4.5V	5.7
Q2	-30	12.7	0.045 @ V_{GS}= -10V	5.3
			0.080 @ V_{GS}= -4.5V	4

Description

This new generation Trench MOSFET from Zetex has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance making it ideal for power management and battery charging functions.

Features

- Low on-resistance
- 4.5V gate drive capability
- Low profile SOIC package



Q1 N-Channel Q2 P-Channel

Applications

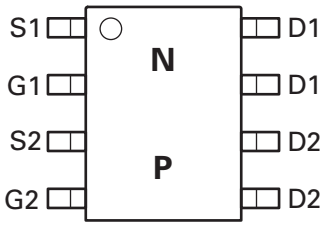
- DC-DC Converters
- SMPS
- Load switching switches
- Motor control
- Backlighting

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMC3F31DN8TA	7	12	500

Device marking

ZXMC
3F31



Top view

Absolute maximum ratings

Parameter	Symbol	N-channel Q1	P-channel Q2	Unit
Drain-Source voltage	V_{DSS}	30	-30	V
Gate-Source voltage	V_{GS}	±20	±20	V
Continuous Drain current @ V_{GS}= 10V; T_A=25°C (b)(d)	I_D	7.3	5.3	A
@ V_{GS}= 10V; T_A=70°C (b)(d)		5.9	4.3	
@ V_{GS}= 10V; T_A=25°C (a)(d)		5.7	4.1	
@ V_{GS}= 10V; T_A=25°C (a)(e)		6.8	4.9	
@ V_{GS}= 10V; T_L=25°C (f)(d)		7.8	5.7	
Pulsed Drain current (c)	I_{DM}	33	23	A
Continuous Source current (Body diode) (b)(d)	I_S	3.5	3.2	A
Pulsed Source current (Body diode) (c)(d)	I_{SM}	33	23	A
Power dissipation at T_A =25°C (a)(d) Linear derating factor	P_D	1.25 10		W mW/°C
Power dissipation at T_A =25°C (a)(e) Linear derating factor	P_D	1.8 14		W mW/°C
Power dissipation at T_A =25°C (b)(d) Linear derating factor	P_D	2.1 17		W mW/°C
Power dissipation at T_L =25°C (f) (d) Linear derating factor	P_D	2.35 19		W mW/°C
Operating and storage temperature range	T_j, T_{stg}	-55 to 150		°C

Thermal resistance

Parameter	Symbol	Value	Unit
Junction to ambient (a)(d)	$R_{\theta JA}$	100	°C/W
Junction to ambient (a)(e)	$R_{\theta JA}$	70	°C/W
Junction to ambient (b)(d)	$R_{\theta JA}$	60	°C/W
Junction to lead (f) (d)	$R_{\theta JL}$	53	°C/W

NOTES:

(a) For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions.

(b) Mounted on FR4 PCB measured at t ≤ 10 sec.

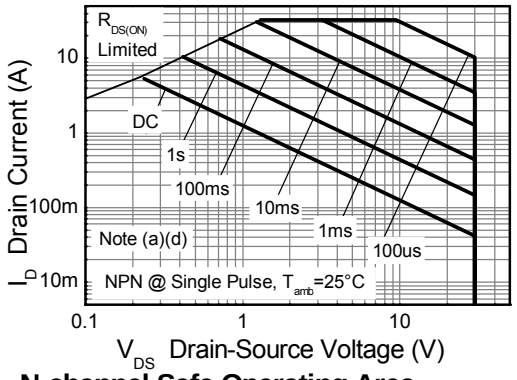
(c) Repetitive rating on 25mm x 25mm FR4 PCB, D=0.02, pulse width 300us – pulse width limited by maximum junction temperature.

(d) For a device with one active die.

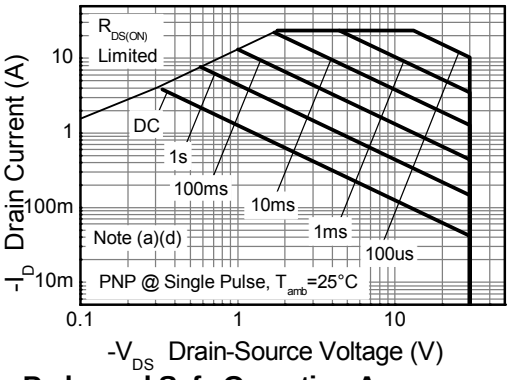
(e) For a device with two active die running at equal power.

(f) Thermal resistance from junction to solder-point (at the end of the drain lead).

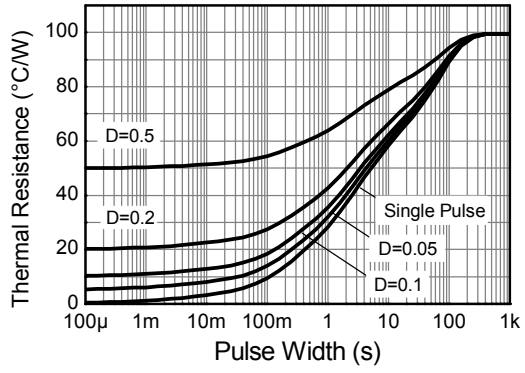
Thermal characteristics



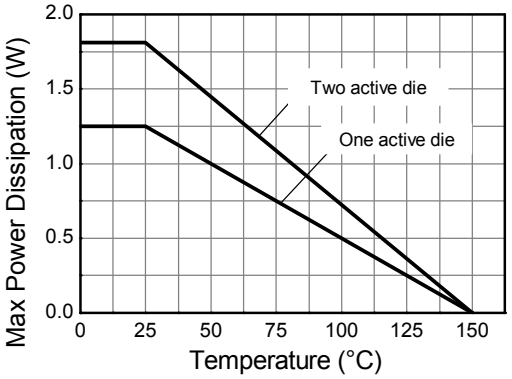
N-channel Safe Operating Area



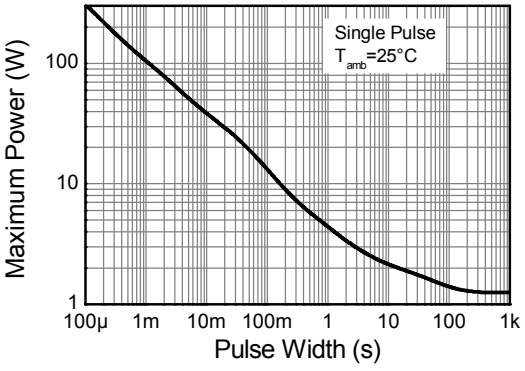
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Q1 N-channel electrical characteristics (at T_{amb} = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	30			V	I_D = 250μA, V_{GS}=0V
Zero Gate voltage Drain current	I_{DSS}			0.5	μA	V_{DS}=30V, V_{GS}=0V
Gate-Body leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source threshold voltage	$V_{GS(th)}$	1.0		3.0	V	I_D= 250μA, V_{DS}=V_{GS}
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.024 0.039	Ω	V_{GS}= 10V, I_D= 7.0A V_{GS}= 4.5, I_D= 6.0A
Forward Transconductance (*) (†)	g_{fs}		16.5		S	V_{DS}= 15V, I_D= 7.0A
Dynamic (†)						
Input capacitance	C_{iss}		608		pF	V_{DS}= 15V, V_{GS}=0V f=1MHz
Output capacitance	C_{oss}		132		pF	
Reverse transfer capacitance	C_{rss}		72		pF	
Switching (‡) (†)						
Turn-on-delay time	$t_{d(on)}$		2.9		ns	V_{DD}= 15V, V_{GS}=10V I_D= 1A $R_G \cong 6.0\Omega$,
Rise time	t_r		3.3		ns	
Turn-off delay time	$t_{d(off)}$		16		ns	
Fall time	t_f		8		ns	
Total Gate charge	Q_g		12.9		nC	V_{DS}= 15V, V_{GS}= 10V I_D= 7A
Gate-Source charge	Q_{gs}		2.5		nC	
Gate-Drain charge	Q_{gd}		2.52		nC	
Source–Drain diode						
Diode forward voltage (*)	V_{SD}		0.82	1.2	V	I_S= 1.7A,V_{GS}=0V
Reverse recovery time (‡)	t_{rr}		12		ns	I_S= 2.2A,di/dt=100A/μs
Reverse recovery charge(‡)	Q_{rr}		4.8		nC	

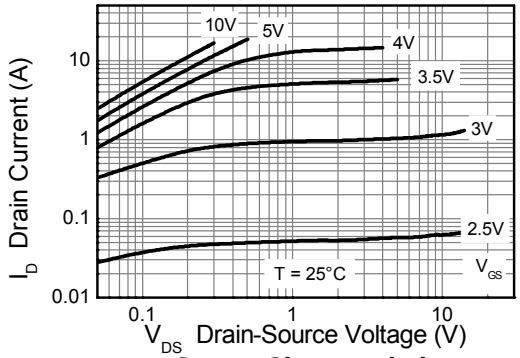
NOTES:

(*) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%.

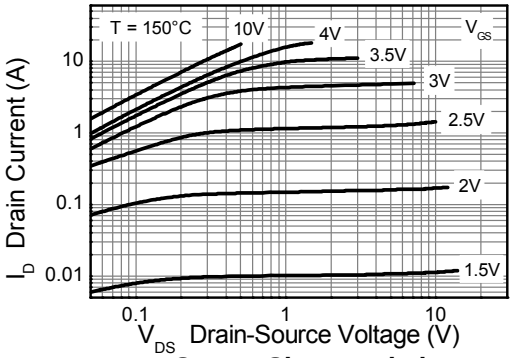
(†)Switching characteristics are independent of operating junction temperature.

(‡)For design aid only, not subject to production testing

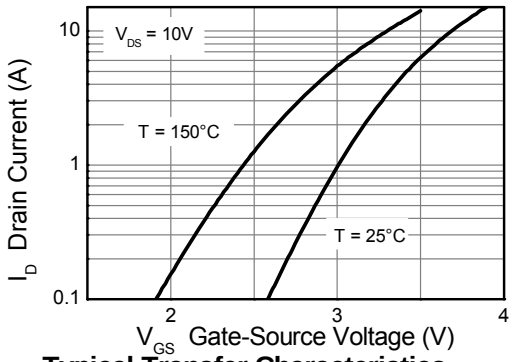
Q1 Typical characteristics



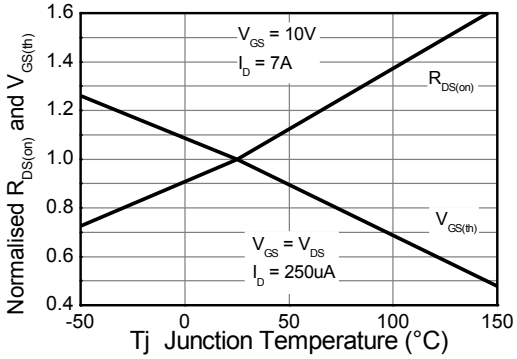
Output Characteristics



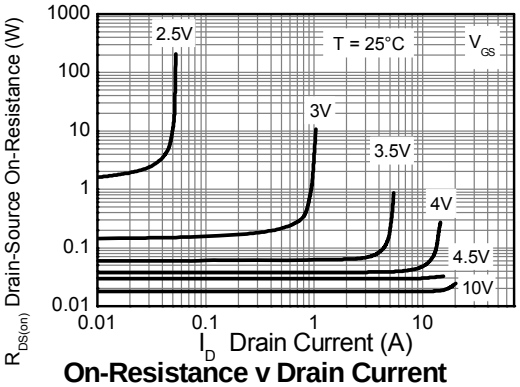
Output Characteristics



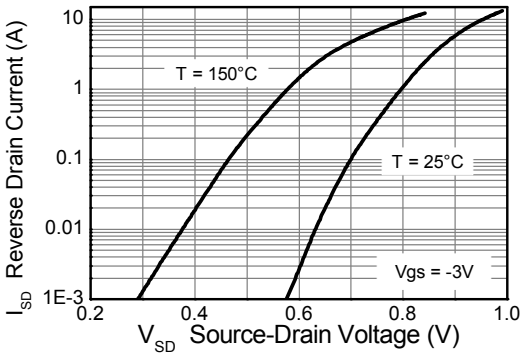
Typical Transfer Characteristics



Normalised Curves v Temperature

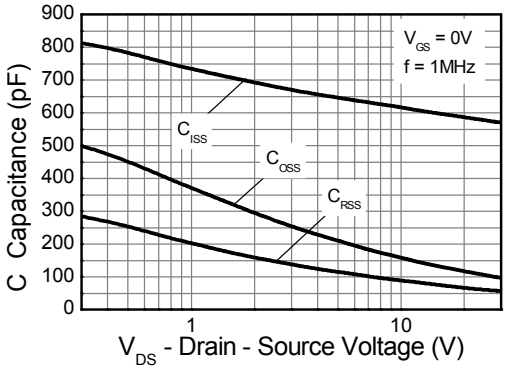


On-Resistance v Drain Current

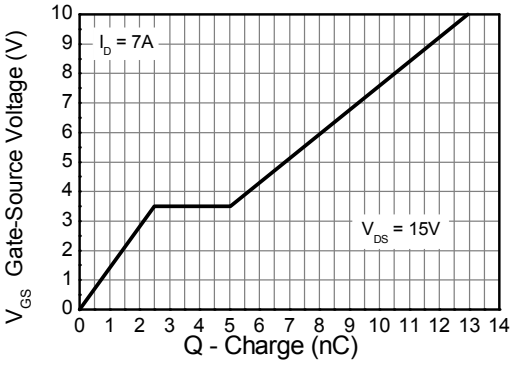


Source-Drain Diode Forward Voltage

Q1 Typical characteristics –cntd.

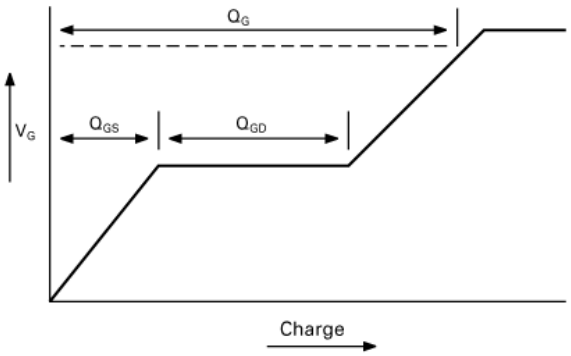


Capacitance v Drain-Source Voltage

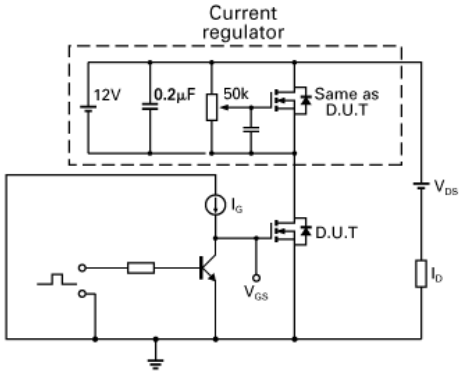


Gate-Source Voltage v Gate Charge

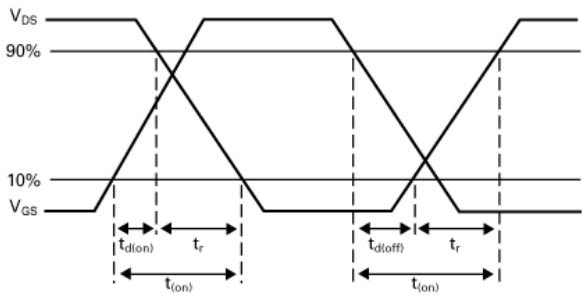
Test circuits



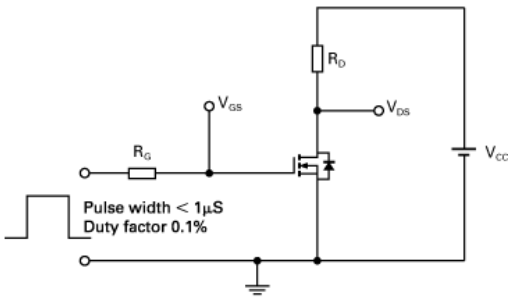
Basic gate charge waveform



Gate charge test circuit



Switching time waveforms



Switching time test circuit

Q2 P-channel electrical characteristics (at T_{amb} = 25°C unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-Source breakdown voltage	$V_{(BR)DSS}$	-30			V	I_D = -250μA, V_{GS}=0V
Zero Gate voltage Drain current	I_{DSS}			-5.0	μA	V_{DS}=-30V, V_{GS}=0V
Gate-Body leakage	I_{GSS}			-100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source threshold voltage	$V_{GS(th)}$	-1.0		-3.0	V	I_D= -250μA, V_{DS}=V_{GS}
Static Drain-Source on-state resistance (*)	$R_{DS(on)}$			0.045 0.080	Ω	V_{GS}= -10V, I_D= -5.0A V_{GS}= -4.5V, I_D= -4.0A
Forward Transconductance (*) (†)	g_{fs}		14		S	V_{DS}= -15V, I_D= -5.0A
Dynamic (†)						
Input capacitance	C_{iss}		670		pF	V_{DS}= -15V, V_{GS}=0V f=1MHz
Output capacitance	C_{oss}		126		pF	
Reverse transfer capacitance	C_{rss}		70		pF	
Switching (‡) (†)						
Turn-on-delay time	$t_{d(on)}$		1.9		ns	V_{DD}= -15V, V_{GS}=-10V I_D= -1A $R_G \cong 6.0\Omega$,
Rise time	t_r		3		ns	
Turn-off delay time	$t_{d(off)}$		30		ns	
Fall time	t_f		21		ns	
Total Gate charge	Q_g		12.7		nC	V_{DS}= -15V, V_{GS}= -10V I_D= -5A
Gate-Source charge	Q_{gs}		2		nC	
Gate-Drain charge	Q_{gd}		2.4		nC	
Source–Drain diode						
Diode forward voltage (*)	V_{SD}		-0.82	-1.2	V	I_S= -2A,V_{GS}=0V
Reverse recovery time (‡)	t_{rr}		16.5		ns	I_S= -2.1A,di/dt=100A/μs
Reverse recovery charge(‡)	Q_{rr}		11.5		nC	

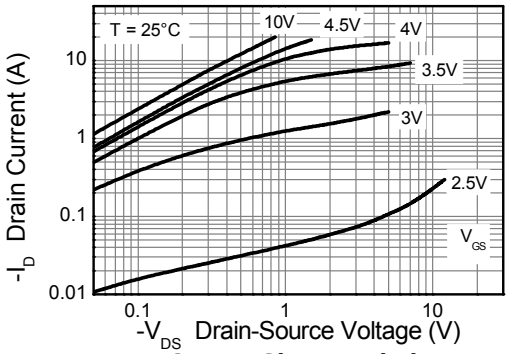
NOTES:

(*) Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%.

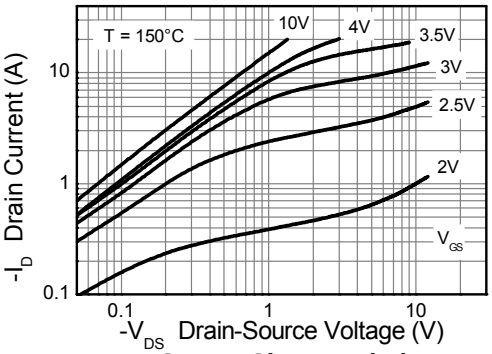
(†)Switching characteristics are independent of operating junction temperature.

(‡)For design aid only, not subject to production testing

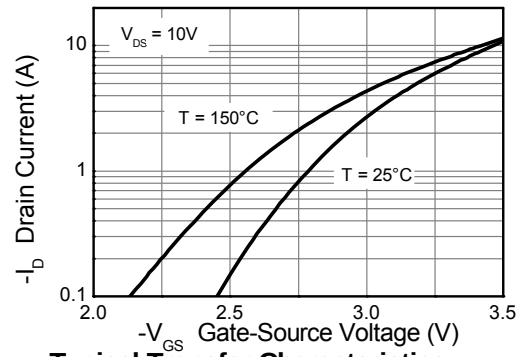
Typical characteristics



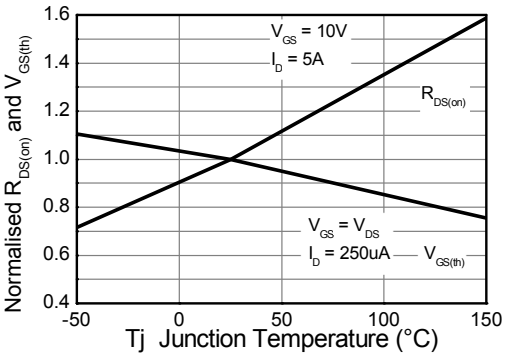
Output Characteristics



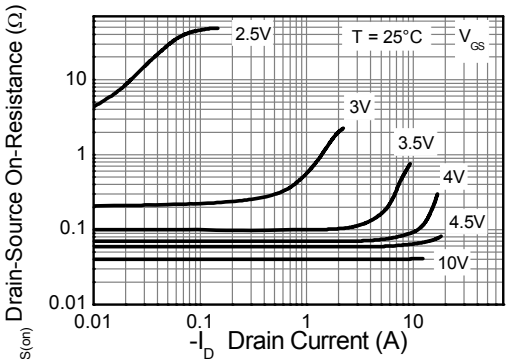
Output Characteristics



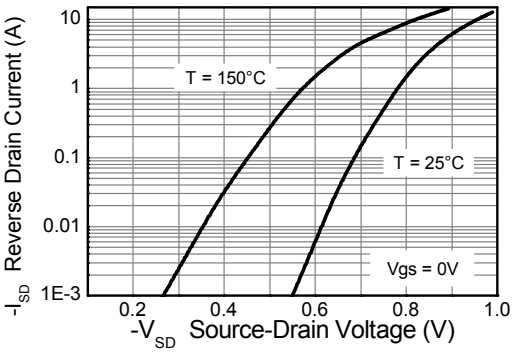
Typical Transfer Characteristics



Normalised Curves v Temperature

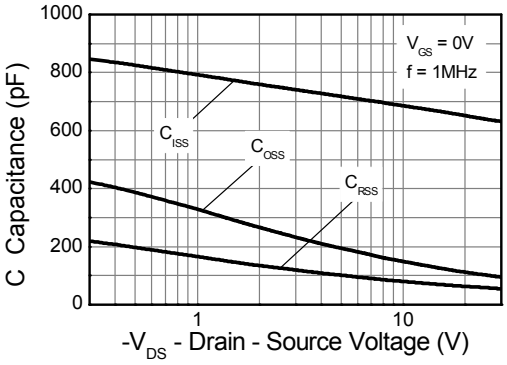


On-Resistance v Drain Current

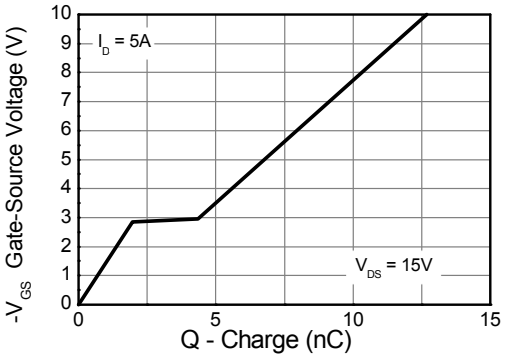


Source-Drain Diode Forward Voltage

Typical characteristics

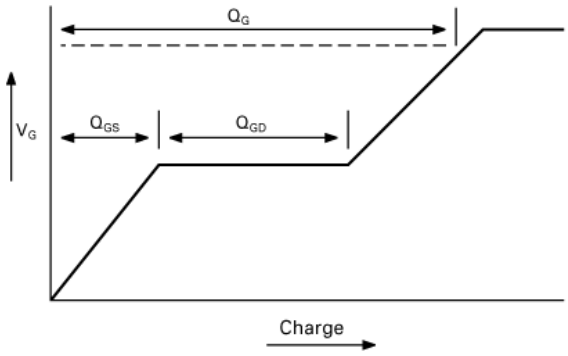


Capacitance v Drain-Source Voltage

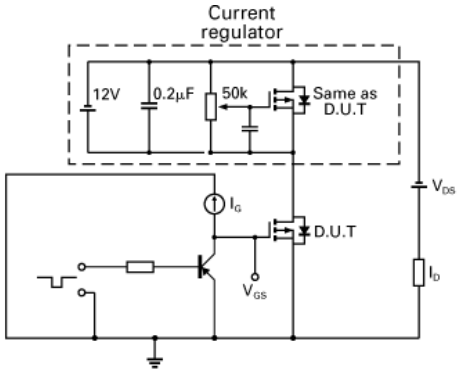


Gate-Source Voltage v Gate Charge

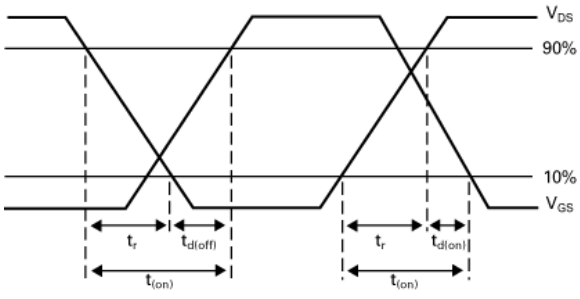
Test circuits



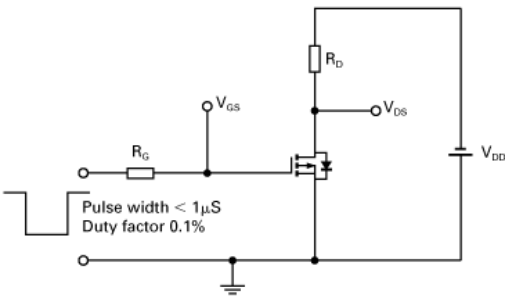
Basic gate charge waveform



Gate charge test circuit

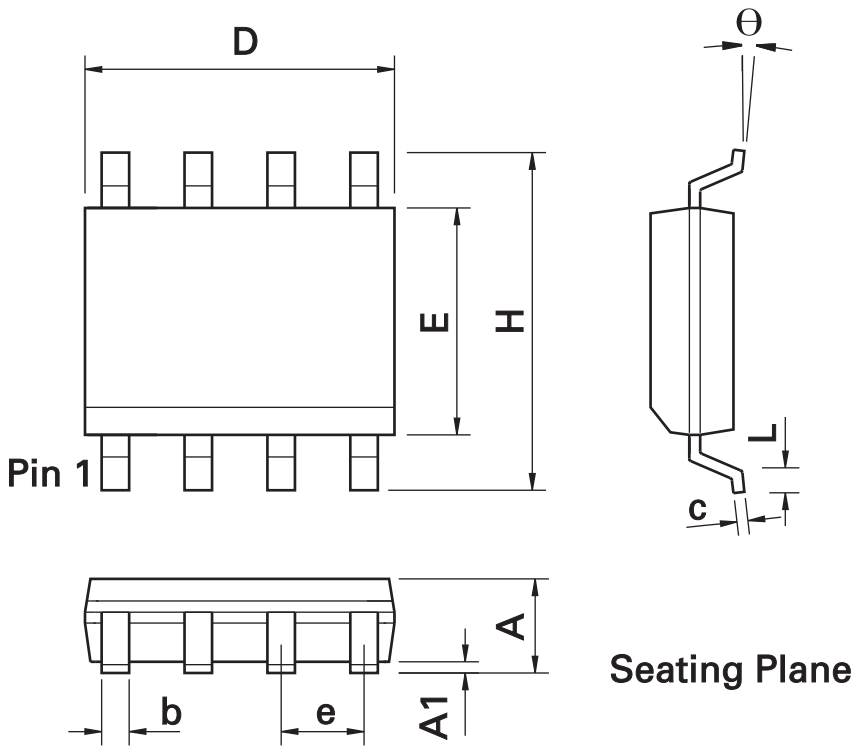


Switching time waveforms



Switching time test circuit

Package outline SO8



SO8 Package Information

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	U	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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or

   2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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ESD (Electrostatic discharge)

Semiconductor devices are susceptible to damage by ESD. Suitable precautions should be taken when handling and transporting devices. The possible damage to devices depends on the circumstances of the handling and transporting, and the nature of the device. The extent of damage can vary from immediate functional or parametric malfunction to degradation of function or performance in use over time. Devices suspected of being affected should be replaced.

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All Diodes Zetex components are compliant with the RoHS directive, and through this it is supporting its customers in their compliance with WEEE and ELV directives.

Product status key:

"Preview"	Future device intended for production at some point. Samples may be available
"Active"	Product status recommended for new designs
"Last time buy (LTB)"	Device will be discontinued and last time buy period and delivery is in effect
"Not recommended for new designs"	Device is still in production to support existing designs and production
"Obsolete"	Production has been discontinued

Datasheet status key:

"Draft version"	This term denotes a very early datasheet version and contains highly provisional information, which may change in any manner without notice.
"Provisional version"	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance. However, changes to the test conditions and specifications may occur, at any time and without notice.
"Issue"	This term denotes an issued datasheet containing finalized specifications. However, changes to specifications may occur, at any time and without notice.

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