GENERAL DESCRIPTION

The XRT86SH328 has a total of 42 independent E1 framers (or 56 independent framers for T1). This Voyager Device maps 21 E1 payloads up to STS-3/ STM-1. The purpose of the 42 framers is to allow back-to-back transmit and receive framers on each of the 21 channel Egress and Ingress data paths. The channel numbering system references the framers according to the block diagram shown in **Figure 1**, where every 4TH Channel is not used in E1 mode.

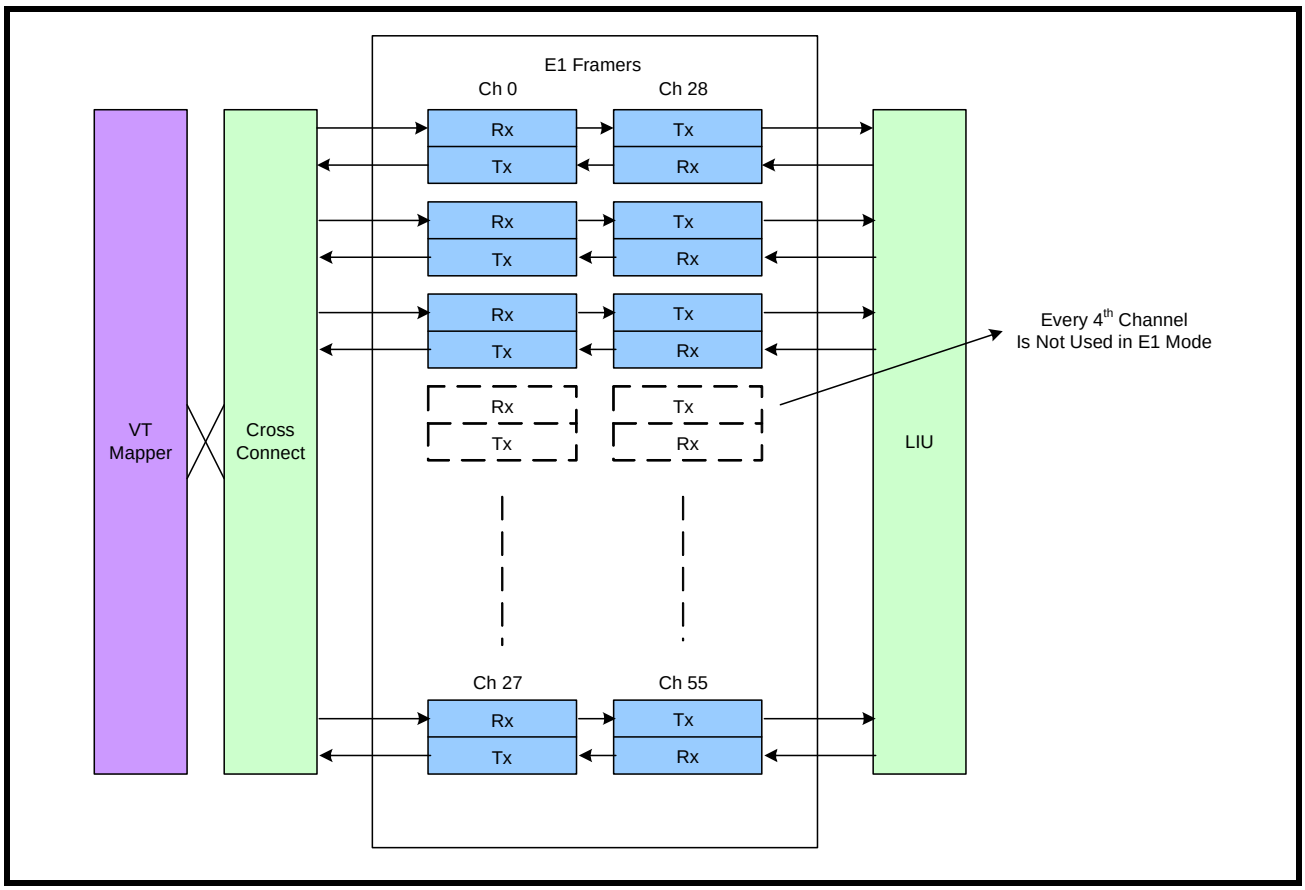
The XRT86SH328 provides E1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers. The slip buffers can be independently enabled or disabled as required and can be configured to frame to the common E1 signal formats.

Each Framer block contains its own Transmit and Receive E1 Framing function. There is 1 Transmit HDLC controller per channel which encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. There is 1 Receive HDLC controller per channel which extracts the payload content of Receive LAPD Message frames from the incoming E1 data stream and write the contents into the Receive HDLC buffers.

The XRT86SH328 fully meets all of the latest E1 specifications: ANSI E1.107-1988, ANSI E1.403-1995, ANSI E1.231-1993, ANSI E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT86SH328 21-CHANNEL E1 FRAMERS (42 TOTAL E1 FRAMERS)



APPLICATIONS

- High-Density E1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- E1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs):
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated E1 interfaces
- Multichannel E1 Test Equipment
- E1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Forty-Two independent, full duplex E1 Tx and Rx Framer/LIUs
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Integrated HDLC controller per channel for transmit and receive, each controller having two 65-byte buffers (buffer 0 / buffer 1)
- HDLC Controllers Support SS7
- Timeslot assignable HDLC
- V5.1 or V5.2 Interface
- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission
- Alarm Indication Signal with Customer Installation signature (AIS-CI)
- Remote Alarm Indication with Customer Installation (RAI-CI)
- Gapped Clock interface mode for Transmit and Receive.
- Intel/Motorola and Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Direct access to D and E channels for fast transmission of data link information
- PRBS, QRSS, and Network Loop Code generation and detection

- Each framer block encodes and decodes the E1 Frame serial data
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 1.8V Inner Core Voltage
- 3.3V I/O operation with 5V tolerant inputs
- 568-pin BGA package with -40°C to +85°C operation

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT86SH328IB	568 Ball BGA	-40°C to +85°C

1.0 MEMORY AND REGISTER MAP

This section provides a complete list of the Voyager E1 register address map as an overview followed by a full description of each register.

1.1 MEMORY MAPPED I/O ADDRESSING

In order to support E1 and/or T1 multiple channel implementation, maintain rich user controlled features, and provide seamless scalability without sacrificing performance for microcontroller access, Voyager E1 operation chooses an addressing scheme to channelize the access for the microcontroller interface. This mapping order and scheme was chosen such that Voyager E1 channel operation is seamless and consistent with its Voyager T1 channel operation, Voyager XRT86SH328 also supports DS1, DS-3, M13 Mux, STS-1/STS-3 SONET Framer/VT Mapper and many other features.

TABLE 1: VOYAGER E1 CHANNEL MAPPING SCHEME

N	E1 CHANNELS
1-3	Channel 1 through Channel 3
4	Reserved
5-7	Channel 4 through Channel 6
8	Reserved
9-11	Channel 7 through Channel 9
12	Reserved
13-15	Channel 10 through Channel 12
16	Reserved
17-19	Channel 13 through Channel 15
20	Reserved
21-23	Channel 16 through Channel 18
24	Reserved
25-27	Channel 19 through Channel 21
28	Reserved

1.2 OVERVIEW OF CONTROL REGISTERS

TABLE 2: MEMORY MAP - E1 FRAMERS

ADDRESS	CONTENTS
0x0001 - 0x004F	SDH Operation Control
0x0202 - 0x027F	Receive TOH Block
0x0281 - 0x02F3	Receive POH Block AU-3 ***NOTE:*** *When 0x02 is replaced with 0x05, the part is processing AU-4. (0x0581 - 0x05F3)*
0x0700 - 0x0753	Transmit TOH Block
0x0781 - 0x07D3	Transmit POH Block AU-3 ***NOTE:*** *When 0x07 is replaced with 0x0A, the part is processing AU-4. (0x0A81 - 0x0AD3)*
0xN000 - 0xN011	E1 Line Interface Unit
0xN100 - 0xNB01	E1 Receive Synchronizer Framer
0xNC03 - 0xNF3F	VT Mapping Operation Control

DESCRIPTION OF THE CONTROL REGISTERS - E1 MODE

TABLE 3: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Control Registers (0xN100 - 0xN1FF)		
Clock and Select Register	CSR	0xN100
Line Interface Control Register	LICR	0xN101
Reserved	-	0xN103 - 0xN106
Framing Select Register	FSR	0xN107
Alarm Generation Register	AGR	0xN108
Synchronization MUX Register	SMR	0xN109
Transmit Signaling and Data Link Select Register	TSDLSR	0xN10A
Framing Control Register	FCR	0xN10B
Receive Signaling & Data Link Select Register	RSDLSR	0xN10C
Receive Signaling Change Register 0	RSCR0	0xN10D
Receive Signaling Change Register 1	RSCR1	0xN10E
Receive Signaling Change Register 2	RSCR2	0xN10F
Receive Signaling Change Register 3	RSCR3	0xN110
Receive National Bits Register	RNBR	0xN111
Receive Extra Bits Register	REBR	0xN112
Data Link Control Register 1	DLCR1	0xN113
Transmit Data Link Byte Count Register 1	TDLBCR1	0xN114
Receive Data Link Byte Count Register 1	RDLBCR1	0xN115
Slip Buffer Control Register	SBCR	0xN116
Reserved	-	0xN117
Interrupt Control Register	ICR	0xN11A
SAI Enable	SAIENR	0xN11C
Reserved	-	0xN11D
Reserved	-	0xN120
BERT Control & Status Register 0	PRBSCSR0	0xN121
Reserved	-	0xN122
BERT Control & Status Register 1	PRBSCSR1	0xN123
For T1 mode only	-	0xN124 - 0xN127
Defect Detection Enable Register	DDER	0xN129
Transmit Sa Select Register	TSASR	0xN130

TABLE 3: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Transmit Sa Auto Control Register 1	TSACR1	0xN131
Transmit Sa Auto Control Register 2	TSACR2	0xN132
Transmit Sa4 Register	TSA4R	0xN133
Transmit Sa5 Register	TSA5R	0xN134
Transmit Sa6 Register	TSA6R	0xN135
Transmit Sa7 Register	TSA7R	0xN136
Transmit Sa8 Register	TSA8R	0xN137
Receive Sa4 Register	RSA4R	0xN13B
Receive Sa5 Register	RSA5R	0xN13C
Receive Sa6 Register	RSA6R	0xN13D
Receive Sa7 Register	RSA7R	0xN13E
Receive Sa8 Register	RSA8R	0xN13F
Reserved - T1 mode only	-	0xN142
BERT Control Register	BCR	0xN163
Time Slot (payload) Control (0xN300 - 0xN3FF)		
Transmit Channel Control Register 0-31	TCCR 0-31	0xN300 - 0xN31F
User Code Register 0-31	TUCR 0-31	0xN320 - 0xN33F
Transmit Signaling Control Register 0 -31	TSCR 0-31	0xN340 - 0xN35F
Receive Channel Control Register 0-31	RCCR 0-31	0xN360 - 0xN37F
Receive User Code Register 0-31	RUCR 0-31	0xN380 - 0xN39F
Receive Signaling Control Register 0-31	RSCR 0-31	0xN3A0 - 0xN3BF
Receive Substitution Signaling Register 0-31	RSSR 0-31	0xN3C0 - 0xN3DF
Receive Signaling Array (0xN500 - 0xN51F)		
Receive Signaling Array Register 0	RSAR0-31	0xN500 - 0xN51F
LAPD Buffer 0		
LAPD Buffer 0 Control Register	LAPDBCR0	0xN600 - 0xN660
LAPD Buffer 1		

TABLE 3: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LAPD Buffer 1 Control Register	LAPDBCR1	0xN700 - 0xN760
Performance Monitor		
Receive Line Code Violation Counter: MSB	RLCVCU	0xN900
Receive Line Code Violation Counter: LSB	RLCVCL	0xN901
Receive Frame Alignment Error Counter: MSB	RFAECU	0xN902
Receive Frame Alignment Error Counter: LSB	RFAECL	0xN903
Receive Severely Errored Frame Counter	RSEFC	0xN904
Receive Synchronization Bit (CRC-6 (T1) CRC-4 (E1) Block) Error Counter: MSB	RSBBECU	0xN905
Receive Synchronization Bit (CRC-6 (T1) CRC-4 (E1) Block) Error Counter: LSB	RSBBECL	0xN906
Receive Far-End Block Error Counter: MSB	RFEBECU	0xN907
Receive Far-End Block Error Counter: LSB	RFEBECL	0xN908
Receive Slip Counter	RSC	0xN909
Receive Loss of Frame Counter	RLFC	0xN90A
Receive Change of Frame Alignment Counter	RCFAC	0xN90B
LAPD Frame Check Sequence Error counter 1	LFCSEC1	0xN90C
PRBS bit Error Counter: MSB	PBECU	0xN90D
PRBS bit Error Counter: LSB	PBECL	0xN90E
Transmit Slip Counter	TSC	0xN90F
Excessive Zero Violation Counter: MSB	EZVCU	0xN910
Excessive Zero Violation Counter: LSB	EZVCL	0xN911
Interrupt Generation/Enable Register Address Map (0xNB00 - 0xNB41)		
Block Interrupt Status Register	BISR	0xNB00
Block Interrupt Enable Register	BIER	0xNB01
Alarm & Error Interrupt Status Register	AEISR	0xNB02
Alarm & Error Interrupt Enable Register	AEIER	0xNB03
Framer Interrupt Status Register	FISR	0xNB04
Framer Interrupt Enable Register	FIER	0xNB05
Data Link Status Register 1	DLSR1	0xNB06
Data Link Interrupt Enable Register 1	DLIER1	0xNB07
Slip Buffer Interrupt Status Register	SBISR	0xNB08
Slip Buffer Interrupt Enable Register	SBIER	0xNB09

TABLE 3: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
Receive Loopback code Interrupt and Status Register	RLCISR	0xNB0A
Receive Loopback code Interrupt Enable Register	RLCIER	0xNB0B
Receive SA (Sa6) Interrupt Status Register	RSAISR	0xNB0C
Receive SA (Sa6) Interrupt Enable Register	RSAIER	0xNB0D
Excessive Zero Status Register	EXZSR	0xNB0E
Excessive Zero Enable Register	EXZER	0xNB0F
SS7 Status Register for LAPD	SS7SR1	0xNB10
SS7 Enable Register for LAPD	SS7ER1	0xNB11
RxLOS/CRC Interrupt Status Register	RLCISR	0xNB12
RxLOS/CRC Interrupt Enable Register	RLCIER	0xNB13
Reserved - T1 mode only	CIAIER	0xNB40 - 0xNB41
LIU Line Interface Unit Global Register Address Map (0x0100 - 0x01FF)		
LIU Global Configuration Register 0	LIU_GLOBAL0	0x0100
LIU Global Configuration Register 1	LIU_GLOBAL1	0x0101
LIU Global Configuration Register 2	LIU_GLOBAL2	0x0102
LIU Global Configuration Register 3	LIU_GLOBAL3	0x0103
LIU Global Configuration Register 4	LIU_GLOBAL4	0x0104
LIU Global Configuration Register 5	LIU_GLOBAL5	0x0105
LIU Global Configuration Register 6	LIU_GLOBAL6	0x0106
Reserved	-	0x0107 - 0x01FF
LIU Line Interface Unit Channel Register Address Map (0xN000 - 0xN011		
LIU Channel Configuration Register 0	LIU_Channel0	0xN000
LIU Channel Configuration Register 1	LIU_Channel1	0xN001
LIU Channel Configuration Register 2	LIU_Channel2	0xN002
LIU Channel Configuration Register 3	LIU_Channel3	0xN003
LIU Channel Configuration Register 4	LIU_Channel4	0xN004
LIU Channel Configuration Register 5	LIU_Channel5	0xN005
LIU Channel Configuration Register 6	LIU_Channel6	0xN006
LIU Channel Configuration Register 7	LIU_Channel7	0xN007
LIU Channel Configuration Register 8	LIU_Channel8	0xN008
LIU Channel Configuration Register 9	LIU_Channel9	0xN009
LIU Channel Configuration Register 10	LIU_Channel10	0xN00A
LIU Channel Configuration Register 11	LIU_Channel11	0xN00B

TABLE 3: REGISTER SUMMARY

FUNCTION	SYMBOL	HEX
LIU Channel Configuration Register 12	LIU_Channel12	0xN00C
LIU Channel Configuration Register 13	LIU_Channel13	0xN00D
LIU Channel Configuration Register 14	LIU_Channel14	0xN00E
LIU Channel Configuration Register 15	LIU_Channel15	0xN00F
LIU Channel Configuration Register 16	LIU_Channel16	0xN010
LIU Channel Configuration Register 17	LIU_Channel17	0xN011

2.0 REGISTER DESCRIPTIONS - E1 MODE

TABLE 4: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0XN100**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LCV Insert	R/W	0	**Line Code Violation Insertion** This bit is used to force a Line Code Violation (LCV) on the transmit output. A “0” to “1” transition on this bit will cause a single LCV to be inserted on the transmit output.
6	Set E1 Mode	R/W	0	**T1/E1 Mode select** This bit is used to program the individual channel to operate in either T1 or E1 mode. 0 = Configures the selected channel to operate in E1 mode. 1 = Configures the selected channel to operate in T1 mode.
5	Sync All Transmit-ters to 8kHz	R/W	0	**Sync All Transmit Framers to 8kHz** This bit permits the user to configure each of the 42 Transmit E1 Framer blocks to synchronize their “transmit output” frame alignment with the 8kHz signal that is derived from the MCLK PLL, as described below. 0 - Disables the “Sync all Transmit Framers to 8kHz” feature for all channels. 1 - Enables the “Sync all Transmit Framers to 8kHz” feature for all channels. ***NOTE:*** *Writing to this bit in register 0x0100 will enable this feature for all channels.* ***NOTE:*** *This bit is only active if the MCLK PLL is used as the “Timing Source” for the Transmit E1 Framer” blocks. CSS[1:0] of this register allows users to select the transmit source of the framer.*
4:2	Reserved	R/W	00	**Reserved**

TABLE 4: CLOCK SELECT REGISTER (CSR) **HEX ADDRESS: 0XN100**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1:0</td><td>CSS[1:0]</td><td>R/W</td><td>01</td><td>Clock Source Select
These bits select the timing source for the Transmit E1 Framer block.

<table>
<tr><th>CSS[1:0]</th><th>TRANSMIT SOURCE FOR THE TRANSMIT E1 FRAMER BLOCK</th></tr>
<tr><td>00/11</td><td>Loop-Timing Mode:The Transmit E1 Framer block will derive its timing from the Received or Recovered Clock signal in 21-Channel Combo Mode only.</td></tr>
<tr><td>01</td><td>Local-Timing Mode: The Transmit E1 Framer block will either use up-stream timing or the TxDS1CLK_n input as its timing source.NOTE: For Aggregation Applications, the user MUST configure all active E1 Framer blocks to operate in this timing mode.</td></tr>
<tr><td>10</td><td>Local-Timing Mode: MCLK PLL Input. This timing option is only available if the user has configured the 21-Channel E1 Framer/LIU Combo Mode.</td></tr>
</table>
</td></tr>
</table>

TABLE 5: LINE INTERFACE CONTROL REGISTER (LICR) **HEX ADDRESS: 0XN101**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>FORCE_LOS</td><td>R/W</td><td>0</td><td>Force Transmit LOS (To the Line Side)
This bit permits the user to configure the transmit direction circuitry (within the channel) to transmit the LOS pattern.
0 - Configures the transmit direction circuitry to transmit “normal” traffic.
1 - Configures the transmit direction circuitry to transmit the LOS Pattern.</td></tr>
<tr><td>6</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
<tr><td>5:4</td><td>LB[1:0]</td><td>R/W</td><td>00</td><td>Framer Loopback Selection
These bits are used to select any of the following loop-back modes for the framer section.
<table>
<tr><th>LB[1:0]</th><th>TYPES OF LOOPBACK SELECTED</th></tr>
<tr><td>00</td><td>Normal Mode (No LoopBack)</td></tr>
<tr><td>01</td><td>Framer Local LoopBack:
When framer local loopback is enabled, the transmit PCM input data is looped back to the receive PCM output data.</td></tr>
<tr><td>10</td><td>Framer Far-End (Remote) Line LoopBack:
When framer remote loopback is enabled, the receive digital data is looped back to the transmit output data.</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3:0</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
</table>

TABLE 6: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	G.706 Annex B CRC-4 Calculation Enable	R/W	0	**G.706 Annex B CRC-4 Calculation Enable** This bit configures the E1 Receive Framer Block to be compliant with ITU-T G.706 Annex B for CRC-to-non-CRC interworking detection. If Annex B is enabled, G.706 Annex B CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400msec while the basic frame alignment signal is present, it is assumed that the remote end is a non CRC-4 equipment. A CRC-to-Non-CRC interworking interrupt will be generated. The CRC-to-Non-CRC interworking interrupt Status can be read from Register Address 0xNB0A. 0 - Configures the Receive E1 Framer block to NOT support the "G.706 Annex B" CRC-4 Multiframe Alignment algorithm. 1 - Configures the Receive E1 Framer block to support the "G.706 Annex B" CRC-4 Multiframe Alignment algorithm.
6	Transmit CRC-4 Error	R/W	0	**Transmit CRC-4 Error** This bit is used to force a continuous errored CRC pattern in the outbound CRC multiframe to be sent on the transmission line. The Transmit E1 Framer Block will implement this error by inverting the value of CRC bit (C1). 0 = Disables the Transmit E1 Framer Block to transmit errored CRC bit. 1 = Forces the Transmit E1 Framer Block to transmit continuous errored CRC bit. ***NOTE:*** *This bit is ignored if CRC multi-Framing is disabled.*

TABLE 6: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>5-4</td><td>CAS MF Align Sel[1:0]</td><td>R/W</td><td>00</td><td>CAS Multiframe Alignment Declaration Algorithm Select[1:0]
These bits allow the user to select which CAS Multiframe Alignment Declaration algorithm the Receive E1 Framer block will employ, according to the table below.

<table>
<tr><th>CAS MF ALIGN SEL[1:0]</th><th>CAS MULTIFRAME ALIGNMENT DECLARATION ALGORITHM SELECTED</th></tr>
<tr><td>00/11</td><td>CAS Multiframe Alignment is Disabled</td></tr>
<tr><td>01</td><td>The “16-Frame” Algorithm
If this alignment algorithm is selected, then the Receive E1 Framer block will monitor the 16th timeslot of each incoming E1 frame and will declare CAS Multiframe alignment (e.g., clear the Loss of CAS Multiframe” defect) condition; anytime that it detects 15 consecutive E1 frames in which bits 1 - 4 (of timeslot 16) do not contain the “CAS Multiframe Alignment” pattern; which is immediately followed by an E1 frame that DOES contain the “CAS Multiframe Alignment” pattern.</td></tr>
<tr><td>10</td><td>The “2-Frame” (ITU-T G.732) Algorithm
If this alignment algorithm is selected, then the Receive E1 Framer block will monitor the 16th timeslot of each incoming E1 frame and will declare CAS Multiframe alignment (e.g., clear the Loss of CAS Multiframe” defect) condition; anytime that it detects a single E1 frame in which bits 1 - 4 (of timeslot 16) do not contain the “CAS Multiframe Alignment” pattern; which is immediately followed by an E1 frame that DOES contain the “CAS Multiframe Alignment” pattern.</td></tr>
</table>

NOTE: For information on the criteria that the Receive E1 Framer block uses in order to declare the “Loss of CAS Multiframe” defect condition, please see register description for the Framing Control Register (FCR - address 0xN10B)</td></tr>
</table>

TABLE 6: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>CRC MF Align Sel[1:0]</td><td>R/W</td><td>00</td><td>CRC Multiframe Alignment Declaration Criteria Select [1:0]
These two bits allow the user to select which CRC-Multiframe Alignment Declaration criteria the Receive E1 Framer block will employ. The Receive E1 Framer block will check for CRC Multiframe Alignment by checking the incoming E1 data-stream and determining whether the international bits (bit 1 of timeslot 0) of non-FAS frames match the CRC multiframe alignment pattern (0,0,1,0,1,1,E1,E2). The table below provides more details on the three different CRC Multiframe Alignment Declaration Criteria.

<table>
<tr><th>CRC MF ALIGN SEL [1:0]</th><th>CRC MULTIFRAME ALIGNMENT DECLARATION CRITERIA SELECTED</th></tr>
<tr><td>00</td><td>CRC Multiframe Alignment is Disabled</td></tr>
<tr><td>01</td><td>CRC Multiframe Alignment is Enabled. Alignment is declared if at least 1 valid CRC multiframe alignment signal (0,0,1,0,1,1,E1,E2) is observed within 8ms.</td></tr>
<tr><td>10</td><td>CRC Multiframe Alignment is Enabled. Alignment is declared if at least 2 valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms.</td></tr>
<tr><td>11</td><td>CRC Multiframe Alignment is Enabled. Alignment is declared if at least 3 valid CRC multiframe alignment signals (0,0,1,0,1,1,E1,E2) are observed within 8ms.</td></tr>
</table>

NOTE: For information on the criteria that the Receive E1 Framer block uses to declare the “Loss of CRC Multiframe Alignment” defect condition, please see register description for the Framing Control Register (FCR - 0xN10B)</td></tr>
<tr><td>1</td><td>Additional Frame Check Enable - FAS</td><td>R/W</td><td>0</td><td>Additional Frame Check Enable - FAS Frame Alignment Declaration
This bit permits the user to configure the Receive E1 Framer block to perform some “additional FAS frame synchronization checking” prior to declaring “FAS Frame Alignment”. If the user implements this feature, then the Receive E1 Framer block will perform some more testing on two additional E1 frames, prior to declaring the “FAS Frame Alignment” condition.
0 - Disables this additional FAS frame checking.
1 - Enables this additional FAS frame checking.</td></tr>
</table>

TABLE 6: FRAMING SELECT REGISTER (FSR) **HEX ADDRESS: 0XN107**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	FAS Frame Align Sel	R/W	0	**FAS Alignment Declaration Algorithm Select** This bit specifies which algorithm the Receive E1 Framer block uses in its search for the FAS Alignment. 0 = Selects the FAS Alignment Algorithm 1 1 = Selects the FAS Alignment Algorithm 2 **FAS Alignment Algorithm 1** If the Receive E1 Framer block has been configured to use “FAS Alignment Algorithm # 1", then it will acquire FAS alignment by performing the following three steps: **Step 1** - The Receive E1 Framer block begins by searching for the correct 7-bit FAS pattern. Go to Step 2 if found. **Step 2** - Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 of the Non-FAS frame is a one. Go back to Step 1 if failed, otherwise, go to step 3. **Step 3** - Check if the FAS is present in the assumed timeslot 0 of the third frame. Go back to Step 1 if failed. After the first three steps (if they all passed), the Receive E1 Framer Block will declare FAS in SYNC if Frame Check Sequence (Bit 1 of this register) is disabled. If Frame Check Sequence (Bit 1 of this register) is enabled, then the Receive E1 Framer Block will need to verify the correct frame alignment for an additional two frames. **FAS Alignment Algorithm 2** If the Receive E1 Framer block has been configured to support “FAS Alignment Algorithm # 2, then it will perform the following 3 steps in order to acquire and declare FAS Frame Alignment with the incoming E1 data-stream. Algorithm 2 is similar to Algorithm 1 but adds a one-frame hold off time after the second step fails. After the second step fails, it waits for the next assumed FAS in the next frame before it begins the new search for the correct FAS pattern. **Step 1** - Algorithm 1 begins by searching for the correct 7-bit FAS pattern. Go to Step 2 if found. **Step 2** - Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timeslot 0 of the Non-FAS frame is a one. Go back to Step 4 if failed, otherwise, go to step 3. **Step 3** - Check if the FAS is present in the assumed timeslot 0 of the third frame. Go back to Step 1 if failed, otherwise, proceed to check for Frame Check Sequence. **Step 4** - Wait for assumed FAS in the next frame, then go back to Step 1 After the first three steps (if they all passed), the Receive E1 Framer Block will declare FAS in SYNC if Frame Check Sequence (Bit 1 of this register) is disabled. If Frame Check Sequence (Bit 1 of this register) is enabled, then the Receive E1 Framer Block will need to verify the correct frame alignment for an additional two frames.

TABLE 7: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>Transmit AUXP Pattern</td><td>R/W</td><td>0</td><td>Transmit Auxiliary (AUXP) Pattern
This bit permits the user to command the Transmit E1 Framer block to transmit the AUXP Pattern to the remote terminal equipment, as depicted below.
0 - Configures the Transmit E1 Framer block to NOT transmit the AUXP Pattern (which is an unframed, repeating 1010... pattern).
1 - Configures the Transmit E1 Framer block to transmit the AUXP Pattern.
The device also supports AUXP pattern detection, please read register (address 0xNB0A) for more detail.</td></tr>
<tr><td>6</td><td>Loss of Frame Declaration Criteria</td><td>R/W</td><td>0</td><td>Loss of Frame Declaration Criteria
This bit permits the user to select the “Loss of Frame Declaration Criteria” for the Receive E1 Framer block, as depicted below.
0 = Loss of Frame is declared immediately if either CRC Multiframe Alignment or FAS Alignment is lost.
1 = Loss of Frame is declared immediately if FAS Alignment is lost. If CRC Multiframe Alignment is lost for more than 8ms, E1 receive framer will force a frame search.</td></tr>
<tr><td>5-4</td><td>Transmit YEL And Multi-YEL[1:0]</td><td>R/W</td><td>00</td><td>Yellow Alarm and Multiframe Yellow Alarm Generation [1:0]
These bits activate or deactivate the transmission of yellow and multiframe yellow alarm. The Yellow alarm and multiframe Yellow alarm can be forced to transmit as’1’, or be inserted upon detection of loss of alignment. The decoding of these bits are explained as follows:
<table><tr><th>YEL[1:0]</th><th>YELLOW ALARM TRANSMITTED</th></tr><tr><td>00/10</td><td>Yellow Alarm and Multiframe Yellow Alarm transmission is disabled.</td></tr><tr><td>01</td><td>Automatic Transmission of Yellow and CAS Multiframe Yellow Alarms are enabled, as described below:
1. Whenever the Receive E1 Framer block declares the LOF (Loss of FAS Framing) defect condition:
The corresponding Transmit E1 Framer block will automatically transmit the Yellow Alarm indicator (by setting Bit 3 of Time-Slot 0, within the non-FAS frames) to 1" whenever (and for the duration that) the Receive E1 Framer block declares the LOF defect condition.
2. Whenever the Receive E1 Framer block declares the “Loss of CAS Multiframe Alignment” defect condition:
The corresponding Transmit E1 Framer block will automatically transmit the CAS Multiframe Yellow Alarm indicator (by setting Bit 6 within “Frame 0" of Time-slot 16) to “1” whenever (and for the duration that) the Receive E1 Framer block declares the Loss of CAS Multiframe Defect condition.</td></tr><tr><td>11</td><td>Force Transmission of Yellow and Multiframe Yellow Alarm
Both Yellow and Multiframe Yellow Alarm are transmitted as ‘1’ when this is enabled.</td></tr></table></td></tr>
</table>

TABLE 7: ALARM GENERATION REGISTER (AGR) **HEX ADDRESS: 0XN108**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>3-2</td><td>Transmit AIS Pattern Select[1:0]</td><td>R/W</td><td>00</td><td>Types of AIS Pattern Generation Select
These bits permit the user to do the following.
a. To select the type of AIS Pattern that the Transmit E1 Framer block will transmit.
b. To force (via Software-control) the transmission of the “selected” AIS Pattern.

<table>
<tr><th>AISG[1:0]</th><th>TYPES OF AIS PATTERN TRANSMITTED</th></tr>
<tr><td>00</td><td>Transmission of AIS Indicator is Disabled
The Transmit E1 Framer block will transmit “normal” E1 traffic to the remote terminal equipment.</td></tr>
<tr><td>01</td><td>Unframed AIS alarm
Transmit E1 Framer block will transmit an Unframed All Ones Pattern, as an AIS Pattern.</td></tr>
<tr><td>10</td><td>The AIS-16 Pattern
In this case, Time-slot 16 (within each outbound E1 frame) will be set to an “All Ones” Pattern.</td></tr>
<tr><td>11</td><td>Framed AIS alarm
Transmit E1 Framer block will transmit a Framed All Ones Pattern, as an AIS Pattern.</td></tr>
</table>

NOTE: For “normal” operation, the user should set these bits to “[0, 0]”.</td></tr>
<tr><td>1-0</td><td>AIS Defect Declaration Criteria[1:0]</td><td>R/W</td><td>00</td><td>AIS Defect Declaration Criteria[1:0]:
These bits permit the user to specify the types of AIS Patterns that the Receive E1 Framer block must detect before it will declare the AIS defect condition.

<table>
<tr><th>AISD[1:0]</th><th>AIS Defect Declaration Criteria</th></tr>
<tr><td>00</td><td>AIS Defect Condition will NOT be declared.</td></tr>
<tr><td>01</td><td>Receive E1 Framer block will detect both Unframed and Framed AIS pattern</td></tr>
<tr><td>10</td><td>Receive E1 Framer block will detect AIS16 (Time Slot 16 AIS) pattern*.</td></tr>
<tr><td>11</td><td>Receive E1 Framer block will detect only Framed AIS pattern</td></tr>
</table>
</td></tr>
</table>

TABLE 8: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-6</td><td>E Bit Source Sel[1:0]</td><td>R/W</td><td>00</td><td>Source for E bits [1:0]
These bits permit the user to specify the source of the E-bits, within each outbound E1 frame, as depicted below.

<table>
<tr><th>ESRC[1:0]</th><th>SOURCE FOR E-BITS</th></tr>
<tr><td>00</td><td>The corresponding Receive E1 Framer block:
In this case, the E-bits will be used to indicate whether the Receive E1 Framer block has detected a CRC error within the most recently received Sub-Multiframe.
The Receive E1 Framer will indicate a received errored sub-multiframe by setting the binary state of E bit from ‘1’ to ‘0’ for each errored sub-multi-frame.</td></tr>
<tr><td>01</td><td>All E bits (within the outbound E1 data-stream) are set to “0”.</td></tr>
<tr><td>10</td><td>All E bits (within the outbound E1 data-stream) are set to “1”.</td></tr>
<tr><td>11</td><td>The outgoing E bits will be used to carry data link information.</td></tr>
</table>

NOTE: This bit is only active if the Transmit E1 Framer block has been configured to internally generate and insert the various Framing Alignment bits within the outbound E1 data-stream. In other words, whenever the “Framing Alignment Pattern Source Select” bit (within Bit 0 of this Register) is set to “0”.</td></tr>
<tr><td>5:4</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>3-2</td><td>Data Link Source Select [1:0]</td><td>R/W</td><td>00</td><td>Data Link Source Select
These bits are used to specify the source of the Data Link bits that will be inserted in the outbound E1 frames. The table below describes the three different sources from which the Data Link bits can be inserted.

<table>
<tr><th>DLSRC[1:0]</th><th>SOURCE OF DATA LINK BITS</th></tr>
<tr><td>00/11</td><td>Data Input - The transmit serial input from the transmit payload data input block will be the source for data link bits</td></tr>
<tr><td>01</td><td>Transmit HDLC Controller - The Transmit HDLC Controller will generate either BOS (Bit Oriented Signaling) or MOS (Message Oriented Signaling) messages which will be inserted into the Data Link bits in the outbound E1frames.</td></tr>
<tr><td>10</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

TABLE 8: SYNCHRONIZATION MUX REGISTER (SMR) **HEX ADDRESS: 0XN109**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	CRC-4 Bits Source Sel	R/W	0	**CRC-4 Bits Source Select** This bit permits the user to specify the source of the CRC-4 bits, within the outbound E1 data-stream, as depicted below. 0 - Configures the Transmit E1 Framer block to internally compute and insert the CRC-4 bits within the outbound E1 data-stream. 1 - Configures the Transmit E1 Framer block to externally accept data from the data input, and to insert this data into the CRC-4 bits within the outbound E1 data-stream. ***NOTE:*** *This bit is ignored if CRC Multiframe Alignment is disabled*
0	Framing Alignment Pattern Source Select	R/W	0	**Framing Alignment Pattern Source Select** This bit permits the user to specify the source of the various "Framing Alignment" bits (which includes the FAS bits, the CRC Multiframe Alignment bits, the E and A bits). 0 - Configures the Transmit E1 Framer block to internally generate and insert these various framing alignment bits into the outbound E1 data-stream. 1 - Configures the Transmit E1 Framer block to externally accept data from the data input, and to insert this data into the FAS, CRC Multiframe, E and A bits within the outbound E1 data-stream. ***NOTE:*** *Users can specify the source for E-bits in register bits 6-7 within this register if Transmit E1 Framer is configured to internally generate the various framing alignment bits (i.e. this bit set to'0').*

TABLE 9: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8ENB	R/W	0	**Transmit Sa8 Enable** This bit specifies if the Sa8 bits (bit 7 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa8 will NOT be used to transport Data Link Information. Sa8 bits will be set to "1" within the outbound E1 data-stream if the Sa8 bits are inserted from the transmit serial input. 1 = Sa8 WILL be used to transport Data Link Information. ***NOTE:*** *Sa8 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xN130) setting.*
6	TxSa7ENB	R/W	0	**Transmit Sa7 Enable** This bit specifies if the Sa7 bits (bit 6 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa7 will NOT be used to transport Data Link Information. Sa7 bits will be set to "1" within the outbound E1 data-stream if the Sa7 bits are inserted from the transmit serial input. 1 = Sa7 WILL be used to transport Data Link Information. ***NOTE:*** *Sa7 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xN130) setting.*

TABLE 9: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	TxSa6ENB	R/W	0	**Transmit Sa6 Enable** This bit specifies if the Sa6 bits (bit 5 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa6 will NOT be used to transport Data Link Information. Sa6 bits will be set to "1" within the outbound E1 data-stream if the Sa6 bits are inserted from the transmit serial input. 1 = Sa6 WILL be used to transport Data Link Information. ***NOTE:*** *Sa6 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xN130) setting.*
4	TxSa5ENB	R/W	0	**Transmit Sa5 Enable** This bit specifies if the Sa5 bits (bit 4 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa5 will NOT be used to transport Data Link Information. Sa5 bits will be set to "1" within the outbound E1 data-stream if the Sa5 bits are inserted from the transmit serial input. 1 = Sa5 WILL be used to transport Data Link Information. *Sa5 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xN130) setting.*
3	TxSa4ENB	R/W	0	**Transmit Sa4 Enable** This bit specifies if the Sa4 bits (bit 3 within timeslot 0 of non-FAS frames) will be involved in the transmission of Data Link Information. 0 = Sa4 will NOT be used to transport Data Link Information. Sa4 bits will be set to "1" within the outbound E1 data-stream if the Sa4 bits are inserted from the transmit serial input. 1 = Sa4 WILL be used to transport Data Link Information. *Sa4 bits can be inserted from either the transmit serial input or register depending on the Transmit SA Select Register (Register Address: 0xN130) setting.*

TABLE 9: TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) **HEX ADDRESS:0XN10A**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>2-0</td><td>TxSIGDL[2:0]</td><td>R/W</td><td>000</td><td>Transmit Signaling and Data Link Select[2:0]:
These bits are used to specify the source for D/E channel, National Bits in timeslot 0 of the non-FAS frames, and Timeslot 16 of the outbound E1 frames. The table below presents the settings of these three bits in detail.
<table>
<tr><th>TXSIGDL [2:0]</th><th>SOURCE OF D/E CHANNEL</th><th>SOURCE OF NATIONAL BITS</th><th>SOURCE OF TIMESLOT 16</th></tr>
<tr><td>000</td><td>Data Input</td><td>Data link</td><td>Data Input</td></tr>
<tr><td>001</td><td>Data Input</td><td>Data link</td><td>CAS signaling is enabled. Time Slot 16 can be inserted from any of the following:
• Data Input
• TSCR Register (0xN340-0xN35F)</td></tr>
<tr><td>010</td><td>Data Input</td><td>Forced to All Ones</td><td>Data Input on time slot 16 only</td></tr>
<tr><td>011</td><td>Data Input</td><td>Forced to All Ones</td><td>CAS signaling is enabled. Time Slot 16 can be inserted from any of the following:
• Data Input
• TSCR Register (0xN340-0xN35F)</td></tr>
<tr><td>100</td><td>Data Input</td><td>Data link</td><td>Data Input</td></tr>
<tr><td>101/ 110/ 111</td><td>Not Used</td><td>Not Used</td><td>Not Used</td></tr>
</table>
</td></tr>
</table>

TABLE 10: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0XN10B**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7</td><td>Reframe</td><td>R/W</td><td>0</td><td>Force Reframe
A ‘0’ to ‘1’ transition will force the Receive E1 Framer to restart the synchronization process. This bit field is automatically cleared (set to 0) after frame synchronization is reached.</td></tr>
<tr><td>6-5</td><td>Loss of CAS MF Align_Sel [1:0]</td><td>R/W</td><td>10</td><td>Loss of CAS Multiframe Alignment Defect Declaration Criteria Select [1:0]
These two bits permit the user to select the “Loss of CAS Multiframe Alignment” defect declaration criteria. Loss of CAS Multiframe Alignment defect is declared based on the number of consecutive CAS multiframes with Multiframe Alignment signal received in error as indicated in the table below.
<table>
<tr><th>CASC[1:0]</th><th>LOSS OF CAS MULTIFRAME ALIGNMENT DECLARATION CRITERIA</th></tr>
<tr><td>00</td><td>2 consecutive CAS Multiframes</td></tr>
<tr><td>01</td><td>3 consecutive CAS Multiframes</td></tr>
<tr><td>10</td><td>4 consecutive CAS Multiframes</td></tr>
<tr><td>11</td><td>8 consecutive CAS Multiframes</td></tr>
</table>
NOTE: These bits are active only if CAS Multiframe Alignment is enabled.</td></tr>
<tr><td>4-3</td><td>Loss of CRC Multiframe Align_Sel[1:0]</td><td>R/W</td><td>00</td><td>Loss of CRC-4 Multiframe Alignment Defect Declaration Criteria Select [1:0]
These two bits permit the user to select the “Loss of CRC-4 Multiframe Alignment” defect declaration criteria for the Channel. The following table presents the different CRC-4 Multiframe Algorithms in terms of the number of consecutive erred CRC-4 multiframe alignments that the E1 Receiver Framer will receive before it declares the “Loss of CRC-4 Multiframe Alignment” defect condition.
<table>
<tr><th>CASC[1:0]</th><th>LOSS OF CRC-4 MULTIFRAME ALIGNMENT DECLARATION CRITERIA</th></tr>
<tr><td>00</td><td>4 consecutive CRC-4 Multiframes Alignment</td></tr>
<tr><td>01</td><td>2 consecutive CRC-4 Multiframes Alignment</td></tr>
<tr><td>10</td><td>8 consecutive CRC-4 Multiframes Alignment</td></tr>
<tr><td>11</td><td>If TBR-4 Standard is Enabled*:
4 consecutive CRC-4 Multiframe Alignment or 915 or more CRC-4 errors
If TBR-4 Standard is Disabled*:
915 or more CRC-4 errors</td></tr>
</table>
NOTE: These bits are only active if CRC Multiframe Alignment is enabled. If CRC multiframe alignment is not found in 8ms, the E1 receive framer will restart the synchronization process.
NOTE: TBR-4 standard is enabled by writing to 0xN112, bit 6.</td></tr>
</table>

TABLE 10: FRAMING CONTROL REGISTER (FCR) **HEX ADDRESS: 0XN10B**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>2-0</td><td>LOF_Declare_Sel [2:0]</td><td>R/W</td><td>011</td><td>Loss of FAS Alignment Defect Declaration Criteria Select [2:0]
These bits permit the user to specify the Loss of FAS Alignment defect declaration criteria. The following table presents the different FAS Alignment Algorithms in terms of the number of consecutive erred FAS patterns within a multiframe that the E1 Receiver Framer will receive before it declares the “Loss of FAS Alignment” defect conditions

<table>
<tr><th>FASC[2:0]</th><th>LOSS OF FAS ALIGNMENT DECLARATION CRITERIA</th></tr>
<tr><td>000</td><td>Setting these bits to ‘b000’ is illegal. Do not use this configuration.</td></tr>
<tr><td>001</td><td>1 FAS Alignment pattern</td></tr>
<tr><td>010</td><td>2 consecutive FAS Alignment patterns</td></tr>
<tr><td>011</td><td>3 consecutive FAS Alignment patterns</td></tr>
<tr><td>100</td><td>4 consecutive FAS Alignment patterns</td></tr>
<tr><td>101</td><td>5 consecutive FAS Alignment patterns</td></tr>
<tr><td>110</td><td>6 consecutive FAS Alignment patterns</td></tr>
<tr><td>111</td><td>7 consecutive FAS Alignment patterns</td></tr>
</table>

NOTE: Loss of FAS alignment will force the E1 receive framer to declare the loss of CAS multiframe alignment and loss of CRC multiframe alignment.</td></tr>
</table>

TABLE 11: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0XN10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RxSa8ENB	R/W	0	**Receive Sa8 Enable** This bit is used to specify whether or not Sa 8 (bit 7 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa8 is not used to receive data link information 1 = Sa8 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
6	RxSa7ENB	R/W	0	**Receive Sa7 Enable** This bit is used to specify whether or not Sa 7 (bit 6 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa7 is not used to receive data link information 1 = Sa7 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
5	RxSa6ENB	R/W	0	**Receive Sa6 Enable** This bit is used to specify whether or not Sa 6 (bit 5 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa6 is not used to receive data link information 1 = Sa6 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
4	RxSa5ENB	R/W	0	**Receive Sa5 Enable** This bit is used to specify whether or not Sa 5 (bit 4 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa5 is not used to receive data link information 1 = Sa5 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*
3	RxSa4ENB	R/W	0	**Receive Sa4 Enable** This bit is used to specify whether or not Sa 4 (bit 3 within timeslot 0 of non-FAS frames) will be used to receive data link information 0 = Sa4 is not used to receive data link information 1 = Sa4 is used to receive data link information ***NOTE:*** *This bit is valid only if the RxSIGDL[2:0] = "000", "001", or "100". (The National bits have been configured to receive data link bits).*

TABLE 11: RECEIVE SIGNALING & DATA LINK SELECT REGISTER (RSDLSR) **HEX ADDRESS: 0XN10C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2-0	RxSIGDL[2:0]	R/W	000	**Receive Signaling and Datalink Select[2:0]:** These bits specify the destination for the data that is to be extracted via D/E channel, National Bits in timeslot 0 of the non-FAS frames, and Timeslot 16 in the outbound frames. The table below presents the settings of these three RxSIGDL bits in detail.

RXSIGDL [2:0]	D/E CHANNEL	NATIONAL BITS	TIME SLOT 16
000	Data Output	Data Link	Data Output
001	Data Output	Data Link	CAS signaling is enabled. Time Slot 16 can be extracted to any of the following: • Data Output • RSAR Register (0xN500-0xN51F)
010	Data Output	Data Link forced to All Ones	Time Slot 16 can be extracted to any of the following: • Data Output • RSAR Register (0xN500-0xN51F)
011	Data Output	Data Link forced to All Ones	CAS signaling is enabled. Time Slot 16 can be extracted to any of the following: • Data Output • RSAR Register (0xN500-0xN51F)
100	Data Output	Data Link	Data Output
101/110/ 111	Not Used	Not Used	Not Used

TABLE 12: RECEIVE SIGNALING CHANGE REGISTER 0 (RSCR 0) **HEX ADDRESS: 0XN10D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch. 0	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 0 through 7 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 0 through 7) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 0 through 7) HAS changed since the last read of this register. ***NOTES:*** *1. Bit 7 (Time-Slot 0) is NOT active, since it carries the FAS and National Bits.* ***NOTE:*** *2. This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch. 1	RUR	0	
5	Ch.2	RUR	0	
4	Ch.3	RUR	0	
3	Ch.4	RUR	0	
2	Ch.5	RUR	0	
1	Ch.6	RUR	0	
0	Ch.7	RUR	0	

TABLE 13: RECEIVE SIGNALING CHANGE REGISTER 1 (RSCR 1) **HEX ADDRESS: 0XN10E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.8	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 8 through 15 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 8 through 15) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 8 through 15) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.9	RUR	0	
5	Ch.10	RUR	0	
4	Ch.11	RUR	0	
3	Ch.12	RUR	0	
2	Ch.13	RUR	0	
1	Ch.14	RUR	0	
0	Ch.15	RUR	0	

TABLE 14: RECEIVE SIGNALING CHANGE REGISTER 2 (RSCR 2) **HEX ADDRESS: 0XN10F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.16	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 16 through 23 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 16 through 23) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 16 through 23) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.17	RUR	0	
5	Ch.18	RUR	0	
4	Ch.19	RUR	0	
3	Ch.20	RUR	0	
2	Ch.21	RUR	0	
1	Ch.22	RUR	0	
0	Ch.23	RUR	0	

TABLE 15: RECEIVE SIGNALING CHANGE REGISTER 3 (RSCR 3) **HEX ADDRESS: 0xN110**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Ch.24	RUR	0	These bits indicate whether the Channel Associated signaling data, associated with Time-Slots 24 through 31 within the incoming E1 data-stream, has changed since the last read of this register, as depicted below. 0 - CAS data (for Time-slots 24 through 31) has NOT changed since the last read of this register. 1 - CAS data (for Time-slots 24 through 31) HAS changed since the last read of this register. ***NOTE:*** *This register is only active if the incoming E1 data-stream is using Channel Associated Signaling.*
6	Ch.25	RUR	0	
5	Ch.26	RUR	0	
4	Ch.27	RUR	0	
3	Ch.28	RUR	0	
2	Ch.29	RUR	0	
1	Ch.30	RUR	0	
0	Ch.31	RUR	0	

TABLE 16: RECEIVE NATIONAL BITS REGISTER (RNBR) **HEX ADDRESS: 0XN111**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Si_FAS	RO	x	**Received International Bit - FAS Frame** This Read Only bit contains the value of the International Bit (e.g., the Si bit) in the most recently received FAS frame.
6	Si_nonFAS	RO	x	**Received International Bit - Non FAS Frame** This Read Only bit contains the value of the International Bit (e.g., the Si bit) in the most recently received non-FAS frame
5	R_ALARM	RO	x	**Received A bit - Non FAS Frame** This Read Only bit contains the value in the Remote Alarm Indication bit (A bit, or bit 3 of non-FAS frame) within the most recently received non-FAS frame.
4	Sa4	RO	x	**Received National Bits** These Read Only bits contain the values of the National bits (Sa4-Sa8) within the most recently received non-FAS frame.
3	Sa5	RO	x	
2	Sa6	RO	x	
1	Sa7	RO	x	
0	Sa8	RO	x	

TABLE 17: RECEIVE EXTRA BITS REGISTER (REBR) **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	In-Frame	RO	0	**In Frame State:** This READ-ONLY bit indicates whether the Receive E1 Framer block is currently declaring the "In-Frame" condition with the incoming E1 data-stream. 0 - Indicates that the Receive E1 Framer block is currently declaring the LOF (Loss of Frame) Defect condition. 1 - Indicates that the Receive E1 Framer block is currently declaring itself to be in the "In-Frame" condition.
6	TBR4_Std	R/W	0	**TBR4 Standard** Setting this bit will force the XRT86SH328 to be compliant with the TBR-4 standard for "Loss of CRC-4 Multiframe Alignment Criteria". 0 - Backward compatible with older framing for Loss of CRC-4 Multiframe Criteria. When CRCC[1:0] (from register 0xN10B) is set to'11', Loss of CRC-4 Multiframe Alignment will declare if 915 or more CRC-4 errors have been detected in 1 second. 1 - "TBR-4 Compliant" Loss of CRC-4 Multiframe Alignment Criteria - When CRCC[1:0] (from register 0xN10B) is set to'11', Loss of CRC-4 Multiframe Alignment will declare if 4 consecutive CRC-4 Multiframe Alignment have been received in error OR if 915 or more CRC-4 errors have been detected in 1 second.
5-4	Reserved	-	-	**Reserved**
3	EX1	RO	x	**Extra Bit 1** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 5 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*
2	ALARMFE	RO	x	**CAS Multi-Frame Yellow Alarm** This READ ONLY bit field indicates the value of the most recently received CAS Multiframe Yellow Alarm Bit (bit 6 within timeslot 16 of frame 0 of the signaling multiframe). 0 = Indicates that the E1 receive framer block is NOT receiving the CAS Multiframe Yellow Alarm. 1 = Indicates that the E1 receive framer block is currently receiving the CAS Multiframe Yellow Alarm. ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*

TABLE 17: RECEIVE EXTRA BITS REGISTER (REBR) **HEX ADDRESS: 0XN112**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	EX2	RO	x	**Extra Bit 2** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 7 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*
0	EX3	RO	x	**Extra Bit 3** This READ ONLY bit field indicates the value of the most recently received Extra Bit value (bit 8 within timeslot 16 of frame 0 of the signaling multiframe). ***NOTE:*** *This bit only has meaning if the framer is using Channel Associated Signaling.*

TABLE 18: DATA LINK CONTROL REGISTER (DLCR) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	Reserved. Please set this bit to'0' for normal operation.
6	MOS ABORT Disable	R/W	0	**MOS ABORT Disable:** This bit permits the user to either enable or disable the "Automatic MOS ABORT" feature within Transmit HDLC Controller. If the user enables this feature, then Transmit HDLC Controller block will automatically transmit the ABORT Sequence (e.g., a zero followed by a string of 7 consecutive "1s") whenever it abruptly transitions from transmitting a MOS type of message, to transmitting a BOS type of message. If the user disables this feature, then the Transmit HDLC Controller Block will NOT transmit the ABORT sequence, whenever it abruptly transitions from transmitting a MOS-type of message to transmitting a BOS-type of message. 0 - Enables the "Automatic MOS Abort" feature 1 - Disables the "Automatic MOS Abort" feature
5	Rx_FCS_DIS	R/W	0	**Receive Frame Check Sequence (FCS) Verification Enable/Disable** This bit permits the user to configure the Receive HDLC Controller Block to compute and verify the FCS value within each incoming LAPD message frame. 0 - Enables FCS Verification 1 - Disables FCS Verification
4	AutoRx	R/W	0	**Auto Receive LAPD Message** This bit configures the Receive HDLC Controller Block to discard any incoming BOS or LAPD Message frame that exactly match which is currently stored in the Receive HDLC1 buffer. 0 = Disables this "AUTO DISCARD" feature 1 = Enables this "AUTO DISCARD" feature.
3	Tx_ABORT	R/W	0	**Transmit ABORT** This bit configures the Transmit HDLC Controller Block to transmit an ABORT sequence (string of 7 or more consecutive 1's) to the Remote terminal. 0 - Configures the Transmit HDLC Controller Block to function normally (e.g., not transmit the ABORT sequence). 1 - Configures the Transmit HDLC Controller block to transmit the ABORT Sequence.

TABLE 18: DATA LINK CONTROL REGISTER (DLCR) **HEX ADDRESS: 0XN113**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	Tx_IDLE	R/W	0	**Transmit Idle (Flag Sequence Byte)** This bit configures the Transmit HDLC Controller Block to unconditionally transmit a repeating string of Flag Sequence octets (0X7E) in the data link channel to the Remote terminal. In normal conditions, the Transmit HDLC Controller block will repeatedly transmit the Flag Sequence octet whenever there is no MOS message to transmit to the remote terminal equipment. However, if the user invokes this "Transmit Idle Sequence" feature, then the Transmit HDLC Controller block will UNCONDITIONALLY transmit a repeating stream of the Flag Sequence octet (thereby overwriting all outbound MOS data-link messages). 0 - Configures the Transmit HDLC Controller Block to transmit data-link information in a "normal" manner. 1 - Configures the Transmit HDLC Controller block to transmit a repeating string of Flag Sequence Octets (0x7E). ***NOTE:*** *This bit is ignored if the* Transmit *HDLC controller is operating in the BOS Mode - bit 0 (MOS/BOS) within this register is set to 0.*
1	Tx_FCS_EN	R/W	0	**Transmit LAPD Message with Frame Check Sequence (FCS)** This bit permits the user to configure the Transmit HDLC Controller block to compute and append FCS octets to the "back-end" of each outbound MOS data-link message. 0 - Configures the Transmit HDLC Controller block to NOT compute and append the FCS octets to the back-end of each outbound MOS data-link message. 1 - Configures the Transmit HDLC Controller block TO COMPUTE and append the FCS octets to the back-end of each outbound MOS data-link message. ***NOTE:*** *This bit is ignored if the transmit HDLC controller has been configured to operate in the BOS mode - bit 0 (MOS/BOS) within this register is set to 0.*
0	MOS/$\overline{\text{BOS}}$	R/W	0	**Message Oriented Signaling/Bit Oriented Signaling Send** This bit permits the user to send LAPD transmission through HDLC Controller Block using either BOS (Bit-Oriented Signaling) or MOS (Message-Oriented Signaling) frames. 0 - Transmit HDLC Controller block BOS message Send. 1 - Transmit HDLC Controller block MOS message Send. ***NOTE:*** *This is not an Enable bit. This bit must be set to '0' each time a BOS is to be sent or '1' each time a MOS is to be sent.*

TABLE 19: TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) **HEX ADDRESS: 0XN114**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxHDLC BUFAvail/ BUFSel	R/W	0	**Transmit HDLC Buffer Available/Buffer Select** This bit has different functions, depending upon whether the user is writing to or reading from this register, as depicted below. **If the user is writing data into this register bit:** 0 - Configures the Transmit HDLC Controller to read out and transmit the data, residing within “Transmit HDLC Buffer # 0", via the Data Link channel to the remote terminal equipment. 1 - Configures the Transmit HDLC Controller to read out and transmit the data, residing within the “Transmit HDLC Buffer #1”, via the Data Link channel to the remote terminal equipment. **If the user is reading data from this register bit:** 0 - Indicates that “Transmit HDLC Buffer # 0" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC Message Buffer, he/she should proceed to write this message into “Transmit HDLC Buffer # 0" - Address location: 0xN600. 1 - Indicates that “Transmit HDLC Buffer # 1" is the next available buffer. In this case, if the user wishes to write in the contents of a new “outbound” Data Link Message into the Transmit HDLC Message Buffer, he/she should proceed to write this message into “Transmit HDLC Buffer # 1" - Address location: 0xN700. ***NOTE:*** *If one of these Transmit HDLC buffers contain a message which has yet to be completely read-in and processed for transmission by the Transmit HDLC controller, then this bit will automatically reflect the value corresponding to the next available buffer when it is read. Changing this bit to the in-use buffer is not permitted.*
6-0	TDLBC[6:0]	R/W	0000000	**Transmit HDLC Message - Byte Count** The exact function of these bits depends on whether the Transmit HDLC Controller is configured to transmit MOS or BOS messages to the Remote Terminal Equipment. **In BOS MODE:** These bit fields contain the number of repetitions the BOS message must be transmitted before the Transmit HDLC controller generates the Transmit End of Transfer (TxEOT) interrupt and halts transmission. If these fields are set to 00000000, then the BOS message will be transmitted for an indefinite number of times. **In MOS MODE:** These bit fields contain the length, in number of octets, of the message to be transmitted. The length of MOS message specified in these bits include header bytes such as the SAPI, TEI, Control field, however, it does not include the FCS bytes.

TABLE 20: RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) **HEX ADDRESS: 0XN115**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RBUFPTR	R/W	0	**Receive HDLC Buffer-Pointer** This bit Identifies which Receive HDLC buffer contains the most recently received HDLC message. 0 - Indicates that Receive HDLC Buffer # 0 contains the contents of the most recently received HDLC message. 1 - Indicates that Receive HDLC Buffer # 1 contains the contents of the most recently received HDLC message.
6-0	RDLBC[6:0]	R/W	0000000	**Receive HDLC Message - byte count** The exact function of these bits depends on whether the Receive HDLC Controller Block is configured to receive MOS or BOS messages. **In BOS Mode:** These seven bits contain the number of repetitions the BOS message must be received before the Receive HDLC controller generates the Receive End of Transfer (RxEOT) interrupt. If these bits are set to “0000000”, the message will be received indefinitely and no Receive End of Transfer (RxEOT) interrupt will be generated. **In MOS Mode:** These seven bits contain the size in bytes of the HDLC message that has been received and written into the Receive HDLC buffer. The length of MOS message shown in these bits include header bytes such as the SAPI, TEI, Control field, AND the FCS bytes.

TABLE 21: SLIP BUFFER CONTROL REGISTER (SBCR) **HEX ADDRESS: 0XN116**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-5	Reserved	-	-	**Reserved**
4	SB_FORCESF	R/W	0	**Force Signaling Freeze** This bit permits the user to freeze any signaling update within the Receive Signaling Array Register -RSAR (0xN500-0xN51F) until this bit is cleared. 0 = Signaling in RSAR is updated immediately. 1 = Signaling in RSAR is not updated until this bit is set to '0'.
3	SB_SFENB	R/W	0	**Signal Freeze Enable Upon Buffer Slips** This bit enables signaling freeze for one multiframe after the receive buffer slips. If signaling freeze is enabled, then the "Receive Channel" will freeze all signaling updates in RSAR (0xN500-0xN51F) for at least "one-multiframe" period, after a "slip-event" has been detected within the "Receive Slip Buffer". 0 = Disables signaling freeze for one multi-frame after receive buffer slips. 1 = Enables signaling freeze for one multi-frame after receive buffer slips.
2-0	Reserved	R/W	1	**Reserved**

TABLE 22: INTERRUPT CONTROL REGISTER (ICR) **HEX ADDRESS: 0XN11A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3	Reserved	-	-	**Reserved**
2	INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** This bit configures all Interrupt Status bits to be either Reset Upon Read or Write-to-Clear 0 = Configures all Interrupt Status bits to be Reset Upon Read (RUR). 1= Configures all Interrupt Status bits to be Write-to-Clear (WC).
1	ENBCLR	R/W	0	**Interrupt Enable Auto Clear** This bit configures all interrupt enable bits to clear or not clear after reading the interrupt status bit. 0= Configures all Interrupt Enable bits to not cleared after reading the interrupt status bit. The corresponding Interrupt Enable bit will stay 'high' after reading the interrupt status bit. 1= Configures all interrupt Enable bits to clear after reading the interrupt status bit. The corresponding interrupt enable bit will be set to 'low' after reading the interrupt status bit.
0	INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** This bit enables the entire E1 Framer Block for Interrupt Generation. 0 = Disables the E1 framer block for Interrupt Generation 1 = Enables the E1 framer block for Interrupt Generation

TABLE 23: SAI ENABLE REGISTER (SAIENR) **HEX ADDRESS: 0XN11C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EXT_AIS	R/W	0	**DS-1 Insertion Upon SONET/SDH and VT Mapper Validation** This bit is used to prevent AIS insertion unless an alarm is detected in the SONET/SDH or VT Mapper Blocks. 0 = Disabled 1 = Enabled
6-5	Reserved	R/W	0	**Reserved**
4	SAI Enable	R/W	0	**SAI Enable** This bit is used to enable the SAI feature which increases the SAI time to 2.5 seconds. 0 = Disabled 1 = Enable SAI
3-0	Reserved	R/W	0	**Reserved**

TABLE 24: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>7-4</td><td>Reserved</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
<tr><td>3</td><td>BERT_Switch</td><td>R/W</td><td>0</td><td>BERT Switch
This bit enables or disables the BERT switch function within the XRT86SH328 device.
By enabling the BERT switch function, BERT functionality will be switched between the receive and transmit framer. E1 Receive framer will generate the BERT pattern and insert it onto the receive interface, and E1 Transmit Framer will be monitoring the transmit interface for BERT pattern and declare BERT LOCK if it has locked onto the input pattern.
If BERT switch is disabled, E1 Transmit framer will generate the BERT pattern and the receive framer will be monitoring the BERT pattern and declare BERT LOCK if it has locked onto the input pattern.
0 = Disables the BERT Switch Feature.
1 = Enables the BERT Switch Feature.</td></tr>
<tr><td>2</td><td>BER[1]</td><td>R/W</td><td>0</td><td rowspan="2">Bit Error Rate
This bit is used to insert PRBS bit error at the rates presented at the table below. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register).
If the PRBS switch function is disabled, bit error will be inserted by the E1 transmit framer out to the line interface if this bit is enabled.
If the PRBS switch function is enabled, bit error will be inserted by the E1 receive framer out to the receive backplane interface if this bit is enabled.
<table><tr><th>BER[1:0]</th><th>BIT ERROR RATE</th></tr><tr><td>00</td><td>Disable Bit Error insertion to the transmit output or receive backplane interface</td></tr><tr><td>01</td><td>Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/1000 (one out of one Thousand)</td></tr><tr><td>10</td><td>Bit Error is inserted to the transmit output or receive backplane interface at a rate of 1/ 1,000,000 (one out of one million)</td></tr><tr><td>11</td><td>Disable Bit Error insertion to the transmit output or receive backplane interface</td></tr></table></td></tr>
<tr><td>1</td><td>BER[0]</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 24: PRBS CONTROL AND STATUS REGISTER 0 (PRBSCSR0) **HEX ADDRESS: 0XN121**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	UnFramedPRBS	R/W	0	**Unframed PRBS Pattern** This bit enables or disables unframed PRBS/QRTS pattern generation (i.e. All timeslots and framing bits are all PRBS/QRTS data). The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 within this register). If PRBS switch function is disabled, E1 Transmit Framer will generate an unframed PRBS 15 or QRTS pattern to the line side if this bit is enabled. If PRBS switch function is enabled, E1 Receive Framer will generate an unframed PRBS 15 or QRTS pattern to the receive backplane interface if this bit is enabled. 0 - Enables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface 1 - Disables an unframed PRBS/QRTS pattern generation to the line interface or to the receive backplane interface

TABLE 25: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSTyp	R/W	0	**PRBS Pattern Type** This bit selects the type of PRBS pattern that the E1 Transmit/ Receive framer will generate or detect. 0 = PRBS $X^{15} + X^{14} +1$ Polynomial generation. 1 = PRBS $X^{23} + X^{18} +1$ Polynomial generation.
6	ERRORIns	R/W	0	**Error Insertion** This bit is used to insert a single error onto the generated BERT pattern selected within this device. A ‘0’ to ‘1’ transition will cause one output bit inverted in the BERT stream. This bit only works if BERT generation is enabled.
5	DATAInv	R/W	0	**BERT Data Invert:** This bit inverts the BERT output data and the Receive BERT input data. 0 - Transmit and Receive Framer will not invert the Transmit BERT and Receive BERT data. 1 - Transmit and Receive Framer will invert the Transmit BERT and Receive BERT data.
4	RxBERTLock	RO	0	**Lock Status** This READ ONLY bit field indicates whether or not the BERT monitor LOCK has occured. 0 = Indicates the Receive BERT has not Locked onto the input patterns. 1 = Indicates the Receive BERT has locked onto the input patterns.

TABLE 25: PRBS CONTROL AND STATUS REGISTER 1 (PRBSCSR1) **HEX ADDRESS: 0XN123**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxBERTEnb	R/W	0	**Receive BERT Detection/Generation Enable** This bit enables or disables the receive BERT pattern detection or generation. The exact function of this bit depends on whether BERT switch function is enabled or not. (bit 3 in register 0xN121). 0 = Disables the Receive BERT pattern Detection/Generation. 1 - Enables the Receive BERT pattern Detection/Generation.
2	TxPRBSEnb	R/W	0	**Transmit BERT Detection/Generation Enable** This bit enables or disables the Transmit BERT pattern detection or generation. The exact function of this bit depends on whether PRBS switch function is enabled or not. (bit 3 in register 0xN121). 0 = Disables the Transmit BERT pattern Detection/Generation. 1 - Enables the Transmit BERT pattern Detection/Generation.
1	RxBypass	R/W	0	**Receive Framer Bypass** This bit enables or disables the Receive E1 Framer bypass. 0 = Disables the Receive E1 framer Bypass. 1 - Enables the Receive E1 Framer Bypass
0	TxBypass	R/W	0	**Transmit Framer Bypass** This bit enables or disables the Transmit E1 Framer bypass. 0 = Disables the Transmit E1 framer Bypass. 1 - Enables the Transmit E1 Framer Bypass

TABLE 26: LOOPBACK CODE CONTROL REGISTER (LCCR) **HEX ADDRESS: 0XN124**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved	-	-	**For T1 mode only**

TABLE 27: TRANSMIT LOOPBACK CODER REGISTER (TLCR) **HEX ADDRESS: 0XN125**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved	-	-	**For T1 mode only**

TABLE 28: RECEIVE LOOPBACK ACTIVATION CODE REGISTER (RLACR) **HEX ADDRESS: 0XN126**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved			**For T1 mode only**

TABLE 29: RECEIVE LOOPBACK DEACTIVATION CODE REGISTER (RLDCR) **HEX ADDRESS: 0XN127**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Reserved			**For T1 mode only**

TABLE 30: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	DEFDET	R/W	1	For defect detection per ANSI T1.231-1997 and T1.403-1999, user should leave this bit set to '1'.
6	**Reserved**	R/O	0	**Reserved**
5	Transmit PDI-P (Upstream) upon LOS	R/W	0	**Transmit PDI-P (Upstream) upon LOS:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the LOS defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the LOS defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon LOS. 1 = Enable this automatic Transmit PDI-P (Upstream) upon LOS. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
4	Transmit AIS (Upstream) upon LOS	R/W	0	**Transmit AIS (Upstream) upon LOS:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the LOS defect condition. 0 - Disables the "Transmit AIS (Upstream) upon LOS. 1 - Enables the "Transmit AIS (Upstream) upon LOS.

TABLE 30: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	Transmit PDI-P (Upstream) upon LOF	R/W	0	**Transmit PDI-P (Upstream) upon LOF:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the LOF defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the LOF defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon LOF. 1 = Enable this automatic Transmit PDI-P (Upstream) upon LOF. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
2	Transmit AIS-P (Upstream) upon LOF	R/W	0	**Transmit AIS (Upstream) upon LOF:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the LOF defect condition. 0 - Disables the "Transmit AIS (Upstream) upon LOF. 1 - Enables the "Transmit AIS (Upstream) upon LOF.

TABLE 30: DEFECT DETECTION ENABLE REGISTER (DDER) **HEX ADDRESS: 0XN129**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Transmit PDI-P (Upstream) upon AIS	R/W	0	**Transmit PDI-P (Upstream) upon Ingress AIS:** This READ/WRITE bit-field configures the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) anytime the Frame Synchronizer block declares the AIS defect within the T1/E1 Ingress Path. If this configuration is implemented then the following events will occur: If the T1/E1 Frame Synchronizer block were to declare the AIS defect within the Ingress Path, then the Transmit SONET POH Processor block automatically transmits the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0xE1-0xFC". Once the T1/E1Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block automatically terminates its transmission of the PDI-P indicator by setting the C2 byte within the upstream STS-1 SPE to the value "0x02". 0 = Disables this automatic Transmit PDI-P (Upstream) upon AIS. 1 = Enable this automatic Transmit PDI-P (Upstream) upon AIS. ***NOTE:*** *C2 Auto Insert Mode on Bit-1 must be enabled on Transmit STS-1/STS-3 Path Control Register - Byte 0 on address location 0x783 to use this feature.*
0	Transmit AIS-P (Upstream) upon AIS	R/W	0	**Transmit AIS (Upstream) upon Ingress AIS:** This READ/WRITE bit-field configures the T1/E1 Frame Synchronizer block to automatically transmit the AIS indicator upstream, towards the Transmit SONET POH Processor block anytime that it detects and declares the AIS defect condition. 0 - Disables the "Transmit AIS (Upstream) upon AIS. 1 - Enables the "Transmit AIS (Upstream) upon AIS.

TABLE 31: TRANSMIT Sa SELECT REGISTER (TSASR) **HEX ADDRESS: 0XN130**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSa8SEL	R/W	0	**Transmit Sa8 bit select** This bit determines whether National Bit (Sa8) is inserted from the transmit serial input or from the Transmit Sa8 register (Register address = 0xN137). 0 = Selects Sa 8 to be inserted from the Transmit Serial input. 1 = Selects Sa 8 to be inserted from the Transmit Sa8 Register.
6	TxSa7SEL	R/W	0	**Transmit Sa7 bit select** This bit determines whether National Bit (Sa7) is inserted from the transmit serial input or from the Transmit Sa7 register (Register address = 0xN136). 0 = Selects Sa 7 to be inserted from the Transmit Serial input. 1 = Selects Sa 7 to be inserted from the Transmit Sa7 Register.
5	TxSa6SEL	R/W	0	**Transmit Sa6 bit select** This bit determines whether National Bit (Sa6) is inserted from the transmit serial input pin or from the Transmit Sa6 register (Register address = 0xN135). 0 = Selects Sa 6 to be inserted from the Transmit Serial input. 1 = Selects Sa 6 to be inserted from the Transmit Sa6 Register.

TABLE 31: TRANSMIT Sa SELECT REGISTER (TSASR) **HEX ADDRESS: 0XN130**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	TxSa5SEL	R/W	0	**Transmit Sa5bit select** This bit determines whether National Bit (Sa5) is inserted from the transmit serial input pin or from the Transmit Sa5 register (Register address = 0xN134). 0 = Selects Sa 5 to be inserted from the Transmit Serial input. 1 = Selects Sa 5 to be inserted from the Transmit Sa5 Register.
3	TxSa4SEL	R/W	0	**Transmit Sa4 bit select** This bit determines whether National Bit (Sa4) is inserted from the transmit serial input pin or from the Transmit Sa4 register (Register address = 0xN133). 0 = Selects Sa 4 to be inserted from the Transmit Serial input. 1 = Selects Sa 4 to be inserted from the Transmit Sa4 Register.
2	LB1ENB	R/W	0	**Local Loopback 1 auto enable** This bit enables or disables local loopback mode when the National bits (Sa5, Sa6) and the A bit (remote alarm bit) received from the transmit backplane interface follows a specific pattern. Local loopback is activated when the National Bits (Sa5, Sa 6) and A bit (remote alarm bit) follow the following pattern from the transmit serial input. Sa5 = 00000000 occur for 8 consecutive times Sa6 = 11111111 occur for 8 consecutive times A = 11111111 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input*
1	LB2ENB	R/W	0	**Local Loopback 2 auto enable** This bit enables or disables local loopback mode when the National bits (Sa5, Sa6) received from the transmit backplane interface follows a specific pattern. Local loopback is activated when the National Bits (Sa5, Sa 6) and A bit (remote alarm bit) follow the following pattern from the transmit serial input. Sa5 = 00000000 occur for 8 consecutive times, and Sa6 = 10101010 occur for 8 consecutive times, and A = 11111111 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input*
0	LBRENB	R/W	0	**Local Loopback release enable** This bit releases the local loopback mode when the National bits (Sa5, Sa6) received from the transmit backplane interface follows a specific pattern. Local loopback is released when the National Bits (Sa5, Sa 6) follow the following pattern from the transmit serial input. Sa5 = 00000000 occur for 8 consecutive times Sa6 = 00000000 occur for 8 consecutive times ***NOTE:*** *This feature only works if Sa bits are provided from the transmit serial input*

TABLE 32: TRANSMIT Sa AUTO CONTROL REGISTER 1 (TSACR1) **HEX ADDRESS: 0XN131**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	LOSLFA_1_ENB	R/W	0	**LOS/LFA 1 automatic transmission** This bit enables the automatic Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Sa5 bit as '1', and Sa6 bit as '0' pattern. See **Table 33** for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS or LFA conditions.
6	LOS_1_ENB	R/W	0	**LOS 1 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) condition. Upon detecting Loss of Signal condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '1', and Sa6 bit as '1110' pattern. See **Table 33** for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS condition.
5	LOSLFA_2_ENB	R/W	0	**LOS/LFA 2 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '0', and Sa6 bit as '0' pattern. See **Table 33** for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS or LFA conditions.
4	LOSLFA_3_ENB	R/W	0	**LOS/LFA 3 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1100' pattern. See **Table 33** for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS/LFA conditions.
3	LOSLFA_4_ENB	R/W	0	**LOS/LFA 4 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) or Loss of frame alignment (LFA) condition. Upon detecting Loss of Signal or Loss of Frame alignment condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1110' pattern. See **Table 33** for the transmit Sa5, Sa6, and A bit pattern upon detecting LOS/LFA conditions.
2-1	Reserved	R/W	0	**Reserved**
0	LOS_2_ENB	R/W	0	**LOS 3 automatic transmission** This bit enables the auto Sa-bit transmission upon detecting Loss of Signal (LOS) condition. Upon detecting Loss of Signal condition, E1 framer will transmit the Sa5 and Sa6 bit as an Auxiliary (10101010...) pattern See **Table 33** for the transmit Sa5, Sa6, and A bit format upon detecting LOS condition.

TABLE 33: CONDITIONS ON RECEIVE SIDE WHEN TSACR1 BITS ARE ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN			COMMENTS
	A	Sa5	Sa6	
LOSLFA_1_ENB: Loss of signal or Loss of frame alignment	X	1	0000	LOS/LFA at TE (FC2)
LOS_1_ENB: Loss of signal	1	1	1110	LOS (FC3)
LOSLFA_2_ENB: LOS or LFA	1	0	0000	LOS/LFA (FCL)
LOSLFA_3_ENB: LOS or LFA	0	1	1100	LOS/LFA (FC4)
LOSLFA_4_ENB: LOS or LFA	0	1	1110	LOS/LFA (FC3&FC4)
Not Used	0	1	1000	
Not Used	1	1	1000	
LOS_2_ENB: LOS	AUXP pattern			LOS (FC1). Transmit AUXP pattern

TABLE 34: TRANSMIT Sa AUTO CONTROL REGISTER 2 (TSACR2) **HEX ADDRESS: 0XN132**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AIS_1_ENB	R/W	0	**AIS reception** This bit enables the automatic Sa-bit transmission upon detecting AIS condition. Upon detecting the AIS condition, E1 framer will transmit the Alarm bit (A bit) as '1', Sa5 bit as '1', and Sa6 bit as '1'. See **Table 35** for the transmit Sa5, Sa6, and A bit pattern upon detecting AIS condition.
6	AIS_2_ENB	R/W	0	**AIS reception** This bit enables the automatic Sa-bit transmission upon detecting AIS condition. Upon detecting the AIS condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', and Sa6 bit as '1'. See **Table 35** for the transmit Sa5, Sa6, and A bit pattern upon detecting AIS condition.
5	Reserved	-	-	**Reserved**
4	Reserved	-	-	**Reserved**
3	CRCREP_ENB[1]	R/W	0	**CRC report** These two bits enable the automatic Sa-bit transmission upon detecting Far End Block Error (i.e. received E bit = 0). Upon detecting the Far End Block Error (FEBE) condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0000', and E bit as '0' pattern if these two bits are set to '01'. If these two bits are set to '10', E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '0', Sa6 bit as '0000', and E bit as '0' pattern upon detecting the Far End Block Error (FEBE). If these two bits are set to '11', E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0001', and E bit as '1' pattern upon detecting the Far End Block Error (FEBE). See **Table 35** for the transmit Sa5, Sa6, E, and A bit pattern upon detecting FEBE condition.
2	CRCREP_ENB[0]	R/W	0	

TABLE 34: TRANSMIT Sa AUTO CONTROL REGISTER 2 (TSACR2) **HEX ADDRESS: 0XN132**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	CRCDET_ENB	R/W	0	**CRC detection** This bit enables the automatic Sa-bit transmission upon detecting CRC-4 error condition. Upon detecting CRC-4 error condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0010', and E bit as '1' pattern. See **Table 35** for the transmit Sa5, Sa6, E, and A bit pattern upon detecting CRC-4 error condition.
0	CRCREC AND DET_ENB	R/W	0	**CRC report and detect** This bit enables automatic Sa-bit transmission upon detecting both Far End Block Error (FEBE) and CRC-4 error conditions. Upon detecting both Far End Block Error (FEBE) and CRC-4 error condition, E1 framer will transmit the Alarm bit (A bit) as '0', Sa5 bit as '1', Sa6 bit as '0011', and E bit as '1' pattern. See **Table 35** for the transmit Sa5, Sa6, E, and A bit pattern upon detecting both FEBE and CRC-4 error conditions.

TABLE 35: CONDITIONS ON RECEIVE SIDE WHEN TSACR2 BITS ENABLED

CONDITIONS	ACTIONS - SENDING PATTERN FOR			
	A	Sa5	Sa6	E
AIS_1_ENB	1	1	1111	X
AIS_2_ENB	0	1	1111	x
CRCREP_ENB = 01, CRC reported (E = 0)	0	1	0000	0
CRCREP_ENB = 10, CRC reported	0	0	0000	0
CRCREP_ENB = 11, CRC reported	0	1	0001	1
CRCDET_ENB	0	1	0010	1
CRCDET/REP_ENB	0	1	0011	1

TABLE 36: TRANSMIT Sa4 REGISTER (TSA4R) **HEX ADDRESS: 0XN133**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa4[7:0]	R/W	11111111	**Transmit Sa4 Sequence** The content of this register sources the transmit Sa4 bits if data link selects Sa 4 bit for transmission and if Sa4 is inserted from register. (i.e. TxSa4ENB bit in register 0xN10A = 1 and TxSa4SEL bit in register 0xN130 = 1). Bit 7 of this register is transmitted in the Sa4 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa4 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 37: TRANSMIT Sa5 REGISTER (TSA5R) **HEX ADDRESS: 0XN134**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa5[7:0]	R/W	11111111	**Transmit Sa5 Sequence** The content of this register sources the transmit Sa5 bits if data link selects Sa 5 bit for transmission and if Sa5 is inserted from register. (i.e. TxSa5ENB bit in register 0xN10A = 1 and TxSa5SEL bit in register 0xN130 = 1). Bit 7 of this register is transmitted in the Sa5 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa5 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 38: TRANSMIT Sa6 REGISTER (TSA6R) **HEX ADDRESS: 0XN135**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa6[7:0]	R/W	11111111	**Transmit Sa6 Sequence** The content of this register sources the transmit Sa6 bits if data link selects Sa 6 bit for transmission and if Sa6 is inserted from register. (i.e. TxSa6ENB bit in register 0xN10A = 1 and TxSa6SEL bit in register 0xN130 = 1). Bit 7 of this register is transmitted in the Sa6 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa6 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 39: TRANSMIT Sa7 REGISTER (TSA7R) **HEX ADDRESS: 0XN136**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa7[7:0]	R/W	11111111	**Transmit Sa7 Sequence** The content of this register sources the transmit Sa7 bits if data link selects Sa 7 bit for transmission and if Sa7 is inserted from register. (i.e. TxSa7ENB bit in register 0xN10A = 1 and TxSa7SEL bit in register 0xN130 = 1). Bit 7 of this register is transmitted in the Sa7 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa7 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 40: TRANSMIT Sa8 REGISTER (TSA8R) **HEX ADDRESS: 0XN137**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TxSa8[7:0]	R/W	11111111	**Transmit Sa8 Sequence** The content of this register sources the transmit Sa8 bits when data link selects Sa 8 bit for transmission and if Sa8 is inserted from register. (i.e. TxSa8ENB bit in register 0xN10A = 1 and TxSa8SEL bit in register 0xN130 = 1). Bit 7 of this register is transmitted in the Sa8 position in frame 2 of the CRC-4 multiframe, and bit 6 of this register is transmitted in the Sa8 position in frame 4 of the CRC-4 multiframe,...etc.

TABLE 41: RECEIVE SA4 REGISTER (RSA4R) **HEX ADDRESS: 0XN13B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa4[7:0]	RO	00000000	**Received Sa4 Sequence** The content of this register stores the Sa 4 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa4 bits if data link selects Sa4 bit for reception. (i.e.RxSa4ENB bit in register 0xN10Ch = 1). Bit 7 of this register indicates the received Sa4 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa4 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 42: RECEIVE SA5 REGISTER (RSA5R) **HEX ADDRESS: 0XN13C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa5[7:0]	RO	00000000	**Received Sa5 Sequence** The content of this register stores the Sa 5 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa5 bits if data link selects Sa5 bit for reception. (i.e.RxSa5ENB bit in register 0xN10Ch = 1). Bit 7 of this register indicates the received Sa5 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa5 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 43: RECEIVE SA6 REGISTER (RSA6R) **HEX ADDRESS: 0XN13D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa6[7:0]	RO	00000000	**Received Sa6 Sequence** The content of this register stores the Sa 6 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa6 bits if data link selects Sa6 bit for reception. (i.e.RxSa6ENB bit in register 0xN10Ch = 1). Bit 7 of this register indicates the received Sa6 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa6 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 44: RECEIVE SA7 REGISTER (RSA7R) **HEX ADDRESS: 0XN13E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa7[7:0]	RO	00000000	**Received Sa7 Sequence** The content of this register stores the Sa 7 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa7 bits if data link selects Sa7 bit for reception. (i.e.RxSa7ENB bit in register 0xN10Ch = 1). Bit 7 of this register indicates the received Sa7 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa7 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 45: RECEIVE SA8 REGISTER (RSA8R) **HEX ADDRESS: 0XN13F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxSa8[7:0]	RO	00000000	**Received Sa8 Sequence** The content of this register stores the Sa 8 bits in the most recently received CRC-4 multiframe. This register is updated when the entire multiframe is received. This register will show the contents of the received Sa8 bits if data link selects Sa8 bit for reception. (i.e.RxSa8ENB bit in register 0xN10Ch = 1). Bit 7 of this register indicates the received Sa8 bit in frame 2 of the CRC-4 multiframe, and bit 6 of this register indicates the received Sa8 bit in frame 4 of the CRC-4 multiframe,...etc.

TABLE 46: BERT CONTROL REGISTER (BCR) **HEX ADDRESS: 0XN163**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	R/W	0	**Reserved**
3-0	BERT[3:0]	R/W	0000	**BERT Pattern Select** 0000 =PRBS X20 + X3 + 1 0011 = QRSS X20 + X17 + 1 0100 = All Ones 0101 = All Zeros 0110 = Reserved 0111 = 1 in 8 (Framed Only) 1000 = Reserved 1001 = Reserved Others = Invalid

BERT Pattern Definition

1 in 8 Framed

0000 0010 ...

TABLE 47: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) **HEX ADDRESS: 0XN300 TO 0XN31F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	Reserved (For T1 mode only)

TABLE 47: TRANSMIT CHANNEL CONTROL REGISTER 0-31 (TCCR 0-31) **HEX ADDRESS: 0XN300 TO 0XN31F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	TxCond(3:0)	R/W	0000	**Transmit Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input PCM data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the remote terminal equipment on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xN300 represents time slot 0, and address 0xN31F represents time slot 31.*

TXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Transmit Programmable User Code Register (0xN320-0xN337),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the BERT pattern (if enabled).
0xF	D/E time slot - The TxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xN10A) will determine the data source for D/E time slots.

TABLE 48: TRANSMIT USER CODE REGISTER 0 - 31 (TUCR 0-31) **HEX ADDRESS: 0XN320 TO 0XN33F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	TUCR[7:0]	R/W	b00010111	**Transmit Programmable User code.** These eight bits allow users to program any code in this register to replace the input PCM data when the Transmit Channel Control Register (TCCR) is configured to replace timeslot octet with programmable user code. (i.e. if TCCR is set to '0x4') The default value of this register is an IDLE Code (b00010111).

TABLE 49: TRANSMIT SIGNALING CONTROL REGISTER 0-31 (TSCR 0-31) HEX ADDRESS: 0XN340 TO 0XN35F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	A (x)	R/W	See Note	**Transmit Signaling bit A or x bit** This bit allows users to provide signaling Bit A for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xN340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xN350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
6	B (y)	R/W	See Note	**Transmit Signaling bit B or y bit** This bit allows users to provide signaling Bit B for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xN340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xN350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
5	C (x)	R/W	See Note	**Transmit Signaling bit C or x bit** This bit allows users to provide signaling Bit C for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xN340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xN350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
4	D (x)	R/W	See Note	**Transmit Signaling bit D or x bit** This bit allows users to provide signaling Bit D in for octets 0-31 if Channel Associated Signaling (CAS) is enabled and if signaling data is inserted from TSCR register (TxSIGSRC[1:0] = 01 in this register) ***NOTE:*** *Users must write to TSCR0 (Address 0xN340) the correct CAS alignment bits (0 bits) in order to get CAS SYNC at the remote terminal. The xyxx bits can be programmed by writing to TSCR16 (0xN350) and programming the TxSIGSRC[1:0] bits within this register to 'b11'.*
3	Reserved	-	See Note	**Reserved**
2	Reserved	-	See Note	**Reserved**

TABLE 49: TRANSMIT SIGNALING CONTROL REGISTER 0-31 (TSCR 0-31) HEX ADDRESS: 0XN340 TO 0XN35F

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	TxSIGSRC[1]	R/W	See Note	**Channel signaling control** These bits determine the source for signaling information. The table below presents the different sources for signaling information corresponding to different settings of these two bits.
0	TxSIGSRC[0]	R/W	See Note	

TXSIGSRC[1:0]	SIGNALING SOURCE SELECTED
00	Signaling data is inserted from input PCM data.
01	Signaling data is inserted from this register (TSCRs).
10	Reserved
11	No signaling data is inserted into the input PCM data. Setting these two bits to '11' will configure the xyxx bits only, where x bits are inserted from this register (TSCR) and y bit reflects the alarm condition.

NOTE: *The default value for register address 0xN340 = 0x01, 0xN341-0xN34F = 0xD0, 0xN350 = 0xB3, 0xN351-0xN35F = 0xD0*

TABLE 50: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**

TABLE 50: RECEIVE CHANNEL CONTROL REGISTER X (RCCR 0-31) **HEX ADDRESS: 0XN360 TO 0XN37F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3-0	RxCOND[3:0]	R/W	0000	**Receive Channel Conditioning for Timeslot 0 to 31** These bits allow the user to substitute the input line data (Octets 0-31) with internally generated Conditioning Codes prior to transmission to the back-plane interface on a per-channel basis. The table below presents the different conditioning codes based on the setting of these bits. ***NOTE:*** *Register address 0xN300 represents time slot 0, and address 0xN31F represents time slot 31.*

RXCOND[1:0]	CONDITIONING CODES
0x0 / 0xE	Contents of timeslot octet are unchanged.
0x1	All 8 bits of the selected timeslot octet are inverted (1's complement) OUTPUT = (TIME_SLOT_OCTET) XOR 0xFF
0x2	Even bits of the selected timeslot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0xAA
0x3	Odd bits of the selected time slot octet are inverted OUTPUT = (TIME_SLOT_OCTET) XOR 0x55
0x4	Contents of the selected timeslot octet will be substituted with the 8 -bit value in the Receive Programmable User Code Register (0xN380-0xN397),
0x5	Contents of the timeslot octet will be substituted with the value 0x7F (BUSY Code)
0x6	Contents of the timeslot octet will be substituted with the value 0xFF (VACANT Code)
0x7	Contents of the timeslot octet will be substituted with the BUSY time slot code (111#_####), where ##### is the Timeslot number
0x8	Contents of the timeslot octet will be substituted with the MOOF code (0x1A)
0x9	Contents of the timeslot octet will be substituted with the A-Law Digital Milliwatt pattern
0xA	Contents of the timeslot octet will be substituted with the μ-Law Digital Milliwatt pattern
0xB	The MSB (bit 1) of input data is inverted
0xC	All input data except MSB is inverted
0xD	Contents of the timeslot octet will be substituted with the BERT pattern (if enabled).
0xF	D/E time slot - The RxSIGDL[2:0] bits in the Transmit Signaling and Data Link Select Register (0xN10C) will determine the data source for Receive D/E time slots.

TABLE 51: RECEIVE USER CODE REGISTER 0-31 (RUCR 0-31) **HEX ADDRESS: 0XN380 TO 0XN39F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxUSER[7:0]	R/W	11111111	**Receive Programmable User code.** These eight bits allow users to program any code in this register to replace the received data when the Receive Channel Control Register (RCCR) is configured to replace timeslot octet with the receive programmable user code. (i.e. if RCCR is set to '0x4')

TABLE 52: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) HEX ADDRESS: 0XN3A0 TO 0XN3BF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	R/W	0	**Reserved**
6	SIGC_ENB	R/W	0	**Signaling substitution enable** This bit enables or disables signaling substitution on the receive side on a per channel basis. Once signaling substitution is enabled, received signaling bits ABCD will be substituted with the ABCD values in the Receive Substitution Signaling Register (RSSR). Signaling substitution only occurs in the output PCM data. The Receive Signaling Array Register (RSAR - Address 0xN500-0xN51F) will not be affected. 0 = Disables signaling substitution on the receive side. 1 = Enables signaling substitution on the receive side.
5	Reserved	R/W	0	**Reserved**
4	DEB_ENB	R/W	0	**Per-channel debounce enable** This bit enables or disables the signaling debounce feature on a per channel basis. When this feature is enabled, the per-channel signaling state must be in the same state for 2 superframes before the Receive Framer updates signaling information on the Receive Signaling Array Register (RSAR). If the signaling bits for two consecutive superframes are not the same, the current state of RSAR will not change. When this feature is disabled, RSAR will be updated as soon as the receive signaling bits have changed. 0 = Disables the Signaling Debounce feature. 1 = Enables the Signaling Debounce feature.
3	RxSIGC[1]	R/W	0	**Signaling conditioning** These bits allow user to select the format of signaling substitution on a per-channel basis, as presented in the table below. **RXSIGC[1:0] — SIGNALING SUBSTITUTION SCHEMES** 00 — **Substitutes all signaling bits with one.** 01 — **Enables 16-code (A,B,C,D) signaling substitution.** Users must write to bits 3-0 in the Receive Signaling Substitution Register (RSSR) to provide the 16-code (A,B,C,D) signaling substitution values. 10 — **Enables 4-code (A,B) signaling substitution.** Users must write to bits 4-5 in the Receive Signaling Substitution Register (RSSR) to provide the 4-code (A,B) signaling substitution values. 11 — **Enables 2-code (A) signaling substitution.** Users must write to bit 6 in the Receive Signaling Substitution Register (RSSR) to provide the 2-code (A) signaling substitution values.
2	RxSIGC[0]	R/W	0	

TABLE 52: RECEIVE SIGNALING CONTROL REGISTER 0-31 (RSCR 0-31) HEX ADDRESS: 0XN3A0 TO 0XN3BF

<table>
<tr><th>BIT</th><th>FUNCTION</th><th>TYPE</th><th>DEFAULT</th><th>DESCRIPTION-OPERATION</th></tr>
<tr><td>1</td><td>RxSIGE[1]</td><td>R/W</td><td>0</td><td rowspan="2">Receive Signaling Extraction.
These bits control per-channel signaling extraction as presented in the table below. Signaling information can be extracted to the Receive Signaling Array Register (RSAR) if the Receive SIgnaling Interface is enabled. .

<table><tr><th>RXSIGE[1:0]</th><th>SIGNALING EXTRACTION SCHEMES</th></tr><tr><td>00</td><td>No signaling information is extracted.</td></tr><tr><td>01</td><td>Enables 16-code (A,B,C,D) signaling extraction.
All signaling bits A,B,C,D will be extracted.</td></tr><tr><td>10</td><td>Enables 4-code (A,B) signaling extraction
Only signaling bits A,B will be extracted.</td></tr><tr><td>11</td><td>Enables 2-code (A) signaling extraction
Only signaling bit A will be extracted.</td></tr></table></td></tr>
<tr><td>0</td><td>RxSIGE[0]</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 53: RECEIVE SUBSTITUTION SIGNALING REGISTER 0-31 (RSSR 0-31) HEX ADDRESS 0XN3C0 TO 0XN3DF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	SIG2-A	R/W	0	**2-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A on a per channel basis when 2-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.
5	SIG4-B	R/W	0	**4-code signaling B** This bit provides the value of signaling bit B to substitute the receive signaling bit B when 4-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.
4	SIG4-A	R/W	0	**4-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A when 4-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.
3	SIG16-D	R/W	0	**16-code signaling D** This bit provides the value of signaling bit D to substitute the receive signaling bit D when 16-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.

TABLE 53: RECEIVE SUBSTITUTION SIGNALING REGISTER 0-31 (RSSR 0-31) HEX ADDRESS 0XN3C0 TO 0XN3DF

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	SIG16-C	R/W	0	**16-code signaling C** This bit provides the value of signaling bit C to substitute the receive signaling bit C when 16-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.
1	SIG16-B	R/W	0	**16-code signaling B** This bit provides the value of signaling bit B to substitute the receive signaling bit B when 16-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.
0	SIG16-A	R/W	0	**16-code signaling A** This bit provides the value of signaling bit A to substitute the receive signaling bit A when 16-code signaling substitution is enabled. Register address 0xN3C0 represents time slot 0, and 0xN3DF represents time slot 31.

TABLE 54: RECEIVE SIGNALING ARRAY REGISTER 0 - 31 (RSAR 0-31) **HEX ADDRESS: 0XN500 TO 0XN51F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Reserved	-	-	**Reserved**
3	A	RO	0	These READ ONLY registers reflect the most recently received signaling value (A,B,C,D) associated with timeslot 0 to 31. If signaling debounce feature is enabled, the received signaling state must be the same for 2 superframes before this register is updated. If the signaling bits for two consecutive superframes are not the same, the current value of this register will not be changed. If the signaling debounce or sig feature is disabled, this register is updated as soon as the received signaling bits have changed. ***NOTE:*** *The content of this register only has meaning when the framer is using Channel Associated Signaling.*
2	B	RO	0	
1	C	RO	0	
0	D	RO	0	

TABLE 55: LAPD BUFFER 0 CONTROL REGISTER (LAPDBCR0) **HEX ADDRESS: 0XN600**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 0	R/W	0	**LAPD Buffer 0 (65-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 0 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register address 0xN114). If buffer 0 is available, writing to buffer 0 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register address 0xN115) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 0 is available to be read, reading buffer 0 (Register 0xN600) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 65 Byte LAPD message can be written into or read from buffer 0 (Register 0xN600) continuously.*

TABLE 56: LAPD BUFFER 1 CONTROL REGISTER (LAPDBCR1) **HEX ADDRESS: 0XN700**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	LAPD Buffer 1	R/W	0	**LAPD Buffer 1 (65-Bytes) Auto Incrementing** This register is used to transmit and receive LAPD messages within buffer 1 of the HDLC controller. Users should determine the next available buffer by reading the BUFAVAL bit (bit 7 of the Transmit Data Link Byte Count Register address 0xN114). If buffer 1 is available, writing to buffer 1 will insert the message into the outgoing LAPD frame after the LAPD message is sent and the data from the transmit buffer 1 cannot be retrieved. After detecting the Receive end of transfer interrupt (RxEOT), users should read the RBUFPTR bit (bit 7 of the Receive Data Link Byte Count Register address 0xN115) to determine which buffer contains the received LAPD message ready to be read. If RBUFPTR bit indicates that buffer 1 is available to be read, reading buffer 1 (Register 0xN700) continuously will retrieve the entire received LAPD message. ***NOTE:*** *When writing to or reading from Buffer 0, the register is automatically incremented such that the entire 65 Byte LAPD message can be written into or read from buffer 0 (Register 0xN600) continuously.*

TABLE 57: PMON RECEIVE LINE CODE VIOLATION COUNTER MSB (RLCVCU) **HEX ADDRESS: 0XN900**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[15]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register LSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts and to clear the PMON count.*
6	RLCVC[14]	RUR	0	
5	RLCVC[13]	RUR	0	
4	RLCVC[12]	RUR	0	
3	RLCVC[11]	RUR	0	
2	RLCVC[10]	RUR	0	
1	RLCVC[9]	RUR	0	
0	RLCVC[8]	RUR	0	

TABLE 58: PMON RECEIVE LINE CODE VIOLATION COUNTER LSB (RLCVCL) **HEX ADDRESS: 0XN901**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLCVC[7]	RUR	0	**Performance Monitor "Receive Line Code Violation" 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the PMON Receive Line Code Violation Counter Register MSB combine to reflect the cumulative number of instances that Line Code Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Line Code Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts and to clear the PMON count.*
6	RLCVC[6]	RUR	0	
5	RLCVC[5]	RUR	0	
4	RLCVC[4]	RUR	0	
3	RLCVC[3]	RUR	0	
2	RLCVC[2]	RUR	0	
1	RLCVC[1]	RUR	0	
0	RLCVC[0]	RUR	0	

TABLE 59: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER MSB (RFAECU) HEX ADDRESS: 0XN902

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[15]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[14]	RUR	0	
5	RFAEC[13]	RUR	0	
4	RFAEC[12]	RUR	0	
3	RFAEC[11]	RUR	0	
2	RFAEC[10]	RUR	0	
1	RFAEC[9]	RUR	0	
0	RFAEC[8]	RUR	0	

TABLE 60: PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER LSB (RFAECL) HEX ADDRESS: 0XN903

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFAEC[7]	RUR	0	**Performance Monitor "Receive Framing Alignment Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Framing Alignment Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Framing Alignment errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Framing Alignment Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFAEC[6]	RUR	0	
5	RFAEC[5]	RUR	0	
4	RFAEC[4]	RUR	0	
3	RFAEC[3]	RUR	0	
2	RFAEC[2]	RUR	0	
1	RFAEC[1]	RUR	0	
0	RFAEC[0]	RUR	0	

TABLE 61: PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) **HEX ADDRESS: 0XN904**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSEFC[7]	RUR	0	**Performance Monitor - Receive Severely Errored frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Severely Errored Frames have been detected by the E1 Framer since the last read of this register. Severely Errored Frame is defined as the occurrence of two consecutive errored frame alignment signals without causing loss of frame condition.
6	RSEFC[6]	RUR	0	
5	RSEFC[5]	RUR	0	
4	RSEFC[4]	RUR	0	
3	RSEFC[3]	RUR	0	
2	RSEFC[2]	RUR	0	
1	RSEFC[1]	RUR	0	
0	RSEFC[0]	RUR	0	

TABLE 62: PMON RECEIVE CRC-4 BIT ERROR COUNTER - MSB (RSBBECU) **HEX ADDRESS: 0XN905**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[15]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[14]	RUR	0	
5	RSBBEC[13]	RUR	0	
4	RSBBEC[12]	RUR	0	
3	RSBBEC[11]	RUR	0	
2	RSBBEC[10]	RUR	0	
1	RSBBEC[9]	RUR	0	
0	RSBBEC[8]	RUR	0	

TABLE 63: PMON RECEIVE CRC-4 BLOCK ERROR COUNTER - LSB (RSBBECL) **HEX ADDRESS: 0XN906**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSBBEC[7]	RUR	0	**Performance Monitor "Receive Synchronization Bit Error 16-Bit Counter" - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Synchronization Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Synchronization Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Synchronization Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RSBBEC[6]	RUR	0	
5	RSBBEC[5]	RUR	0	
4	RSBBEC[4]	RUR	0	
3	RSBBEC[3]	RUR	0	
2	RSBBEC[2]	RUR	0	
1	RSBBEC[1]	RUR	0	
0	RSBBEC[0]	RUR	0	

TABLE 64: PMON RECEIVE FAR-END BLOCK ERROR COUNTER - MSB (RFEBECU) **HEX ADDRESS: 0XN907**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[15]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register LSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[14]	RUR	0	
5	RFEBEC[13]	RUR	0	
4	RFEBEC[12]	RUR	0	
3	RFEBEC[11]	RUR	0	
2	RFEBEC[10]	RUR	0	
1	RFEBEC[9]	RUR	0	
0	RFEBEC[8]	RUR	0	

TABLE 65: PMON RECEIVE FAR END BLOCK ERROR COUNTER -LSB (RFEBECL) **HEX ADDRESS: 0XN908**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RFEBEC[7]	RUR	0	**Performance Monitor - Receive Far-End Block Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Receive Far-End Block Error Counter Register MSB" combine to reflect the cumulative number of instances that the Receive Far-End Block errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive Far-End Block Error counter. ***NOTE:*** *The Receive Far-End Block Error Counter will increment once each time the received E-bit is set to zero. This counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.* ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	RFEBEC[6]	RUR	0	
5	RFEBEC[5]	RUR	0	
4	RFEBEC[4]	RUR	0	
3	RFEBEC[3]	RUR	0	
2	RFEBEC[2]	RUR	0	
1	RFEBEC[1]	RUR	0	
0	RFEBEC[0]	RUR	0	

TABLE 66: PMON RECEIVE SLIP COUNTER (RSC) **HEX ADDRESS: 0XN909**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RSC[7]	RUR	0	**Performance Monitor - Receive Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Slip events have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a E1 frame by the receive slip buffer.*
6	RSC[6]	RUR	0	
5	RSC[5]	RUR	0	
4	RSC[4]	RUR	0	
3	RSC[3]	RUR	0	
2	RSC[2]	RUR	0	
1	RSC[1]	RUR	0	
0	RSC[0]	RUR	0	

TABLE 67: PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) **HEX ADDRESS: 0XN90A**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RLFC[7]	RUR	0	**Performance Monitor - Receive Loss of Frame Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Loss of Frame condition have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *This counter counts once every time the Loss of Frame condition is declared. This counter provides the capability to measure an accumulation of short failure events.*
6	RLFC[6]	RUR	0	
5	RLFC[5]	RUR	0	
4	RLFC[4]	RUR	0	
3	RLFC[3]	RUR	0	
2	RLFC[2]	RUR	0	
1	RLFC[1]	RUR	0	
0	RLFC[0]	RUR	0	

TABLE 68: PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) **HEX ADDRESS: 0XN90B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	RCFAC[7]	RUR	0	**Performance Monitor - Receive Change of Frame Alignment Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Receive Change of Framing Alignment have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *Change of Framing Alignment (COFA) is declared when the newly-locked framing pattern is different from the one offered by off-line framer.*
6	RCFAC[6]	RUR	0	
5	RCFAC[5]	RUR	0	
4	RCFAC[4]	RUR	0	
3	RCFAC[3]	RUR	0	
2	RCFAC[2]	RUR	0	
1	RCFAC[1]	RUR	0	
0	RCFAC[0]	RUR	0	

TABLE 69: PMON LAPD FRAME CHECK SEQUENCE ERROR COUNTER 1 (LFCSEC1) **HEX ADDRESS: 0XN90C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	FCSEC1[7]	RUR	0	**Performance Monitor - LAPD Frame Check Sequence Error Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Frame Check Sequence Error have been detected by the LAPD Controller since the last read of this register.
6	FCSEC1[6]	RUR	0	
5	FCSEC1[5]	RUR	0	
4	FCSEC1[4]	RUR	0	
3	FCSEC1[3]	RUR	0	
2	FCSEC1[2]	RUR	0	
1	FCSEC1[1]	RUR	0	
0	FCSEC1[0]	RUR	0	

TABLE 70: PMON PRBS BIT ERROR COUNTER MSB (PBECU) **HEX ADDRESS: 0XN90D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Performance Monitor - E1 PRBS Bit Error 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 PRBS Bit Error Counter Register LSB" combine to reflect the cumulative number of instances that the ReceiveE1 PRBS Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive E1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 71: PMON PRBS BIT ERROR COUNTER LSB (PBECL) **HEX ADDRESS: 0XN90E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Performance Monitor - E1 PRBS Bit Error 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 PRBS Bit Error Counter Register MSB" combine to reflect the cumulative number of instances that the ReceiveE1 PRBS Bit errors has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive E1 PRBS Bit Error counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 72: PMON TRANSMIT SLIP COUNTER (TSC) **HEX ADDRESS: 0XN90F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Performance Monitor - Transmit Slip Counter (8-bit Counter)** These Reset-Upon-Read bit fields reflect the cumulative number of instances that Transmit Slip events have been detected by the E1 Framer since the last read of this register. ***NOTE:*** *A slip event is defined as a replication or deletion of a E1 frame by the transmit slip buffer.*
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

TABLE 73: PMON EXCESSIVE ZERO VIOLATION COUNTER MSB (EZVCU) **HEX ADDRESS: 0XN910**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[15]	RUR	0	**Performance Monitor - E1 Excessive Zero Violation 16-Bit Counter - Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 Excessive Zero Violation Counter Register LSB" combine to reflect the cumulative number of instances that the ReceiveE1 Excessive Zero Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Most Significant byte of this 16-bit of the Receive E1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[14]	RUR	0	
5	EZVC[13]	RUR	0	
4	EZVC[12]	RUR	0	
3	EZVC[11]	RUR	0	
2	EZVC[10]	RUR	0	
1	EZVC[9]	RUR	0	
0	EZVC[8]	RUR	0	

TABLE 74: PMON EXCESSIVE ZERO VIOLATION COUNTER LSB (EZVCL) **HEX ADDRESS: 0XN911**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	EZVC[7]	RUR	0	**Performance Monitor - E1 Excessive Zero Violation 16-Bit Counter - Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON E1 Excessive Zero Violation Counter Register MSB" combine to reflect the cumulative number of instances that the ReceiveE1 Excessive Zero Violation has been detected by the Receive E1 Framer block since the last read of this register. This register contains the Least Significant byte of this 16-bit of the Receive E1 Excessive Zero Violation counter. ***NOTE:*** *For all 16-bit wide PMON registers, user must read the MSB counter first before reading the LSB counter in order to read the accurate PMON counts. To clear PMON count, user must read the MSB counter first before reading the LSB counter in order to clear the PMON count.*
6	EZVC[6]	RUR	0	
5	EZVC[5]	RUR	0	
4	EZVC[4]	RUR	0	
3	EZVC[3]	RUR	0	
2	EZVC[2]	RUR	0	
1	EZVC[1]	RUR	0	
0	EZVC[0]	RUR	0	

TABLE 75: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Sa6	RO	0	**Sa6 Block Interrupt Status** This bit Indicates whether or not the SA 6 block has an interrupt request awaiting service. 0 - Indicates no outstanding SA 6 block interrupt request is awaiting service 1 - Indicates the SA 6 block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the SA6 block Interrupt Status register (address 0xNB0C) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the SA6 Interrupt Status Register*
6-5	Reserved			**For T1 mode only**
4	ONESEC	RO	0	**One Second Interrupt Status** This bit indicates whether or not the framer has experienced a One Second interrupt since the last read of this register. 0 = Indicates One Second interrupt has not occurred since the last read of this register 1 = Indicates One Second interrupt has occurred since the last read of this register
3	HDLC	RO	0	**HDLC Block Interrupt Status** This bit indicates whether or not the HDLC block has any interrupt request awaiting service. 0 = Indicates no outstanding HDLC block interrupt request is awaiting service 1 = Indicates HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the corresponding Data Link Status Registers to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Data Link Status Registers that generated the interrupt.*
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** This bit indicates whether or not the Slip Buffer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding Slip Buffer Block interrupt request is awaiting service 1 = Indicates Slip Buffer block has an interrupt request awaiting service. Interrupt Service routine should branch to the interrupt source and read the Slip Buffer Interrupt Status register (address 0xNB08) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the Slip Buffer Interrupt Status Register.*

TABLE 75: BLOCK INTERRUPT STATUS REGISTER (BISR) **HEX ADDRESS: 0XNB00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** This bit indicates whether or not the Alarm & Error Block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service 1 = Indicates the Alarm & Error Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the corresponding alarm and error status registers (address 0xNB02, 0xNB0E, 0xNB40) to clear the interrupt. ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the corresponding Alarm & Error Interrupt Status register that generated the interrupt.*
0	E1 FRAME	RO	0	**E1 Framer Block Interrupt Status** This bit indicates whether or not the E1 Framer block has any outstanding interrupt request awaiting service. 0 = Indicates no outstanding interrupt request is awaiting service. 1 = Indicates the E1 Framer Block has an interrupt request awaiting service. Interrupt service routine should branch to the interrupt source and read the E1 Framer status register (address 0xNB04) to clear the interrupt ***NOTE:*** *This bit will be reset to 0 after the microprocessor has performed a read to the E1 Framer Interrupt Status register.*

TABLE 76: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_ENB	R/W	0	**SA6 Block interrupt enable** This bit permits the user to either enable or disable the SA 6 Block for interrupt generation. If the user writes a “0” to this register bit and disables the SA 6 Block for interrupt generation, then all SA 6 interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the SA6 Block interrupt at the “Block Level” will be enabled. However, the individual SA 6 interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.
6-5	Reserved			**For T1 mode only**
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** This bit permits the user to either enable or disable the One Second Interrupt for interrupt generation. 0 - Disables the One Second Interrupt within the device. 1 - Enables the One Second interrupt at the “Source-Level”.

TABLE 76: BLOCK INTERRUPT ENABLE REGISTER (BIER) **HEX ADDRESS: 0XNB01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** This bit permits the user to either enable or disable the HDLC Block for interrupt generation. If the user writes a “0” to this register bit and disables the HDLC Block for interrupt generation, then all HDLC interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the HDLC Block interrupt at the “Block Level” will be enabled. However, the individual HDLC interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all SA6 Block interrupt within the device. 1 - Enables the SA6 interrupt at the “Block-Level”.
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** This bit permits the user to either enable or disable the Slip Buffer Block for interrupt generation. If the user writes a “0” to this register bit and disables the Slip Buffer Block for interrupt generation, then all Slip Buffer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Slip Buffer Block interrupt at the “Block Level” will be enabled. However, the individual Slip Buffer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Slip Buffer Block interrupt within the device. 1 - Enables the Slip Buffer interrupt at the “Block-Level”.
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** This bit permits the user to either enable or disable the Alarm & Error Block for interrupt generation. If the user writes a “0” to this register bit and disables the Alarm & Error Block for interrupt generation, then all Alarm & Error interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the Alarm & Error Block interrupt at the “Block Level” will be enabled. However, the individual Alarm & Error interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all Alarm & Error Block interrupt within the device. 1 - Enables the Alarm & Error interrupt at the “Block-Level”.
0	E1FRAME_ENB	R/W	0	**E1 Framer Block Enable** This bit permits the user to either enable or disable the E1 Framer Block for interrupt generation. If the user writes a “0” to this register bit and disables the E1 Framer Block for interrupt generation, then all E1 Framer interrupts will be disabled for interrupt generation. If the user writes a “1” to this register bit, the E1 Framer Block interrupt at the “Block Level” will be enabled. However, the individual E1 Framer interrupts at the “Source Level” still need to be enabled in order to generate that particular interrupt to the interrupt pin. 0 - Disables all E1 Framer Block interrupt within the device. 1 - Enables the E1 Framer interrupt at the “Block-Level”.

TABLE 77: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx LOF State	RO	0	**Receive Loss of Frame State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the “Loss of Frame” condition within the incoming E1 data-stream, as described below. Loss of Frame is declared when “FASC” number of consecutive frames, where “FASC” indicates the Loss of FAS Alignment Criteria in the Framing Control Register (0xN10B), bit 2-0. 0 – The Receive E1 Framer block is NOT currently declaring the “Loss of Frame” condition. 1 – The Receive E1 Framer block is currently declaring the “Loss of Frame” condition.
6	RxAIS State	RO	0	**Receive Alarm Indication Status Defect State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the AIS defect condition within the incoming E1 data-stream, as described below. AIS defect is declared when AIS condition persists for 250 microseconds (2 frames). AIS defect is cleared when more than 2 zeros are detected in two consecutive frames (250us) 0 – The Receive E1 Framer block is NOT currently declaring the AIS defect condition. 1 – The Receive E1 Framer block is currently declaring the AIS defect condition.
5	RxMYEL Status	RUR/ WC	0	**Change of CAS Multiframe Yellow Alarm Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the CAS multiframe yellow alarm interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the CAS Multiframe Yellow Alarm. **2.** Whenever the Receive E1 Framer block clears the CAS Multiframe Yellow Alarm CAS Multiframe Yellow Alarm is declared whenever the received ‘y’ bit in Time Slot 16 of Frame 0 is set to ‘1’. 0 = Indicates that the “Change of CAS Multiframe Yellow Alarm” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change of CAS Multiframe Yellow Alarm” interrupt has occurred since the last read of this register.
4	LOS State	RO	0	**Framer Receive Loss of Signal (LOS) State** This READ-ONLY bit indicates whether or not the Receive E1 framer is currently declaring the Loss of Signal (LOS) condition within the incoming DS1 data-stream, as described below LOS defect is declared when LOS condition persists for 175 consecutive bits. LOS defect is cleared when LOS condition is absent or when the received signal reaches a 12.5% ones density for 175 consecutive bits. 0 = The Receive DS1 Framer block is NOT currently declaring the Loss of Signal (LOS) condition. 1 = The Receive DS1 Framer block is currently declaring the Loss of Signal (LOS) condition.

TABLE 77: ALARM & ERROR INTERRUPT STATUS REGISTER (AEISR) **HEX ADDRESS: 0XNB02**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	LCV Int Status	RUR/ WC	0	**Line Code Violation Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the Receive E1 LIU block has detected a Line Code Violation interrupt since the last read of this register. 0 = Indicates that the Line Code Violation interrupt has not occurred since the last read of this register. 1 = Indicates that the Line Code Violation interrupt has occurred since the last read of this register.
2	Rx LOF State Change	RUR/ WC	0	**Change in Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Loss of Frame Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive E1 Framer block clears the Loss of Frame condition 0 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has occurred since the last read of this register
1	RxAIS State Change	RUR/ WC	0	**Change in Receive AIS Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive AIS Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the AIS condition. **2.** Whenever the Receive E1 Framer block clears the AIS condition 0 = Indicates that the "Change in Receive AIS condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive AIS condition" interrupt has occurred since the last read of this register
0	RxYEL State Change	RUR/ WC	0	**Change in Receive Yellow Alarm Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Yellow Alarm Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Yellow Alarm condition. **2.** Whenever the Receive E1 Framer block clears the Yellow Alarm condition 0 = Indicates that the "Change in Receive Yellow Alarm condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Yellow Alarm condition" interrupt has occurred since the last read of this register

TABLE 78: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Rx_YEL_STATE	RO	0	**Receive Yellow Alarm State** This READ-ONLY bit indicates whether or not the Receive E1 Framer block is currently declaring the Yellow Alarm condition within the incoming E1 data-stream, as described below. Yellow alarm or Remote Alarm Indication (RAI) is declared when the 'A' bit of two consecutive non-FAS frames is set to '1', which is equivalent to taking 375us to declare a RAI condition. Yellow alarm is cleared when the 'A' bit of two consecutive non-FAS frames is set to 0, which is equivalent to taking 375us to clear a RAI condition. 0 – The Receive E1 Framer block is NOT currently declaring the Yellow Alarm condition. 1 – The Receive E1 Framer block is currently declaring the Yellow Alarm condition.
6	Reserved	-	-	**Reserved**
5	RxMYEL ENB	R/W	0	**Change of CAS Multiframe Yellow Alarm Interrupt Enable**. This bit permits the user to either enable or disable the "Change in CAS Multiframe Yellow Alarm" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares CAS Multiframe Yellow Alarm. **2.** The instant that the Receive E1 Framer block clears the CAS Multiframe Yellow Alarm. 0 – Disables the "Change in CAS Multiframe Yellow Alarm" Interrupt. 1 – Enables the "Change in CAS Multiframe Yellow Alarm" Interrupt.
4	-	R/W	0	**This bit should be set to'0' for proper operation.**
3	LCV ENB	R/W	0	**Line Code violation interrupt enable** This bit permits the user to either enable or disable the "Line Code Violation" interrupt within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when Line Code Violation is detected. 0 = Disables the interrupt generation when Line Code Violation is detected. 1 = Enables the interrupt generation when Line Code Violation is detected.
2	RxLOF ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Loss of Frame Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive E1 Framer block clears the Loss of Frame condition. 0 – Disables the "Change in Loss of Frame Condition" Interrupt. 1 – Enables the "Change in Loss of Frame Condition" Interrupt.

TABLE 78: ALARM & ERROR INTERRUPT ENABLE REGISTER (AEIER) **HEX ADDRESS: 0XNB03**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxAIS ENB	R/W	0	**Change in AIS Condition interrupt enable** This bit permits the user to either enable or disable the "Change in AIS Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the AIS condition. **2.** The instant that the Receive E1 Framer block clears the AIS condition. 0 – Disables the "Change in AIS Condition" Interrupt. 1 – Enables the "Change in AIS Condition" Interrupt.
0	RxYEL ENB	R/W	0	**Change in Yellow alarm Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Yellow Alarm Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Yellow Alarm condition. **2.** The instant that the Receive E1 Framer block clears the Yellow Alarm condition. 0 – Disables the "Change in Yellow Alarm Condition" Interrupt. 1 – Enables the "Change in Yellow Alarm Condition" Interrupt.

TABLE 79: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA Status	RUR/ WC	0	**Change of CAS Multiframe Alignment Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change of CAS multiframe alignment" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the "Loss of CAS Multiframe Alignment". **2.** Whenever the Receive E1 Framer block clears the "Loss of CAS Multiframe Alignment" Loss CAS Multiframe Alignment is declared when the "CASC" number of consecutive CAS Multiframe Alignment signals have been received in error, where CASC sets the criteria for Loss of CAS multiframe. CASC can ben programmed through Framing Control Register (FCR - address 0xN10B, bit 6-5) 0 = Indicates that the "Change of CAS Multiframe Alignment" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change of CAS Multiframe Alignment" interrupt has occurred since the last read of this register. ***NOTES:*** *This bit only has meaning when Channel Associated Signaling (CAS) is enabled.*
6	NBIT Status	RUR/ WC	0	**Change in National Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in National Bits" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever any one of the National Bits (Sa4-Sa8) within the incoming non-FAS E1 frames has changed. 0 = Indicates that the "Change in National Bits" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in National Bits" interrupt has occurred since the last read of this register.
5	SIG Status	RUR/ WC	0	**Change in CAS Signaling Bits Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in CAS Signaling Bits" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever any one of the four signaling bits values (A,B,C,D) has changed in any one of the 30 channels within the incoming E1 frames. Users can read the signaling change registers (address 0xN10D-0xN110) to determine which signalling channel has changed. 0 = Indicates that the "Change in CAS Signaling Bits" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in CAS Signaling Bits" interrupt has occurred since the last read of this register. ***NOTE:*** *This bit only has meaning when Channel Associated Signaling (CAS) is enabled.*

TABLE 79: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	COFA Status	RUR/ WC	0	**Change of FAS Framing Alignment (COFA) Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change of FAS Framing Alignment" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects a Change of FAS Framing Alignment Signal (e.g., the FAS bits have appeared to move to a different location within the incoming E1 data stream). 0 = Indicates that the "Change of FAS Framing Alignment (COFA)" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change of FAS Framing Alignment (COFA)" interrupt has occurred since the last read of this register.
3	LOF Status	RUR/ WC	0	**Change in Loss of Frame Condition Interrupt Status**. This Reset-Upon-Read bit field indicates whether or not the "Change in Receive Loss of Frame Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Loss of Frame condition. **2.** Whenever the Receive E1 Framer block clears the Loss of Frame condition 0 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Receive Loss of Frame condition" interrupt has occurred since the last read of this register
2	FMD Status	RUR/ WC	0	**Frame Mimic Detection Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Frame Mimic Detection" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects the presence of Frame Mimic bits (i.e., the Payload bits have appeared to mimic the Framing pattern within the incoming E1 data stream). 0 = Indicates that the "Frame Mimic Detection" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Frame Mimic Detection" interrupt has occurred since the last read of this register.

TABLE 79: FRAMER INTERRUPT STATUS REGISTER (FISR) **HEX ADDRESS: 0XNB04**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	Sync Error Status	RUR/ WC	0	**CRC-4 Error Interrupt Status.** This Reset-Upon-Read bit field indicates whether or not the “CRC-4 Error” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects a CRC-4 Error within the incoming E1 sub-multiframe. 0 = Indicates that the “CRC-4 Error” interrupt has not occurred since the last read of this register. 1 = Indicates that the “CRC-4 Error” interrupt has occurred since the last read of this register.
0	Framing Error Status	RUR/ WC	0	**Framing Error Interrupt Status** This Reset-Upon-Read bit field indicates whether or not a “Framing Error” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt whenever the Receive E1 Framer block detects one or more Framing Alignment Bit Error within the incoming E1 data stream. 0 = Indicates that the “Framing Error” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Framing Error” interrupt has occurred since the last read of this register. ***NOTE:*** *This bit doesn't not necessarily indicate that synchronization has been lost.*

TABLE 80: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	COMFA ENB	R/W	0	**Change in CAS Multiframe Alignment Interrupt Enable** This bit permits the user to either enable or disable the "Change in CAS Multiframe Alignment" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Loss of CAS Multiframe Alignment condition. **2.** The instant that the Receive E1 Framer block clears the Loss of CAS Multiframe Alignment condition. 0 – Disables the "Change in CAS Multiframe Alignment" Interrupt. 1 – Enables the "Change in CAS Multiframe Alignment" Interrupt.
6	NBIT ENB	R/W	0	**Change in National Bits Interrupt Enable** This bit permits the user to either enable or disable the "Change in National Bits" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a change in the National Bits (Sa4-Sa8) within the channel. 0 = Disables the Change in National Bits Interrupt 1 - Enables the Change in National Bits Interrupt
5	SIG ENB	R/W	0	**Change in CAS Signaling Bits Interrupt Enable** This bit permits the user to either enable or disable the "Change in CAS Signaling Bits" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a change in the any four signaling bits (A,B,C,D) in any one of the 30 signaling channels. Users can read the signaling change registers (address 0xN10D-0xN110) to determine which signalling channel has changed state. 0 = Disables the Change in Signaling Bits Interrupt 1 - Enables the Change in Signaling Bits Interrupt ***NOTE:*** *This bit has no meaning when Channel Associated Signaling is disabled.*
4	COFA ENB	R/W	0	**Change of FAS Framing Alignment (COFA) Interrupt Enable** This bit permits the user to either enable or disable the "Change in FAS Framing Alignment (COFA)" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a Change of FAS Framing Alignment Signal (e.g., the FAS bits have appeared to move to a different location within the incoming E1 data stream). 0 – Disables the "Change of FAS Framing Alignment (COFA)" Interrupt. 1 – Enables the "Change of FAS Framing Alignment (COFA)" Interrupt.

TABLE 80: FRAMER INTERRUPT ENABLE REGISTER (FIER) **HEX ADDRESS: 0XNB05**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	LOF ENB	R/W	0	**Change in Loss of Frame Condition interrupt enable** This bit permits the user to either enable or disable the "Change in Loss of Frame Condition" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** The instant that the Receive E1 Framer block declares the Loss of Frame condition. **2.** The instant that the Receive E1 Framer block clears the Loss of Frame condition. 0 – Disables the "Change in Loss of Frame Condition" Interrupt. 1 – Enables the "Change in Loss of Frame Condition" Interrupt.
2	FMD ENB	R/W	0	**Frame Mimic Detection Interrupt Enable** This bit permits the user to either enable or disable the "Frame Mimic Detection" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects the presence of Frame mimic bits (i.e., the payload bits have appeared to mimic the framing bit pattern within the incoming E1 data stream). 0 – Disables the "Frame Mimic Detection" Interrupt. 1 – Enables the "Frame Mimic Detection" Interrupt.
1	SE_ENB	R/W	0	**Synchronization Bit (CRC-4) Error Interrupt Enable** This bit permits the user to either enable or disable the "CRC-4 Error Detection" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects a CRC-4 error within the incoming E1 sub-multiframe. 0 – disable the "CRC-4 Error Detection" Interrupt. 1 – enable the "CRC-4 Error Detection" Interrupt.
0	FE_ENB	R/W	0	**Framing Bit Error Interrupt Enable** This bit permits the user to either enable or disable the "Framing Alignment Bit Error Detection" Interrupt, within the XRT86SH328 device. If the user enables this interrupt, then the Receive E1 Framer block will generate an interrupt when it detects one or more Framing Alignment Bit error within the incoming E1 data stream. 0 – disable the "Framing Alignment Bit Error Detection" Interrupt. 1 – enable the "Framing Alignment Bit Error Detection" Interrupt. ***NOTE:*** *Detecting Framing Alignment Bit Error doesn't not necessarily indicate that synchronization has been lost.*

TABLE 81: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	MSG TYPE	RO	0	**HDLC Message Type Identifier** This READ ONLY bit indicates the type of data link message received by Receive HDLC Controller. Two types of data link messages are supported within the XRT86SH328 device: Message Oriented Signaling (MOS) or Bit-Oriented Signalling (BOS). 0 = Indicates Bit-Oriented Signaling (BOS) type data link message is received 1 = Indicates Message Oriented Signaling (MOS) type data link message is received
6	TxSOT	RUR/ WC	0	**Transmit HDLC Controller Start of Transmission (TxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the "Transmit HDLC Controller Start of Transmission (TxSOT) "Interrupt has occurred since the last read of this register. Transmit HDLC Controller will declare this interrupt when it has started to transmit a data link message. For sending large HDLC messages, start loading the next available buffer once this interrupt is detected. 0 = Transmit HDLC Controller Start of Transmission (TxSOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC Controller Start of Transmission interrupt (TxSOT) has occurred since the last read of this register.
5	RxSOT	RUR/ WC	0	**Receive HDLC Controller Start of Reception (RxSOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register. Receive HDLC Controller will declare this interrupt when it has started to receive a data link message. 0 = Receive HDLC Controller Start of Reception (RxSOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC Controller Start of Reception (RxSOT) interrupt has occurred since the last read of this register
4	TxEOT	RUR/ WC	0	**Transmit HDLC Controller End of Transmission (TxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit HDLC Controller End of Transmission (TxEOT) Interrupt has occurred since the last read of this register. Transmit HDLC Controller will declare this interrupt when it has completed its transmission of a data link message. For sending large HDLC messages, it is critical to load the next available buffer before this interrupt occurs. 0 = Transmit HDLC Controller End of Transmission (TxEOT) interrupt has not occurred since the last read of this register 1 = Transmit HDLC Controller End of Transmission (TxEOT) interrupt has occurred since the last read of this register

TABLE 81: DATA LINK STATUS REGISTER 1 (DLSR1) **HEX ADDRESS: 0XNB06**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxEOT	RUR/ WC	0	**Receive HDLC Controller End of Reception (RxEOT) Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive HDLC Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register. Receive HDLC Controller will declare this interrupt once it has completely received a full data link message, or once the buffer is full. 0 = Receive HDLC Controller End of Reception (RxEOT) interrupt has not occurred since the last read of this register 1 = Receive HDLC Controller End of Reception (RxEOT) Interrupt has occurred since the last read of this register
2	FCS Error	RUR/ WC	0	**FCS Error Interrupt Status** This Reset-Upon-Read bit indicates whether or not the FCS Error Interrupt has occurred since the last read of this register. Receive HDLC Controller will declare this interrupt when it has detected the FCS error in the most recently received data link message. 0 = FCS Error interrupt has not occurred since the last read of this register 1 = FCS Error interrupt has occurred since the last read of this register
1	Rx ABORT	RUR/ WC	0	**Receipt of Abort Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Abort Sequence interrupt has occurred since last read of this register. Receive HDLC Controller will declare this interrupt if it detects the Abort Sequence (i.e. a string of seven (7) consecutive 1's) in the incoming data link channel. 0 = Receipt of Abort Sequence interrupt has not occurred since last read of this register 1 = Receipt of Abort Sequence interrupt has occurred since last read of this register
0	RxIDLE	RUR/ WC	0	**Receipt of Idle Sequence Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receipt of Idle Sequence interrupt has occurred since the last read of this register. The Receive HDLC Controller will declare this interrupt if it detects the flag sequence octet (0x7E) in the incoming data link channel. If RxIDLE "AND" RxEOT occur together, then the entire HDLC message has been received. 0 = Receipt of Idle Sequence interrupt has not occurred since last read of this register 1 = Receipt of Idle Sequence interrupt has occurred since last read of this register.

TABLE 82: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) **HEX ADDRESS: 0XNB07**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Reserved	-	-	**Reserved**
6	TxSOT ENB	R/W	0	**Transmit HDLC Controller Start of Transmission (TxSOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC Controller Start of Transmission (TxSOT) “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Transmit HDLC Controller will generate an interrupt when it has started to transmit a data link message. 0 = Disables the Transmit HDLC Controller Start of Transmission (TxSOT) interrupt. 1 = Enables the Transmit HDLC Controller Start of Transmission (TxSOT) interrupt.
5	RxSOT ENB	R/W	0	**Receive HDLC Controller Start of Reception (RxSOT) Interrupt Enable** This bit enables or disables the “Receive HDLC Controller Start of Reception (RxSOT) “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC Controller will generate an interrupt when it has started to receive a data link message. 0 = Disables the Receive HDLC Controller Start of Reception (RxSOT) interrupt. 1 = Enables the Receive HDLC Controller Start of Reception (RxSOT) interrupt.
4	TxEOT ENB	R/W	0	**Transmit HDLC Controller End of Transmission (TxEOT) Interrupt Enable** This bit enables or disables the “Transmit HDLC Controller End of Transmission (TxEOT) “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Transmit HDLC Controller will generate an interrupt when it has finished transmitting a data link message. 0 = Disables the Transmit HDLC Controller End of Transmission (TxEOT) interrupt. 1 = Enables the Transmit HDLC Controller End of Transmission (TxEOT) interrupt.
3	RxEOT ENB	R/W	0	**Receive HDLC Controller End of Reception (RxEOT) Interrupt Enable** This bit enables or disables the “Receive HDLC Controller End of Reception (RxEOT) “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC Controller will generate an interrupt when it has finished receiving a complete data link message. 0 = Disables the Receive HDLC Controller End of Reception (RxEOT) interrupt. 1 = Enables the Receive HDLC Controller End of Reception (RxEOT) interrupt.

TABLE 82: DATA LINK INTERRUPT ENABLE REGISTER 1 (DLIER1) HEX ADDRESS: 0XNB07

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	FCS ERR ENB	R/W	0	**FCS Error Interrupt Enable** This bit enables or disables the “Received FCS Error “Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC Controller will generate an interrupt when it has detected the FCS error within the incoming data link message. 0 = Disables the “Receive FCS Error” interrupt. 1 = Enables the “Receive FCS Error” interrupt.
1	RxABORT ENB	R/W	0	**Receipt of Abort Sequence Interrupt Enable** This bit enables or disables the “Receipt of Abort Sequence“ Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC Controller will generate an interrupt when it has detected the Abort Sequence (i.e. a string of seven (7) consecutive 1’s) within the incoming data link channel. 0 = Disables the “Receipt of Abort Sequence” interrupt. 1 = Enables the “Receipt of Abort Sequence” interrupt.
0	RxIDLE ENB	R/W	0	**Receipt of Idle Sequence Interrupt Enable** This bit enables or disables the “Receipt of Idle Sequence“ Interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive HDLC Controller will generate an interrupt when it has detected the Idle Sequence Octet (i.e. 0x7E) within the incoming data link channel. 0 = Disables the “Receipt of Idle Sequence” interrupt. 1 = Enables the “Receipt of Idle Sequence” interrupt.

TABLE 83: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSB_FULL	RUR/ WC	0	**Transmit Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Full interrupt has occurred since the last read of this register. The transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Full interrupt has occurred since the last read of this register.
6	TxSB_EMPT	RUR/ WC	0	**Transmit Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register. The transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Empty interrupt has occurred since the last read of this register.
5	TxSB_SLIP	RUR/ WC	0	**Transmit Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. The transmit Slip Buffer Slips interrupt is declared when the transmit slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Transmit Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Transmit Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Transmit Slip Buffer Empty Interrupt (bit 6 of this register) or the Transmit Slip Buffer Full Interrupts (bit 7 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 83: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	CAS SYNC	RO	0	**CAS Multiframe Alignment is in SYNC** This READ ONLY bit field indicates whether or not the E1 Receive Framer Block is declaring CAS Multiframe Alignment LOCK status. The E1 Receive Framer Block will declare the CAS Multiframe Alignment LOCK status according to the CAS Multiframe Alignment Algorithm as described in the Framing Select Register (FSR - address 0xN107). The E1 Receive Framer Block will declare the CAS Multiframe Alignment LOSS OF LOCK status when CASC number of consecutive CAS Multi-frame Alignment Signals have been received in error, where CASC sets the Loss of CAS Multiframe Alignment Criteria, as described in the Fram-ing Control Register (FCR - address 0xN10B). 0 = Indicates that the E1 Receive Framer Block is currently declaring CAS Multiframe LOSS OF LOCK status 1 = Indicates that the E1 Receive Framer Block is currently declaring CAS Multiframe LOCK status ***NOTE:*** *In E1 mode, this bit has no meaning if Channel Associated Signaling is disabled.*
3	CRCMLOCK	RO	0	**CRC Multiframe is in SYNC** This READ ONLY bit field indicates whether or not the E1 Receive Framer Block is declaring the E1 CRC Multiframe Alignment LOCK status. The E1 Receive Framer declares the CRC Multiframe Alignment LOCK status according to the CRC Multiframe Alignment Declaration Criteria which can be selected in the Framing Select Register (FSR - address 0xN107) The E1 Receive Framer declares the CRC Multiframe Alignment LOSS OF LOCK status according to the Loss CRC Multiframe Alignment Criteria selected in the Framing Control Register (FCR - address 0xN10B) 0 = Indicates that the E1 Receive Framer is currently declaring E1 CRC Multiframe Alignment LOSS OF LOCK status 0 = Indicates that the E1 Receive Framer is currently declaring E1 Multi-frame Alignment LOCK status ***NOTE:*** *In E1 mode, this bit has no meaning if CRC Multiframe Alignment is disabled.*
2	RxSB_FULL	RUR/ WC	0	**Receive Slip buffer Full Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Full interrupt has occurred since the last read of this register. The Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Full interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Full interrupt has occurred since the last read of this register.

TABLE 83: SLIP BUFFER INTERRUPT STATUS REGISTER (SBISR) **HEX ADDRESS: 0XNB08**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	RxSB_EMPT	RUR/ WC	0	**Receive Slip buffer Empty Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Empty interrupt has occurred since the last read of this register. The Receive Slip Buffer Empty interrupt is declared when the receive slip buffer is emptied. If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Empty interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Empty interrupt has occurred since the last read of this register.
0	RxSB_SLIP	RUR/ WC	0	**Receive Slip Buffer Slips Interrupt Status** This Reset-Upon-Read bit indicates whether or not the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. The Receive Slip Buffer Slips interrupt is declared when the receive slip buffer is either filled or emptied. This interrupt bit will be set to '1' in either one of these two conditions: **1.** If the receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Indicates that the Receive Slip Buffer Slips interrupt has not occurred since the last read of this register. 1 = Indicates that the Receive Slip Buffer Slips interrupt has occurred since the last read of this register. ***NOTE:*** *Users still need to read the Receive Slip Buffer Empty Interrupt (bit 1 of this register) or the Receive Slip Buffer Full Interrupts (bit 2 of this register) to determine whether transmit slip buffer empties or fills.*

TABLE 84: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxFULL_ENB	R/W	0	**Transmit Slip Buffer Full Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Full interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Full interrupt is declared when the transmit slip buffer is filled. If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Transmit Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
6	TxEMPT_ENB	R/W	0	**Transmit Slip Buffer Empty Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Empty interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Empty interrupt is declared when the transmit slip buffer is emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Transmit Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
5	TxSLIP_ENB	R/W	0	**Transmit Slip Buffer Slips Interrupt Enable** This bit enables or disables the Transmit Slip Buffer Slips interrupt within the XRT86SH328 device. Once this interrupt is enabled, the transmit Slip Buffer Slips interrupt is declared when either the transmit slip buffer is filled or emptied. If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. The interrupt status bit will be set to '1' in either one of these two conditions: **1.** If the transmit slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the transmit slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Disables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Transmit Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.
4-3	Reserved	-	-	**Reserved**

TABLE 84: SLIP BUFFER INTERRUPT ENABLE REGISTER (SBIER) **HEX ADDRESS: 0XNB09**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	RxFULL_ENB	R/W	0	**Receive Slip Buffer Full Interrupt Enable** This bit enables or disables the Receive Slip Buffer Full interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Full interrupt is declared when the receive slip buffer is filled. If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and the interrupt status bit will be set to '1'. 0 = Disables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills 1 - Enables the Receive Slip Buffer Full interrupt when the Transmit Slip Buffer fills.
1	RxEMPT_ENB	R/W	0	**Receive Slip buffer Empty Interrupt Enable** This bit enables or disables the Receives Slip Buffer Empty interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Empty interrupt is declared when the Receive slip buffer is emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. 0 = Disables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties 1 - Enables the Receive Slip Buffer Empty interrupt when the Transmit Slip Buffer empties.
0	RxSLIP_ENB	R/W	0	**Receive Slip buffer Slips Interrupt Enable** This bit enables or disables the Receive Slip Buffer Slips interrupt within the XRT86SH328 device. Once this interrupt is enabled, the Receive Slip Buffer Slips interrupt is declared when either the Receive slip buffer is filled or emptied. If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and the interrupt status bit will be set to '1'. The interrupt status bit will be set to '1' in either one of these two conditions: **1.** If the Receive slip buffer is emptied and a READ operation occurs, then a full frame of data will be repeated, and this interrupt bit will be set to '1'. **2.** If the Receive slip buffer is full and a WRITE operation occurs, then a full frame of data will be deleted, and this interrupt bit will be set to '1'. 0 = Disables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills 1 - Enables the Receive Slip Buffer Slips interrupt when the Transmit Slip Buffer empties or fills.

TABLE 85: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	AUXPSTAT	RO	0	**AUXP state** This READ ONLY bit indicates whether or not the Receive E1 Framer Block is currently detecting Auxiliary (101010....) pattern. 0 = Indicates that the Receive E1 Framer Block is NOT currently detecting the Auxiliary (101010....)Pattern. 1 = Indicates that the Receive E1 Framer Block is currently detecting the Auxiliary (101010....)Pattern.
6	AUXPINT	RUR/WC	0	**Change in Auxiliary Pattern interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Auxiliary Pattern" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Auxiliary Pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Auxiliary Pattern 0 = Indicates that the "Change in Auxiliary Pattern" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Auxiliary Pattern" interrupt has occurred since the last read of this register
5	NONCRCSTAT	RO	0	**CRC-4-to-non-CRC-4 interworking state** This READ ONLY bit indicates the status of CRC-4 interworking status when Annex B is enabled. (MODENB bit in register 0xN107) When Annex B is enabled, G.706 Annex B CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400msec while the basic frame alignment signal is present, it is assumed that the remote end is a non CRC-4 equipment. Then, a CRC-to-Non-CRC interworking interrupt status will be generated. 0 = Indicates CRC-4 to non-CRC-4 interworking is NOT established. 1 = Indicates CRC-4 to non-CRC-4 interworking is established.

TABLE 85: RECEIVE LOOPBACK CODE INTERRUPT AND STATUS REGISTER (RLCISR) HEX ADDRESS: 0XNB0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	NONCRCINT	RUR/WC	0	**Change of CRC-4-to-non-CRC-4 interworking interrupt Status -** This Reset-Upon-Read bit field indicates whether or not the "Change in CRC-4 to Non-CRC-4 interworking" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the CRC-4 to non-CRC-4 interworking condition. **2.** Whenever the Receive E1 Framer block detects the non-CRC-4 to CRC-4 interworking condition. 0 = Indicates that the "Change in CRC-4 to non-CRC-4 interworking" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in CRC-4 to non-CRC-4 interworking" interrupt has occurred since the last read of this register
3-0				**For T1 mode only**

TABLE 86: RECEIVE LOOPBACK CODE INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB0B**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
6	AUXPINTENB	R/W	0	**Change in Auxiliary Pattern interrupt enable** This READ WRITE bit field enables or disables the "Change in Auxiliary Pattern" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Auxiliary Pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Auxiliary Pattern 0 = Disables the "Change in Auxiliary Pattern" interrupt within the E1 Receive Framer. 1 - Enables the "Change in Auxiliary Pattern" interrupt within the E1 Receive Framer.
5	Reserved	-	-	**Reserved**
4	NONCRCENB	R/W	0	**Change of CRC-4-to-non-CRC-4 interworking interrupt Enable** This bit enables or disables the "Change in CRC-4 to Non-CRC-4 interworking" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the CRC-4 to non-CRC-4 interworking condition. **2.** Whenever the Receive E1 Framer block detects the non-CRC-4 to CRC-4 interworking condition. 0 = Disables the "Change in CRC-4 to non-CRC-4 interworking" interrupt within the E1 Receive Framer. 1 - Enables the "Change in CRC-4 to non-CRC-4 interworking" interrupt within the E1 Receive Framer.
3-2	Reserved	-	-	**Reserved**
1-0	Reserved			**For T1 mode only**

TABLE 87: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111	RUR/ WC	0	**Change in Debounced Sa6 = 1111 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1111" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1111 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1111 pattern. 0 = Indicates that the "Change in Debounced Sa6=1111" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1111" interrupt has occurred since the last read of this register
6	SA6_1110	RUR/ WC	0	**Change in Debounced Sa6 = 1110 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1110" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1110 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1110 pattern. 0 = Indicates that the "Change in Debounced Sa6=1110" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1110" interrupt has occurred since the last read of this register
5	SA6_1100	RUR/ WC	0	**Change in Debounced Sa6 = 1100 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1100" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1100 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1100 pattern. 0 = Indicates that the "Change in Debounced Sa6=1100" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1100" interrupt has occurred since the last read of this register

TABLE 87: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SA6_1010	RUR/ WC	0	**Change in Debounced Sa6 = 1010 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1010" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1010 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1010 pattern. 0 = Indicates that the "Change in Debounced Sa6=1010" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1010" interrupt has occurred since the last read of this register
3	SA6_1000	RUR/ WC	0	**Change in Debounced Sa6 = 1000 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=1000" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1000 pattern. 0 = Indicates that the "Change in Debounced Sa6=1000" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=1000" interrupt has occurred since the last read of this register
2	SA6_001x	RUR/ WC	0	**Change in Debounced Sa6 = 001x Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=001x" interrupt has occurred since the last read of this register, where x is don't care. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 001x pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 001x pattern. 0 = Indicates that the "Change in Debounced Sa6=001x" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=001x" interrupt has occurred since the last read of this register

TABLE 87: RECEIVE SA INTERRUPT STATUS REGISTER (RSAISR) **HEX ADDRESS: 0XNB0C**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA6_other	RUR/ WC	0	**Debounced Sa6 = other Combination Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=other combination" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when it detects the Debounced Sa 6 equals to any other combinations. 0 = Indicates that the "Debounced Sa6 = other combination" interrupt has not occurred since the last read of this register 1 = Indicates that the "Debounced Sa6 = other combination" interrupt has occurred since the last read of this register
0	SA6_0000	RUR/ WC	0	**Change in Debounced Sa6 = 0000 Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Debounced Sa6=0000" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 0000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 0000 pattern. 0 = Indicates that the "Change in Debounced Sa6=0000" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Debounced Sa6=0000" interrupt has occurred since the last read of this register

TABLE 88: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_1111_ENB	R/W	0	**Change in Debounced Sa6 = 1111 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1111” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1111 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1111 pattern. 0 = Disables the “Change in Debounced Sa6=1111” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1111” interrupt within the Receive E1 Framer Block
6	SA6_1110_ENB	R/W	0	**Change in Debounced Sa6 = 1110 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1110” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1110 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1110 pattern. 0 = Disables the “Change in Debounced Sa6=1110” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1110” interrupt within the Receive E1 Framer Block
5	SA6_1100_ENB	R/W	0	**Change in Debounced Sa6 = 1100 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=1100” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1100 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1100 pattern. 0 = Disables the “Change in Debounced Sa6=1100” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=1100” interrupt within the Receive E1 Framer Block

TABLE 88: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	SA6_1010_ENB	R/W	0	**Change in Debounced Sa6 = 1010 Interrupt Enable** This bit enables or disables the "Change in Debounced Sa6=1010" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1010 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1010 pattern. 0 = Disables the "Change in Debounced Sa6=1010" interrupt within the Receive E1 Framer Block 1 - Enables the "Change in Debounced Sa6=1010" interrupt within the Receive E1 Framer Block
3	SA6_1000_ENB	R/W	0	**Change in Debounced Sa6 = 1000 Interrupt Enable** This bit enables or disables the "Change in Debounced Sa6=1000" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 1000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 1000 pattern. 0 = Disables the "Change in Debounced Sa6=1000" interrupt within the Receive E1 Framer Block 1 - Enables the "Change in Debounced Sa6=1000" interrupt within the Receive E1 Framer Block
2	SA6_001x_ENB	R/W	0	**Change in Debounced Sa6 = 001x Interrupt Enable** This bit enables or disables the "Change in Debounced Sa6=001x" interrupt within the E1 Receive Framer, where x is don't care. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 001x pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 001x pattern. 0 = Disables the "Change in Debounced Sa6=001x" interrupt within the Receive E1 Framer Block 1 - Enables the "Change in Debounced Sa6=001x" interrupt within the Receive E1 Framer Block

TABLE 88: RECEIVE SA INTERRUPT ENABLE REGISTER (RSAIER) **HEX ADDRESS: 0XNB0D**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA6_other_ENB	R/W	0	**Debounced Sa6 = Other Combination Interrupt enable** This bit enables or disables the “Debounced Sa6=other combination” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when it detects the debounced Sa6 equals to any other combination. 0 = Disables the “Debounced Sa6=other combination” interrupt within the Receive E1 Framer Block 1 - Enables the “Debounced Sa6=other combination” interrupt within the Receive E1 Framer Block
0	SA6_0000_ENB	R/W	0	**Change in Debounced Sa6 = 0000 Interrupt Enable** This bit enables or disables the “Change in Debounced Sa6=0000” interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Debounced Sa6 equals to the 0000 pattern. **2.** Whenever the Receive E1 Framer block no longer detects the Debounced Sa6 equals to the 0000 pattern. 0 = Disables the “Change in Debounced Sa6=0000” interrupt within the Receive E1 Framer Block 1 - Enables the “Change in Debounced Sa6=0000” interrupt within the Receive E1 Framer Block

TABLE 89: EXCESSIVE ZERO STATUS REGISTER (EXZSR) **HEX ADDRESS: 0XNB0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
5	SA7_EQ_0_STAT	RO	0	**Received Sa7 Equals '0' State** This READ ONLY bit field indicates whether or not the Receive E1 Framer is currently declaring the "Sa7 Equals 0" status within the incoming E1 National Bits. The "Received Sa7 Equals 0" status will be set to '1' if the received Sa7 is 0 for at least 2 out of 3 times. 0 = Indicates the E1 Receive Framer is currently not declaring the "Received Sa7 Equals 0" status. 1 = Indicates the E1 Receive Framer is currently declaring the "Received Sa7 Equals 0" status.
4-2	Reserved	-	-	**Reserved**
1	SA7_EQ_0_INT	RUR/ WC	0	**Change in "Sa 7 Equals 0" Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Sa7 Equals 0" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Received Sa7 equals to 0 for at least 2 out of 3 times. **2.** Whenever the Receive E1 Framer block no longer detects the Received Sa7 equals to the 0. 0 = Indicates that the "Change in Sa7 Equals 0" interrupt has not occurred since the last read of this register 1 = Indicates that the "Change in Sa7 Equals 0" interrupt has occurred since the last read of this register
0	EXZ_STATUS	RUR/ WC	0	**Change in Excessive Zero Condition Interrupt Status** This Reset-Upon-Read bit field indicates whether or not the "Change in Excessive Zero Condition" interrupt within the E1 Receive Framer Block has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive E1 Framer block clears the Excessive Zero Condition 0 = Indicates the "Change in Excessive Zero Condition" interrupt has NOT occurred since the last read of this register 1 = Indicates the "Change in Excessive Zero Condition" interrupt has occurred since the last read of this register

TABLE 90: EXCESSIVE ZERO ENABLE REGISTER (EXZER) **HEX ADDRESS: 0XNB0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
1	SA7_EQ_0_ENB	R/W	0	**Change in "Sa 7 Equals 0" Interrupt Enable** This bit enables or disables the "Change in Sa7 Equals 0" interrupt within the Receive E1 Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Received Sa7 equals to 0 for at least 2 out of 3 times. **2.** Whenever the Receive E1 Framer block no longer detects the Received Sa7 equals to the 0. 0 = Disables the "Change in Sa7 Equals 0" interrupt within the E1 Receive Framer Block. 1 = Enables the "Change in Sa7 Equals 0" interrupt within the E1 Receive Framer Block.
0	EXZ_ENB	R/W	0	**Change in Excessive Zero Condition Interrupt Enable** This bit enables or disables the "Change in Excessive Zero Condition" interrupt within the E1 Receive Framer. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block detects the Excessive Zero Condition. **2.** Whenever the Receive E1 Framer block clears the Excessive Zero Condition 0 = Disables the "Change in Excessive Zero Condition" interrupt within the Receive E1 Framer Block 1 - Enables the "Change in Excessive Zero Condition" interrupt within the Receive E1 Framer Block

TABLE 91: SS7 STATUS REGISTER FOR LAPD (SS7SR) **HEX ADDRESS: 0XNB10**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_STATUS	RUR/ WC	0	**SS7 Interrupt Status for LAPD Controller** This Reset-Upon-Read bit field indicates whether or not the "SS7" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 = Indicates that the "SS7" interrupt has not occurred since the last read of this register 1 = Indicates that the "SS7" interrupt has occurred since the last read of this register

TABLE 92: SS7 ENABLE REGISTER FOR LAPD (SS7ER) **HEX ADDRESS: 0XNB11**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
0	SS7_ENB	R/W	0	**SS7 Interrupt Enable for LAPD Controller** This bit enables or disables the "SS7" interrupt within the LAPD Controller. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt when the Received LAPD message is more than 276 Bytes in length. 0 - Disables the "SS7" interrupt within the LAPD Controller. 1 - Enables the "SS7" interrupt within the LAPD Controller.

TABLE 93: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
4	AIS16	RO	0	**AIS 16 State** This bit indicates whether or not the Receive E1 Framer is declaring AIS 16 (Time slot 16 = All Ones Signal) alarm condition. 0 - Indicates the Receive E1 Framer is currently NOT declaring the AIS16 alarm condition. 1 - Indicates the Receive E1 Framer is currently declaring the AIS16 alarm condition.
3	RxLOSINT	RUR/ WC	0	**Change in Receive LOS condition Interrupt Status** This bit indicates whether or not the "Change in Receive LOS condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares the Receive LOS condition. **2.** Whenever the Receive E1 Framer block clears the Receive LOS condition. 0 = Indicates that the "Change in Receive LOS Condition" interrupt has not occurred since the last read of this register. 1 = Indicates that the "Change in Receive LOS Condition" interrupt has occurred since the last read of this register.

TABLE 93: RXLOS/CRC INTERRUPT STATUS REGISTER (RLCISR) **HEX ADDRESS: 0XNB12**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
2	CRCLOCK_INT	RUR/ WC	0	**Change in CRC Multiframe Alignment In-Frame Interrupt Status** This bit indicates whether or not the E1 Receive Framer block has lost or gained CRC Multiframe Alignment since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares CRC Multiframe Alignment LOCK. **2.** Whenever the Receive E1 Framer block declares Loss of CRC Multiframe Alignment. 0 = Indicates that the “Change in CRC Multiframe Alignment In-Frame” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in CRC Multiframe Alignment In-Frame” interrupt has occurred since the last read of this register.
1	CASLOCK_INT	RUR/ WC	0	**Change in CAS Multiframe Alignment In-Frame Interrupt Status** This bit indicates whether or not the E1 Receive Framer block has lost or gained CAS Multiframe Alignments since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares CAS Multiframe Alignment LOCK. **2.** Whenever the Receive E1 Framer block declares Loss of CAS Multiframe Alignment. 0 = Indicates that the “Change in CAS Multiframe Alignment In-Frame” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in CAS Multiframe Alignment In-Frame” interrupt has occurred since the last read of this register.
0	AIS16_INT	RUR/ WC	0	**Change in AIS16 Alarm Condition Interrupt Status** This bit indicates whether or not the “Change in AIS16 Alarm Condition” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive E1 Framer block will generate an interrupt in response to either one of the following conditions. **1.** Whenever the Receive E1 Framer block declares AIS16 (TimeSlot 16 = All Ones) condition. **2.** Whenever the Receive E1 Framer block clears AIS16 (TimeSlot 16 = All Ones) condition. 0 = Indicates that the “Change in AIS16 Condition” interrupt has not occurred since the last read of this register. 1 = Indicates that the “Change in AIS16 Condition” interrupt has occurred since the last read of this register.

TABLE 94: RXLOS/CRC INTERRUPT ENABLE REGISTER (RLCIER) **HEX ADDRESS: 0XNB13**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
3	RxLOS_ENB	R/W	0	**Change in Receive LOS Condition Interrupt Enable** This bit enables the "Change in Receive LOS Condition" interrupt. 0 = Enables "Change in Receive LOS Condition" Interrupt. 1 = Disables "Change in Receive LOS Condition" Interrupt.
2	CRCLOCK_ENB	R/W	0	**Change in CRC Multiframe Alignment In-Frame Interrupt Enable** This bit enables the "Change in CRC Multiframe Alignment In-Frame" interrupt. 0 = Enables "Change in CRC Multiframe Alignment In-Frame" Interrupt. 1 = Disables "Change in CRC Multiframe Alignment In-Frame" Interrupt.
1	CASLOCK_ENB	R/W	0	**Change in CAS Multiframe Alignment In-Frame Interrupt Enable** This bit enables the "Change in CAS Multiframe Alignment In-Frame" interrupt. 0 = Enables "Change in CAS Multiframe Alignment In-Frame" Interrupt. 1 = Disables "Change in CAS Multiframe Alignment In-Frame" Interrupt.
0	AIS16_ENB	R/W	0	**Change in AIS16 Condition Interrupt Enable** This bit enables the "Change in AIS16 (Time Slot 16 = All Ones) Condition" interrupt. 0 = Enables "Change in AIS 16 Condition" Interrupt. 1 = Disables "Change in AIS 16 Condition" Interrupt.

3.0 LIU GLOBAL CONTROL REGISTERS

TABLE 95: LIU GLOBAL CONTROL REGISTER 0 (ADDRESS = 0X0100)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	ATAOS	Reserved				TCLKCNTL	LIU Soft-ware RESET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Reserved:

BIT 6 - ATAOS: Automatic Transmit All Ones Upon RLOS Condition

If ATAOS is selected, an all ones pattern will be transmitted on any channel that experiences an RLOS condition. If an RLOS condition does not occur, TAOS will remain inactive.

0 = Disabled

1 = Enabled

Bits [5:2] - Reserved:

BIT 1 - TCLKCNTL

If TCLKCNTL is selected, and if the transmit clock to the DS-1 framer is missing, Low, or High, then the transmitter outputs to the line interface will send an All Ones Signal.

0 = Disabled

1 = Enabled

BIT 0 - LIU Software RESET:

Writing a 1 to this bit for more than 10µS initiates a device reset for all internal circuits except the microprocessor register bits. To reset the registers to their default setting, use the Hardware Reset pin (See the pin description for more details)

0 = Disabled

1 = Enabled

TABLE 96: LIU GLOBAL CONTROL REGISTER 1 (ADDRESS = 0X0101)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVB_OF	PLL19_Dis	Reserved	Slicer Level Select [1:0]		RXMUTE	EXLOS	ICT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT 7 - Line Code Violation / Counter Overflow Monitor Select

This bit is used to select the monitoring activity between the LCV and the counter overflow status. When the 16-bit LCV counter saturates, the counter overflow condition is activated. By default, the LCV activity is monitored by bit D4 in register 0xN005, where N is equal to the channel number.

} 0 - Monitoring LCV

} 1 - Monitoring the counter overflow status

BIT 6 - PLL 19.44MHz Disable

This bit is used in conjunction with the DS-1/E1 recovered clock to synchronize to a 19.44MHz clock source. If this bit is set High, one of the 28 channel recovered line clocks, or an external line clock and be used to provide this synchronization.

} 0 - Disabled

} 1 - Enabled

BIT 5 - Reserved

BIT [4:3] - Slicer Level Select [1:0]

These bits are to used to select the amplitude level that is used by the receive line interface to determine whether the input data is High or Low.

00 - 50%

01 - 45%

10 - 55%

11 - 68%

BIT 2 - RxMUTE

This bit is used to force the receive DS-1/E1 signals Low to prevent chattering any time that the DS-1/E1 receiver inputs at Rtip/Rring experience an RLOS condition.

} 0 - Disabled

} 1 - Enabled

BIT 1 - EXLOS

The number of zeros required to declare a Digital Loss of Signal is extended to 4,096.

} 0 - Normal RLOS operation

} 1 - EXLOS enabled

BIT 0 - In Circuit Testing

For Internal use only. This bit should be set to Low.

This bit forces all Ingress and Egress signals to be High-Z.

} 0 - Disabled

} 1 - Enabled (Force High-Z)

TABLE 97: LIU GLOBAL CONTROL REGISTER 2 (ADDRESS = 0X0102)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved				CLKSEL[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:4] - Reserved

BIT [3:0] - Input Clock Selection

These bits are used to select the frequency of the input clock source to the PLL. Any state not listed is reserved.

0000 = 2.048 MHz

0001 = 1.544 MHz

1000 = 4.096 MHz

1001 = 3.088 MHz

1010 = 8.192 MHz

1011 = 6.176 MHz

1100 = 16.384 MHz

1101 = 12.352 MHz

1110 = 2.048 MHz

1111 = 1.544 MHz

TABLE 98: LIU GLOBAL CONTROL REGISTER 3 (ADDRESS = 0X0103)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 6	DS1/E1 LIU Global Interrupt Status Channel 5	DS1/E1 LIU Global Interrupt Status Channel 4	DS1/E1 LIU Global Interrupt Status Channel 3	DS1/E1 LIU Global Interrupt Status Channel 2	DS1/E1 LIU Global Interrupt Status Channel 1	DS1/E1 LIU Global Interrupt Status Channel 0
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 0 to 6

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 99: LIU GLOBAL CONTROL REGISTER 4 (ADDRESS = 0X0104)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 13	DS1/E1 LIU Global nterrupt Status Channel 12	DS1/E1 LIU Global nterrupt Status Channel 11	DS1/E1 LIU Global nterrupt Status Channel 10	DS1/E1 LIU Global nterrupt Status Channel 9	DS1/E1 LIU Global nterrupt Status Channel 8	DS1/E1 LIU Global nterrupt Status Channel 7
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 7 to 13

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 100: LIU GLOBAL CONTROL REGISTER 5 (ADDRESS = 0X0105)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global nterrupt Status Channel 20	DS1/E1 LIU Global nterrupt Status Channel 19	DS1/E1 LIU Global nterrupt Status Channel 18	DS1/E1 LIU Global nterrupt Status Channel 17	DS1/E1 LIU Global nterrupt Status Channel 16	DS1/E1 LIU Global nterrupt Status Channel 15	DS1/E1 LIU Global nterrupt Status Channel 14
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 14 to 20

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

TABLE 101: LIU GLOBAL CONTROL REGISTER 6 (ADDRESS = 0X0106)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DS1/E1 LIU Global Interrupt Status Channel 27	DS1/E1 LIU Global Interrupt Status Channel 26	DS1/E1 LIU Global Interrupt Status Channel 25	DS1/E1 LIU Global Interrupt Status Channel 24	DS1/E1 LIU Global Interrupt Status Channel 23	DS1/E1 LIU Global Interrupt Status Channel 22	DS1/E1 LIU Global Interrupt Status Channel 21
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT 7 - Reserved

BIT [6:0] - Global Channel Interrupt Status - Channels 21 to 27

These RUR bit fields are used to indicate which channel experienced a change in status relative to alarm indications. If a channel experiences a change in alarm status, the associated bit for that channel will be set High. Once this register is read back, these bit fields will automatically return Low.

4.0 T1/E1 LIU CHANNEL CONTROL REGISTERS

- **(N ranges from 0x01 to 0x1C)**

TABLE 102: LIU CHANNEL CONTROL REGISTER 0 (ADDRESS = 0XN000)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS/QRSS	PRBS_Rx_Tx	RXON	EQC[4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - PRBS/QRSS:

These bits are used to select between QRSS and PRBS. To send the a QRSS or PRBS pattern, the TxTEST[2:0] bits in register 0xN002h must be programmed.

} 0 = QRSS

} 1 = PRBS

BIT6 - PRBS/QRSS Direction Select Rx/Tx:

This bit is used to select which direction is used to send the PRBS/QRSS pattern if enabled within the TxTEST[2:0] bits in register 0xN002h.

} 0 = Line Interface (Ttip/Tring)

} 1 = System Side Interface (Clock/Data)

BIT 5 - RXON Receiver Enable:

This bit is used enable the receiver line interface. By default, the receivers are turned off to support redundancy.

} 0 = Disabled.

} 1 = Enabled.

BIT [4:0] - Equalizer Control and Line Build Out:

These bits are used to select the equalizer control and line build out.

Selection Chart for Equalizer Control and Line Build-Out

EQC[4:0]	T1/E1 MODE RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
01000	T1 Short Haul	0 - 133 Ft (0.6dB)	100Ω TP	B8ZS
01001	T1 Short Haul	133 - 266 Ft (1.2dB)	100Ω TP	B8ZS
01010	T1 Short Haul	266 - 399 Ft (1.8dB)	100Ω TP	B8ZS
01011	T1 Short Haul	399 - 533 Ft (2.4dB)	100Ω TP	B8ZS
01100	T1 Short Haul	533 - 655 Ft (3.0dB)	100Ω TP	B8ZS
01101	T1 Short Haul	Arbitrary Pulse	100Ω TP	B8ZS
10000	T1 Short Haul	0dB	100Ω TP	B8ZS
10001	T1 Short Haul	-7.5dB	100Ω TP	B8ZS
10010	T1 Short Haul	-15dB	100Ω TP	B8ZS
10011	T1 Short Haul	-22dB	100Ω TP	B8ZS
11100	E1 Short Haul	ITU G.703	75Ω Coax	HDB3
11101	E1 Short Haul	ITU G.703	120Ω TP	HDB3

TABLE 103: LIU CHANNEL CONTROL REGISTER 1 (ADDRESS = 0XN001)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTSEL	TxTSEL	TERSEL[1:0]		JASEL[1:0]		JABW	FIFOSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - RxTSEL:

This bit is used for the receive line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

} 0 = External Impedance

} 1 = Internal Impedance

BIT6 - TxTSEL:

This bit is used for the transmit line interface to select between Internal (automatic line impedance) and External (high impedance) modes.

} 0 = External Impedance

} 1 = Internal Impedance

BIT [5:4] - TERSEL[1:0]:

These bits are used to select the line impedance for internal termination control.

} 00 = 100Ω

} 01 = 110Ω

} 10 = 75Ω

} 11 = 120Ω

BIT [3:2] - JASEL[1:0]:

These bits are used to select which path the Jitter Attenuator is placed.

} 00 = Disabled.

} 01 = Transmit Line Interface Path

} 10 = Receive Line Interface Path

} 11 = Receive Line Interface Path

BIT 1 - Jitter Attenuator Band Width:

The jitter band width is a global setting that is applied in both transmit and receive directions.

} 0 = 10 Hz

} 1 = 1.5 Hz

BIT 0 - First In First Out Bit Depth:

This bit is used to select the depth of the FIFO within both the Receive and Transmit Jitter Attenuators.

} 0 = 32-Bit FIFO

} 1 = 64-Bit FIFO

TABLE 104: LIU CHANNEL CONTROL REGISTER 2 (ADDRESS = 0XN002)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INVQRSS	TxTEST[2:0]			TXON	LOOP[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Invert QRSS:

INVQRSS is used to invert the transmit QRSS pattern set by the TxTEST[2:0] bits. By default, INVQRSS is disabled and the QRSS will be transmitted with normal polarity.

} 0 = Standard QRSS pattern

} 1 = Inverted QRSS pattern

BIT [6:4] - Tx Test Pattern [2:0]:

These bits are used to select a Test Pattern to be sent to the transmit line interface. If bit 6 in register 0xN000h is set High, then the Test Pattern will be sent out on the receive DS-1/E1 system side.

} 0XX = No Test Pattern

} 100 = Tx QRSS

} 101 = Tx TAOS

} 110 = Reserved

} 111 = Reserved

BIT 3 - TXON Transmitter Enable:

This bit is used enable the transmitter line interface. By default, the transmitters are turned off to support redundancy.

} 0 = Disabled.

} 1 = Enabled.

BIT [2:0] - Loop Back Mode Select [2:0]:

These bits are used to select a loop back mode for diagnostic testing. These bits only represent the loop back modes supported in the LIU section of Voyager. For other loop back mode options, see the register map in other modes of operation.

} 0XX = No Loop Back

} 100 = Dual Loop Back

} 101 = Analog Loop Back

} 110 = Remote Loop Back

} 111 = Digital Loop Back

TABLE 105: LIU CHANNEL CONTROL REGISTER 3 (ADDRESS = 0XN003)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxRES[1:0]		CODES	Reserved	E1ARBIT	INSBPV	INSBER	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT [7:6] - Receiver Fixed External Termination:

RxRES[1:0] are used to select the value for a high precision external resistor to improve return loss.

} 00 = None

} 01 = 240Ω

} 10 = 210Ω

} 11 = 150Ω

BIT 5 - CODES Encoding / Decoding Select:

This bit is used to select the type of encoding/decoding the transmitter and receiver will generate/process.

} 0 = HDB3 (E1), B8ZS (T1)

} 1 = AMI Coding

BIT 4 - Reserved:

BIT 3 - E1Arbitrary Pulse Select:

This bit is used to enable the Arbitrary Pulse Generator for shaping the transmit pulse when E1 mode is selected.

} 0 = Disabled (Normal E1 Pulse Shape ITU G.703)

} 1 = Arbitrary Pulse Enabled

BIT 2 - Insert Bipolar Violation:

When this bit transitions from Low to High, a bipolar violation will be inserted in the transmitted data from TPOS, QRSS/ PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

} 0 to 1 Transition = Insert one bipolar violation

BIT 1 - Insert Bit Error:

When this bit transitions from Low to High, a bit error will be inserted in the transmitted QRSS/PRBS pattern. The state of this bit will be sampled on the rising edge of TCLK. To ensure proper operation, it is recommended to write a 0 to this bit before writing a 1.

} 0 to 1 Transition = Insert one bit error

BIT 0 - Reserved:

TABLE 106: LIU CHANNEL CONTROL REGISTER 4 (ADDRESS = 0XN004)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIE	FLSIE	LCVIE	Reserved	AISDIE	RLOSIE	QRPDIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

} 0 = Masks the DMO function

} 1 = Enables interrupt generation for DMO

BIT 5 - FIFO Limit Status Interrupt Enable:

} 0 = Masks the FLS function

} 1 = Enables interrupt generation for FLS

BIT 4 - Line Code Violation Interrupt Enable:

} 0 = Masks the LCV function

} 1 = Enables interrupt generation for LCV

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

} 0 = Masks the AIS function

} 1 = Enables interrupt generation for AIS

BIT 1 - Receive Loss of Signal Interrupt Enable:

} 0 = Masks the RLOS function

} 1 = Enables interrupt generation for RLOS

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

} 0 = Masks the QRPD function

} 1 = Enables interrupt generation for QRPD

TABLE 107: LIU CHANNEL CONTROL REGISTER 5 (ADDRESS = 0XN005)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMO	FLS	LCV	Reserved	AISD	RLOS	QRPD
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT6 - Digital Monitor Output:

This bit indicates the DMO activity. An interrupt will not occur unless the DMOIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = Transmit output driver has failures

BIT 5 - FIFO Limit Status:

This bit indicates whether the RD/WR pointers are within 3-Bits. An interrupt will not occur unless the FLSIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = RD/WR FIFO pointers are within ±3-Bits

BIT 4 - Line Code Violation:

This bit serves a dual purpose. By default, this bit monitors the line code violation activity. However, if bit 7 in register 0x0101h is set High, this bit monitors the overflow status of the internal LCV counter. An interrupt will not occur unless the LCV/OFIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = A line code violation, bipolar violation, or excessive zeros has occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal:

This bit indicates the AIS activity. An interrupt will not occur unless the AISIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = An all ones signal is detected

BIT 1 - Receive Loss of Signal:

This bit indicates the RLOS activity. An interrupt will not occur unless the RLOSIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = An RLOS condition is present

BIT 0 - Quasi Random Pattern Detection:

This bit indicates that a QRPD has been detected. An interrupt will not occur unless the QRPDIE is set High in register 0xN004h and the global interrupt enable has been set.

} 0 = No Alarm

} 1 = A QRP is detected

TABLE 108: LIU CHANNEL CONTROL REGISTER 6 (ADDRESS = 0XN006)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	DMOIS	FLSIS	LCVIS	Reserved	AISDIS	RLOSIS	QRPDIS
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NOTE: These register bits are Reset Upon Read. They will be set High anytime a change in status occurs. Once these bits are read back, they will automatically be set Low.

BIT7 - Reserved:

BIT6 - Digital Monitor Output Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 5 - FIFO Limit Status Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 4 - Line Code Violation Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 3 - Reserved:

BIT 2 - Alarm Indication Signal Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 1 - Receive Loss of Signal Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

BIT 0 - Quasi Random Pattern Detection Interrupt Enable:

} 0 = No change

} 1 = Change in status occurred

TABLE 109: LIU CHANNEL CONTROL REGISTER 7 (ADDRESS = 0XN007)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ENROM	Reserved	Reserved	RST	UPDATE	HI/LO	UPDATE	RST
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Enable ROM for LCV Counter:

This bit is used to enable data from an internal LCV counter to be read back.

} 0 = Disabled.

} 1 = Enabled.

BIT [6:5] - Reserved:

BIT 4 - Reset Internal LCV Counter:

This bit is used to reset the Internal LCV counters for this channel to its default state 0000h. This bit must be set High for a minimum of 1mS.

} 0 = Normal Operation

} 1 = Reset LCV Counter

BIT 3 - Update LCV Counter:

This bit is used to latch the contents of the internal LCV counter for this channel so that the values can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

} 0 = Normal Operation

} 1 = Updates LCV Counter

BIT 2 - High Byte / Low Byte Select:

This bit is used to select which byte of the 16-bit LCV value will be placed in the read back registers.

} 0 = Lower Byte LCV[7:0]

} 1 = Upper Byte LCV[15:8]

BIT 1 - Update LCV Counter:

This bit is used to latch the contents of the internal LCV counter for this channel so that the value can be read. When the HI/LO bit is set Low, initiating this update bit places the lower 8 bits of the 16-bit word in register 0xN011h. When the HI/LO bit is set High, initiating this update bit places the upper 8 bits of the 16-bit word in register 0xN010h.

} 0 = Normal Operation

} 1 = Update LCV Counter

BIT 0 - Reset Internal LCV Counter:

This bit is used to reset the Internal LCV counters for this channel to its default state 0000h. This bit must be set High for a minimum of 1mS.

} 0 = Normal Operation

} 1 = Reset LCV Counter

TABLE 110: LIU CHANNEL CONTROL REGISTER 8 (ADDRESS = 0XN008)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S1	B5S1	B4S1	B3S1	B2S1	B1S1	B0S1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 1:

The transmit output pulse is divided into 8 individual segments. This register is used to program the first segment which corresponds to the overshoot of the pulse amplitude. There are four segments for the top portion of the pulse and four segments for the bottom portion of the pulse. Segment number 5 corresponds to the undershoot of the pulse. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 111: LIU CHANNEL CONTROL REGISTER 9 (ADDRESS = 0XN009)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S2	B5S2	B4S2	B3S2	B2S2	B1S2	B0S2
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 2:

The transmit output pulse is divided into 8 individual segments. This register is used to program the second segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 112: LIU CHANNEL CONTROL REGISTER 10 (ADDRESS = 0XN00A)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S3	B5S3	B4S3	B3S3	B2S3	B1S3	B0S3
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 3:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Third segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 113: LIU CHANNEL CONTROL REGISTER 11 (ADDRESS = 0XN00B)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S4	B5S4	B4S4	B3S4	B2S4	B1S4	B0S4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 4:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fourth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 114: LIU CHANNEL CONTROL REGISTER 12 (ADDRESS = 0XN00C)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S5	B5S5	B4S5	B3S5	B2S5	B1S5	B0S5
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 5:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Fifth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 115: LIU CHANNEL CONTROL REGISTER 13 (ADDRESS = 0XN00D)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S6	B5S6	B4S6	B3S6	B2S6	B1S6	B0S6
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 6:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Sixth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 116: LIU CHANNEL CONTROL REGISTER 14 (ADDRESS = 0XN00E)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S7	B5S7	B4S7	B3S7	B2S7	B1S7	B0S7
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 7:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Seventh segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 117: LIU CHANNEL CONTROL REGISTER 15 (ADDRESS = 0XN00F)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	B6S8	B5S8	B4S8	B3S8	B2S8	B1S8	B0S8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT7 - Reserved:

BIT [6:0] - Arbitrary Pulse Generation Segment 8:

The transmit output pulse is divided into 8 individual segments. This register is used to program the Eighth segment of the pulse amplitude. The MSB of each segment is the sign bit.

- **If Sign Bit (BIT6) =:**

} 0 - Negative Direction

} 1 - Positive Direction

TABLE 118: LIU CHANNEL CONTROL REGISTER 16 (ADDRESS = 0XN010)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVHI7	LCVHI6	LCVHI5	LCVHI4	LCVHI3	LCVHI2	LCVHI1	LCVHI0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter High Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the upper byte of the 16-bit LCV counter word.

TABLE 119: LIU CHANNEL CONTROL REGISTER 17 (ADDRESS = 0XN011)

BIT7	BIT6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LCVLO7	LCVLO6	LCVLO5	LCVLO4	LCVLO3	LCVLO2	LCVLO1	LCVLO0
RO	RO	RO	RO	RO	RO	RO	RO
0	0	0	0	0	0	0	0

BIT [7:0] - Internal LCV Counter Low Byte:

Once the internal LCV counter has been enabled and updated, these bits contain the lower byte of the 16-bit LCV counter word.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	May 2008	Final release datasheet of the XRT86SH328 E1 Framer + LIU Register Description.
1.0.1	August 2008	Updated bit register description 0x0101, 0xN001, 0xN003, 0xN129.