## GENERAL DESCRIPTION

The XRT86SH328 (Voyager) is a physical layer SONET/SDH to PDH mapper/demapper which enables T1/E1 aggregation to STS-3/STM-1 or STS1/STM0 via standard VT1.5/VT2 or VC-11/VC-12 to AU-3 and TUG-3/AU-4 mapping protocols. Voyager supports all the framing, mapping and grooming functions required for STS-3/STM-1 mapper applications. The device generates and terminates all SONET/SDH Regenerator Section, Multiplexer Section and Path Overhead including the low-order Virtual Container (VC) Path Overhead. T1/E1 framing is transparent; therefore, the device neither generates nor terminates the E1 frame.

A single Voyager performs mapping of 28 aysnchrounous T1 spans to VT1.5/STS-1 in SONET or VC-11/TU-11/TUG-2/VC-3/AU-3/STM-0 in SDH. The Voyager can also alternatively map 21 asynchronous E1 spans to VT2/STS-1 or VC-12/TU-12/TUG-2/VC-3/AU-3/STM-0. Mapping to STS-3/STM-1 requires (3) Voyager devices with one acting as "master" framer and two acting as "slave" framers. In this configuration, Voyager performs all the necessary framing, pointer processing and mapping functions required for mapping 84 x T1 spans to VT1.5/STS-1/STS-3 in SONET or either VC11/TU11/TUG-2/VC-3/AU-3/STM1 or VC-11/TU-11/TUG-2/TUG-3/VC-4/AU-4/STM-1 in SDH. Alternatively, 63 x E1 spans can also be map to VT2/STS-1/STS-3 in SONET or either VC-12/TU-12/TUG-2/VC-3/AU-3/STM-1 or VC-12/TU-12/TUG-2/TUG-3/VC-4/AU-4/STM-1 in SDH.

FIGURE 1. SIMPLIFIED BLOCK DIAGRAM
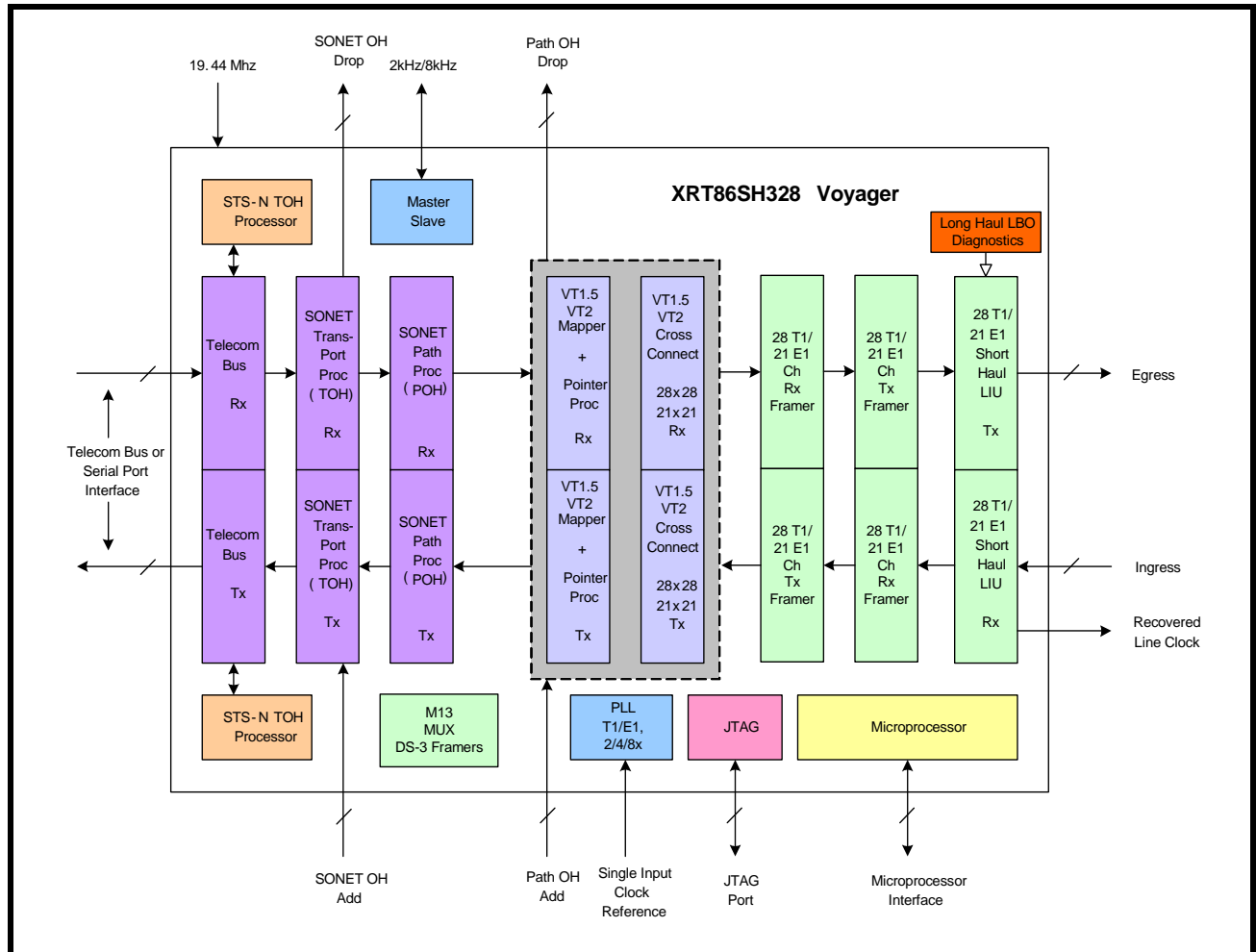
PACKAGE ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT86SH328IB	568 PBGA-TEP	-40℃ to +85℃

FEATURES

VT Mapper

- Maps up to 28 synchronous or asynchronous T1 signals to SONET STS-1 SPE (Synchronous Payload Envelope) via VT1.5 Virtual Tributaries or to SDH STM-0 AU-3 payload capacity via TUG-2 and TU-11 Tributary Groups.

- Maps up to 21 synchronous or asynchronous E1 signals to SONET STS-1 SPE (Synchronous Payload Envelope) via VT2 Virtual Tributaries or to SDH STM-0 AU-3 payload capacity via TUG-2 and TU-12 Tributary Groups.

- Dynamic VT/TU size selection.

- Inserts valid V5 bit interleaved parity BIP-2 in the transmit direction.

- Detects and counts V5 BIP-2 errors for performance monitoring.

- Configurable remote error indication REI-V/LP-REI insertion for V5 BIP-2 errors.

- Supports proprietary V5 remote loopcodes.

- Detects and counts remote errors.

- Automatic receive monitor functions include VT/TU remote defect indication RDI-V/LP-RDI, VT/TU remote failure indication RFI-V/LP-RFI, VT/TU remote error indication REI-V/LP-REI, BIP-2 errors, VT/TU AIS, VT/TU Automatic Protection Switching (APS) signalling for low order path level, and VT/TU loss of pointer LOP-V/LP-LOP.

- Automatic receive monitoring functions can be configured to provide an interrupt to the control system, or the device can be operated in a polled mode.

- Test pattern generation and detection/dropping for setup and maintenance.

- User configurable for VT/TU label, AIS-V/LP-AIS, RDI-V/LP-RDI, RFI-V/LP-RFI, REI-V/LP-REI, APS, force BIP-2 errors, or unequipped tributary insertion.

T1 Framing Synchronizer

- Fifty-Six independent, full duplex T1 Tx and Rx Framer/LIUs

- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx

- Supports Robbed Bit Signaling (RBS)

- Supports ISDN Primary Rate Interface (ISDN PRI) signaling

- Integrated HDLC controller per channel for transmit and receive, each controller having two 64-byte buffers (buffer 0 / buffer 1)

- HDLC Controllers Support SS7

- Timeslot assignable HDLC

- Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission

- Alarm Indication Signal with Customer Installation signature (AIS-CI)

- Remote Alarm Indication with Customer Installation (RAI-CI)

- Gapped Clock interface mode for Transmit and Receive.

- Parallel search algorithm for fast frame synchronization

- Direct access to D and E channels for fast transmission of data link information

● PRBS, QRSS, and Network Loop Code generation and detection

● Each framer block encodes and decodes the T1 Frame serial data

● Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms

● Detects OOF, LOF, LOS errors and COFA conditions

● Loopbacks: Local (LLB) and Line remote (LB)

● Performance monitor with one second polling

● Accepts external 8kHz Sync reference

E1 Framing Synchronizer

● Forty-Two independent, full duplex E1 Tx and Rx Framer/LIUs

● Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx

● Supports Channel Associated Signaling (CAS)

● Supports Common Channel Signalling (CCS)

● Supports ISDN Primary Rate Interface (ISDN PRI) signaling

● Integrated HDLC controller per channel for transmit and receive, each controller having two 64-byte buffers (buffer 0 / buffer 1)

● HDLC Controllers Support SS7

● Timeslot assignable HDLC

● V5.1 or V5.2 Interface

● Automatic Performance Report Generation (PMON Status) can be inserted into the transmit LAPD interface every 1 second or for a single transmission

● Alarm Indication Signal with Customer Installation signature (AIS-CI)

● Remote Alarm Indication with Customer Installation (RAI-CI)

● Gapped Clock interface mode for Transmit and Receive.

● Parallel search algorithm for fast frame synchronization

● Direct access to D and E channels for fast transmission of data link information

● PRBS, QRSS, and Network Loop Code generation and detection

● Each framer block encodes and decodes the E1 Frame serial data

● Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms

● Detects OOF, LOF, LOS errors and COFA conditions

● Loopbacks: Local (LLB) and Line remote (LB)

● Performance monitor with one second polling

● Accepts external 8kHz Sync reference

SONET/SDH Transmitter

- Performs standard STS1/STS3 or STM-0/STM-1 transmit processing.

- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253

- Provides a 51.84MHz STS1/STM-0 serial LVCMOS/LVTTL interface or 6MHz/19MHz 8-bit STS1/STS3 or STM-0/STM-1 telecom bus parallel interface.

- Performs SONET/SDH frame insertion and accepts external frame synchronization.

- Performs optional transmit data scrambling.

- Performs POH/HP, SONET/SDH OH generation/insertion.

- Generates transmit payload pointer (H1, H2) (fixed at 522) with NDF insertion.

- Inserts A1/A2 with optional error mask.

- Computes and inserts BIP-8 (B1, B2) with optional error mask.

- Generates AIS-L/HP-AIS, REI-L/HP-REI and RDI-L/HP-RDI according to receiver state with option of SW or HW insertion.

- Inserts LOS, forces SEF by software.

- Generates RDI-P/LP-RDI and REI-P/LP-REI automatically with optional SW or HW override.

- Inserts fixed-stuff columns, calculates and inserts B3 error code.

SONET/SDH Receiver

- Performs standard STS1/STS3 or STM-0/STM-1 receive processing.

- Conforms to ITU-T I.432, ANSI T1.105, and Bellcore-253.

- Provides fully programmable threshold detection for SD and SF conditions.

- Provides a 51.84MHz STS1/STM-0 serial LVCMOS/LVTTL interface or 6MHz/19MHz 8-bit STS1/STS3 or STM-0/ STM-1 telecom bus parallel interface.

- Provides Section Trace buffer with mismatch detection and invalid message detection.

- Performs SONET/SDH frame synchronization.

- Supports NDF, positive stuff and negative stuff for pointer processor.

- Performs receive data de-scrambling.

- Performs POH/HP, SONET/SDH OH interpretation/extraction.

- Interprets payload pointer (H1, H2).

- Detects Out Of Frame (OOF), Loss Of Frame (LOF), Loss Of Signal (LOS), APS failure.

- Detects Line Alarm Indication(L-AIS/HP-AIS), Line remote Defect Indication (L-RDI/HP-RDI), Loss Of Pointer.

- Detects Path/High-Order Path Alarm Indication Signal, Remote Defect Indication, Extended RDI.

- Provides C2 byte signal label monitor with Payload Loss Mismatch (PLM-P/HP-PLM) detection.

- Supports Path/High Order Trace buffer with Trace Identifier Mismatch (TIM-P/HP-TIM) and invalid message detection.

- Computes and compares B3, REI-L/HP-REI and REI-P/LP-REI errors.

- Computes and compares BIP-8 (B1, B2) and counts the errors.

TABLE OF CONTENTS

1.0 PIN DESCRIPTIONS

1.1 *MICROPROCESSOR INTERFACE PINS*

568 Ball	Pin Name	Type	Description
L30 M29 M30 N28 N29 P29 R30 R27 R28 T29 T27 U29 U28 V29 W30 W29 V27 AA30	A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I	**Address Input Pins** These address input pins are used for the microprocessor interface to the XRT86SH328. For timing information, please refer to the timing diagrams in the Electrical Specifications section of this datasheet.
N27 P26 P27 R29 T30 T26 U27 U26	D7 D6 D5 D4 D3 D2 D1 D0	I/O	**Bi-Directional Data Bus Pins** These bi-directional data bus pins are used for the microprocessor interface to the XRT86SH328. For timing information, please refer to the timing diagrams in the Electrical Specifications section of this datasheet.
V30	ALE / AS	I	**Address Latch Enable / Address Strobe** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
U30	CS	I	**Chip Select Input**
N30	INT	O	**Interrupt Request Output** This active-low output signal will be asserted any time the XRT86SH328 is requesting interrupt service from the microprocessor. *NOTE: This output pin is open-drain and requires a 10kΩ pull-up resistor.*
V28	RD / DS / WE	I	**Read Strobe / Data Strobe** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
Y30	WR / R/W	I	**Write Strobe / Read-Write Operation Identifier** The function of this input pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.
R26	RDY / Dtack / TA	O	**Ready or DTACK Output** The function of this output pin depends on the microprocessor interface mode. See the microprocessor section for timing diagrams.

1.1   *MICROPROCESSOR INTERFACE PINS*

568 BALL	PIN NAME	TYPE	DESCRIPTION
P1	Reset	I	**Hardware Reset** It is recommended to initiate a HW reset upon power up before configuring the device. This pin must be pulled "Low" for a minimum of 10μS to activate the reset circuitry. During a HW reset, all outputs will be tri-stated and all on-chip registers will be reset to their default values.Note: This pin has an internal 10kΩ pull-up resistor.
T28	PCLK	I	**Microprocessor Interface Clock Input** This input clock signal is only used for the synchronous microprocessor interface modes. This pin is ignored in the asynchronous microprocessor interface mode.Note: The input frequency range of PCLK is 66MHz.
AF3 AG2 AH1	PTYPE2 PTYPE1 PTYPE0	I	**Microprocessor Type Select Inputs** These input pins are used to select the microprocessor mode according to the following table: <table><tr><th>PTYPE[2:0]</th><th>Microprocessor Interface Mode</th></tr><tr><td>000</td><td>Intel Asynchronous</td></tr><tr><td>001</td><td>Motorola Asynchronous</td></tr><tr><td>101</td><td>Power PC 403</td></tr><tr><td>111</td><td>MPC86x</td></tr></table>
P30	DBEN	I	**Data Bus Enable** This active-low input pin is used to enable the bi-directional data bus. To disable the data bus, this pin must be pulled "High". For normal operation, this pin should be pulled "Low".
T5	EXT_INT_1	I/O	**External Interrupt Input 1/Recovered Line Clock Ouptut** <u>Input:</u> This pin can be used to force an interrupt request to the microprocessor by pulling this pin "High". The interrupt will be generated within a dedicated internal register and on the INT output pin. <u>Output:</u> This pin can output one of the 28 channel recovered line clocks selected by register 0x004E. See RCLK_IO pin for the second recovered line clock that's available. ***NOTE:** If not used, this pin should be "left floating".*
T3	EXT_INT_0	I	**External Interrupt Input 0** This pin can be used to force an interrupt request to the microprocessor by pulling this pin "High". The interrupt will be generated within a dedicated internal register and on the INT output pin. If the XRT86SH328 is used to generate a 19.44MHz output clock (with an external VCXO), then this pin should be connected to the output of the VCXO so that the internal LIU can complete the PLL loop. ***NOTE:** If not used, this pin should be pulled "Low".*

1.1   *MICROPROCESSOR INTERFACE PINS*

568 BALL	PIN NAME	TYPE	DESCRIPTION
W27	$\overline{REQ1}$	O	**DMA Cycle Request Output - DMA Controller 1 (Read)** This output pin is used to indicate that DMA transfers (Read) are requested by a given Receive DS1/E1 Framer block. The DMA Read cycle starts by asserting the DMA Request $\overline{REQ1}$ output pin "Low". The DMA Controller should then respond by asserting the $\overline{ACK1}$ input pin by pulling it "Low" to indicate that it is ready to accept data. The Receive DS1/E1 Framer block should then place new data on the Microprocessor Data Bus, each time the READ signal is asserted.
Y29	$\overline{REQ0}$	O	**DMA Cycle Request Output - DMA Controller 0 (Write)** This output pin is used to indicate that the DMA transfers (Write) are requested by a given Transmit DS1/E1 Framer block. The DMA Write cycle starts by asserting the DMA Request $\overline{REQ0}$ "Low". In response, the DMA Controller should then assert the $\overline{ACK0}$ (DMA Acknowledge) input pin by toggling it "Low" to indicate that it is ready to start the transfer. The external DMA Controller should then place new data on the Microprocessor Data bus each time the Write Signal is asserted.
AA29	$\overline{ACK1}$	I	**DMA Cycle Acknowledge Input - DMA Controller 1 (Read)** The external DMA Controller should assert this input pin by pulling it "Low" after the internal DMA Controller has asserted the $\overline{REQ1}$ output signal. After completion of the DMA cycle, the external DMA Controller should de-assert this input pin after the $\overline{REQ\_1}$ output pin has been de-asserted. *Note: Internally pulled "High".*
W28	$\overline{ACK0}$		**DMA Cycle Acknowledge Input - DMA Controller 0 (Write)** The external DMA Controller should assert this input pin by pulling it "Low" after the Internal DMA Controller asserted the $\overline{REQ0}$ output signal. After completion of the DMA cycle, the external DMA Controller should de-assert this input pin after the $\overline{REQ0}$ output pin has been de-asserted. *Note: Internally pulled "High".*
P28	BLAST	I	**Reserved** This pin can be left floating or tied to ground.

1.2   BOUNDARY SCAN AND OTHER TEST PINS

568BALL	PIN NAME	TYPE	DESCRIPTION
JTAG Test Pins			
F4	TCK	I	**Test Clock Input** This pin is used for the boundary scan clock input. For normal operation, this pin should be pulled "Low".
H6	TDI	I	**Test Data Input** This pin is used for the boundary scan input data signal. For normal operation, this pin should be pulled "High". *NOTE: Internally Pulled "High" with a 50kΩ pull-up resistor.*
E4	TDO	O	**Test Data Output** This pin is used for the boundary scan output data signal.
C2	TMS	I	**Test Mode Select** This pin is used for the boundary scan test mode select input signal. For normal operation, this pin should be pulled "High". *NOTE: Internally Pulled "High" with a 50kΩ pull-up resistor.*
G5	TRST	I	**Test Mode Reset** This pin is used for the boundary scan reset input signal. For normal operation, this pin should be pulled "High". *NOTE: Internally Pulled "High" with a 50kΩ pull-up resistor.*
Analog Continuity and Test Pins			
R4	TESTMODE	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
L1	SCAN_MODE	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
AD5	SCAN_ENB	I	**For Factory Use Only** For normal operation, this pin must be pulled "Low".
C15 E15	ATP_RING1 ATP_TIP1	I/O	**Analog Test Point - TIP/RING 1** These pins along with the TMS and TCK boundary scan pins are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with channels 0 through 13 for T1 test operation (channel 0 through 10 for E1 test operation). *NOTE: If not used, these pins should be left floating.*
AF15 AJ14	ATP_RING2 ATP_TIP2	I/O	**Analog Test Point - TIP/RING 2** These pins along with the TMS and TCK boundary scan pins are used to perform continuity checks between the TTIP/TRING and RTIP/RRING pins associated with channels 14 through 27 for T1 test operation (channel 11 through 21 for E1 test operation). *NOTE: If not used, these pins should be left floating.*
D15 AH14	ANALOG1 ANALOG2	O	**For Factory Use Only** These pins should be left floating
A14 AG14	SENSE1 SENSE2	O	**For Factory Use Only** These pins should be left floating

1.3 GENERAL PURPOSE INPUT AND OUTPUT PINS

568 BALL	PIN NAME	TYPE	DESCRIPTION
GPIO Pins			
H5 D2 G4 C1 AC5 AD4 AE3 AF2	GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0	I/O	**General Purpose I/O** Each of these pins can be configured to function as either a general purpose input or output pin by programming the GPIO registers outlined in the register map. One register is used to set the direction of each pin, while the other register is used to Read/Write the value of each pin dependent on its direction. *NOTE: If not used, these pins should be left floating.*

1.4 TIMING AND CLOCK SIGNALS

568 BALL	PIN NAME	TYPE	DESCRIPTION
Timing and Clock Pins			
E3	MCLK	I	**Master Clock PLL Reference Input Clock** This input functions as the reference input pin to the PLL master clock and can accept any of the following signals by programming the appropriate internal register. 1.544/ 2.048 / 3.088/ 4.096 / 6.176/ 8.192 / 13.352/ 16.384 MHz.
F5	EXT_OSC_ENB	I	**External Oscillator Enable** This pin must be pulled "Low".
R1	EXT_OSC	I	**External Oscillator** This pin must be pulled "Low".
R3	TX51_19MHZ	I	**Transmit STS-3/STM-1 Timing Reference Input** The function of this pin depends upon which mode the XRT86SH328 has been configured to operate in. **SONET/SDH Over Serial Interface (STS-1/STM-0 Only)** In this case, the XRT86SH328 will be configured to transmit data at a rate of 51.84MHz on the system side serial interface. Provide a 51.84MHz clock signal to this pin. The Transmit STS-1/STM-0 POH and TOH Processor blocks will use this clock signal as its timing reference. **SONET/SDH Over Telecom Bus Interface** In this case, the XRT86SH328 will be configured to output either an STS-3/STM-1 or STS-1/STM-0 signal via the Transmit Telecom Bus Interface. Provide a 19.44MHz clock signal to this pin for STS-3/STM-1 or a 6.48MHz clock for STS-1/STM-0 applications. The Transmit POH and TOH Processor blocks will use this clock signal as its timing reference.

1.4   TIMING AND CLOCK SIGNALS

568 BALL	PIN NAME	TYPE	DESCRIPTION
P5	TxSBFP_IN_OUT	I/O	**Transmit System Bus Frame Pulse Input / Output** The direction of this frame pulse is determined by whether the XRT86SH328 is the Master of Slave device in STS-3/STM-1 shared Telecom Bus applications whereby three Voyager devices are connected together. **If the XRT86SH328 (along with two other XRT86SH328 devices) is configured to exchange STS-3/STM-1 data over a common Telecom Bus, and this particular device is the Master Device - TxSBFP_OUT:** The Master XRT86SH328 will pulse this output pin "High" when it outputs the very first A1 byte (of a given outbound STS-3/STM-1 frame) via the Transmit Telecom Bus Interface. This pin will be kept "Low" at all other times. **If the XRT86SH328 (along with two other XRT86SH328 devices) is configured to exchange STS-3/STM-1 data over a common Telecom Bus, and this particular device is the Slave Device - TxSBFP_IN:** The Transmit TOH Processor Block (within a given slave device) can be configured to initiate its generation of a new outbound STS-3/STM-1 frame based upon an externally supplied 8kHz clock signal to this input pin. The Transmit Telecom Bus Interface will begin transmitting the very first byte of a given STS-3/STM-1 frame, upon sensing a rising edge of the 8kHz/2kHz signal on this pin.
19.44Mhz Reference Pins			
E20	VCT_1944	O	**19.44MHz Output Clock Reference for Recovered Clock Synchronization** The purpose of this clock is to provide a 19.44MHz clock that is synchronous to either an externally provided clock (to Pin C9) or to one of the 28 selectable recovered line clocks from the LIU. See Register 0x004F. If this pin is used, it must source an external VCXO and the output of the VCXO must feed back to Pin T3 (EXT_INT_0) so that the internal LIU can complete the PLL loop.
A25	Is_T1_E1B	I	**Recovered Clock Frequency Select** This input signal is used to indicate the frequency of the RCLK_IO pin if RCLK_IO is configured as an input. "Low" = E1, "High" = T1.
C9	RCLK_IO	I/O	**Recovered Clock Input/Output:** This bi-directional clock can be used in two different modes: 1. As an input, the LIU will use this clock as its internal clock timing synchronization of the 19.44Mhz clock reference (Pin E20, VCT_1944). 2. As an output, it is one of 28 recoverd line clocks selected by the Recovered Clock Select [4:0] bits and output through this pin. See Register 0x004F.
M13 MUX Clock Pins (If this mode is not used, tie input pins to GND and leave output pins floating)			
R2	Tx44MHzCLK	I	**Transmit DS3 Timing Reference Input** This input functions as the reference input pin to the M13 MUX PLL master clock and can accept 44.736MHz +/-20ppm. ***NOTE:*** *This pin is only used in the M13 MUX modes. If not used, tie this pin to GND.*

1.4 TIMING AND CLOCK SIGNALS

568 BALL	PIN NAME	TYPE	DESCRIPTION
T4	DS2INCLK	I	**Receive DS2 Clock Input** Either tie this input clock pin to the DS2OUTCLK signal (Pin T2), or supply a 6.312MHz clock externally. **NOTE:** *This pin is only used in the M13 MUX modes. If not used, tie this pin to GND.*
T2	DS2OUTCLK	O	**Transmit DS2 Clock Output** The output signal will be a 6.312MHz clock generated from the internal M13 MUX PLL.

1.5   LOW SPEED LINE INTERFACE SIGNALS

568 Ball	Pin Name	Type	Description
T1/E1 Receive Line Interface Signals			
AG27	RTIP27	I	**Receive T1/E1 Line Input - Positive Polarity Signal**
AG25	RTIP26		RTIP and RRING are differential analog input pins that receive standard T1/E1
AJ26	RTIP25		Return-to-Zero data, coupled through a 1:1 transformer. The transformer blocks
AG22	RTIP24		the DC line bias and allows the inputs to be level shifted to mid-power supply.
AH21	RTIP23		*NOTE: It is recommended to use a transfomer with a center tap pin connected*
AH19	RTIP22		*to ground through a 0.1μF capacitor.*
AK18	RTIP21		
AH12	RTIP20		
AK8	RTIP19		
AK6	RTIP18		
AJ5	RTIP17		
AK2	RTIP16		
AF6	RTIP15		
AE5	RTIP14		
A1	RTIP13		
A2	RTIP12		
F9	RTIP11		
A5	RTIP10		
D10	RTIP9		
D12	RTIP8		
C13	RTIP7		
E17	RTIP6		
E18	RTIP5		
C22	RTIP4		
C24	RTIP3		
E23	RTIP2		
F23	RTIP1		
E27	RTIP0		

1.5   LOW SPEED LINE INTERFACE SIGNALS

568 BALL	PIN NAME	TYPE	DESCRIPTION
T1/E1 Receive Line Interface Signals			
AH28	RRING27	I	**Receive T1/E1 Line Input - Negative Polarity Signal**
AE23	RRING26		RTIP and RRING are differential analog input pins that receive standard T1/E1
AH25	RRING25		Return-to-Zero data, coupled through a 1:1 transformer. The transformer blocks
AF21	RRING24		the DC line bias and allows the inputs to be level shifted to mid-power supply.
AJ22	RRING23		*NOTE: It is recommended to use a transfomer with a center tap pin connected*
AF18	RRING22		*to ground through a 0.1μF capacitor.*
AF17	RRING21		
AJ11	RRING20		
AJ9	RRING19		
AJ7	RRING18		
AF9	RRING17		
AG6	RRING16		
AJ2	RRING15		
AE4	RRING14		
B1	RRING13		
B3	RRING12		
E8	RRING11		
B6	RRING10		
E11	RRING9		
A10	RRING8		
A12	RRING7		
A20	RRING6		
C20	RRING5		
D21	RRING4		
A27	RRING3		
C26	RRING2		
D26	RRING1		
D28	RRING0		

1.5   LOW SPEED LINE INTERFACE SIGNALS

568 BALL	PIN NAME	TYPE	DESCRIPTION
T1/E1 Transmit Line Interface Signals			
AG26	TTIP27	O	**Transmit T1/E1 Line Output - Posittive Polarity Signal**
AF23	TTIP26		TTIP and TRING are differential analog output pins that transmit standard T1/ E1 Return-to-Zero data. The amplitude of the output pulse is half the nominal T1/E1 standard and level shifted to $V_{CC}/2$ to allow for optimum pulse shaping capability. Therefore, it's necessary to couple these analog outputs to a 1:2 step-up transformer to apply a gain of 2x. It is recommended to connect a 0.68μF capacitor in series with each TTIP signal. See **Figure 49** on page 110.
AG23	TTIP25		
AJ23	TTIP24		
AJ21	TTIP23		
AK19	TTIP22		
AK17	TTIP21		
AF14	TTIP20		
AF13	TTIP19		
AJ8	TTIP18		
AJ6	TTIP17		
AJ4	TTIP16		
AE8	TTIP15		
AF4	TTIP14		
E5	TTIP13		
C5	TTIP12		
A4	TTIP11		
C8	TTIP10		
D11	TTIP9		
A11	TTIP8		
D14	TTIP7		
D17	TTIP6		
B20	TTIP5		
D20	TTIP4		
A26	TTIP3		
C25	TTIP2		
D25	TTIP1		
C28	TTIP0		

1.5   LOW SPEED LINE INTERFACE SIGNALS

568 Ball	Pin Name	Type	Description
T1/E1 Transmit Line Interface Signals			
AF25	TRING27	O	**Transmit T1/E1 Line Output - Negative Polarity Signal**
AJ27	TRING26		TTIP and TRING are differential analog output pins that transmit standard T1/
AF22	TRING25		E1 Return-to-Zero data. The amplitude of the output pulse is half the nominal
AK25	TRING24		T1/E1 standard and level shifted to $V_{CC}/2$ to allow for optimum pulse shaping
AF19	TRING23		capability. Therefore, it's necessary to couple these analog outputs to a 1:2
AJ19	TRING22		step-up transformer to apply a gain of 2x.
AH17	TRING21		
AK11	TRING20		
AJ10	TRING19		
AG10	TRING18		
AK4	TRING17		
AH5	TRING16		
AG5	TRING15		
AH2	TRING14		
C3	TRING13		
F8	TRING12		
C6	TRING11		
E10	TRING10		
B9	TRING9		
C12	TRING8		
E14	TRING7		
C18	TRING6		
B21	TRING5		
A24	TRING4		
B25	TRING3		
D24	TRING2		
E24	TRING1		
E26	TRING0		

1.6   HIGH SPEED SERIAL INTERFACE

568 Ball	Pin Name	Type	Description
STS-1 Receive Serial Interface (For Details on the M13 MUX mode, contact factory for more information)			
T1	RxSTS1CLK	I	**Receive STS-1 Serial Input Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the serial interface is enabled, the XRT86SH328 samples data on the rising edge of this input clock signal.
U1	RxSTS1DATA	I	**Receive STS-1 Serial Input Data** Apply the serial input data to this pin, and it can be sampled on either the rising edge or falling edge of the RxSTS1CLK input pin.
U2	RxSTS1FRAME	I	**Receive STS-1 Serial Frame Pulse** This input pin should be connected to the Frame Pulse to indicate when the first bit of the current STS-1 frame occurs if connected to an external device, where this option is available.
U5	RxSTS1LOS	I	**Receive STS-1 Serial Loss of Signal** If the high speed serial interface is connected to an external LIU (Line Interface Unit), then this input signal can be connected to the LOS output pin from the LIU.
STS-1 Transmit Serial Interface			
P3	TxSTS1CLK	O	**Transmit STS-1 Serial Output Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the serial interface is enabled, then the XRT86SH328 updates data on the rising edge of this output clock signal. The source of this clock can be a buffered clock derived from the recovered line clock in loop timing mode, or buffered from the internal master clock in local timing mode.
R5	TxSTS1DATA	O	**Transmit STS-1 Serial Output Data** The serial output data can be updated on either the rising edge or falling edge of the TxSTS1CLK output pin.
P2	TxSTS1FRAME	O	**Transmit STS-1 Serial Frame Pulse** This output frame pulse is used to indicate when the first bit of the current STS-1 frame is transmitted if connected to an external device, where this option is available.

1.7   HIGH SPEED TELECOM BUS INTERFACE

568 Ball	Pin Name	Type	Description
STS-3/STM-1 Receive Telecom Bus Interface			
V2	RxD_CLK	I	**Receive STS-3/STM-1 Telecom Input Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the Telecom Bus is enabled, then all telecom bus signals are sampled on the rising edge of this input clock. This clock should be 19.44MHz for STS-3/STM-1 or 6.48MHz for STS-1/STM-0.
V5	RxD_DP	I	**Receive STS-3/STM-1 Telecom Data Polarity** This input pin can be configured to operate as the EVEN or ODD parity value of either the Receive Telecom Data Bus RxD_D[7:0] or the Payload Indicator RxD_PL and Frame Pulse RxD_C1J1V1_FP. ***NOTE:*** *This pin should be pulled "Low" if the part is configured for Re-Phase On.*
V3	RxD_PL	I	**Receive STS-3/STM-1 Telecom Payload Indicator** This input pin is used to indicate when payload bytes within an STS-3/STM-1 frame are being processed. This pin should be pulled "High" for the entire duration of the payload bytes, and pulled "Low" at all other times.
W3	RxD_ALARM	I	**Receive STS-3/STM-1 Telecom Alarm Status** This input pin should be pulled "High" corresponding to any signal that is carrying either the AU-AIS or TU-AIS indicator. At all other times, this pin should be pulled "Low". If this pin is pulled "High", the XRT86SH328 will automatically declare the AU-AIS or TU-AIS defect.
Y1	RxD_C1J1V1_FP	I	**Receive STS-3/STM-1 Telecom Frame Pulse** The XRT86SH328 can be configured for Re-Phase On or Re-Phase Off, meaning that frame synchronization can be externally supplied to this input pin, or the XRT86SH328 can gain frame synchronization from the incoming data. **Re-Phase Off** This pin is ignored and can be tied to ground or left floating. **Re-Phase On** This pin should be pulled "High" during the C1 byte, J1 byte, and V1 byte. At all other times, this pin should be pulled "Low". ***NOTE:*** *When 3 XRT86SH328 chips share the telecom bus in a Master/Slave mode, the C1 bytes must be aligned on all three input pins. The J1 and/or V1 bytes do not have to be aligned.*
AE1 AD1 AA4 AC1 AB2 AB1 AA2 Y3	RxD_D7 RxD_D6 RxD_D5 RxD_D4 RxD_D3 RxD_D2 RxD_D1 RxD_D0	I	**Receive STS-3/STM-1 Telecom Input Data Bus** These input pins are sampled on the rising edge of the Receive Telecom Input Clock RxD_CLK. The MSB of the data bus is bit 7, and the LSB is bit 0.

1.7   HIGH SPEED TELECOM BUS INTERFACE

568 Ball	Pin Name	Type	Description
STS-3/STM-1 Transmit Telecom Bus Interface			
M1	TxD_CLK	O	**Transmit STS-3/STM-1 Telecom Output Clock** The high speed system bus can be configured to operate over a standard parallel telecom bus or a serial interface. If the Telecom Bus is enabled, then all telecom bus signals are updated on the falling edge of this output clock. The source of this clock can be a buffered clock derived from the recovered line clock in loop timing mode, or buffered from the internal master clock in local timing mode. This clock should be 19.44MHz for STS-3/STM-1 or 6.48MHz for STS-1/STM-0.
L2	TxD_DP	O	**Transmit STS-3/STM-1 Telecom Data Polarity** This output pin can be configured to operate as the EVEN or ODD parity value of either the Transmit Telecom Data Bus TxD_D[7:0] or the Payload Indicator TxD_PL and Frame Pulse TxD_C1J1V1_FP.
N3	TxD_PL	O	**Transmit STS-3/STM-1 Telecom Payload Indicator** This output pin is used to indicate when payload bytes within an STS-3/STM-1 frame are being transmitted. This pin will be pulled "High" for the entire duration of the payload bytes, and pulled "Low" at all other times. *NOTE: This pin should have an external pull-down resistor of 330Ω*
K1	TxD_ALARM	O	**Transmit STS-3/STM-1 Telecom Alarm Status** This output pin will be pulled "High" corresponding to any signal that is carrying either the AU-AIS or TU-AIS indicator. At all other times, this pin will be pulled "Low".
M2	TxD_C1J1V1_FP	O	**Transmit STS-3/STM-1 Telecom Frame Pulse** The XRT86SH328 can be configured for Re-Phase On or Re-Phase Off, meaning that frame synchronization can be externally provided to the system or act as a simple Frame Pulse. **Re-Phase Off** This pin is pulled "High" during the A1 byte. At all other times, this pin is pulled "Low". **Re-Phase On** This pin is pulled "High" during the C1 byte, J1 byte, and V1 byte. At all other times, this pin is pulled "Low". *NOTE: 1. When 3 XRT86SH328 chips share the telecom bus in a Master/Slave mode, all three chips will output this signal.* *NOTE: 2. This pin should have an external pull-down resistor of 330Ω.*
G2 J3 H2 G1 J2 H1 J1 K2	TxD_D7 TxD_D6 TxD_D5 TxD_D4 TxD_D3 TxD_D2 TxD_D1 TxD_D0	O	**Transmit STS-3/STM-1 Telecom Output Data Bus** These output pins are updated on the falling edge of the Transmit Telecom Output Clock TxD_CLK. The MSB of the data bus is bit 7, and the LSB is bit 0.

1.8   HIGH SPEED SECTION AND PATH OVERHEAD BUS

568 Ball	Pin Name	Type	Description
Receive Section and Path Overhead Extraction Bus			
AA3	RxOH	O	**Receive TOH/POH Data Output Port** The extracted TOH/POH overhead bytes will be updated on this output pin on the falling edge of RxOHCLK. Therefore, RxOH should be sampled using the rising edge of RxOHCLK.
W5	RxOHCLK	O	**Receive TOH/POH Overhead Clock Output** This output clock signal is used as the timing reference for the Receive Overhead Extraction Bus. This clock will update all output extraction bus pins on its falling edge.
Y5	RxOHFRAME	O	**Receive TOH/POH Overhead Frame Boundary Indicator** The Receive TOH/POH Data Output Port will pulse this output pin "High" for one period of RxOHCLK, coincident to whenever it is extracting the very first bit of the STS-3/STM-1 frame in the Section Overhead (A1) and the very first bit of the Path Overhead (J1). If RxPOH_IND is "Low" during this Frame Pulse, then that bit is A1. If RxPOH_IND is "High" during this Frame Pulse, then that bit is J1. This pin will be pulled "Low" at all other times.
Y4	RxOHVALID	O	**Receive TOH/POH Overhead Data Valid Indicator** This output pin will be pulled "High" when the extracted TOH and POH bytes are ready to be sampled from the overhead bus. This pin will be pulled "Low" at all other times. If RxPOH_IND is "Low" while RxOHVALID is "High", then TOH is valid. If RxPOH_IND is "High" while RxOHVALID is "High", then POH is valid. This pin will be pulled "Low" at all other times.
AB3	RxPOH_IND	O	**Receive POH Indicator** The Receive Path Overhead Indicator will pull "High", coincident to whenever it is extracting Path Overhead data via the RxOH output pin. Conversely, this pin will pull "Low", coincident to whenever it is extracting Section Overhead data via the RxOH output pin. This pin will be updated on the falling edge of RxOHCLK.
Transmit Section and Path Overhead Insertion Bus			
E1	TxOHEN	O	**Transmit TOH/POH Overhead Port Enable Output** The state of this output pin determines the time period when the XRT86SH328 can accept TOH/POH overhead bytes. The Overhead Insertion Bus is active when this pin is pulled "High".
F2	TxOH	I	**Transmit TOH/POH Data Input Port** If the System Side Terminal Equipment intends to insert its own value for a given overhead TOH or POH byte into the outbound STS-3 or STM-1 data-stream, then the System Side Terminal Equipment is expected to apply the overhead bytes to this input pin while asserting the TxOHINS input pin. This input pin is sampled upon the rising edge of TxOHCLK.
H3	TxOHCLK	O	**Transmit TOH/POH Overhead Clock Output** This output clock signal is used as the timing reference for the Transmit Overhead Insertion Bus. This clock will sample all input insertion bus pins on its rising edge.

1.8 HIGH SPEED SECTION AND PATH OVERHEAD BUS

568 BALL	PIN NAME	TYPE	DESCRIPTION
J4	TxOHFRAME	I/O	**Transmit TOH/POH Overhead Frame Boundary Indicator** The Transmit TOH/POH Data Input Port will pulse this output pin "High" for one period of TxOHCLK, coincident to whenever it is processing the very first TOH byte of a given outbound STS-3/STM-1 frame in the Section Overhead (A1) and the very first bit of the Path Overhead (J1). If TxPOH_IND is "Low" during this Frame Pulse, then that bit is A1. If TxPOH_IND is "High" during this Frame Pulse, then that bit is J1. This pin will be pulled "Low" at all other times.
F1	TxOHINS	I	**Transmit TOH/POH Overhead Insertion Input** If the System Side Terminal Equipment intends to insert its own value for a given overhead TOH or POH byte into the outbound STS-3 or STM-1 data-stream, then this input pin should be pulled "High" coincident with the TOH or POH bytes. This input pin is sampled upon the rising edge of TxOHCLK.
K5	TxPOH_IND	I/O	**Transmit POH Indicator** The Transmit TOH/POH Data Input Port will toggle and hold this output pin "High", coincident to whenever it is ready to accept POH data via the TxOH input pin. Conversely, this pin will hold this pin "Low", coincident to whenever it is ready to accept TOH data via the TxOH input pin. This pin will be updated on the falling edge of TxOHCLK as an output (or sampled on the rising edge as an input).

1.9 HIGH SPEED TU POH OVERHEAD BUS

568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive TU POH Extraction Bus			
AA5	RxTUPOH	O	**Receive TU POH Data Output Port** This output pin will output the contents of the VC-4 POH bytes within the incoming STM-1 data-stream. This output is updated on the falling edge of RxTUPOHCLK.
AB4	RxTUPOHCLK	O	**Receive TU POH Overhead Clock Output** If the XRT86SH328 along with two other devices has been configured to operate in the STM-1/TUG-3 Mode, this output clock signal is used as the timing reference for the Receive VC-4 POH Overhead Extraction Bus. This clock will update all output extraction bus pins on its falling edge.
AD2	RxTUPO-HFRAME	O	**Receive TU POH Data Output Port - Frame Boundary Output** The Receive TU POH Data Output Port will pulse this output pin "High" for one period of RxTUPOHCLK, coincident to whenever it is extracting the very first bit of the VC-4 POH. This pin will be pulled "Low" at all other times.
AB5	RxTUPOHVALID	O	**Receive TU POH Data Output Port - Overhead Indicator Output** This output pin will be pulled "High" when the extracted VC-4 POH bytes are ready to be sampled from the overhead bus. This pin will be pulled "Low" at all other times.
Transmit TU POH Insertion Bus			
D1	TxTUPOHEN	O	**Transmit TU POH Overhead Port Enable Output** The state of this output pin determines the time period when the XRT86SH328 can accept VC-4 POH overhead bytes. The Overhead Insertion Bus is active when this pin is pulled "High".

1.9 HIGH SPEED TU POH OVERHEAD BUS

568 BALL	PIN NAME	TYPE	DESCRIPTION
F3	TxTUPOH	I	**Transmit TU POH Data Input Port** If the System Side Terminal Equipment intends to insert its own value for a given VC-4 POH byte, then the System Side Terminal Equipment is expected to apply the overhead bytes to this input pin while asserting the TxTUPOHINS input pin. This input pin is sampled upon the rising edge of TxTUPOHCLK.
H4	TxTUPOHCLK	O	**Transmit TU POH Overhead Clock Output** This output clock signal is used as the timing reference for the Transmit Overhead Insertion Bus. This clock will sample all input insertion bus pins on its rising edge.
G3	TxTUPO-HFRAME	I/O	**Transmit TU POH Overhead Frame Boundary Indicator** The Transmit TU POH Data Input Port will pulse this output pin "High" for one period of TxTUPOHCLK, coincident to whenever it is processing the very first VC-4 POH byte. This pin will be pulled "Low" at all other times.
J5	TxTUPOHINS	I	**Transmit TU POH Overhead Insertion Input** If the System Side Terminal Equipment intends to insert its own value for a given overhead VC-4 POH byte, then this input pin should be pulled "High" coincident with the TU POH bytes. This input pin is sampled upon the rising edge of TxTUPOHCLK.

1.10   Framer + LIU Combo Mode

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive Interface for the Framer Combo or M13 MUX Modes			
AF27	RxDS1CLK27	O	**Receive DS-1 Output Clock**
AJ30	RxDS1CLK26		These output pins are the recovered line clocks from each DS-1 channel. In the event that the receiver is experiencing an RLOS condition, this clock will track an internal DS-1 master clock so that there is a constant clock on this output.
AE28	RxDS1CLK25		
AD28	RxDS1CLK24		
AD29	RxDS1CLK23		
AD30	RxDS1CLK22		
AB30	RxDS1CLK21		*NOTE: For the DS1 Add/Drop Port, contact the factory for more information.*
U3	RxDS1CLK20		
W1	RxDS1CLK19		
Y2	RxDS1CLK18		
W5	RxDS1CLK17		
Y5	RxDS1CLK16		
AB4	RxDS1CLK15		
AB5	RxDS1CLK14		
H4	RxDS1CLK13		
E1	RxDS1CLK12		
J3	RxDS1CLK11		
J2	RxDS1CLK10		
K2	RxDS1CLK9		
M2	RxDS1CLK8		
P3	RxDS1CLK7		
M27	RxDS1CLK6		
L27	RxDS1CLK5		
J28	RxDS1CLK4		
K26	RxDS1CLK3		
J26	RxDS1CLK2		
H26	RxDS1CLK1		
G26	RxDS1CLK0		

1.10　Framer + LIU Combo Mode

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive Interface for the Framer Combo or M13 MUX Modes			
AC25	RxDS1DATA27	O	**Receive DS-1 Output Data**
AF28	RxDS1DATA26		These output pins are the recovered data from each DS-1 channel. This data is presented in single rail NRZ format.
AA25	RxDS1DATA25		
AA26	RxDS1DATA24		
Y26	RxDS1DATA23		*NOTE: For the DS1 Add/Drop Port, contact the factory for more information.*
W26	RxDS1DATA22		
Y28	RxDS1DATA21		
U4	RxDS1DATA20		
V4	RxDS1DATA19		
W4	RxDS1DATA18		
Y4	RxDS1DATA17		
AB3	RxDS1DATA16		
AA5	RxDS1DATA15		
AC4	RxDS1DATA14		
D1	RxDS1DATA13		
H3	RxDS1DATA12		
H2	RxDS1DATA11		
H1	RxDS1DATA10		
K1	RxDS1DATA9		
N3	RxDS1DATA8		
R5	RxDS1DATA7		
K30	RxDS1DATA6		
K28	RxDS1DATA5		
H29	RxDS1DATA4		
G29	RxDS1DATA3		
H27	RxDS1DATA2		
C30	RxDS1DATA1		
B30	RxDS1DATA0		

1.10   Framer + LIU Combo Mode

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Receive Interface for the Framer Combo or M13 MUX Modes			
AG28	RxDS1Frame27	O	**Receive DS-1 Frame Boundary Indicator Output**
AC26	RxDS1Frame26		These output pins are the recovered Frame Pulse indicator from each DS-1
AB26	RxDS1Frame25		channel.
AE29	RxDS1Frame24		
AE30	RxDS1Frame23		
Y27	RxDS1Frame22		
V26	RxDS1Frame21		
V1	RxDS1Frame20		
W2	RxDS1Frame19		
AA1	RxDS1Frame18		
AA3	RxDS1Frame17		
AC2	RxDS1Frame16		
AD2	RxDS1Frame15		
AG1	RxDS1Frame14		
G3	RxDS1Frame13		
G2	RxDS1Frame12		
G1	RxDS1Frame11		
J1	RxDS1Frame10		
L2	RxDS1Frame9		
M1	RxDS1Frame8		
P2	RxDS1Frame7		
L28	RxDS1Frame6		
J29	RxDS1Frame5		
G30	RxDS1Frame4		
E30	RxDS1Frame3		
D30	RxDS1Frame2		
D29	RxDS1Frame1		
C29	RxDS1Frame0		

1.10 Framer + LIU Combo Mode

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Transmit Interface for the Framer Combo or M13 MUX Modes			
AJ29	TxDS1CLK27	I	**Transmit DS-1 Input Clock**
AD26	TxDS1CLK26		These input pins are the transmit line clocks for each DS-1 channel. A 1.544MHz clock should be applied to this pin for T1 mode, or 2.048MHz for E1 mode.
AG29	TxDS1CLK25		
AF29	TxDS1CLK24		
AB27	TxDS1CLK23		
AA27	TxDS1CLK22		*NOTE: For the DS1 Add/Drop Port, contact the factory for more information.*
AA28	TxDS1CLK21		
T1	TxDS1CLK20		
U5	TxDS1CLK19		
Y1	TxDS1CLK18		
Y3	TxDS1CLK17		
AB2	TxDS1CLK16		
AD1	TxDS1CLK15		
AF1	TxDS1CLK14		
F3	TxDS1CLK13		
K5	TxDS1CLK12		
L5	TxDS1CLK11		
M5	TxDS1CLK10		
L3	TxDS1CLK9		
M3	TxDS1CLK8		
P4	TxDS1CLK7		
N26	TxDS1CLK6		
K29	TxDS1CLK5		
H30	TxDS1CLK4		
F30	TxDS1CLK3		
F29	TxDS1CLK2		
E29	TxDS1CLK1		
E28	TxDS1CLK0		

1.10   *Framer + LIU Combo Mode*

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Transmit Interface for the Framer Combo or M13 MUX Modes			
AE26	TxDS1DATA27	I	**Transmit DS-1 Input Data**
AH29	TxDS1DATA26		These input pins are used to supply the transmit data for each DS-1 channel.
AD27	TxDS1DATA25		This data should be presented in single rail NRZ format.
AC27	TxDS1DATA24		
AF30	TxDS1DATA23		*NOTE: For the DS1 Add/Drop Port, contact the factory for more information.*
AB28	TxDS1DATA22		
AB29	TxDS1DATA21		
U1	TxDS1DATA20		
V2	TxDS1DATA19		
V5	TxDS1DATA18		
AA2	TxDS1DATA17		
AC1	TxDS1DATA16		
AE1	TxDS1DATA15		
AE2	TxDS1DATA14		
J5	TxDS1DATA13		
F2	TxDS1DATA12		
F1	TxDS1DATA11		
L4	TxDS1DATA10		
N5	TxDS1DATA9		
N4	TxDS1DATA8		
N2	TxDS1DATA7		
M28	TxDS1DATA6		
J30	TxDS1DATA5		
K27	TxDS1DATA4		
H28	TxDS1DATA3		
G28	TxDS1DATA2		
F28	TxDS1DATA1		
F27	TxDS1DATA0		

1.10   Framer + LIU Combo Mode

Some of these pins are shared with other modes. The purpose of the Framer Combo mode is to operate the chip in 28 independent DS1 Framer + LIU channels. In this mode, the Telecom Bus, SONET/SDH Mapper, Overhead Port, and the Cross Connect functions are not available. If Voyager is not operating in the 28-channel Framer Combo mode, the unshared input pins can be tied to GND or left floating. The unshared output pins should be left floating.

568 BALL	PIN NAME	TYPE	DESCRIPTION
Transmit Interface for the Framer Combo or M13 MUX Modes			
AK30	TxDS1Frame27	I	**Transmit DS-1 Frame Boundary Indicator Input**
AE27	TxDS1Frame26		These input pins are used to supply the transmit Frame Pulse indicator for each DS-1 channel. In the event that a frame pulse does not exist, the DS-1 framer block has the ability to gain frame synchronization from the incoming data stream.
AH30	TxDS1Frame25		
AG30	TxDS1Frame24		
AC28	TxDS1Frame23		
AC29	TxDS1Frame22		
AC30	TxDS1Frame21		
U2	TxDS1Frame20		
V3	TxDS1Frame19		
W3	TxDS1Frame18		
AB1	TxDS1Frame17		
AA4	TxDS1Frame16		
AC3	TxDS1Frame15		
AA6	TxDS1Frame14		
E2	TxDS1Frame13		
J4	TxDS1Frame12		
K4	TxDS1Frame11		
K3	TxDS1Frame10		
M4	TxDS1Frame9		
P5	TxDS1Frame8		
N1	TxDS1Frame7		
L29	TxDS1Frame6		
M26	TxDS1Frame5		
L26	TxDS1Frame4		
J27	TxDS1Frame3		
K25	TxDS1Frame2		
G27	TxDS1Frame1		
H25	TxDS1Frame0		

1.11 POWER AND GROUND PINS

568 BALL	PIN NAME	TYPE	DESCRIPTION
Power Supply Pins			
J6, AD3, AB25, P17, R17, U17, P16, P15, T16, T15, R16, R15, U16, U15, P14, T14, R14, U14, T17	1.8V Digital	-	**1.8V Digital Power Supply**
AH3, A23, A16, B17, A17, B15, B10, B16, F10, E6, AK15, AG15, AK14, AH6, AK13, AJ16, AG19, AK26, AK29, E25, B26, AF12, J25	1.8V Analog	-	**1.8V Analog Power Supply**
T18, R18, N16, N15, V16, V15, T13, R13	3.3V Digital	-	**3.3V Digital Power Supply**
AK3, AG3, AG4, AH4, AJ3, AF8, AH9, AG11, AH7, AK5, AG12, AK10, AJ12, AK12, AH16, AJ17, AJ18, AG18, AK21, AK22, AF20, AK24, AJ25, AE21, AG24, AK28, AJ28, AE24, D27, B29, B28, F22, A28, E22, D22, B24, E19, B22, A21, D18, A19, A18, B14, A13, D13, E13, A9, C10, A7, D9, E9, B5, A3, D6, F7, D4	3.3V Analog	-	**3.3V Analog Power Supply**
Ground Pins			
G6, D3, D16, C16, AC6, AD6, AJ1, AF5, AE7, AK1, AF7, AE9, AG7, AE10, AG8, AF10, AF11, AF16, AJ15, AH15, AK7, AH10, AK9, AH11, AG13, AH13, AJ13, AG16, AK16, AG17, AH18, AK20, AJ20, AH20, AG20, AG21, AJ24, AH23, AH24, AK27, AE22, AH26, AF24, AH27, AF26, AD25, G25, F26, F24, A30, C27, A29, B27, F21, D23, E21, C23, B23, C21, A22, D19, C19, B19, B18, C17, E16, A15, C14, B13, B12, B11, C11, E12, A8, A6, B7, C7, D8, D7, B4, E7, C4, D5, B2, P18, P28, N18, N17, V18, V17, U18, P13, N14, N13, V14, V13, U13	GND	-	**Ground**
No Connect Pins			
AG9, AH22, B8, AH8, AK23, AB6, K6	NC	-	**No Connect**

2.0 APPLICATIONS AND PHYSICAL INTERFACE GENERAL OVERVIEW

NOTE: *In addition to SONET, Voyager supports all SDH functions including VC-11/VC-12 TUG-3 and AU-3 Mapping Protocols. For the purpose of concise reading, all SONET Standard and Virtual Tributary terminologies used in this document also directly apply to their counterpart SDH Standard and Virtual Container terminologies.*

The XRT86SH328 (Voyager) is a highly integrated, monolithic device designed for cost-sensitive SONET/SDH to PDH mapper applications. Voyager supports all the framing, mapping and grooming functions required for T1/E1 aggregation to STS-1/STS-3 via VT1.5/VT2 mapping protocols or to STM-1 via standard VC-11/VC-12 to AU-3 and TUG-3/AU-4 mapping protocols. The device generates and terminates all SONET Transport (Section and Line) and Path Overhead including Virtual Tributaries (VT) Overhead or SDH Regenerator Section, Multiplexer Section and Path Overhead including the low-order Virtual Container (VC) Path Overhead. T1/E1 framing is transparent; therefore, the device neither generates nor terminates the T1/E1 frame.

Voyager includes a standard serial LVCMOS/LVTTL (STS1) interface or a parallel Telecom Bus interface to SONET STS1 or STS3 Framer/Mapper with SONET-to-PDH Desynchronizer, VT1.5/VT2 Mapper, VT1.5/VT2 Cross-Connect and a 28-channel T1 or 21-channel E1 Short Haul LIU with integrated egress frame synchronizer for T1/E1 bit-retiming. Voyager also provides alarm and performance monitoring for all STS1/STS3 and VT1.5/VT2 overhead in compliance with Telcordia GR-499/GR-253 CORE and ITU-T G.703/G.783 standards. Transport (Section and Line) and Path overhead may be inserted/extracted via serial interfaces provided in transmit and receive directions.

The 28-channel T1 and/or 21-channel E1 Short Haul LIU provides line termination and generation in compliance with GR-253 and G.703 standards, supporting T1/E1 (2.048Mbps) 75Ω and 120Ω applications. The LIU receiver includes adaptive equalizer, clock and data recovery, and B8ZS/HDB3 decoding with performance monitoring of Loss of Signal, Line Code Violations and Excessive Zeros. The LIU transmitter includes B8ZS/HDB3 encoder, transmit pulse shaping and line driver. The LIU also provides a half-duplex jitter attenuator which may be applied in either the transmit or receive data path.

T1/E1 spans are mapped to VT1.5/VT2 via the Virtual Tributary Unit (VT) mapper. VT1.5/VT2 grooming support provided for both transmit and receive directions on a per T1/E1 basis via the integrated, full-duplex 28x28 VT1.5 or 21x21 VT2 Cross-Connect. The SONET framer/mapper supports generation and termination of STS1 and STS3 Transport (Section and Line) and Path overhead and also performs SONET to PDH desynchronization.

A single Voyager performs mapping of 28 asynchronous T1 or 21 asynchronous E1 spans or any combination of T1 and E1 via VT1.5 and VT2 mapping structure into the seven VT Groups of the STS1 Synchronous Payload Envelope. Likewise, VC-11/TU-11 and VC-12/TU-12 mapping into either TUG-2/VC-3/AU-3/STM-0 or TUG-2/TUG-3/AU-4/STM-1 is also supported. VT mapping to STS3 requires (3) Voyager devices with one acting as "master" framer and two acting as "slave" framers. In this configuration, Voyager performs all the necessary framing, pointer processing and mapping functions required for mapping 84xT1 or 63xE1 spans or any combination of both T1 and E1 via VT1.5 and VT2 mapping structure into twenty-one VT Groups of the STS3 Synchronous Payload Envelope. Similarly, VC-11/TU-11 and VC-12/TU-12 mapping into either TUG-2/VC-3/AU-3/STM-1 or TUG-2/TUG-3/VC-4/AU-4/STM-1 is also supported.

FIGURE 1. APPLICATION DIAGRAM
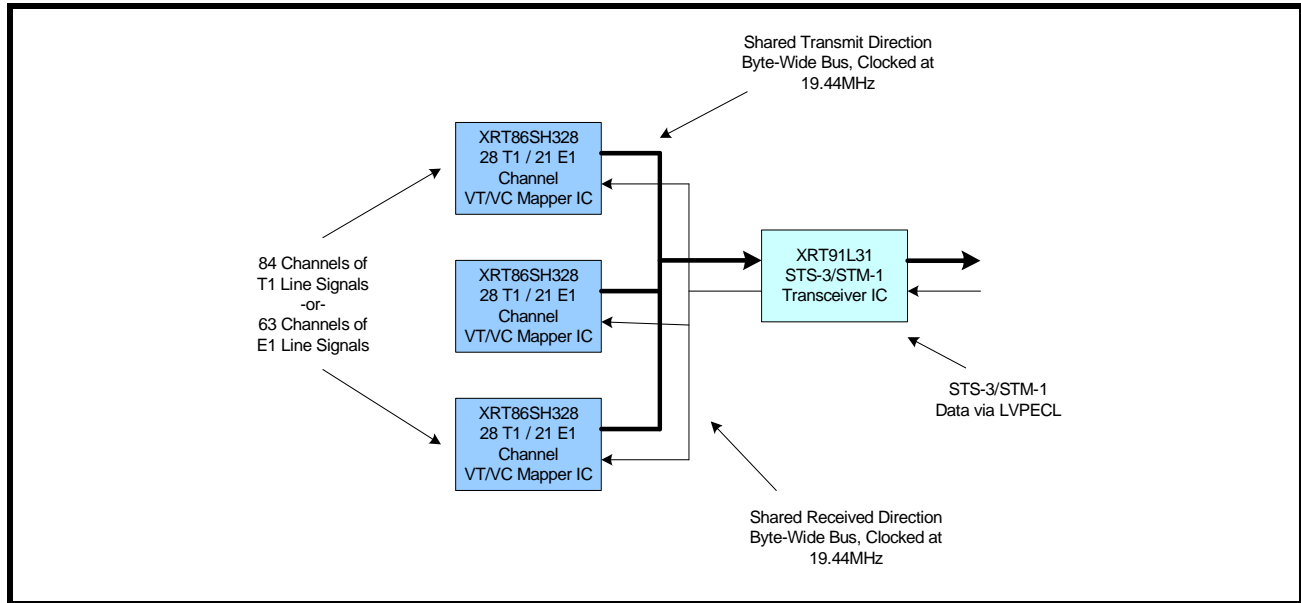
2.1   Physical Interface

Voyager consists of several physical interfaces supporting the T1/E1 Line Interface, STS1/STS3 Line Interface, SONET TOH/POH and VT-POH Overhead Insertion and Extraction Interfaces, Timing and Synchronization Interfaces, Microprocessor Interface and JTAG/Testability Interfaces. The diagram shown in **Figure 2** illustrates organization and applied nomenclature of these interfaces

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FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE PHYSICAL INTERFACE
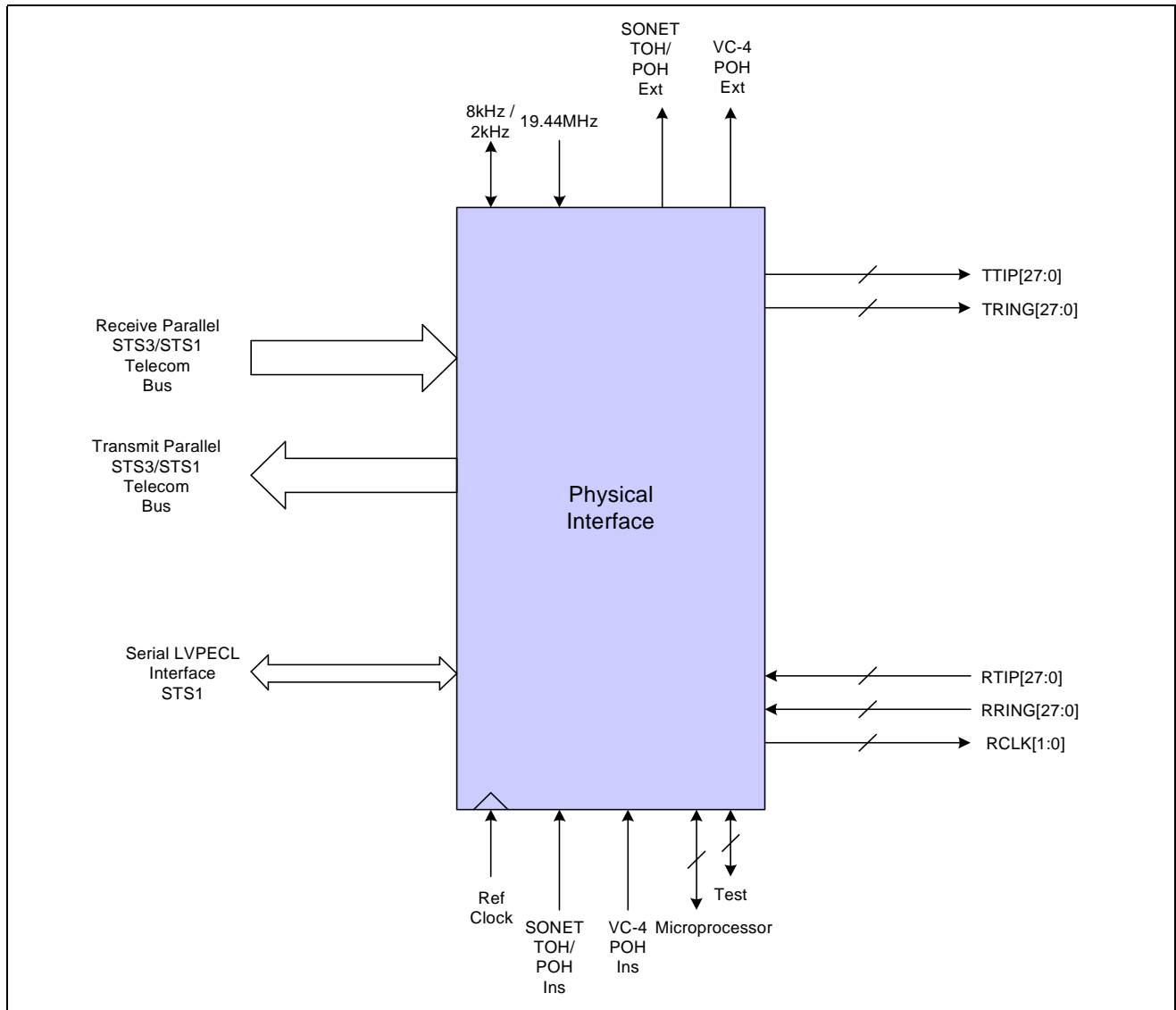
2.2   Telecom Bus Interface

Voyager applications typically require transport of STS3 signals over optical networks. Therefore, Voyager provides a standard Telecom Bus which supports direct connection to STS3 optical transceivers such as the XRT91L30, SONET STS1/STS3/STS12 Multirate Transceiver (CDR+SERDES). The signaling protocol defined for the Voyager Telecom Bus supports the multiplexing of STS1 data streams required to create an aggregate STS3 signal. However, the Telecom Bus also provides direct output of a single STS1 data stream at 6.48MHz to support STS1 mapping applications.

FIGURE 3.   SIMPLIFIED BLOCK DIAGRAM OF THE TELECOM BUS INTERFACE
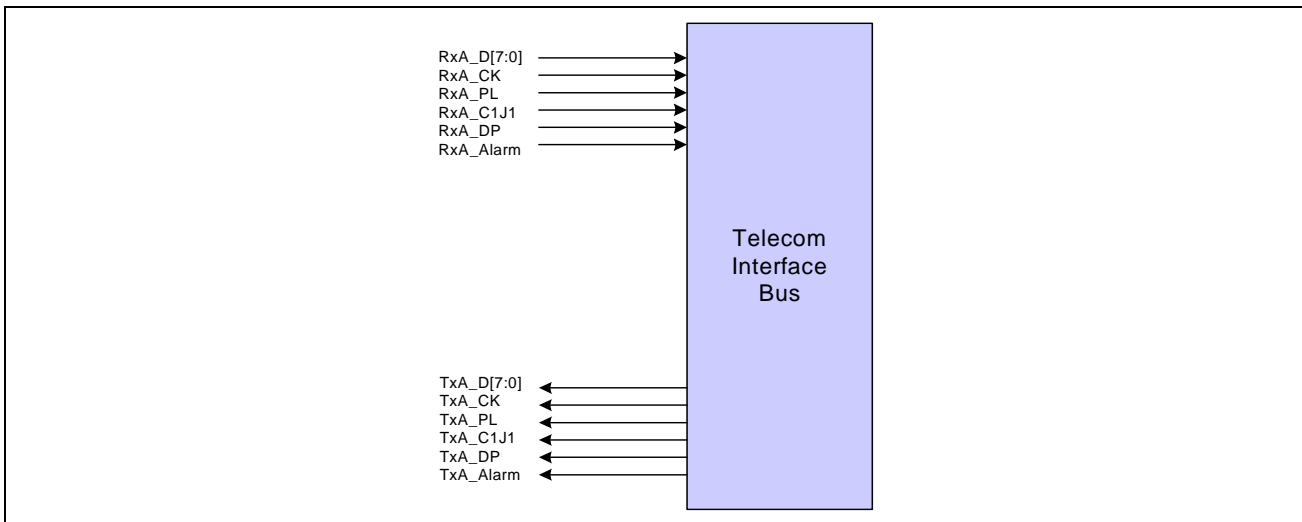
- The Transmit Telecom Bus Interface provides the ingress STS1/STS3 data stream output
- The Receive Telecom Bus Interface provides the egress STS1/STS3 data stream input

The Telecom Bus interface consists of the following input/output signal.

Transmit Telecom Bus Interface

- •TxA_D[7:0] 8-bit parallel telecom data bus
- •TxA_CK 19.44/6.48 MHz telecom bus clock
- •TxA_PL Payload location indicator
- •TxA_C1J1 J0(C1)/J1/V1 byte location indicator
- •TxA_DP Telecom data bus parity indicator
- •TxA_Alarm AIS-L/AIS-P/VT SPE AIS alarm indicator

Receive Telecom Bus Interface

- •RxA_D[7:0] 8-bit parallel telecom data bus
- •RxA_CK 19.44/6.48 MHz telecom bus clock
- •RxA_PL Payload location indicator
- •RxA_C1J1 J0(C1)/J1/V1 byte location indicator
- •RxA_DP Telecom data bus parity indicator
- •RxA_Alarm AIS-L/AIS-P/VT SPE AIS alarm indicator

2.3   STS1 Serial Interface SONET Frame Synchronization and Timing Interface

In addition to the parallel telecom bus, the high speed interface has the option to transmit and receive data through an STS1 interface. STS3 is NOT supported with the serial interface.

FIGURE 4. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL PORT INTERFACE
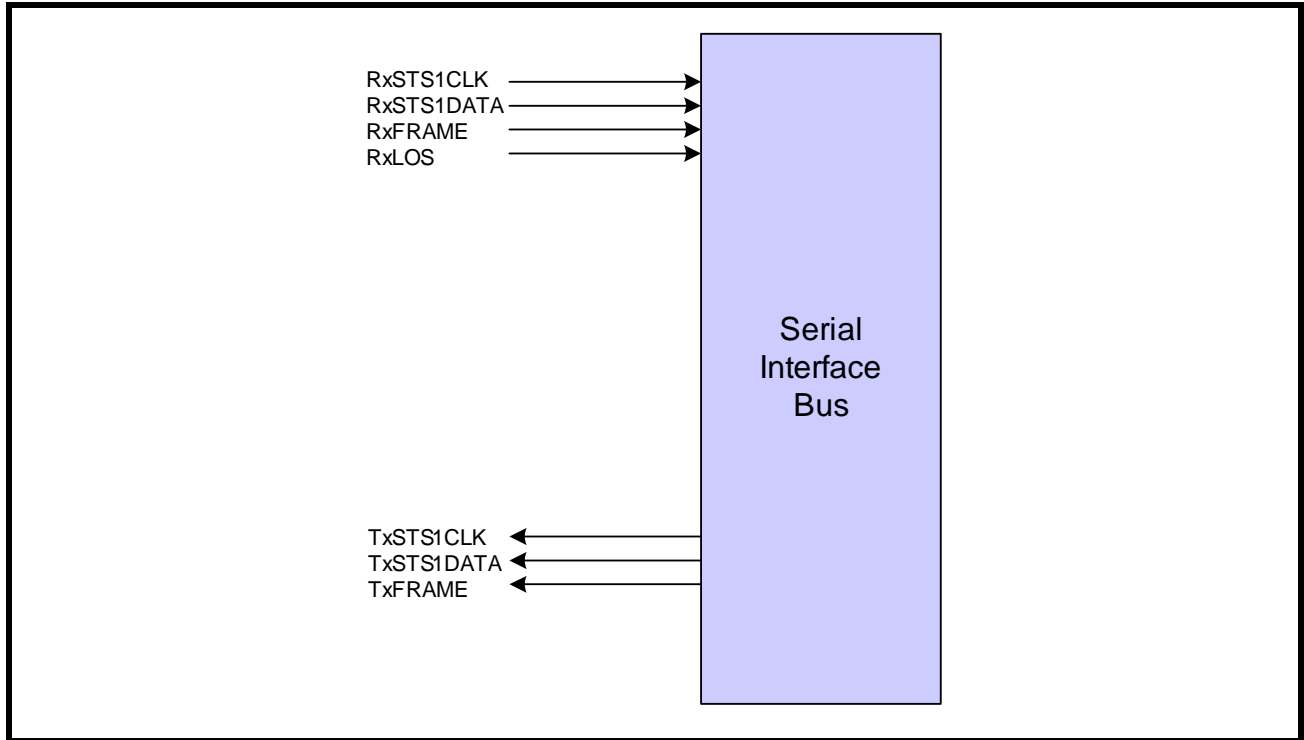
- The Transmit Serial Interface provides the ingress STS1 data stream output
- The Receive Serial Interface provides the egress STS1 data stream input

The Serial Interface consists of the following input/output signal.

Transmit Serial Interface

- •TxSTS1CLK Transmit serial interface clock
- •TxSTS1DATA Transmit serial interface data
- •TxSTS1FRAME Transmit serial interface frame pulse

 Receive Serial Interface

- •RxSTS1CLK Receive serial interface clock
- •RxSTS1DATA Receive serial interface data
- •RxSTS1FRAME Receive serial interface frame pulse
- •RxSTS1LOS Receive serial interface loss of signal

2.4   SONET Frame Synchronization and Timing Interface

SONET Section layer processing at the STS3 level is managed by a combination of overhead processing performed in the "master" framer as well as through synchronization of the SONET framing engines within the "master" and "slave" framers. The "master" device supports insertion and monitoring of B1 BIP-8 overhead and also distributes an 8kHz / 2kHz frame sync to the "slave" devices. The "slave" devices source this frame sync as the reference for all SONET framer/mapper blocks. In particular, the SONET framing, scrambling and descrambling blocks rely upon this frame sync to ensure the "master" and "slave" devices remain synchronized at all times.

The XRT86SH328 requires a 19.44MHz input clock reference for timing of the Telecom Bus, SONET Framers, SONET Overhead processors, VT1.5/VT2 Mapper and VT1.5/VT2 Cross-Connects for STS3 applications. The same 19.44MHz reference should be applied to all three Voyager device when operating in STS3 mapper mode. In the case of STS1 applications, the device will accept a 6.48MHz reference input.

FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE SONET FRAME SYNCHRONIZATION
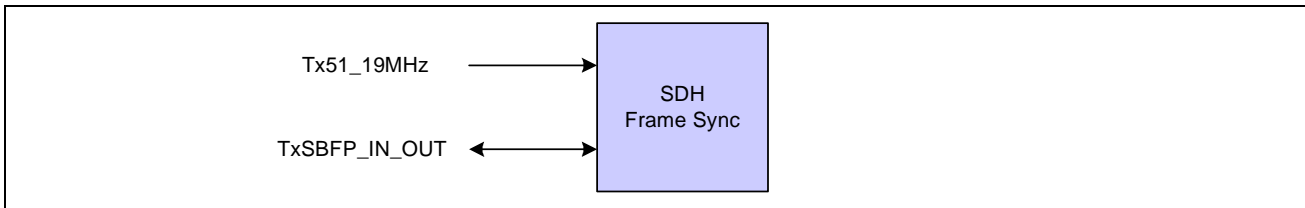
The SDH Frame Synchronization and Timing Interface consists of the following signals.

- •Tx51_19MHz Transmit STS3/STS1 Timing Reference Input
- •TxSBFP_IN_OUT System Frame Pulse (Frame Synchronization Signal)

2.5   SONET Overhead Add-Drop Interfaces

SONET Overhead Add-Drop Interfaces provide access to the SONET Section, Line, and Path Overhead. Please note there is no external interface providing access to the VT1.5/VT2 Path Overhead. These interfaces allow flexible insertion and extraction of overhead and alarm data, thereby enabling proprietary processing of the SONET frame.

FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF THE SONET OVERHEAD ADD-DROP INTERFACE
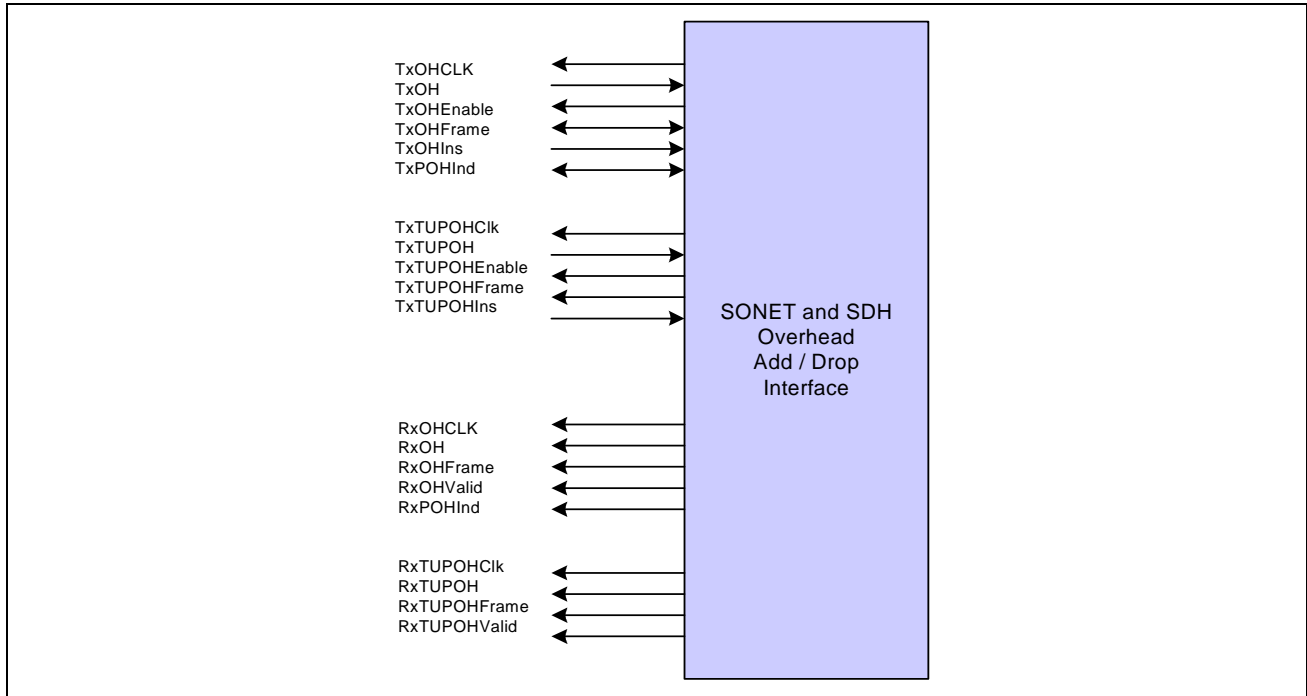
- The Transmit SONET TOH/POH Overhead Interface allows insertion of Section, Line, and Path overhead data within the transmit STS3/STS1 data stream.
- For SDH operation, the Transmit TU POH Overhead Interface allows insertion of High-Order Path overhead data within the transmit VC-4 POH data stream.
- The Receive SONET TOH/POH Overhead Interface allows extraction of Section, Line, and Path overhead data from within the receive STS3/STS1 data stream.
- For SDH operation, the Receive TU POH Overhead Interface allows extraction of High-Order Path overhead data from within the receive VC-4 POH data stream.

The SONET Overhead Insertion/Extraction Interfaces consist of the following signals.

Transmit SONET TOH/POH Insertion Bus (TxOH)

- •TxOHCLK Transmit overhead clock
- •TxOH Transmit overhead data
- •TxOHEnable Transmit overhead bus enable
- •TxOHFrame Transmit overhead frame boundary indicator
- •TxOHIns Transmit overhead Insertion Control
- •TxPOHInd Transmit overhead SOH/POH Indicator

Transmit TU POH Insertion Bus (TxTUPOH)

- •TxTUPOHClk TxTUPOH clock
- •TxTUPOH TxTUPOH data
- •TxTUPOHEnable TxTUPOH bus enable
- •TxTUPOHFrame TxTUPOH frame boundary indicator
- •TxTUPOHIns TxTUPOH insertion control

Receive SONET TOH/POH Overhead Extraction Bus (RxOH)

- •RxOHClk Receive overhead clock
- •RxOH Receive overhead data
- •RxOHFrame Receive frame boundary indicator
- •RxOHValid Receive valid indicator
- •RxPOHInd Receive overhead SOH/POH indictor

Receive TU POH Extraction Bus (RxTUPOH)

- •RxTUPOHClk RxTUPOH clock
- •RxTUPOH RxTUPOH data
- •RxTUPOHFrame RxTUPOH frame boundary indicator
- •RxTUPOHValid RxTUPOH valid indicator

2.6   T1/E1 Short Haul Line Interface

Voyager's T1/E1 Short Haul LIU provides the physical interface for 75Ω Coax and 120Ω Twisted Pair applications. With selectable 75Ω/120Ω internal termination and option for high impedance on both transmit and receive LIU interfaces, the device supports 1:1 and 1+1 redundancy with hitless hot-swapping for Coax and Twisted pair designs with a single Bill-of-Materials. The T1/E1 transmit driver and receive equalizer are designed specifically to meet G.703 T1/E1 Short Haul transport requirements.

The T1/E1 Short Haul Line Interfaces consist of the following signals.

T1/E1 Transmit Line Output Signals

- •TTIP[0:27] T1 or TTIP[0:20] E1Transmit TIP data
- •TRING[0:27] T1 or TRING[0:20] E1 Transmit RING data

T1/E1 Receive Line Input Signals

- •RTIP[0:27] T1 or RTIP[0:20] E1 Receive TIP data
- •RRING[0:27] T1 or RRING[0:20] E1 Receive RING data

Note: TTIP/TRING and RTIP/RING pins are grouped in pairs such as TTIP0/TRING0.

2.7   *T1/E1 Timing Interface*

Timing support within the 28/21-channel LIU includes sourcing of an external reference input clock and recovery of the incoming receive T1/E1 Line clock. This reference clock input frequency should be either 2.048MHz, 4.096MHz, 8.192MHz, or 16.386Mhz. The T1/E1 LIU includes a Master Clock Synthesizer which accepts this input clock reference and derives a 2.048MHz reference functions such as Clock and Data Recovery as well as timing of the T1/E1 transmit output data stream. The Clock and Data Recovery circuit recovers the incoming receive T1/E1 Line clocks, which can be multiplexed to one of the two dedicated output pins, RCLK_REC[1:0]. Either the T1/E1 LIU reference clock input or the recovered receive T1/E1 Line clock may be used as the timing source for the transmit T1/E1 data stream bit-retiming function.

The T1/E1 Timing Interface consists of the following signals.

•MCLK 2.048/4.096/8.192/16.384MHz reference clock input
•RCLK_REC[1:0] Recovered T1/E1 (Receive) line clock outputs

2.8   *Microprocessor Interface*

Voyager provides a standard microprocessor interface supporting Intel, Motorola, PowerPC and Mips synchronous/asynchronous PIO bus interfaces. The microprocessor interface provides an 18-bit address and 8-bit data bus interface for configuration, control, status monitoring with up to 66 MHz read/write access. The device allows a noon-multiplexed address and data bus, supports reset-upon-read/write-clear for control of status registers and provides programmable interrupt signal.

The Microprocessor Interface consists of the following signals.

•A[0:17] 18-bit Address Bus
•D[7:0] 8-bit Data Bus
•ALE/AS Address Latch Enable/Address Strobe
•CS Chip Select
•INT Interrupt
•RD/DS/WE Read Strobe/Data Strobe/Write Enable
•RDY'/DTACK/RDY/TA Ready, DTACK, or Transfer Acknowledge
•RESET Hardware Reset Input
•mPCLK Microprocessor Interface Clock Input
•WR'/RW Write Strobe/Read-Write Operation Identifier
•PTYPE[2:0] Microprocessor Interface Type Selector
•DBEN/OE Bi-Directional Data Bus Enable

3.0 FUNCTIONAL DESCRIPTION

The XRT86SH328 includes the following functional blocks

Ingress Data Path Functional Blocks

- T1/E1 Receive LIU plus Clock and Data Recovery (RxT1/E1LIU)
- Transmit TU VC-4 POH Insertion Bus (TxTUPOH)
- VT1.5/VT2 Transmit Virtual Tributary Mapper and Overhead Processor (TxVTPOHProc)
- VT1.5/VT2 Transmit Cross-Connect (TxVT1.5/VT2XC)
- Transmit SONET TOH/POH Insertion Bus (TxTPOH)
- SONET Transmit Mapper and Path Overhead Processor (TxPOHProc)
- SONET Transmit Framer and Transport Overhead Processor (TxTOHProc)
- Transmit Telecom Bus (TxTBus)

Egress Data Path Functional Blocks

- Receive Telecom Bus (RxTBus)
- SONET Receive Framer and Transport Overhead Processor (RxTOHProc)
- SONET Receive Mapper and Path Overhead Processor (RxPOHProc)
- SONET Receive TOH/POH Overhead Extraction Bus (RxTPOH)
- VT1.5/VT2 Receive Virtual Tributary Overhead Processor (RxVTPOHProc)
- Receive TU VC-4 POH Extraction Bus (RxTUPOH)
- VT1.5/VT2 Receive Cross-Connect (RxVT1.5/VT2XC)
- T1/E1 Transmit Frame Synchronizer and Bit-Retimer (TxE1Frm)
- T1/E1 Transmit LIU (TxE1LIU)

FIGURE 7. FUNCTIONAL BLOCK DIAGRAM
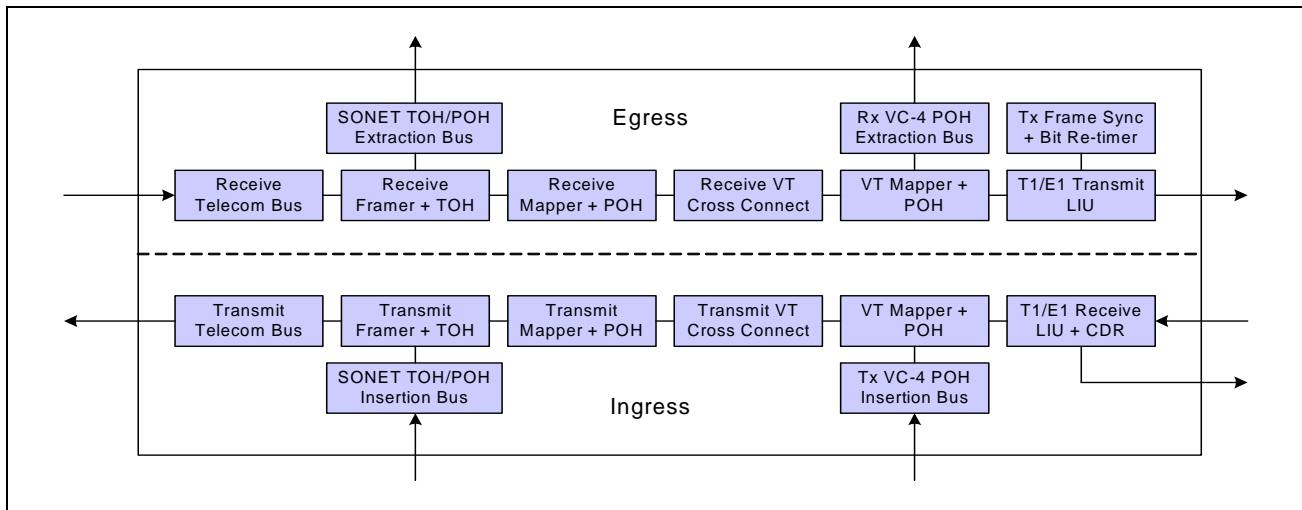
3.1 Ingress Data Path Functional Blocks

The Ingress data path is defined as the flow of data from the T1/E1 LIU Receiver input through the VT Mapper and SONET Framer/Mapper to the Transmit Telecom Bus. The following sections describe the general functions and detailed features for each block within the ingress data path.

FIGURE 8. SIMPLIFIED BLOCK DIAGRAM OF THE INGRESS DATA PATH
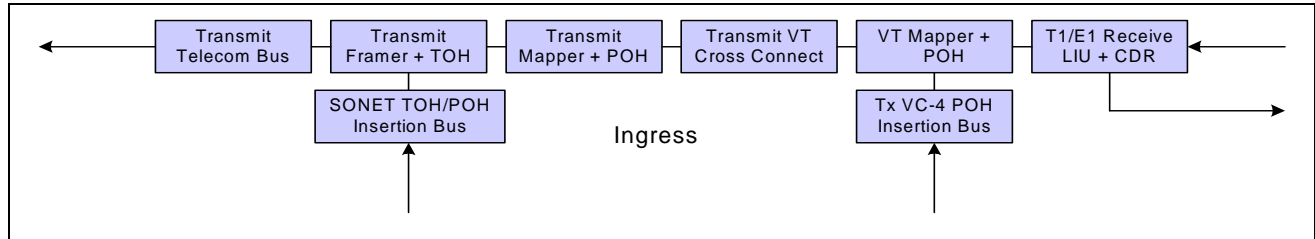
3.2 T1/E1 Receive LIU (RxT1/E1LIU)

- Loss of signal (RLOS) according to Telcordia GR-253 and ITU-T G.775 and ETS300233
- Internal impedance matching on receive for 75Ω or 120Ω
- Power down on a per channel basis
- Selectable crystal-less digital jitter attenuators (JA) with 32-bit or 64-bit FIFO that can be selected in the receive path
- Receive inputs may be set to high impedance for protection or redundancy applications on a per channel basis
- R3 Technology for 1:1 or 1+1 redundancy without relays
- On chip digital clock and data recovery for high input jitter tolerance
- QRSS, TAOS, and Network Loop Codes for receive diagnostics
- Supports remote loop back modes

3.3 Transmit Virtual Circuit - 4 POH Overhead Insertion Bus (TxTUPOH)

The SDH Transmit High-Order Path Overhead (TxTUPOH) Insertion Bus provides capability to receive the TU Virtual Circuit - 4 High-Order Path Overhead (VC-4 POH) from an external processor. Data received by the TxTUPOH block may be optionally inserted into the outgoing VC-4 POH overhead during generation of the corresponding overhead byte within the TxLOPOHProc block.

3.4   VT1.5/VT2 Transmit VT-POH Mapper and Overhead Processor (TxVTPOHProc)

The VT1.5/VT2 Transmit Virtual Tributary Overhead Processor performs asynchronous mapping of T1 and E1 spans into VT1.5 and VT2 payloads. The TxVTPOHProc receives 28 independent T1 or 21 independent E1 or any combination of T1 and E1 (within permissible VT Grouping) data streams from the Receive T1/E1 LIU block and maps these T1/E1 spans to VT1.5 and/or VT2. This block generates all the necessary VT Path Overhead including functions supported within the V5, J2, N2, and K4 bytes.

The primary features of the TxLOPOHProc block include the following functions

- •Maps (28/21) independent T1/E1 spans into VT1.5/VT2 payloads
- •Generates the VT1.5/VT2 Virtual Tributary Path Overhead
- •Supports VT Path Overhead Generation including V5, J2, N2, and K4
- •V5 overhead generations support includes:
- •BIP-2 Parity
- •Virtual Tributary Path Signal Label
- •Virtual Tributary Path Remote Error Indicator (VT-REI)
- •Virtual Tributary Path Remote Failure Indicator (VT-RFI)
- •Virtual Tributary Path Remote Defect Indicator (VT-RDI)
- •J2 overhead generation supports Virtual Tributary Access Path Identifier (VT-API) Messaging
- •N2 overhead generation supports for Virtual Tributary Tandem Connection Monitoring (VT-TCM)
- •K4 overhead support for Virtual Tributary APS Signaling
- •Generates VT1.5/VT2 stuff bits, overhead bits, justification opportunity bits, and justification control bits to support rate adaptation between the incoming T1/E1 signals and the SONET transmit timing reference
- •Virtual Tributary Path overhead may be optionally forced to reflect values configured within the software register map or those received by the TxTUPOH Insertion Bus.

3.5   VT1.5/VT2 Transmit Cross-Connect (TxVT1.5/VT2XC)

The VT1.5/VT2 Transmit Cross-Connect operates in parallel with the VT1.5/VT2 Transmit Virtual Tributary Path Overhead Processor to support grooming of the ingress VT1.5/VT2 paths. The TxVT1.5/VT2XC block provides a 28x28 VT1.5 or 21x21 VT2 cross-connect which performs grooming of the VT1.5 and VT2 signals to support rearrangement, or reordering, of the T1 and E1 traffic received from the T1/E1 Line Interface before mapping within the STS1/STS3 payload.

3.6   Transmit SONET TOH/POH Insertion Bus (TxTPOH)

The SONET Transmit TOH and POH Overhead Insertion Bus receives section and path overhead data from an internal processor for the purpose of insertion within the corresponding byte of the outgoing STS1/STS3 signal. This block receives the section and path overhead from external pins and provides this data to the TxPOHProc and TxTOHProc.

3.7 *SONET Transmit Mapper and Path Overhead Processor (TxPOHProc)*

The SONET Transmit Mapper and Path Overhead Processor receives VT1.5/VT2 overhead and payload data stream from the TxVTPOHProc block and maps this data to VT Groups within the STS1 SPE or in SDH mode to either VC-3/AU-3 or TUG-3/VC-4/AU-4. The TxPOHProc block performs all the mapping and overhead generation functions required at the Path layer. The TxPOHProc provides fixed pointer generation with a pointer value of "522" and also supports B3 parity calculation/insertion and Path alarm generation. Data received by the TxTPOH block may be optionally inserted into the outgoing path overhead during generation of the corresponding overhead byte within the TxPOHProc block.

The primary features of the TxPOHProc block include the following functions

Payload Pointer Overhead

- Fixed payload pointer (H1, H2, H3) generation with user programmable value (default = "522")
- Supports NDF insertion within H1/H2 pointer
- Performs mapping of VT1.5/VT2 data streams into VT Groups within the STS1 SPE or in SDH mode to either VC-3/AU-3 or TUG-3/VC-4/AU-4
- Supports insertion of Alarm Indication Signal - Path (AIS-P or AU-AIS) based on alarm and defects detected within the incoming egress STS1/STS3 signal
- Performs B3 parity calculation and Insertion
- C2 Signal Label Insertion
- Remote Defect Indication - Path (RDI-P) alarm insertion
- Remote Error Indication - Path (REI-P) alarm insertion
- Supports H4 Virtual Tributary/Tributary Unit Multiframe Indicator insertion
- F3 User Channel overhead generation
- Supports K3 APS signaling
- Supports N1 Path Tandem Connection signaling
- Path overhead may be optionally forced to reflect values configured within the software register map or those received by the TxTPOH Insertion Bus.

3.8   *SONET Transmit Framer and Transport Overhead Processor (TxTOHProc)*

The SONET Transmit Framer and Transport Overhead Processor receives the data from the TxPOHProc and completes the multiplexing and overhead generation process to create the STS1/STS3 signal output to the Transmit Telecom Bus. The TxTOHProc performs all the overhead processing required for Section (Regenerator) and Line (Multiplexer Section). The block includes supports or A1A2 frame generation, B1/B2 parity calculation, Section Trace Messaging, DCC Messaging, and K1/K2 APS support. Data received by the TxTPOH block may be optionally inserted into the outgoing section overhead during generation of the corresponding overhead byte within the TxTOHProc block.

The primary features of the TxTOHProc block include the following functions compliant

Section (Regeneration Section) Overhead

•Frame Generation with the A1/A2 bytes with optional alignment to external 8 kHz / 2 kHz frame sync
•Provides optional error mask for A1/A2 frame bit error generation
•Optional support for generation of LOS and SEF condition
•Scrambling
•Insertion of J0 Section Trace Message
•B1 Parity calculation and insertion with optional error mask
•E1 Orderwire and F1 User Channel overhead insertion
•Data communication channels (DCC messaging) insertion within D1-D3 and D4-D12

Line (Multiplexer Section) Overhead

•B2 Parity calculation and insertion with optional error mask
•K1/K2 signaling for APS, Alarm Indication and Remote Device Indication
•Alarm Indication Signal - Line (AIS-L) alarm generation
•Remote Defect Indication - Line (RDI-L) alarm generation
•Remote Error Indicator - Line (REI-L) alarm generation
•Alarm generation based on incoming upstream defects and optional software/hardware control
•Data communication channels (DCC messaging) insertion within D4-D12
•S1 processing for Synchronization Status Monitor
•M0/M1 generation for reporting of B2 bit/block error counts to upstream equipment
•E2 Orderwire overhead insertion

3.9 Transmit Telecom Bus (TxTBus)

The Transmit Telecom Bus provides the ingress data path STS1/STS3 physical interface for connection to an STS1/STS3 transceiver module, downstream processor or backplane connection.

- STS1 Mode: 8-bit parallel bus operating at 6.48MHz
- STS3 Mode: 8-bit parallel bus operating at 19.44MHz

The Transmit Telecom Bus provides a physical interface between the optical transceiver module and Voyager for the ingress data path. This bus operates at 19.44Mbps for STS3 applications and 6.48Mpbs for STS1 applications using an 8-bit parallel data bus. The primary function of this block is transmission of data to the optical transceiver, or other upstream processor. Data received from the SONET Transmit Framer and Section Overhead Processor is sent out on the TxTBus. STS1 timeslots for the aggregate STS3 signals are previously byte-aligned. Therefore, the TxTBus performs the STS3 multiplex function in order to create the aggregate STS3 output signal.

For STS3 applications, the TxTBus within the "slave" devices will send/assert on the correct STS1 time slot (time slot 1 or time slot 2) for the appropriate STS1 channel. The TxTBus within the 'master' device will send the STS1 signal for time slot "0". The result is a time domain multiplexing of STS1 signals at the TxTBus which creates the aggregate/channelized STS3 signal. The "master" device monitors the TxTBus data during the "slave" device output timeslots for the purpose of B1 parity calculation.

The TxTBus supports the following features:

- Optional configuration for the TxTBus Clock polarity (positive/negative polarity)
- Optional Parity calculation for either the data bus only or the combination of the data bus, PL, C1J1 and Alarm signals.
- Optional configuration of the TxTBus Data Parity polarity (positive/negative polarity
- Optional configuration of the TxTBus C1J1 indicator for frame phase indication, payload phase indication or both

3.10 Egress Data Path Functional Blocks

The Egress data path is defined as the flow of data from the Receive Telecom Bus input through the SONET Framer/Mapper and VT Mapper to the T1/E1 LIU Transmit output as shown below in **Figure 9**. The following sections describe the general function and detailed features for each block within the egress data path.

FIGURE 9. SIMPLIFIED BLOCK DIAGRAM OF THE EGRESS DATA PATH
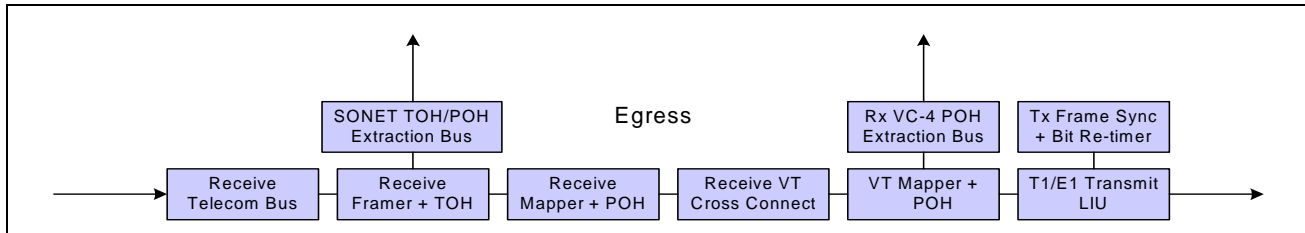
3.11 Receive Telecom Bus (RxTBus)

The Receive Telecom Bus provides the physical interface between the optical transceiver module and Voyager for the egress data path. This bus operates at 19.44Mbps for STS3 applications and 6.48Mpbs for STS1 applications using an 8-bit parallel data bus. The primary function of this block is reception of data from the optical transceiver, or other upstream processor. Data received by the RxTBus is byte-aligned and passed to the SONET Receive Framer and Transport Overhead Processor.

For STS3 applications, the RxTBus within the "slave" devices will sense only the correct STS1 time slot (time slot 1 or time slot 2) for the appropriate STS1 channel. The RxTBus within the 'master' device will sense the STS1 signal for time slot "0". In addition, the RxTBus within the 'master' device will also sense all STS1 time slots for the aggregate/channelized STS3 signal in order to support the appropriate monitoring of section overhead functions such as B1 parity.

The RxTBus supports the following features:

- •Optional configuration for the RxTBus Clock polarity (positive/negative polarity)
- •Optional Parity monitoring for either the data bus only or the combination of the data bus, PL, C1J1 and Alarm signals.
- •Optional configuration of the RxTBus Data Parity polarity (positive/negative polarity
- •Optional configuration of the RxTBus C1J1 indicator for frame phase detection, payload phase detection or both
- •Byte-Alignment of incoming STS1/STS3 data
- •Automatic Insertion of downstream AIS-P based on incoming RxD_Alarm pin status

3.12   *SONET Receive Framer and Transport Overhead Processor (RxTOHProc)*

The SONET Receive Framer and Transport Overhead Processor receives the STS1/STS3 data stream from the RxTBus and performs all the overhead processing required for Section (Regenerator) and Line (Multiplexer Section) termination. The RxTOHProc supports performance, defect and alarm monitoring for all Section and Line overhead data. The RxTOHProc allows user access to the incoming TOH data through microprocessor accessed registers or via the Receive SONET TOH/POH Overhead Extraction Bus (RxTPOH).

The primary features of the RxTOHProc block include the following functions

Section (Regeneration Section) Overhead

- •Loss of Signal alarm detection
- •Frame-Alignment of A1/A2 bytes
- •Severely Errored Frame (SEF), or Out-of-Frame (OOF) alarm detection
- •Loss of Frame (LOF) alarm detection
- •Descrambling
- •Detects J0 Section Trace Message and provides indication of
- •J0 Section Trace Message: Mismatch
- •J0 Section Trace Message: Invalid
- •B1 Parity monitoring with Signal Degrade (SD) and Signal Fail (SF) alarm detection
- •Includes programmable thresholds for declaration of SD and SF conditions
- •Extracts E1 Orderwire and F1 User Channel overhead
- •Extracts data communication channels (DCC messaging) from D1-D3 and D4-D12

Line (Multiplexer Section) Overhead

- •B2 Parity monitoring with Signal Degrade (SD) and Signal Fail (SF) alarm
- •Includes programmable thresholds for declaration of SD and SF conditions
- •K1/K2 processing for APS, Alarm Indication and Remote Device Indication
- •Detects APS failure indicated within the K1/K2 bytes
- •Alarm Indication Signal - Line (AIS-L) alarm detection
- •Remote Defect Indication - Line (RDI-L) alarm detection
- •Extracts data communication channels (DCC) messaging from D4-D12
- •S1 processing for Synchronization Status Monitor
- •Remote Error Indicator - Line (REI-L) alarm detection
- •M0/M1 processing for collection of upstream B2 bit/block error counts
- •Extracts E2 Orderwire overhead

Section and Line (Regenerator and Multiplexer Section) Error Counters:

- •Provides 32-bit saturating counter of OOF/SEF errors
- •Provides 32-bit saturating counter of LOF errors
- •Provides 32-bit saturating counter of LOS errors
- •Provides 32-bit saturating counter of SD errors
- •Provides 32-bit saturating counter of SF errors
- •Provides 32-bit saturating counter of RDI-L errors
- •Provides 32-bit saturating counter of REI-L errors
- •Provides 32-bit saturating counter of BIP-8 B1 errors
- •Provides 32-bit saturating counter of BIP-8 B2 errors

3.13   *SONET Receive Mapper and Path Overhead Processor (RxPOHProc)*

The SONET Receive Mapper and Path Overhead Processor receives the Path Overhead and payload data stream from the RxSOHProc and performs all the overhead processing required for Path termination. The RxSOHProc supports performance, defect and alarm monitoring for all Path overhead data. This block also performs pointer processing and demapping of the STS1/STS3 SPE payload. The RxPOHProc terminates the STS1 SPE and passes the VT1.5 and VT2 mapped data to the Receive VT1.5/VT2 Virtual Tributary Overhead Processor. For SDH operation, the RxPOHProc also terminates the AU-4/VC-3/TUG-3/TUG-2 or AU-3/VC-3/TUG-2 overhead, and passes the VC-11/VC-12 mapped data to the Receive VC-11/VC-12 Virtual Tributary Overhead Processor. The block supports user access to the incoming VC-4 POH data through microprocessor accessed registers or via the Receive SONET TOH/POH Overhead Extraction Bus (RxTPOH).

The primary features of the RxPOHProc block include the following functions compliant with ITU-T …

Payload Pointer Overhead

•Interprets payload pointer (H1, H2, H3), performs payload extraction and provides monitoring for
•Loss of Pointer (LOP) alarm detection
•New Data Flag (NDF)
•Positive and Negative stuff events
•Alarm Indication Signal - Path (AIS-P or AU-AIS) alarm detection

Path Overhead Termination

•Detects J1 Path Trace Message and provides indication of
•J1 Path Trace Message: Trace Identifier Mismatch - Path (TIM-P)
•J1 Path Trace Message: Invalid
•B3 Parity monitoring
•C2 Signal Label Monitoring within indication of Invalid, Unequipped, and Payload label mismatch status
•Remote Defect Indication - Path (RDI-P) alarm detection
•Remote Error Indication - Path (REI-P) alarm detection
•Supports H4 Virtual Tributary/Tributary Unit Multiframe Indicator
•Extracts F3 User Channel overhead
•Supports K3 APS signaling
•Supports N1 Path Tandem Connection Signaling

Error Counters include the following:

•Provides 32-bit saturating counter of LOP
•Provides 32-bit saturating counter of AIS-P errors
•Provides 32-bit saturating counter of BIP-8 B3 errors
•Provides 32-bit saturating counter of REI-P errors

4.0 VOYAGER HARDWARE ARCHITECTURE AND ALGORITHMS

This section intends to provide a description of the overall Voyager architecture and functions of each module inside the chip. The detailed information about each module will be addressed in the following subsections. **Figure 10** represents a simplified block diagram of this device.

FIGURE 10. VOYAGER ARCHITECTURE
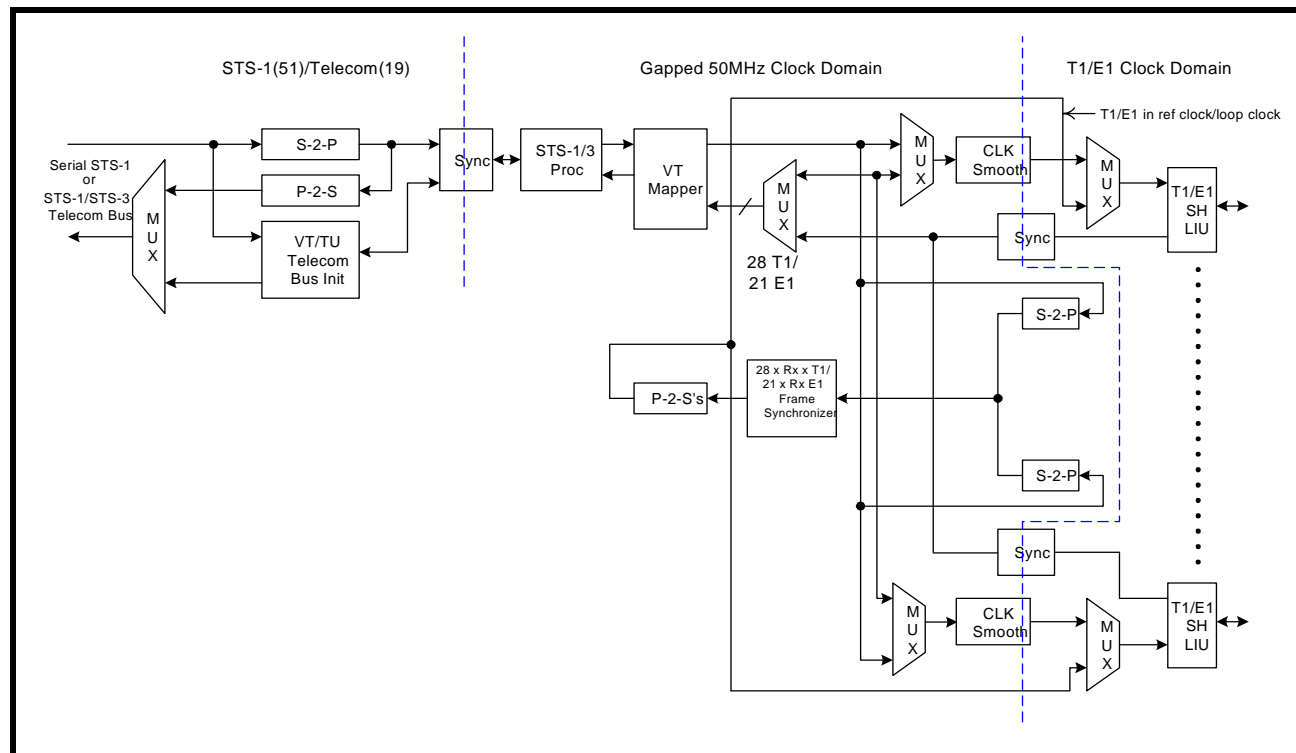
4.1   *MULTIPLEXING STRUCTURE*

Figure 11 shows the relationship between various multiplexing elements that are defined and illustrates possible multiplexing structures.

VT TYPE	VT-SPE LINE RATE	VT MAX PAYLOAD RATE
VT1.5	1 664 kb/s	1 600 kbit/s
VT2	2 240 kbit/s	2 176 kbit/s

FIGURE 11. VOYAGER SONET MULTIPLEXING STRUCTURE
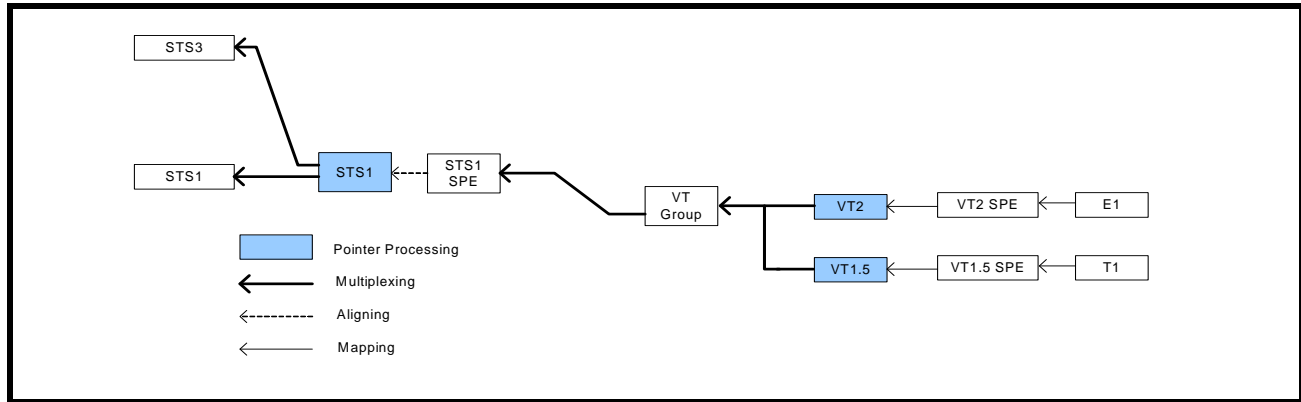
FIGURE 12. VOYAGER SDH MULTIPLEXING STRUCTURE

49
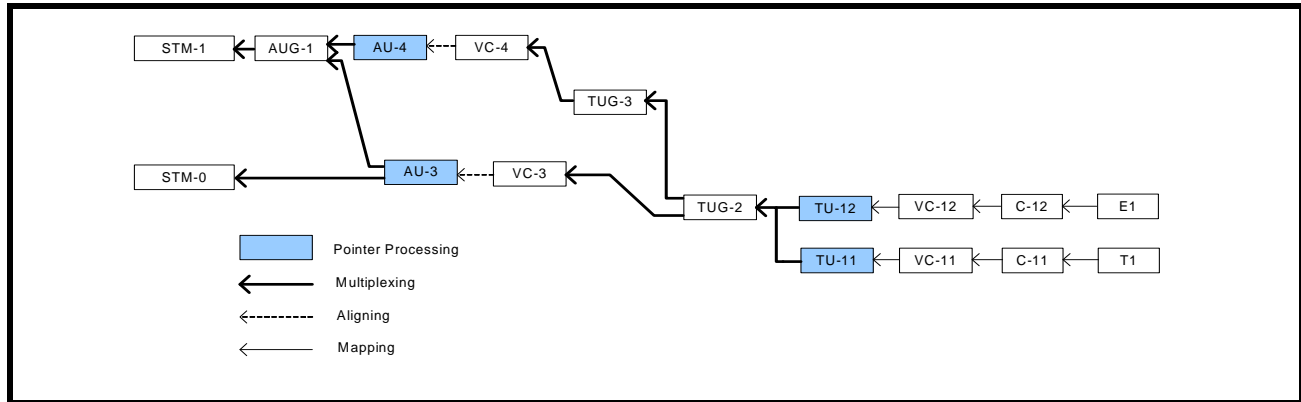
4.2   FUNCTIONAL BLOCKS

The Voyager device is functionally, as well as architecturally, divided into the following blocks and modules:

- Transceiver Interface
- STS1/STS3 Transmit Framer (Tx Transport Overhead Processor)
- STS1/STS3 Transmit TOH (Transport OverHead) Interface
- STS1/STS3 Receive Framer (Rx Transport Overhead Processor)
- STS1/STS3 Receive TOH (Transport Overhead) Interface
- STS1/STS3 Transmit Pointer Processor (Tx Path Overhead processor)
- STS1/STS3 Transmit POH (Path OverHead) Interface
- STS1/STS3 Receive Pointer Processor (Rx Path Overhead Processor)
- STS1/STS3 Receive POH (Path Overhead) Interface
- VT Mapper
- 28 T1/ 21 E1 Port Cross Connect
- T1/E1 Receive Framing Synchronizer
- LIU Control Interface
- LIU Modules
- Microprocessor Interface
- Interrupt Controller
- Performance Monitor

The operations and functions of these blocks are discussed in detail in the following sections. This section gives an overview of the operation of this device.

4.3   SONET TRANSMIT DATA FLOW

The SONET transmit blocks allow flexible insertion of Transport and Path overhead bytes through both hardware and software. The blocks also perform primitive SONET tasks such as data scrambling, BIP-8 calculation and insertion, and fixed stuff columns insertion. The blocks are used to transmit a SONET STS1/ STS3 stream with any permissible VT Group composition. The location of the SPE within the STS1/STS3 frame is fixed with a pointer offset of 522, which results in the J1 byte immediately trailing the last Z0 byte in the transport overhead.

Figure 13 shows the general structure of an SONET transmitter. As in the case of SONET receive blocks, the SONET transmit blocks are reusable blocks that are configured to transmit any compositions of any STS-N stream (3 and 1). The SONET transmit block consists of a transport section (txspoh_proc and txspoh_cont blocks) and 5 path sections.

The txspoh_cont path overhead block receives path overhead data from both software and hardware and allows software to select the version that is forwarded to the txspoh_proc path processor block. Software can also specify actions on the SPE data such as AIS-P insertion and RDI-P insertion.

The txspoh_proc block receives payload data from the VT Mapper interface and path overhead data from the txspoh_cont block and performs a multiplexing function using the location information from the txspoh_proc transport processor block. The txspoh_proc block also generates the H1/H2 pointer bytes and provides them on its output data port at the appropriate instances in the transport overhead. Since there can be multiple path blocks for a SONET transmitter, the txspoh_proc block only puts bytes onto its output data ports when the current transmit time slot belongs to its path. Otherwise, zeros are placed on the output data port. The data from all the txspoh_proc blocks are ORed together before being forwarded to the txstoh_proc block.

The txstoh_cont transport control block receives transport overhead data from both software and hardware and allows software to specify the version that is forwarded to the txstoh_proc block. Software also specifies actions such as AIS-L insertion, LOS insertion, and BIP-8 error insertions.

The txstoh_proc block accepts SPE data from the txspoh_proc blocks and transport overhead data from the txstoh_cont block. The txstoh_proc block generates transmit location signals and chooses from the appropriate input data stream for each byte location in the frame. The txstoh_proc also generates time advanced versions of the location signals for the other SONET transmit blocks to facilitate pipelining.

FIGURE 13. SONET TRANSMITTER GENERAL STRUCTURE
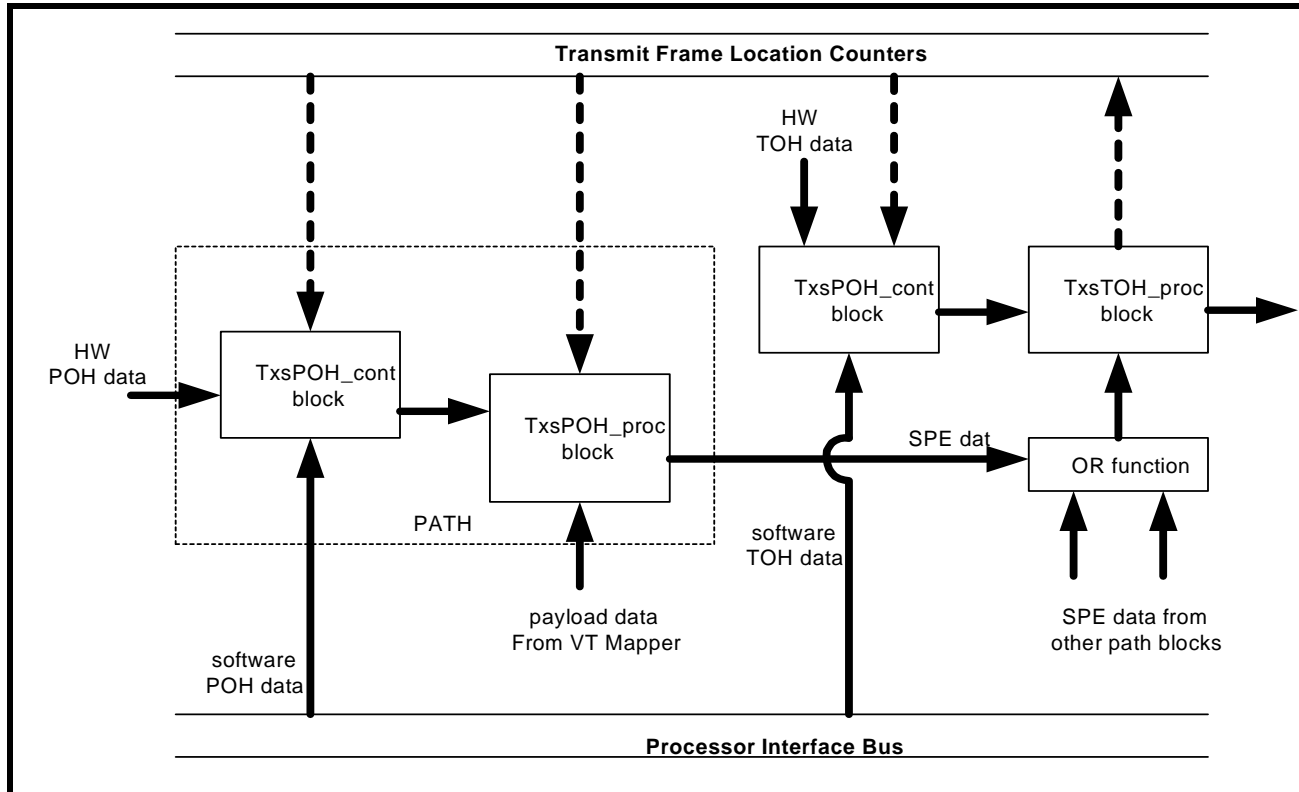
4.4 SONET RECEIVE DATA FLOW

The SONET receive blocks receive SONET STS1/STS3 signals with various VT Group compositions and perform the necessary transport and path overhead processing. Strobe signals are generated for downstream circuitry to extract the payload data.

Figure 14 shows the general composition of an SONET STS1/STS3 receiver. The receiver consists of a transport section and a path section. The receive transport section consists of one rxstoh_proc block which finds frame synchronization, performs error checking, de-scrambles the data, contains one rxstoh_stat block which provides the register file for the SONET receive transport section, maintains some counters and buffers, and contains one rxstoh_cap block which captures all the transport overhead bytes for possible processing by the software. The receive path section consists of 5 path blocks. Each path block consists of one rxspoh_proc block which does pointer processing and error checking, one rxspoh_stat block which provides the register file for the receive path section and maintains some counters and buffers, and one rxspoh_cap block which captures all the path overhead bytes for processing by software. The SONET receive (and transmit) blocks support a 32 bit internal data bus width. The wider data width allows the SONET receiver/transmitter to limit the internal clock speed to a reasonable number for high bandwidth STS3 streams.

The byte align block is an auxiliary block acting as a simple barrel shifter to align the incoming bytes according to the rxstoh_proc block's requests.

FIGURE 14. GENERAL COMPOSITION OF A SONET STS-N RECEIVER
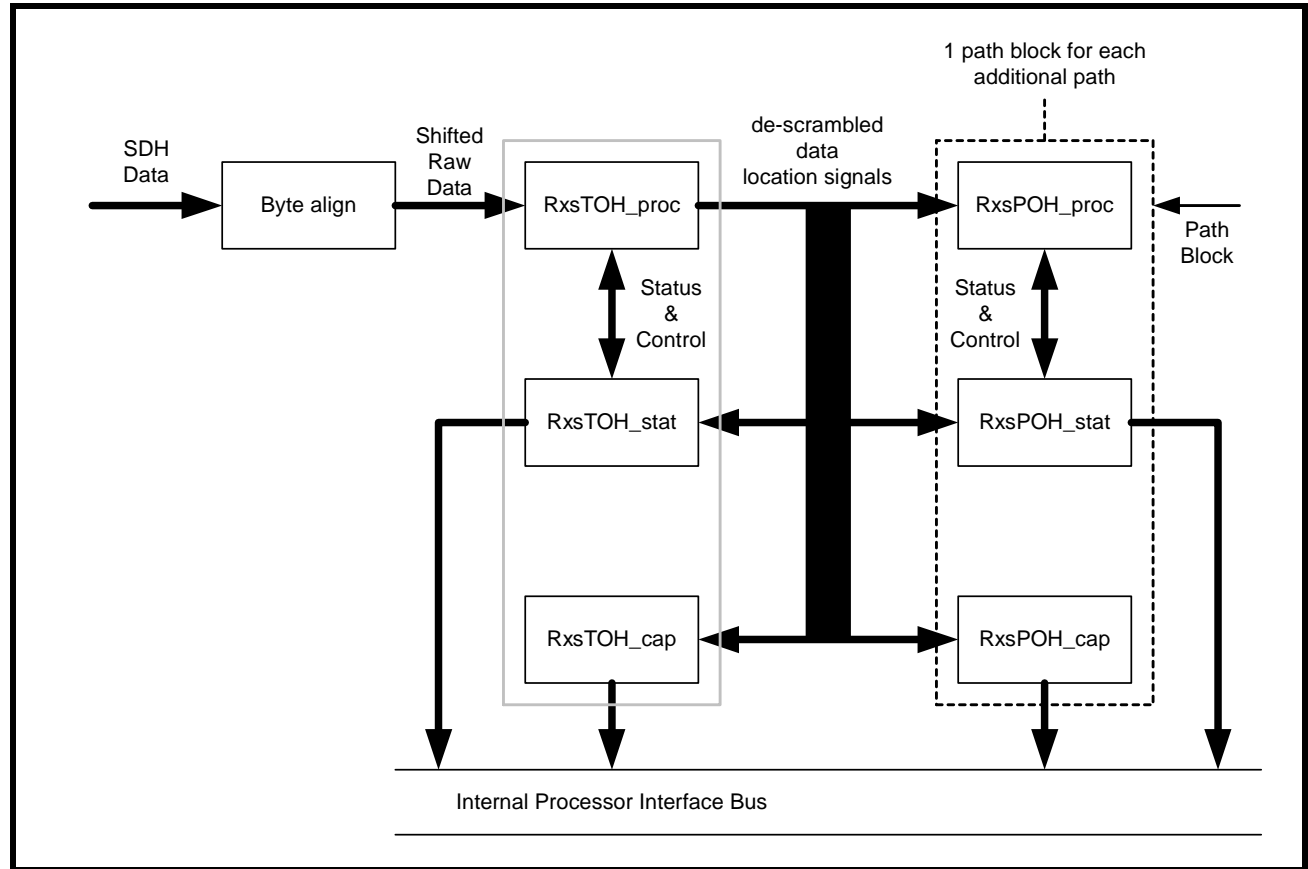
4.5 VT MAPPER

The VTM VT/TU Mapper block is designed to map T1/E1 signals into a SONET VT1.5 and/or VT2 structured in VT Groups or an SDH VC-11 and/or VC-12 to AU-3 which in turn can be mapped respectively into an STS1/STM-0 or into an aggregate/channelized STS3/STM-1. In addition, T1/E1 can also be map to an SDH VC-11 and/or VC-12 to TUG-3 which in turn can be mapped respectively into an STM-1. This reusable block provides all of the functions necessary to insert and drop any valid VT combination of up to 28 asynchronous T1 or up to 21 asynchronous E1 signals to or from a SONET STS1 Synchronous Payload Envelope or an SDH STM-0 VC-3 / STM-1 VC-4 Payload Capacity.

On the STS1/STS3 side, the reusable block has an 8-bit data bus. This allows it to interface to the other blocks that will process the higher layers of overhead. On the T1/E1 side, this block has bit serial data inputs and outputs. The VTM contains built-in test pattern insertion and drop capabilities that allow end-to-end testing for initial setup or maintenance without the need for external test equipment. Built-in loopbacks on both sides provide maximum flexibility for use in a number of SONET or T1/E1 products including terminal multiplexers, add/drop multiplexers, or digital cross connects. A high-speed microprocessor interface and full user programmability for VT/TU slot insertion and drop control provide maximum flexibility for T1/E1 configuration.

FIGURE 15. TOP LEVEL BLOCK DIAGRAM
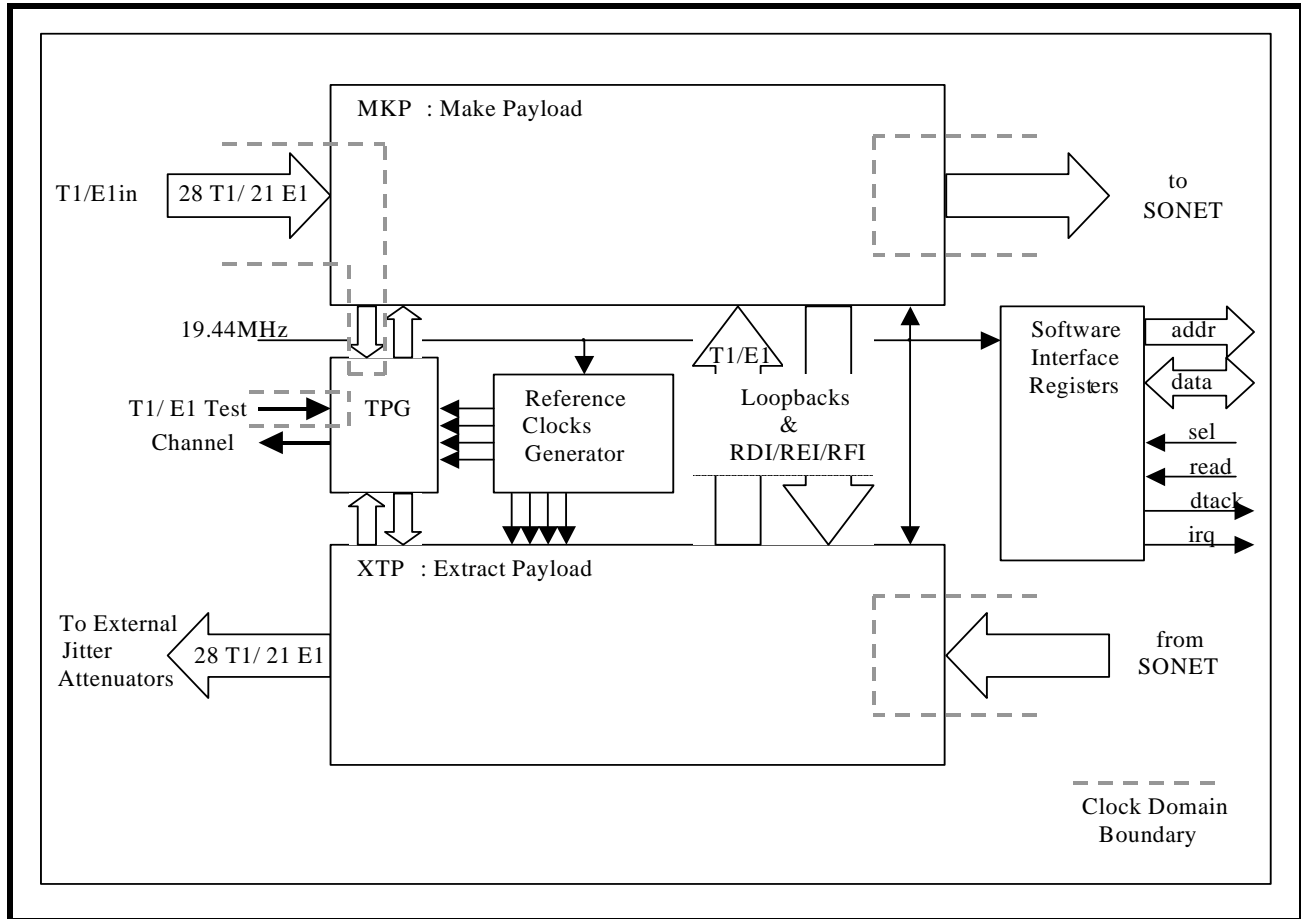
The T1/E1 to SONET section shown in the top part of **Figure 15**, handles the deserialization of the up to 28 T1/21 E1 incoming signals. It handles the VT Path Overhead (SDH: VC Path Overhead) processing and Fixed Stuff insertion to generate a byte-serial stream on the 8-bit mid bus ready to be processed by the Path, Line and Section Overhead processing blocks to produce an STS1 or STS3 signal.

The SONET to T1/E1 section shown in the bottom part of **Figure 15** accepts a byte-serial stream on the mid bus, removes the Fixed Stuff and extracts the Virtual Tributaries (SDH: Tributary Units) to create up to 28 T1/21 E1 signals with gapped clocks.

4.6   *INTERRUPTS AND STATUS*

An interrupt pin (INT) is provided for microcontroller interface. This interrupt pin provides interrupts in response to alarm conditions, error events, messages received, error counter overflows, synchronization indication, and parity errors. The interrupt scheme is organized in a Hierarchical Status Reporting architecture to provide a means for a microcontroller to identify the source of interrupt. Status registers record the latest situation of condition events. An interrupt will be generated if the ENABLE bit corresponding to a given status is set in the interrupt enable register.

Each block contains several sources of interrupts. These interrupts are first multiplexed at the block level. Then the interrupts from different blocks are integrated to generate an interrupt signal on the INT pin. The multiplexing of these interrupts is thus at two levels:

1.   Source Level.

2.   Block Level

At the source level, interrupts may be individually enabled or disabled. All interrupts in a block are multiplexed to produce a block level interrupt. These block level interrupts may then be separately enabled or disabled. **Figure 16** is a simplified block diagram of the status reporting hierarchy.

FIGURE 16. INTERRUPT HIERARCHY
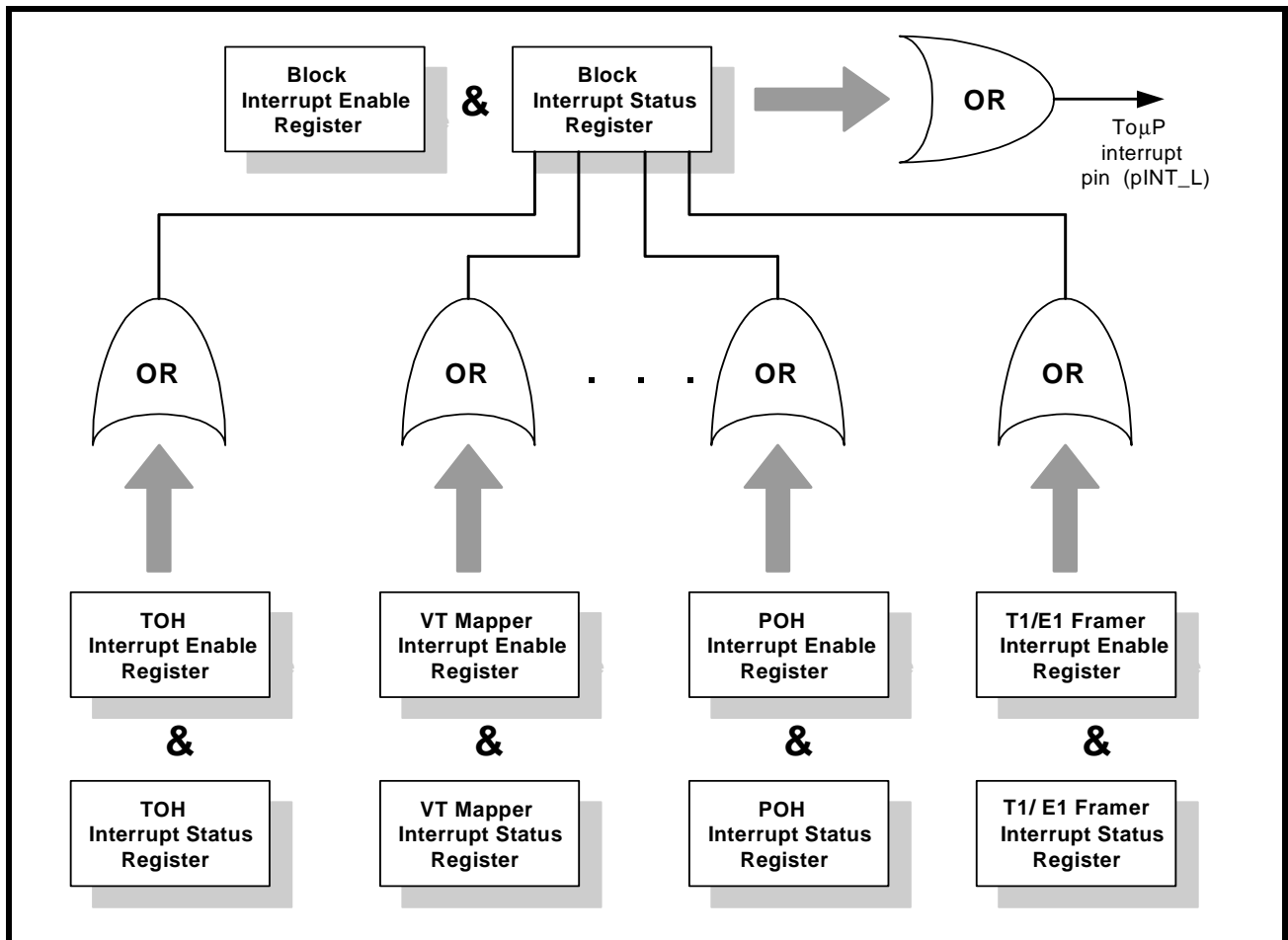
4.7   INTERRUPT PROCESSING AND CONTROL

Each time an interrupt occurs, a microprocessor can identify the source of the interrupt by searching through the status hierarchy. The search will cause the status register on the search tree to be read. Reading of the leaf status register will clear the ENABLE bit(s) associated with the interrupting status bit(s) if the ENBCLR bit in Interrupt Control Register is set.   This will prevent continuous interrupts to be generated once the microcontroller services the status register. Reading of the leaf status register will also reset the status bit(s) if the Reset Upon Read (RUR) option in the Interrupt Control Register has been enabled. Otherwise, a write is required to clear the bit(s) in the status registers. To clear the bit(s) in the status registers, the microcontroller needs to write a mask (0 to mask and 1 to clear) to this register to identify the bit that it wants to clear.

STATUS POLLING

The SONET framer supports status polling capability for all status registers. The operation is executed by preceding a read of these registers with a write. When a one is written to a bit position, the read register will be updated with the current value and the status bit will be cleared. When a zero is written to a bit position, the read register will not be updated and the previous value will be held. This scheme allows an external microcontroller to individually poll certain bits without modifying the other bits in the register.

4.8   STS1/STS3 RECEIVE TRANSPORT PROCESSOR

RXSTOH_PROC BLOCK

The rxstoh_proc block has an 8 bit internal interface bus. The rxstoh_proc block performs the following functions: Byte alignment, LOS detection, frame alignment, de-scrambling, BIP processing, and line RDI and AIS detection. The rxstoh_proc block also generates location signals for the rest of the SONET receive blocks.

BYTE_ALIGN BLOCK

The byte_align block acts as a barrel shifter which shifts the parallel SONET input stream according to requests from the framer in the rxstoh_proc block. **Figure 17** shows the functional diagram of the byte_align block.

FIGURE 17. BYTE_ALIGN BLOCK FUNCTIONAL DIAGRAM
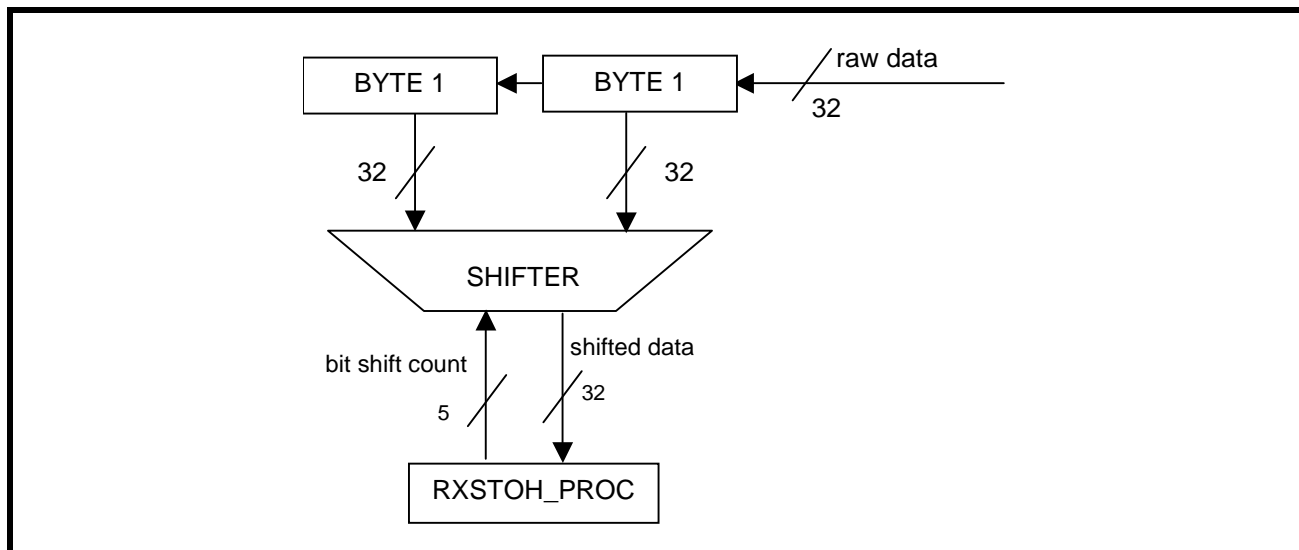
LOS (Loss of Signal) DETECTION

The rxstoh_proc block monitors the incoming scrambled data for the absence of 1's. The SONET standard has the following two rules for handling LOS defects which are observed by the rxstoh_proc block.

- A SONET NE shall monitor all incoming SONET signals (before de-scrambling) for an "all-zeros pattern," where an all-zeros pattern corresponds to no light pulses for OC-N optical interfaces and no voltage transitions for STS1 and STS3 electrical interfaces. A LOS defect shall be detected when an all-zeros pattern on the incoming SONET signal lasts 100μs or longer. If an all-zeros pattern lasts 2.3μs or less, a LOS defect shall not be detected.

- A SONET NE shall terminate a LOS defect when the incoming signal has two consecutive valid framing alignment patterns and during the intervening time (one frame), no all-zeros pattern qualifying as a LOS defect exists.

The rxstoh_proc block allows the software to specify the number of all zero bytes before a LOS defect is declared and clears the LOS defect when the conditions stated are satisfied.

The rxstoh_proc block also monitors the LOPC (loss of optical carrier) input which when asserted, causes the rxstoh_proc block to automatically assert AIS downstream (this feature is programmable by software). This feature is useful when the off-chip optical instrument has detected a loss of carrier but the amplifier data output to the chip still contains random transitions.

FRAME ALIGNMENT

The rxstoh_proc block monitors the incoming stream for A1 and A2 patterns to determine frame alignment. The following SONET standard rules concerning finding frame alignment are observed by the rxstoh_proc block.

- The A1 byte shall be set to '11110110' (Hex F6) and the A2 byte shall be se to '00101000' (Hex 28) in all STS1's within an STS-N.

- The framing pattern observed by an SONET NE shall include a subset of the A1 and A2 bytes contained in the incoming STS-N electrical or OC-N signal.

- An SEF defect shall be detected when the incoming signal has a minimum of 4 consecutive erred framing patterns. The maximum SEF detection time shall be 625μs for a random signal.

- The framing algorithm used to check the alignment shall be such that an SEF defect is not detected more than an average of once every 6 minutes while the BER of the STS-N electrical or OC-N signal is 10^{-3}.

- Once an SEF defect has been detected, the SONET NE shall terminate the SEF defect upon detecting two successive error-free framing patterns.

- All incoming SONET signals shall be monitored for LOF. A SONET NE shall detect an LOF defect when an SEF defect on the incoming SONET signal persists for 3ms.

- The SONET NE shall terminate an LOF defect 1ms to 3ms after terminating the SEF defect on the incoming SONET signal, if the SEF defect is not (re)detected before the LOF defect is terminated.

The rxstoh_proc block implements the optional 3ms integration timer to deal with SEF and LOF defects. The integration timer consists of an SEF timer and an in-frame timer that operates as follows:

The in-frame timer is activated (accumulates) when an SEF defect is absent. It stops accumulating and is reset to zero when an SEF defect is detected. The SEF timer is activated (accumulates) when an SEF is present. It stops accumulating when the SEF defect is terminated. It is reset to zero when the SEF defect is absent continuously for 3ms (i.e., the in-frame timer reaches 3ms). An LOF defect is detected when the accumulated SEF timer reaches the 3ms threshold. Once detected, the LOF defect is terminated when the in-frame timer reaches 3ms (24 frames).

When SEF is low (i.e., the framer currently has frame alignment), the rxstoh_proc block allows the software to specify the number of correct A1 fields that must be followed by the same number of correct A2 fields for the framing pattern to be considered correct. When the rxstoh_proc is searching for frame (i.e., the SEF defect has been declared), all bits of all the A1 and A2 bytes must be correct in order for the A1 or A2 byte to be considered valid.

Once a frame has been located, the rxstoh_proc block outputs the current row, column, and time slot of the de-scrambled data. Note that for the 8-bit version of rxstoh_proc, a time slot is the same as an STS slot where as for the 32-bit version of rxstoh_proc, each time slot contains 4 STS slots (byte lanes). The software can also force the SEF condition which causes the rxstoh_proc to re-find frame.

Alternatively, the SONET framer also monitors a frame pulse input. When the frame pulse input is asserted, the framer automatically assumes the current byte on the input data bus is the first A1 byte.

The software can force the SEF condition in the framer in the rxstoh_proc block by writing a "1" to the appropriate register file bit. This causes the rxstoh_proc block to declare an SEF alarm and re-find frame. The bit is cleared after the rxstoh_proc block has rediscovered frame alignment (after at least 1 frame) and the SEF alarm has been removed.

De-scrambling

The rxstoh_proc de-scrambles all bytes of the incoming stream except for theA1, A2, and J0/Z0 bytes. The following SONET standard rule is observed by rxstoh_proc. De-scrambling can be disabled via software.

SONET interface signals shall be scrambled (i.e., scrambled at the transmitter and de-scrambled at the receiver) using a frame synchronous scrambler of sequence length 127, operating at the line rate. The generating polynomial for the scrambler shall be $1+x6+x7$. The scrambler shall be reset to '1111111' on the most-significant bit of the byte following the Z0 byte in the Nth STS1 (i.e., the byte following the last Z0 byte). That bit and all subsequent bits to be scrambled shall be added, modulo 2, to the output from the x7 position of the scrambler. The scrambler shall run continuously from that bit on throughout the remainder of the STS-N frame.

BIP Processing

The rxstoh_proc block calculates BIP-8 over the pertinent bytes of the incoming stream for comparison with both the B1 and B2 fields of the transport overhead. The B1 and B2 values are calculated according to the following SONET standard rules:

- The B1 byte in a line-side signal shall carry a BIP-8 code, using even parity. The section BIP-8 shall be calculated over all bits of the previous STS-N frame after scrambling and placed in the B1 byte of the current STS-N frame before scrambling.

- The B2 byte shall be provided in all STS1's within an STS-N to carry a Line BIP-8 code, using even parity. The Line BIP-8 shall be calculated over all bits of the Line Overhead and the Synchronous Payload Envelope of the previous STS1 frame before scrambling, and placed in the B2 byte of the current STS1 frame before scrambling.

The rxstoh_proc block outputs an error mask to the rxstoh_stat block after each comparison with B1/B2. Note that only the first B1 byte of an STS-N stream contains the BIP-8 bits. The second through the Nth B1 bytes are all undefined. The number of B2 bytes is equal to the number of STS1's within the STS-N signal. Two memories are used in the B2 error code calculations. One memory is used to store the running value of the B2 error calculations. This memory is a 12x8/32 dual port RAM with one port for reads and one port for writes. This is necessary because as the hardware is calculating the B2 code for each STS1, it needs to store the new value into the memory and at the same time fetch the current code for the next STS1 from memory. The second memory is a single port 12x8/32 RAM used to store the final B2 codes for all the STS1's. This memory is read at the B2 byte locations for comparisons and written into the A1 byte locations to store the final B2 codes for the previous frame. For the 8 bit version of the rxstoh_proc block, the B2 RAM widths are 8 bits. For the 32 bit version of rxstoh_proc block, the B2 RAM widths are 32 bits.

LINE RDI AND AIS DETECTION

The rxstoh_proc block monitors the 3 least significant bits of the first K2 byte for RDI-L and AIS-L detection. The AIS-L detection algorithm follows the following SONET standard rules:

- LTE shall detect an AIS-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte contain the '111' pattern in 5 consecutive frames

- LTE shall terminate the AIS-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte have any pattern other than '111' in five consecutive frames.

NOTE: *The number of consecutive observations is 5. Also, bits 6, 7 and 8 in the SONET standard refer to the least significant 3 bits. The RDI-L detection algorithm follows the following SONET standard rules:*

- LTE shall detect an RDI-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte contains the '110' pattern in 5 to 10 consecutive frames

- LTE shall terminate the RDI-L defect on the incoming signal when bits 6, 7, and 8 of the K2 byte have any pattern other than '110' in five to 10 consecutive frames.

DOWNSTREAM AIS INSERTION

The rxstoh_proc block will insert path AIS-P in the downstream data when prompted by the rxstoh_stat block.

RXSTOH_STAT BLOCK

The rxstoh_stat block has an 8 bit internal bus. The rxstoh_stat block contains the status and control registers for the Transport overhead blocks. In addition, the rxstoh_stat block monitors the S1, REI-L, and K1/K2 fields of the Transport overhead. The rxstoh_stat block also monitors the B1 and B2 error masks and accumulates the bit or word error events.

SYNCHRONIZATION STATUS (S1) MONITOR

The rxstoh_stat block extracts the synchronization status (S1) byte from the line overhead and monitors it for change. The S1 byte is only defined for the first STS1 in an STS3 signal. The extraction algorithm is defined by the SONET standard as:

- A change in the S1 synchronization status message shall be detected if at least 8 consecutive samples (these may or may not be consecutive SONET frames) of bits 5-8 (least significant 4 bits) of the S1 byte have the same (new) value. The sampling rate shall be such that the maximum time to detect a change (assuming no transmission errors) is 1 second.

- For S1 messages, if no validated synchronization status message is detected (e.g., due to transmission errors or the receipt of an undefined message) for a period of greater than 10 seconds, the NE shall consider the reference failed.

The rxstoh_stat block monitors the S1 byte for 8 consecutive identical values after which the new value is stored in a register for access by software. The rxstoh_stat block also implements a counter for an unstable S1. This counter is incremented for each byte that differs from the previously received byte. An invalid S1 condition is declared when the S1 counter reaches 32. The S1 counter is cleared to 0 when 8 consecutive identical S1 bytes are received. Upon detection of an invalid S1 condition, the software can then set up a 10s timer to detect for S1 reference failure.

REI-L (M0/M1) MONITOR

The M0/M1 field contains the line remote error indicator (REI-L) count. For an STS1 stream, the count is contained in the first REI-L byte (M0 byte) whereas for an STS3 or higher stream, the count is contained in the third REI-L byte (M1 byte). The rxstoh_stat block interprets the REI-L field according to the following SONET standard rules:

- LTE terminating an OC-1 or STS1 electrical signal shall set bits 5 through 8 of the M0 byte to indicate (to the upstream LTE) the count of the interleaved-bit block errors that it has detected based on the BIP-8 (B2) byte. The error count shall be a binary number from zero (i.e., 0000) to 8 (i.e., 1000). The remaining seven values represented by the four REI-L bits (i.e., 1001 through 1111) shall not be transmitted, and shall be interpreted by receiving LTE as zero errors.

- LTE terminating an OC-N or STS-N electrical signal (N greater than or equal to 3) shall set the M1 byte to indicate (to the upstream LTE) the count of the interleaved-bit block errors that it has detected using the B2 bytes. For values of N below 48, the error count shall be a binary number from zero to 8xN. The remaining possible values [i.e., 255-(8xN)] represented by the eight REI-L bits shall not be transmitted and shall be interpreted by the receiving LTE as zero errors. For N equal to 48, the count shall be truncated at 255.

The rxstoh_stat accumulates the REI-L counts in a 20 bit saturation counter. The count is transferred to a holding register and reset by software request. The rxstoh_stat also flags any non zero REI-L counts. The

software can configure the rxstoh_stat block to accumulate either bit errors or error events. An error event is defined as any non-zero REI-L count.

Since 8000 frames are received each second and the maximum REI-L count of each frame is 255, the software should poll (and clear) the M1 counter at least once every $2^{32}/(8000 \times 255)$ = 2105 seconds.

K1/K2 MONITOR

The rxstoh_stat block filters and captures the first K1 and K2 bytes of the STS-N stream for APS processing by the software. The filtering is done based on the following SONET standard rule:

- A new code on the received K1 and K2 bytes shall replace the current received code if it is received identically in five consecutive frames.

In addition, rxstoh_stat also monitors the K1 byte for inconsistent APS byte error according to the following definition of the SONET standard.

"An inconsistent APS byte occurs when no three (five) consecutive K1 bytes of the last 12 successive frames are identical, starting with the last frame containing a previously consistent byte."

When an inconsistent APS byte occurs, a flag is set to notify the software. When a new K1/K2 code is detected, a flag is set to notify the software.

B1 ERROR MONITOR

The rxstoh_stat block monitors the B1 error mask from the rxstoh_proc block and accumulates the error count in a 16 bit saturation counter. Upon software request, the count is transferred to a holding register and reset. The software specifies whether to accumulate B1 error bits or events where an error event is defined as any non-zero B1 error mask received from the rxstoh_proc block. A flag is set to notify the software whenever a B1 error event occurs.

Since 8000 frames are received each second and the maximum B1 error count of each frame is 8, the counter will saturate after $2^{32}/(8000 \times 8)$ = 67108 seconds

B2/SD/SF ERROR MONITOR

The rxstoh_stat block accumulates the B2 error count using a 32 bit counter in the same manner as the B1 error counter. Since 8000 frames are received each second and the maximum B2 error count of each frame is 384, the software should poll (and clear) the M1 counter at least once every $2^{32}/(8000 \times 384)$ = 1398 seconds.

In addition, the rxstoh_stat block monitors BIP-2 codes for Signal Fail (SF) and Signal Degrade (SD) conditions. The SD/SF monitoring is done using a discretized sliding window protocol in which the sliding window size is de-composed into 8 sub-intervals. SD/SF is declared if the total B2 error count of all the sub-intervals exceeds a given threshold. Similarly, SD/SF is cleared when the total B2 error count is below a given threshold. In addition, the user can specify a burst tolerance threshold for each sub-interval. The B2 error count for each sub-interval is saturated at the burst tolerance threshold. The window size and thresholds for declaring and clearing SD/SF alarms are specified separately. The window size and thresholds for SD and SF are also specified separately. As a result, 4 sliding windows are needed. The sliding window is implemented by the rxstoh_berm block, 4 of which are instantiated by the rxstoh_stat block.

The setting and clearing of the SF and SD signals adhere to the following SONET standard rules and recommendations:

- Loss of Signal, Loss of Frame, AIS-L defects, and a Line BER exceeding 10^{-3} on an incoming OC-N shall be detected as SF conditions on that line.

- The BER threshold for an SF condition may be required to be user-provisionable over the range of 10^{-3} to 10^{-5}

- A BER exceeding the SD threshold on an incoming OC-N shall be detected as an SD condition on that line

- The BER threshold for an SD condition shall be user-provisionable over the range of 10^{-5} to 10^{-9}

The rxstoh_stat block lets software specify the time interval over which to monitor the B2 error counts and the thresholds over/under which to set/clear the SF and SD conditions.

SEF FORCE

Software can force the SEF condition in the frame finder in the rxstoh_proc block by writing a "1" to the appropriate register file bit. This causes the rxstoh_proc block to re-find frame. The bit is cleared after the rxstoh_proc block has rediscovered frame alignment (after at least 1 frame).

SECTION TRACE (J0) MONITOR

The SONET standard has defined the J0 byte as a 1 byte or 16 byte message in the following manner:

This byte is used to transmit repetitively a Section Access Point Identifier so that a Section receiver can verify its continued connection to the intended transmitter. Within a national network, or within the domain of a single operator, this Section Access Point Identifier may use either a single byte (containing the code 0-255) or the Access Point Identifier format as defined in clause 3/G.831. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport.

A 16-byte frame is defined for the transmission of Section Access Point Identifiers where these conform to the definition contained in clause 3/G.831. The first byte of the string is a frame start marker and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 T.50 characters (international Reference Version) required for the Section Access Point Identifier. The 16 byte frame description is given in the table below:

TABLE 1: 16-BYTE FRAME FOR TRAIL APID

BYTE #	VALUE (BIT 1, 2, … ,8)						
1	1	C1	C2	C3	C4	C5	C6	C7
2	0	X	X	X	X	X	X	X
3	0	X	X	X	X	X	X	X
:	:			:			
16	0	X	X	X	X	X	X	X

NOTES:
1. C1 to C7 is the result of the CRC-7 calculation over the previous frame. C1 is the MSB. The description of this CRC-7 calculation is given in Annex B
2. 0XXXXXXX represents a T.50 character.

.2

In the case of inter-working of equipment implementing the STS identifier functionality and equipment employing the Section Trace function, the latter shall interpret the pattern "0000001" in J0 as "Section Trace - unspecified". This unspecified Section Trace can also be used if no use of the Section Trace is made.

The rxstoh_stat block enables software to specify the length of the J0 section trace message. This length could be 1 or 16 for SONET, and 64 should the SONET standard in the future specify the J0 byte as a Section Trace Byte. The software also specifies whether to look for an LF or a starting "1" bit when the rxstoh_stat block is trying to locate the start of the message. The software also specifies the number (3 or 5) of consecutive consistent Section Trace messages that must be observed before it is accepted.

An interrupt is generated when a new Section Trace message is accepted as valid. The valid Section Trace message is compared with an expected Section Trace message downloaded to memory by software. A J0 mismatch (J0_MIS) flag is raised if the 2 messages are not identical. The rxstoh_stat block also implements a J0 unstable counter. The J0 unstable counter is incremented for each byte that differs from the previously received byte. An invalid J0 condition is declared when the J0 unstable counter reaches 8. The J0 unstable counter is cleared to 0 when a valid J0 is accepted.

The SONET receive section trace buffer uses a 128x8 single port memory and a 64x8 single port memory. The memories are organised as shown in **Figure 18**. The 128x8 single port ram has 2 segments:

■ One segment stores the current accepted trace message

■ One segment stores the previous received trace message

The 64x8 single port ram stores the expected trace message which is downloaded by the CPU.

Whenever a new trace message is accepted as valid, the valid message buffer and the previous message buffer swap in the sense that what used to be the valid message buffer segment is now the segment for storing the previous received message and vice versa. The CPU downloads new expected trace messages to the new expected message buffer. Since comparisons between the expected trace message buffer and the accepted trace message buffer are not valid when the CPU is downloading to the expected trace message buffer, the J0 mismatch interrupt should be disabled during downloading of the expected trace message buffer.

FIGURE 18. RECEIVE TRACE BUFFER MEMORY
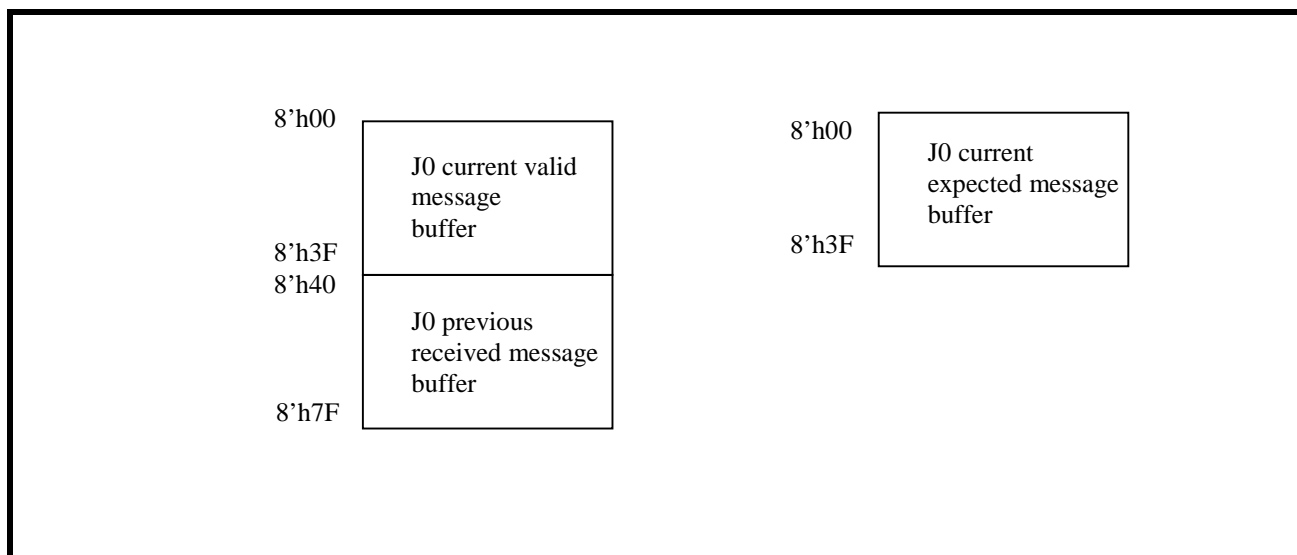
DOWNSTREAM AIS INSERTION CONTROL

The rxstoh_stat block can be configured to cause downstream AIS insertion when any of the following conditions are detected: AIS-L, LOS, LOF, LOPC, SD, SF, J0 mismatch, and J0 unstable. Downstream AIS insertion to the path section is done according to the following SONET standard:

■ LTE shall generate AIS-P downstream for the affected STS paths within 125µs of detecting an AIS-L defect (or a lower layer, traffic-related, near-end defect) or (if the STS pointer is processed) an LOP-P defect on the incoming signal, or the failure of STS PTE supporting provisioned path origination functions. The AIS-P shall be generated as all-ones in the H1, H2 and H3 bytes, and the entire STS SPE.

■ LTE shall deactivate the AIS-P within 125µs of terminating the defect that caused it to be sent, or in the case of a local equipment failure, within 125µs of clearing the failure or determining that standby equipment has been switched in. LTE that performs STS pointer processing shall deactivate AIS-P by constructing a correct STS pointer with a set NDF, followed by normal pointer operations, as well as ceasing to insert the all ones pattern in the STS SPE. LTE that does not perform STS pointer processing shall deactivate AIS-P by ceasing the insertion of all ones in the H1, H2 and H3 bytes, and the STS SPE.

The software can enable or disable the insertion of path AIS-P on detection of any of the aforementioned conditions. If path AIS insertion is necessary, then an enable signal to the rxstoh_proc block is activated which causes the rxstoh_proc block to insert all ones in the pertinent bytes.

RXSTOH_CAP BLOCK

The rxstoh_cap block has an 8 bit internal interface bus. The rxstoh_cap block captures the contents of the SONET overhead for up to 3 STS1 slots and stores them for access by the external processor. On a read access from the processor interface, the bit rxstoh_cap block accepts a 9 bit address of the form: xxxxxyyyy where xxxxx specifies the field number and yyyy specifies the time slot number of the 4 bytes that are requested.

One 944x8 (STS3) or 256x8 (STS1) single port RAM is used to capture and hold the SONET OH contents for the processor of each byte-slice module. The memory is divided into one 512 x 8 (only 432 is used) and one 432 x 8 segments. One segment captures the SONET overhead bytes from the current frame while the other segment stores the transport overhead bytes from the previous frame. The two segments are swapped after every frame in the sense that what used to be the current SONET OH byte capture segment is now the holding segment for the previous frame and vice versa.

When the last SONET overhead byte of the current frame has been written into memory, an interrupt is generated to notify the software. The contents of the SONET overhead memory will be preserved for one frame (i.e., until the next SONET OH capture generates an interrupt) for access by the software.

The captured SONET OH bytes are available to the processor via indirect memory registers. The addressing scheme used to access the SONET OH bytes is shown in **Table 2**. Each access to a captured SONET OH byte consists of writing the corresponding address into the SONET OH capture indirect address register followed by a read/write to/from the SONET OH capture indirect data register.

TABLE 2: ADDRESSING SCHEME USED TO ACCESS THE SONET OH BYTES

ADDR[9:2]	Byte 3 (MSB)	Byte 2	Byte 1	Byte 0 (LSB)
{5'h00, 2'h0}	A1 (STS-0)	A1 (STM-0)	A1 (STS-2)	A1 (STM-1)
{5'h00, 2'h1}	A1 (STS-4)	A1 (STS-5)	A1 (STS-6)	A1 (STS-7)
{5'h00, 2'h2}	A1 (STS-8)	A1 (STS-9)	A1 (STM-00)	A1 (STM-01)
{5'h00, 2'h3}	unused	unused	unused	Unused
{5'h01, 2'h0}	A2 (STS-0)	A2 (STM-0)	A2 (STS-2)	A2 (STM-1)
{5'h01, 2'h1}	A2 (STS-4)	A2 (STS-5)	A2 (STS-6)	A2 (STS-7)
{5'h01, 2'h2}	A2 (STS-8)	A2 (STS-9)	A2 (STM-00)	A2 (STM-01)
{5'h01, 2'h3}	unused	unused	unused	Unused
. . .	. . .	. . .	. . .	. . .
{5'h1A, 2'h0}	E2	byte 26 (STM-0)	Byte 26 (STS-2)	byte 26 (STM-1)
.	.	.	.	.
{5'h1A, 2'h2}	byte 26 (STS-8)	byte 26 (STS-9)	byte 26 (STM-00)	byte 26 (STM-01)
{5'h1A, 2'hC}	unused	unused	unused	unused
. .	. .	. .	. .	..

When this module is used for the STS1 or STS3 port, the captured SONET overhead bytes are serialized and sent as outputs from the chip (with the exception of the M0 byte which is replaced by the more useful M1 byte from the third STS1). The bytes are multiplexed onto a single bit stream as shown in **Figure 19**. The RxOH,

RxOHFRAME, and RxOHVALID signals are updated on the falling edge of RxOHCLK. When used on the STS1/STS3 side, the bytes captured are sent out to the external interface through an 8-bit bus.

FIGURE 19. RECEIVE TRANSPORT OVERHEAD INTERFACE TIMING
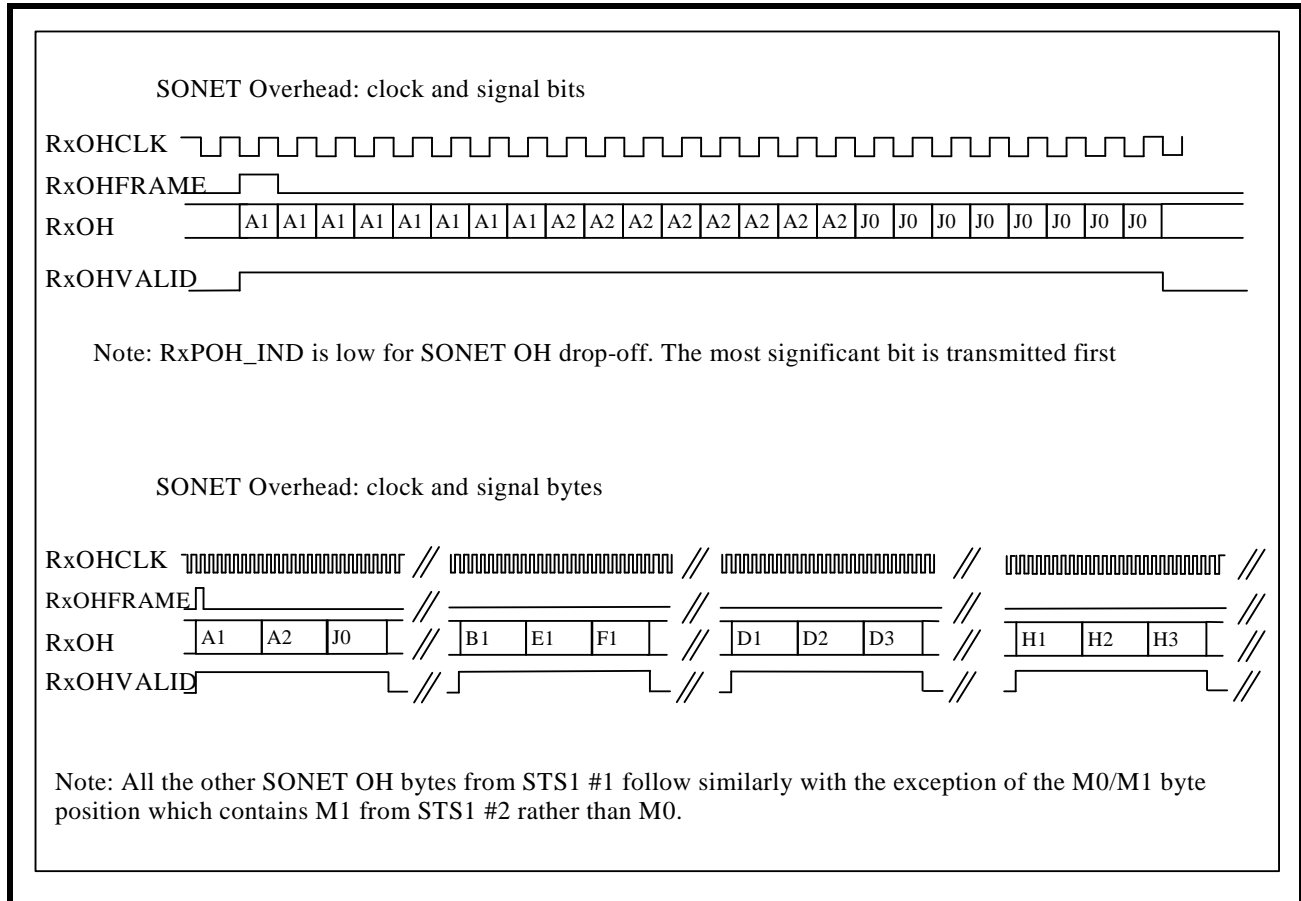
STS1/STS3 RECEIVE PATH PROCESSOR

RXSPOH_PROC BLOCK

The pointer processing operation of the rxspoh_proc block is described by the following SONET standard rules:

- The pointer value shall be a binary number with a range of 0 to 782, and shall indicate the offset between the pointer word (the last byte of the H3 field) and the first byte of the STS SPE.

- A pointer increment operation shall be indicated by inverting the I-bits of the pointer word. The positive stuff byte shall appear immediately after the H3 byte in the frame containing the inverted I-bits.

- A pointer decrement operation shall be indicated by inverting the D-bits of the pointer word. The H3 byte shall be used as the negative stuff byte, (i.e., it is used to carry an SPE byte in the frame containing the inverted D-bits).

- The increment/decrement decision should be made at the receiver by a match of 8 or more of the 10 I- and D-bits to either the increment or decrement indication.

- A normal NDF shall be indicated (during normal operation) by a '0110' code in the N-bits. The NDF shall be set by inverting the N-bits to '1001'. The new alignment of the STS PSE shall be indicated by the pointer value accompanying the set NDF and takes effect at the offset indicated.

- The decoding at the pointer processor shall be performed by majority voting (i.e., the NDF shall be detected as being set if three or four of the N-bits match the '1001' code). If a set NDF is detected, then the coincident pointer value shall replace the current value at the offset indicated by the new pointer value.

- The first STS1 within an STS-Nc shall have a normal pointer word

- All subsequent STS1's within the STS-Nc shall have their pointer values (i.e., bits 7 through 16) set to all-ones, and their N-bits set to '1001' (i.e., set NDFs).

- A pointer processor in an NE that is transmitting or receiving an STS-Nc SPE shall perform the operations indicated by the pointer in the first STS1 of the STS-Nc on all N of the STS1's in that STS-Nc.

- During normal operation, the pointer value locates the start of the STS SPE within the STS Envelop Capacity.

- Any variation from the current pointer value shall be ignored unless a consistent new value is received three times consecutively, or the variation is one of the operations in rules 4, 5, or 6.

- Any consistent new value received three times in succession shall replace the current value at the offset indicated by the new pointer value.

- If the pointer word contains the concatenation indicator, then the operations performed on that STS1 are identical to those performed on the first STS1 within the STS-Nc. Rules 4 and 5 do not apply to this pointer word.

- If an increment is detected, then the byte following H3 shall be considered a positive stuff byte, and the current pointer value shall be incremented by one.

- If a decrement is detected, then H3 shall be considered a negative stuff byte, and the current pointer value shall be decrement by one.

- If a set NDF is detected, then the coincident pointer value replaces the current value at the offset indicated by the new pointer value.

- STS PTE and LTE that processes the STS pointer shall monitor for LOP-P. An LOP-P defect shall be detected if a valid pointer is not found in N consecutive frames (where 8 is less than or equal to N less than or equal to 10), or if N consecutive NDFs (other than in a concatenation indicator) are detected. An LOP-P defect shall not be detected when LTE is receiving and relaying an all-ones STS pointer, or when STS PTE is receiving pointers that qualify as those necessary to cause the detection of an AIS-P defect (i.e., three or more consecutive all-ones pointers)

- STS PTE and LTE that processes the STS pointers shall terminate an LOP-P defect when the STS has a valid pointer with a normal NDF, or a valid concatenation indicator, in three consecutive frames.

- STS PTE shall terminate an LOP-P defect when it detects an AIS-P defect.

■ STS PTE shall detect an AIS-P defect when the H1 and H2 bytes for an STS path contain an all-ones pattern in three consecutive frames. For an STS-Nc path, only the H1 and H2 bytes of the first STS1 need to be observed.

■ STS PTE shall terminate an AIS-P defect when the H1 and H2 bytes for the STS path contain a valid STS Pointer with a set NDF, or when they contain valid, identical STS Pointers with normal NDFs for three consecutive frames. For an STS-Nc path, the concatenation indicators must also be valid.

■ STS PTE should terminate an AIS-P defect when it detects an LOP-P defect.

The rxspoh_proc block chooses N as 8. Note that for a pointer to be considered valid, the following two conditions from the SONET standard need to be satisfied:

"A pointer with an in-range value, the N-bits are set to their normal value."

The SONET standard also provides the following recommendation:

"If a pointer processor detects an increment or decrement operation within three frames after another pointer change operation (e.g. due to transmission errors), it can either ignore that operation or interpret it as a valid operation.

In addition, if the rxspoh_proc is operating in an SONET environment, then the SS bits of the pointer word must be '10'. The above rules can be concisely summarized by the FSM in **Table 3**.

In **Table 3**, the label *n x event_type* denotes an event of event_type occurring in n consecutive pointers. The event types are defined in **Table 3**.

FIGURE 20. POINTER PROCESSING FSM
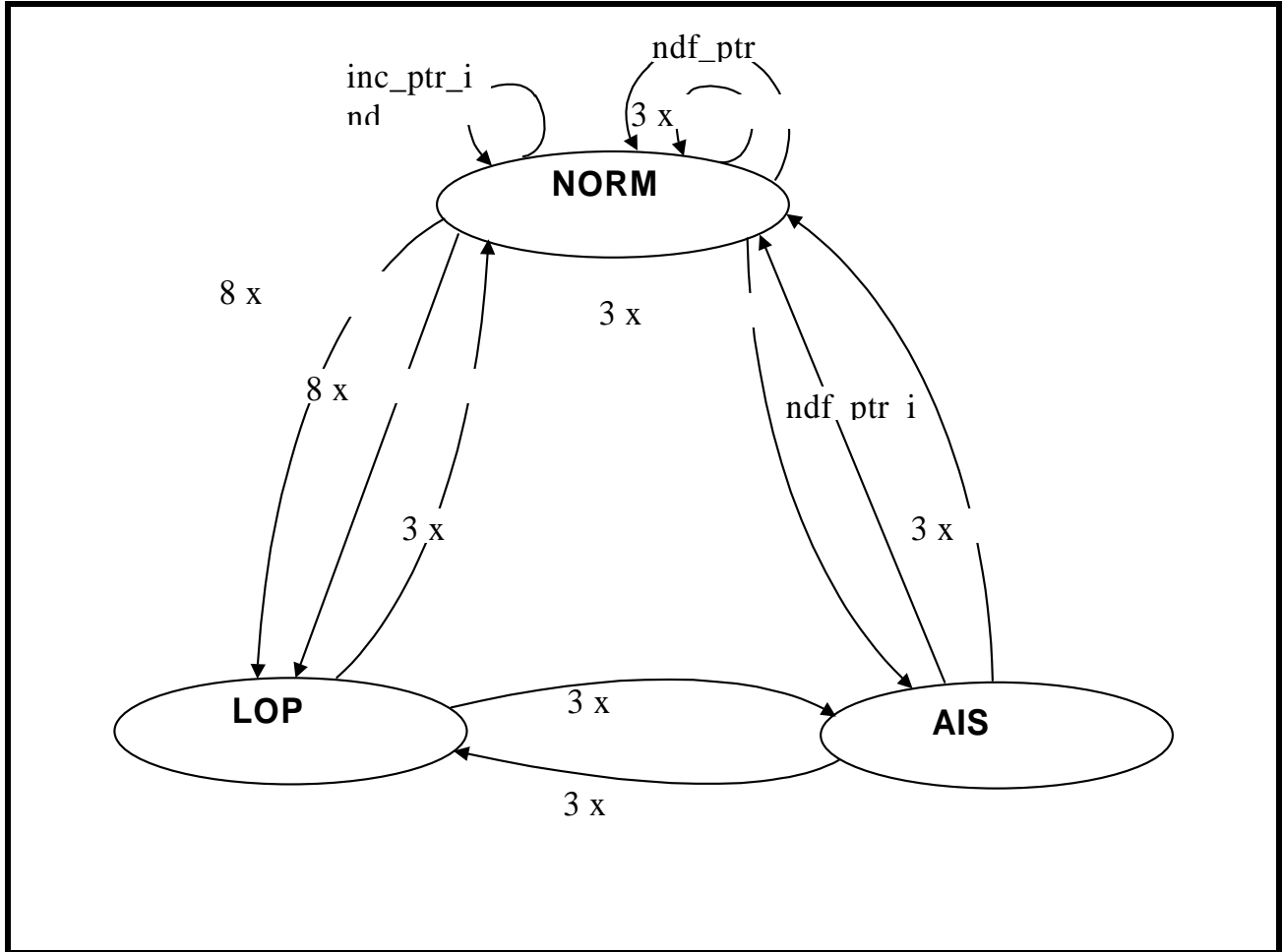
TABLE 3: SONET POINTER EVENT TYPES

EVENT (INDICATION)	DESCRIPTION
norm_ptr_ind	disabled NDF + ss + offset value equal to active offset
ndf_ptr_ind	enabled NDF + ss + offset value in range of 0 to 782.
ais_ptr_ind	H1 = 'hFF', H2 = 'hFF'
inc_ptr_ind	disabled NDF + ss+ majority of I bits inverted + no majority of D bits inverted + previous ndf_ptr_ind, inc_ptr_ind, or dec_ptr_ind more than 3 frames ago
dec_ptr_ind	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous ndf_ptr_ind, inc_ptr_ind, or dec_ptr_ind more than 3 frames ago
inv_ptr_ind	not any of the above
new_ptr_ind	disabled NDF + ss + offset in range of 0 to 782 but no equal to active offset.

B3 PROCESSING

The rxspoh_proc block calculates the path BIP-8 over the pertinent bytes of the incoming stream for comparison with the B3 field of the path overhead. The B3 value is calculated according to the following SONET standard:

- The B3 byte shall carry a BIP-8 code, using even parity. The STS Path BIP-8 shall be calculated over all bits (783 bytes for an STS1 SPE or Nx783 bytes for an STS-Nc SPE, regardless of any pointer adjustments) of the previous STS SPE before scrambling and placed in the B3 byte of the current STS SPE before scrambling.

The rxspoh_proc block outputs an error mask to the rxspoh_stat block after each comparison with B3.

PAYLOAD EXTRACTION

The rxspoh_stat block determines the positions of the payload bytes within each frame and generates the appropriate byte lane enables for the VT Mapper interface.

In an STM signal, the fixed columns are defined as the 3 columns following the POH column . The rxspoh_stat block will detect the arrival of the fixed stuff bytes and will not generate any byte lane enables for the VT Mapper interface during the fixed stuff bytes.

DOWNSTREAM AIS INSERTION

The rxspoh_proc block will insert path AIS in the downstream data when prompted by the rxspoh_stat block.

RXSPOH_CONCAT BLOCK

The rxspoh_concat block has an 8 bit internal bus. The concatenated pointer indicator has the value 1001_1111_1111_1111. The SONET standard gives a recommendation on concatenated pointer processing similar to that of **Figure 21**. In **Figure 21**, the following events are defined:

conc_ind: NDF enabled + ss1111111111

ais_ptr_ind: 11111111 11111111

inv_ptr_ind: Any other.

The rxspoh_concat block processes the concatenation pointer indicator for each STS slot according to **Figure 21** and provides the current concatenated pointer indicator FSM state of each slot via registers.

FIGURE 21. CONCATENATED POINTER INDICATOR PROCESSING FSM
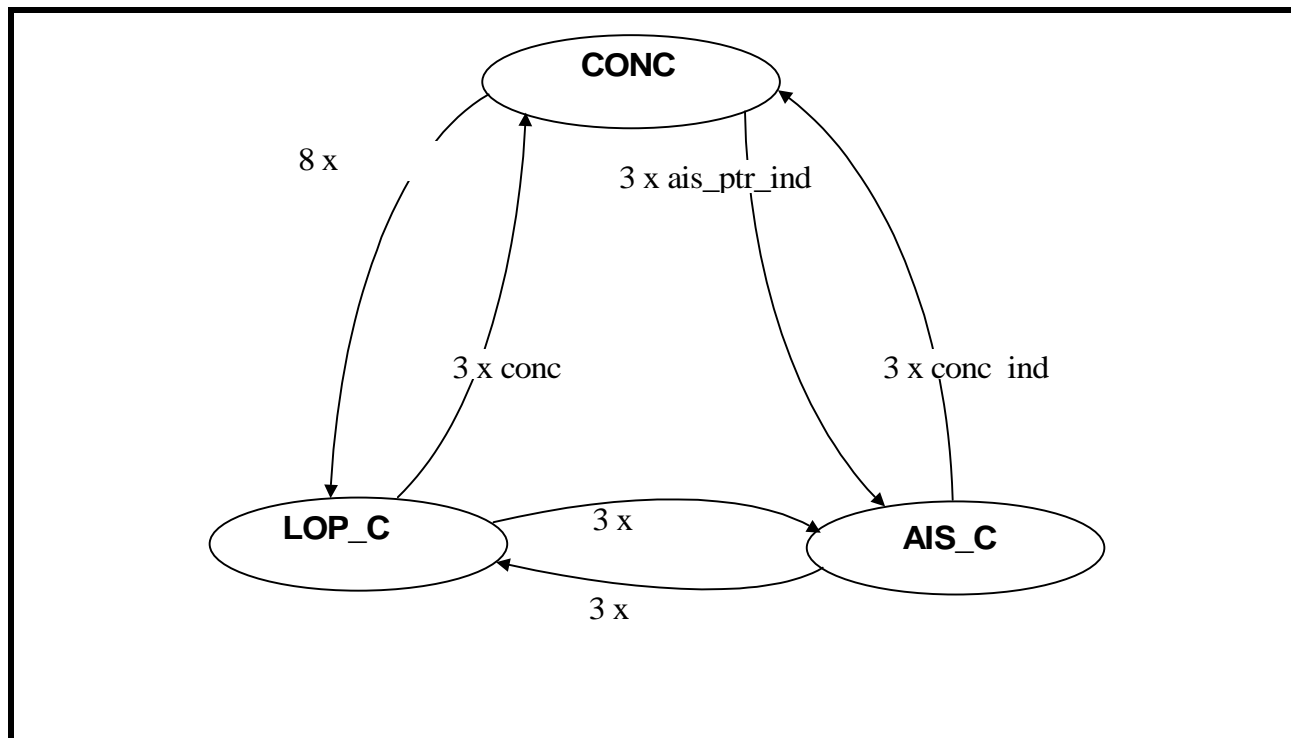
RXSPOH_STAT BLOCK

The rxspoh_stat block captures the status signals from the path overhead blocks and stores them in registers. The rxspoh_proc block also accumulates REI-P counts from the G1 field and stores them in a 32 bit counter.

B3 MONITOR

The rxstoh_stat block monitors the B3 error mask from the rxspoh_proc block and accumulates the error count in a 16 bit saturation counter. Upon software request, the count is transferred to a holding register and reset. The software specifies whether to accumulate B3 error bits or B3 error events where an error event is defined as any non-zero B3 error mask received from the rxspoh_proc block. An interrupt is flagged to notify software whenever a B3 error event occurs.

RDI-P MONITOR

There have been two versions of definition for the path RDI defect in the SONET standard. The older version is called single-bit RDI-P (SRDI-P) and uses only bit 5 (4th least significant bit) of the G1 byte. The current version is called the enhanced RDI-P (ERDI-P)and uses bits 5, 6 and 7 of the G1 byte. The ERDI-P is declared when bits 5, 6, and 7 of the G1 byte contain anything other than '011, 000, 001'. The SONET standard has the following standard with respect to receiving the RDI-P signal:

- STS PTE shall generate an appropriate RDI-P signal, as specified in **Table 4**, within 100ms of detecting a listed defect.
- When STS PTE generates a particular type of RDI-P signal, it shall generate it for at least 10 frames.
- STS PTE that does not support ERDI-P shall detect a one-bit RDI-P defect when a "1" is received in bit 5 of G1 for 10 consecutive frames
- STS PTE that supports ERDI-P shall detect an RDI-P defect when one of the RDI-P defect codes shown in **Table 4** (one-bit or enhanced) is received for 5 to 10 consecutive frames
- STS PTE that does not support ERDI-P shall terminate the one-bit RDI-P defect when a "0" is received in bit 5 of G1 for 10 consecutive frames.

■ STS PTE that supports ERDI-P shall terminate a particular type of RDI-P defect (one-bit or enhanced) when a code other than the code corresponding to that defect is received for 5 to 10 consecutive frames

TABLE 4: RDI-P SETTINGS AND INTERPRETATION

G1 BITS 5, 6 AND 7	PRIORITY OF ERDI-P CODES	TRIGGER	INTERPRETATION
0xx	not applicable (for SRDI-P only, bits 6 and 7 should be '00')	No defects	No RDI-P defect
1xx	not applicable (for SRDI-P only, bits 6 and 7 should be '00')	AIS-P, LOP-P	one-bit RDI-P defect
001	4	No defects	No RDI-P defect
010	3	PLM-P, LCD-P	ERDI-P Payload Defect
101	2	AIS-P, LOP-P	ERDI-P Server Defect
110	1	UNEQ-P, TIM-P	ERDI-P Connectivity defect

The rxspoh_stat block allows software to specify the type of RDI-P error to monitor. The software also programs the number of consecutive consistent RDI-P codes that must be observed before it is accepted as valid. When a new valid RDI-P is detected, a flag is set for software and the RDI-P code that caused the condition is captured in a register. The rxspoh_stat block also implements a RDI-P unstable counter. The RDI-P unstable counter is incremented for each byte that differs from the previously received byte. An invalid RDI-P condition is declared when the RDI-P unstable counter reaches the software specified threshold. The RDI-P unstable counter is cleared to 0 when a valid RDI-P code is accepted.

REI-P MONITOR

Bits 1 through 4 (most significant 4 bits) of the G1 byte are allocated to convey the path REI (REI-P) function and are defined in the SONET standard as:

■ STS PTE shall set bits 1 through 4 of the G1 byte to indicate (to the upstream STS PTE) the count of interleaved-bit block errors that it has detected based on the STS Path BIP-8 byte (B3). The error count shall be a binary number from zero to 8. The remaining seven values shall not be transmitted and shall be interpreted by receiving STS PTE as zero errors.

The rxspoh_stat accumulates the REI-P counts in a 16 bit saturation counter. The count is transferred to a holding register and reset by software request. The rxspoh_stat also flags any non zero REI-L counts. The software can configure the rxstoh_stat block to accumulate either bit errors or error events. An error event is defined as any non-zero REI-P count.

SIGNAL LABEL (C2) MONITOR

The C2 byte is allocated to indicate the contents of the STS SPE and is treated as a signal label. The rxspoh_stat block monitors the C2 byte for several conditions according to the SONET standard.

■ STS PTE shall detect an STS Payload Label Mismatch (PLM-P) defect within 250ms of the onset of at least five consecutive samples (which may or may not be consecutive frames) of mismatched STS Signal Labels (C2 byte), as specified in **Table 5**.
■ STS PTE should detect a PLM-P defect immediately upon receipt of five contiguous frames with mismatched STS Signal Labels, as specified in **Table 5**.
■ STS PTE shall terminate a PLM-P defect within 250ms of detecting the onset of at least five consecutive samples (which may or may not be consecutive frames) of matched STS Signal Labels.
■ STS PTE should terminate a PLM-P defect immediately upon receipt of five contiguous frames with matched STS Signal Labels, as specified in **Table 5**.
■ STS PTE shall terminate a PLM-P defect upon detecting an UNEQ-P defect.

- STS PTE shall detect an STS Path Unequipped (UNEQ-P) defect within 10ms of the onset of at least 5 consecutive samples (which may or may not be consecutive frames) of unequipped STS Signal Labels (C2 byte = 00hex)

- STS PTE should detect an UNEQ-P defect immediately upon receipt of five contiguous frames with unequipped STS Signal Labels, as specified in **Table 5**.

- STS PTE shall terminate an UNEQ-P defect within 10ms of the onset of at least five consecutive samples (which may or may not be consecutive frames) of STS Signal Labels that are not unequipped.

- STS PTE should terminate an UNEQ-P defect immediately upon receipt of five contiguous frames with STS Signal Labels that are not unequipped, as specified in **Table 5**.

TABLE 5: STS SIGNAL LABEL MISMATCH DEFECT CONDITIONS

PROVISIONED STS PTE FUNCTIONALITY	RECEIVED PAYLOAD LABEL (C2 BYTE, IN HEX FORMAT)	DEFECT
Any Equipped functionality (C2 = anything except H00)	Unequipped (00)	UNEQ-P
Any Equipped functionality	Equipped - Non Specific (01)	none (Matched)
Equipped - Non Specific (C2 = H01)	A value corresponding to any Payload Specific functionality	none (Matched)
Any Payload Specific functionality (C2 = anything except H00 or H01)	A value corresponding to the same payload specific functionality as the provisioned functionality	none (Matched)
Any Payload Specific functionality	A value corresponding to a different payload specific functionality as the provisioned functionality	PLM

The rxspoh_stat block allows software to specify the expected signal label and compares it with the observed value. If the values mismatch, then a path label mismatch (PLM) error is declared. If the observed value is 00hex, then a path unequipped (UNEQ) error is declared (and PLM cleared). If the observed value matches the expected value, then PLM is cleared. If the observed value changes, then a flag is set for software. For a C2 label to be considered valid, it must be received in 5 consecutive frames. The rxspoh_stat blocks also implements a C2 unstable counter. The C2 unstable counter is incremented for each byte that differs from the previously received byte. An invalid C2 condition is declared when the C2 unstable counter reaches 5. The C2 unstable counter is cleared to 0 when 5 consecutive identical C2 bytes are received. The rxspoh_stat block implements a mismatch mechanism that can be summarised in **Table 6**.

TABLE 6: TRUTH TABLE FOR PATH LABEL ERROR CONDITIONS

EXPECTED VALUE	RECEIVED VALUE	ACTION
00	00	match
00	01	mismatch
00	XX	mismatch
01	00	UNEQ-P
01	01	match
01	XX	match
XX	00	UNEQ-P
XX	01	match
XX	XX	match
XX	YY	mismatch

PATH TRACE (J1) MONITOR

The J1 byte of the path overhead is used as a path trace identifier. The path trace identifier is monitored using the following SONET standard rules:

- A SONET NE that contains STS PTE shall allow the user to provision, on a per-path basis, the contents of the STS Path Trace carried in the J1 byte of the STS path overhead originated by the PTE. The transmitted STS Path Trace string shall be 64 bytes in length.

- A SONET NE that contains STS PTE shall support a feature that allows the contents of the STS Path Traces to be provisioned as ASCII characters. In addition, the following apply:

- The feature shall allow the user to enter a string of up to 62 characters

- The feature shall place no restriction on the content of the string except that the characters shall be ASCII printable characters

- The NE shall automatically pad the string entered by the user to 62 characters using ASCII NULL characters, and then add <CR> and <LF> characters (i.e., 'OD' and '0A' for a total of 64 characters

- Each 8 bit ASCII character shall be loaded into one J1 byte.

- A SONET NE shall support a feature to allow the user to provision the expected ASCII-based path trace for each STS path that it terminates and for which TIM-P detection has been activated. In addition, the following apply:

    1. The feature shall allow the user to enter a string of up to 62 characters

    2. The feature shall place no restriction on the contents of the string, except that

    3. The characters shall be ASCII printable characters.

- STS PTE shall detect a TIM-P defect within 30 seconds (or less) when none of the sampled 64-byte STS path trace strings match the provisioned expected value.

- STS PTE shall terminate a TIM-P defect within 30 seconds (or less) when four-fifth (or more) of the sampled STS path trace strings match the provisioned expected value

- A SONET NE that is monitoring for changes of the incoming path trace shall detect when a sustained change in the path trace content occurs. Upon detecting a sustained change, the NE shall send a message to an OS. The level of the message shall be Not Alarmed, and it shall include both the previously received path trace, and the new path trace (assuming they are ASCII-based).

- A SONET NE that is monitoring for a mismatch between the incoming path trace and an expected path trace for diagnostics purposes shall detect when a sustained mismatch occurs. Upon detecting a sustained mismatch, the NE shall set an indication for that path and send a message to an OS. The level of the message shall be Not Alarmed, and it shall include both the expected path trace, and the new path trace (assuming they are ASCII-based).

- A SONET that is monitoring the incoming path trace for diagnostic purposes and that has detected a sustained mismatch shall detect when the incoming path trace matches the expected path trace. Upon detecting a match, the NE shall clear the indication for that path and send a clear message to the OS (if the mismatch was reported to an OS).

The SONET standard defines the path trace message length to be a 16 or 64 byte length message. The message format is such that the termination line feed <LF> byte of the message always has the value "0x0A" and for 64 byte messaging to include a carriage return <CR> byte of the value "0x0D" before the <LF> byte, while the preceding bytes in the message can have user specified values. For SDH, the message format is such that the first byte of the message always has a "1" in its most significant bit while the subsequent bytes in the message all have a "0" in their most significant bits. There is no <CR> or <LF> termination bytes in SDH J1 path trace message format.

The rxspoh_stat block allows software to specify the length of the J1 Path Trace message. This length could be 1 or 16 or 64 bytes for SONET. The software also specifies whether to look for an <LF> terminating byte when the rxspoh_stat block is trying to locate the end of the message in SONET or a starting "1" bit when the rxspoh_stat block is trying to locate the start of the message in SDH. Software also specifies the number (3 for

SONET or 5 for SDH) of consecutive consistent path trace messages that must be observed before it is accepted.

An interrupt is generated when a new Path Trace message is accepted as valid. The valid Path Trace message is compared with an Expected Path Trace message downloaded to memory by software. A J1 mismatch (J0_MIS) flag is raised if the 2 messages are not identical. The rxspoh_stat block also implements a J1 unstable counter. The J1 unstable counter is incremented for each byte that differs from the previously received byte. An invalid J1 condition is declared when the J1 unstable counter reaches 8. The J1 unstable counter is cleared to 0 when a valid J0 is accepted.

The SONET receive path trace buffers use a 128x8 single port memory and a 64x8 single port memory as in the case of the SONET receive path trace buffers.
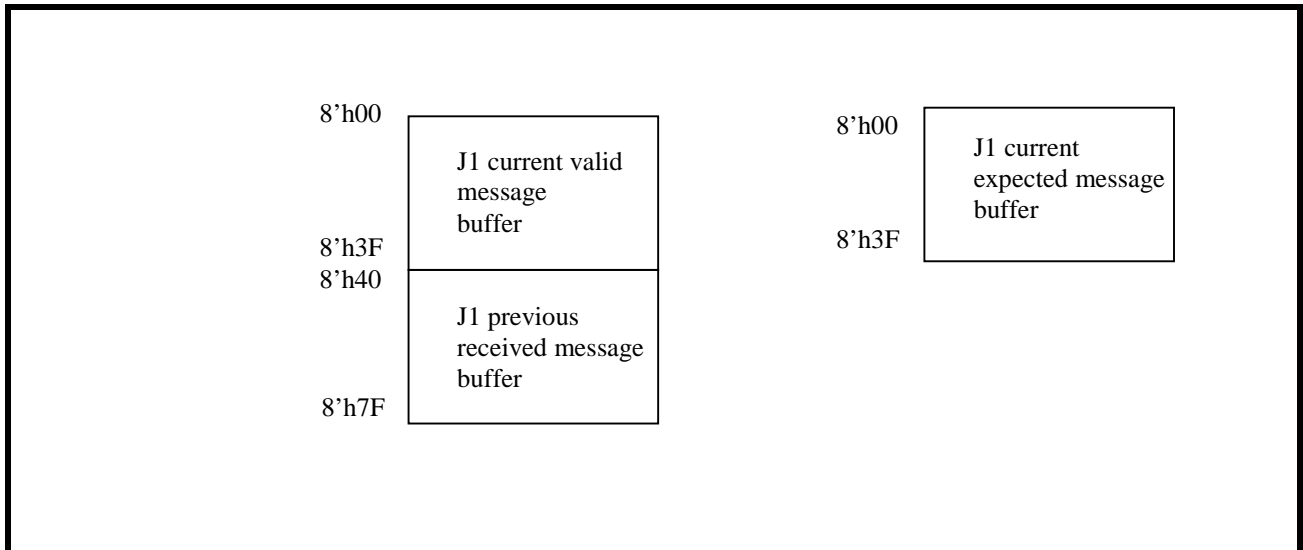
DOWNSTREAM AIS INSERTION CONTROL

The rxspoh_stat block can be configured to cause downstream AIS insertion to the cell processor when any of the following conditions are detected: AIS-P, LOP-P, TIM-P, J1 unstable, PLM-P, UNEQ-P and C2 unstable. Downstream AIS insertion to the cell processor is done by sending all ones in all the extracted payload bytes.

The software can enable or disable the insertion of path AIS to the cell processor on detection of any of the aforementioned conditions. If AIS insertion is necessary, then an enable signal to the rxspoh_proc block is activated which causes the rxspoh_proc block to insert all ones in the payload bytes on the 'rbyte' port to the VT Mapper cell processor.

RXSPOH_CAP BLOCK

The rxspoh_cap block captures the contents of the path overhead and stores them for access by the external processor. The nine path overhead bytes are stored in registers. The rxspoh_cap block issues an interrupt once all the path overhead bytes (9 bytes) for the current frame have been captured. When the last path overhead byte of the current frame has been written to its register, an interrupt is raised to notify the software. The contents of the captured path overhead bytes are preserved for one frame (i.e., until the next capture interrupt) for access by the software.

The captured path overhead bytes are serialized and sent as outputs from the chip as shown in **Figure 22**. RxOHFRAME, RxOH, and RxOHVALID are updated on the falling edge of RxOHCLK. The rate of RxOHCLK is programmable in the range from 1.215MHz to 38.88MHz.

FIGURE 22. PATH OVERHEAD INTERFACE TIMING
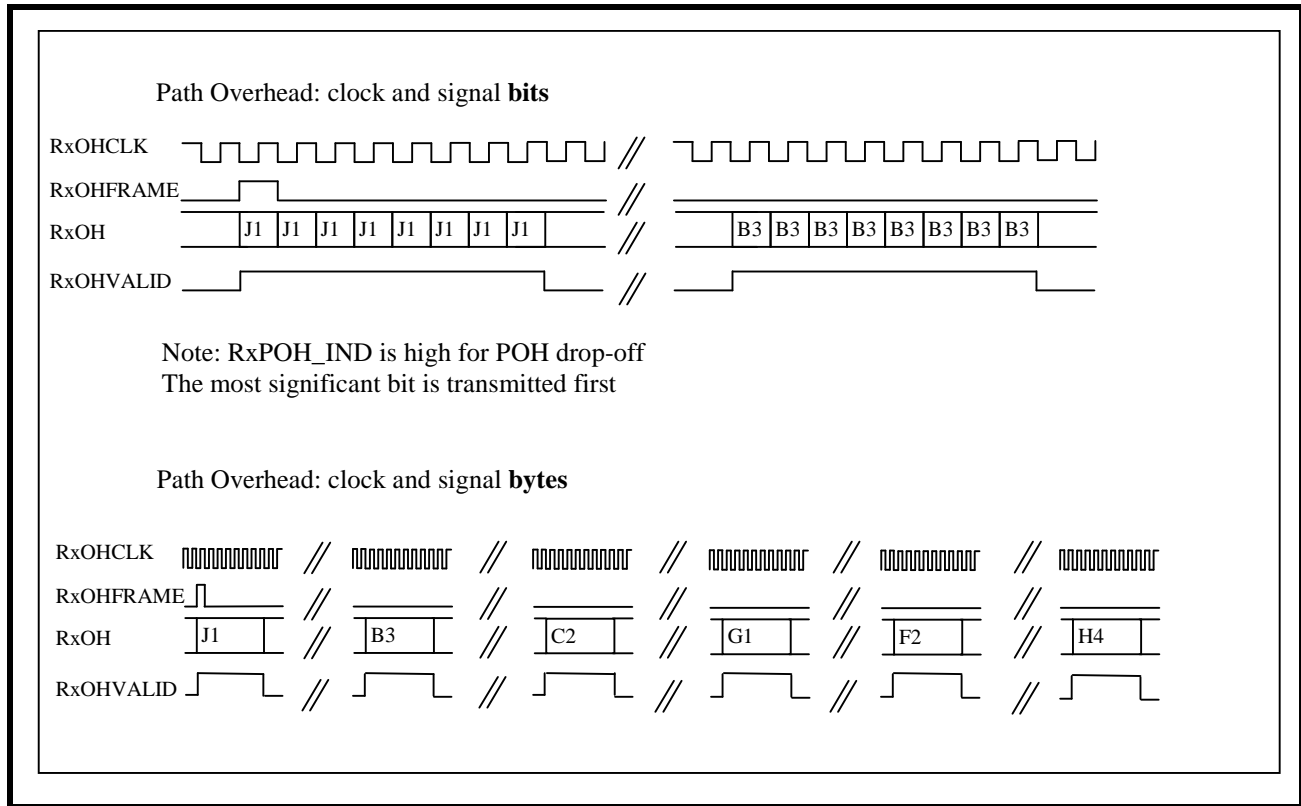
STS1/STS3 TRANSMIT TRANSPORT PROCESSOR

TXSTOH_INS BLOCK

The txstoh_ins block provides a serial port for hardware insertion of the transport overhead bytes. The hardware inserted SONET OH bytes, if enabled, override the contents of the SONET OH software registers during transmission. The hardware inserted SONET OH bytes are forwarded to the txstoh_cont block along with the enable signal. The SONET OH port also has an enable input which allows hardware to override the contents of the SONET OH software registers without going through the processor interface. The following picture shows the transport overhead J0 byte being enabled. The TxOHFRAME and TxOHEN signals are updated on the falling edge of TxOHCLK while the TxOHINS and TxOH signals are sampled on the second rising edge of TxOHCLK following the assertion of TxOHEN.

The rate of TxOHCLK is programmable within the range from 2.43 MHz to 38.88 MHz.

FIGURE 23. TRANSMIT TRANSPORT OVERHEAD INTERFACE TIMING
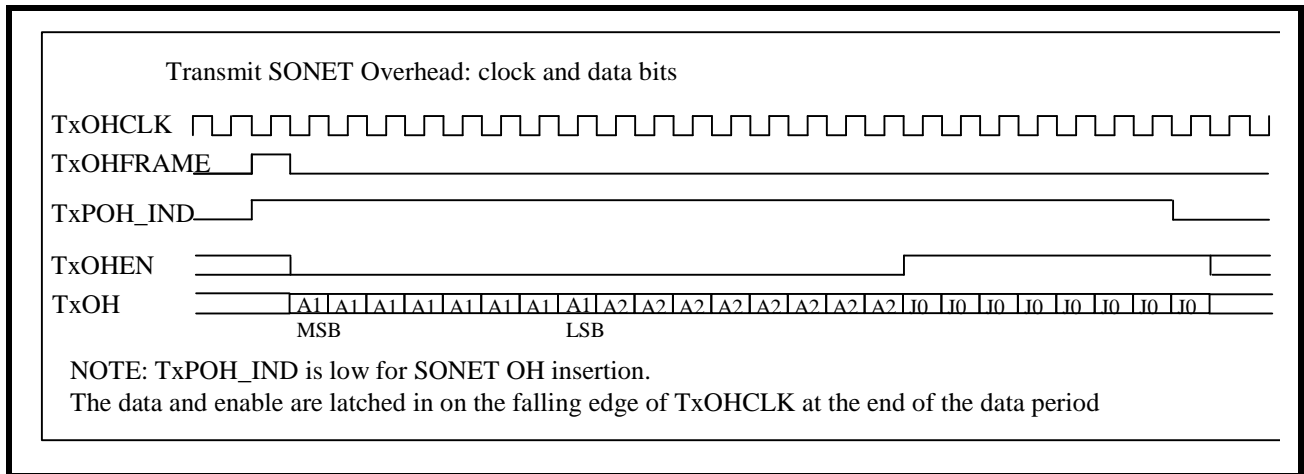
HARDWARE RDI-L INSERTION

Hardware can enable RDI-L insertion by setting the most significant bit of the B2 byte to "1" on the TTOH serial input line. Note that software must first enable hardware RDI-L insertion. The state of the TTOHIns pin has no effect during the B2 slots.

TXSTOH_CONT BLOCK

The txstoh_proc has one 8 bit internal data bus interface. The txstoh_cont block provides the register file and internal processor interface for the Transport Section of the SONET transmitter. It selects the value of the Transport overhead bytes from either hardware or software according to the control registers and forwards them to the txstoh_proc block for transmission. The hardware value is specified through a parallel data input port. If the Transport overhead bytes are serially entered into the chip, it is assumed that a serial to parallel data converter has converted the data to parallel format and has placed the data on the input of the txstoh_cont block at the appropriate instances during transmission. The txstoh_cont also provides control for the transmission of Section Trace message (J0 byte).

A1/A2 GENERATION

The txstoh_cont block generates alternate A1 and A2 values based on hardware or software requests and sends them to the txstoh_proc block via the tx_toh_data lines. The txstoh_cont block accepts A1/A2 values from the hardware input, or alternatively, software can specify an error mask indicating the A1/A2 bytes in which errors should be inserted for diagnostic purposes. A1/A2 errors are always inserted on frame boundaries, i.e., the A1/A2 error mask is only sampled at the start of every frame.

B1 ERROR MASK GENERATION

The txstoh_cont block allows software to insert errors into the B1 value calculated and transmitted by the txstoh_proc block. By writing to an appropriate register bit, a software controlled error mask is used to insert errors into the B1 byte.

B2 ERROR MASK GENERATION

The txstoh_cont block allows software to control B2 BER generation through two registers: A byte error mask register and a bit error mask register. The byte error mask specifies which of the B2 bytes are to be corrupted and the bit error mask specifies which bits are to be inverted in the B2 bytes that are to be corrupted. In the case of an 8 bit internal data bus, each bit in the B2 byte error mask corresponds to 4 bytes (i.e., one time slot). The B2 byte and bit error masks are sampled before the first B2 byte of each frame if B2 error insertion is enabled by software.

SCRAMBLING

The txstoh_cont block allows software to disable scrambling by setting a bit in the control register. Otherwise, the SONET data is scrambled using the identical algorithm as the de-scrambling process.

K1/K2 CONTROL

The K1/K2 bytes contain the APS code. The APS code transmitted either come from software registers or from hardware via the TxOH serial pin. Note that the 3 least significant bits of the K2 byte (bits 6, 7 and 8) may be overridden by an RDI-L alarm.

RDI-L CONTROL (K2 BITS 6, 7, AND 8)

The RDI-L indication bits consist of the 3 least significant bits of the K2 byte. The bits usually contain portions of the transmitted APS code. However, they are overridden with the RDI-L pattern 3'b110 if any of the following software configurable conditions occur: LOS, LOF, or AIS-L. RDI-L can also be inserted from hardware via the TxOH serial pin or forced by software. RDI-L insertion is done according to the following SDH rules:

■ TE shall generate RDI-L within 125µs of detecting an AIS-L defect (or a lower-layer, traffic-related, near-end defect). The LTE shall generate RDI-L by inserting the code '110' in bits 6, 7, and 8 of the K2 byte.

The lower-layer, traffic-related, near-end defects referred to by R6-200 are LOS and LOF from the receiver blocks.

■ If bits 6 through 8 of the K2 byte are not used for other purposes (e.g., the linear APS mode indication), the LTE shall deactivate RDI-L by inserting the code '000' in bits 6, 7, and 8 of the K2 byte within 125μs of terminating the defect that caused it.

■ If bits 6 through 8 of the K2 byte are used for other purposes, the LTE shall deactivate RDI-L by inserting an appropriate code in bits 6, 7, and 8 of the K2 byte within 125μs of terminating the defect that caused it to be sent (assuming it has been sent for any minimum RDI-L assertion time supported by the NE).

■ When LTE generates RDI-L, it should generate it for at least 20 frames.

SECTION TRACE GENERATION (J0/Z0)

The txstoh_cont block allows three methods in the transmission of the J0/Z0 bytes:

Method 1: The J0 byte is set to all 1 in accordance with the SONET standard.

● Unless it is being used for a defined purpose (e.g., to carry a Section Trace message once the details of that feature are defined) each J0 and Z0 byte shall be set to a binary number corresponding to its order of appearance in the STS-N frame (i.e., the J0 byte shall be set to 00000001, the first Z0 byte shall be set to 00000010, etc.).

Method 2: The J1 byte is obtained from the hardware input

Method 3: The J1 byte is obtained from the message written by software into the J1 message buffer

Method 1 is the default unless the software control specifies otherwise. The Z0 bytes are always generated according to the above rules.

The Section Trace (J0) transmit buffers use a 64x8 single port ram as in the case of the Path Trace transmit buffers. The memory segments contain the J0 Section Trace buffers and operate in the same way as the J1 transmit Path Trace buffers.

REI-L GENERATION (M0/M1)

The txstoh_cont block allows three methods in the transmission of the M0/M1 bytes:

Method 1 : The REI-L signal is set according to the B2 error count by the receiver blocks from the most recently received frame

Method 2 : The REI-L signal is obtained from the hardware input

Method 3 : The REI-L signal is obtained from software

Method 1 is the default unless software chooses to enable either method 2 or 3.

S1/F1/E1/E2 SELECTION

The txstoh_cont block allows either hardware or software insertion of the S1, F1, E1, and E2 bytes. The default generation method for the S1 byte is reading from the software registers. The default generation method for the E1, F1, and E2 bytes is hardware insertion. The registers contain all zeros upon reset.

DATACOM (D1-D12) SELECTION

The data communication bytes are inserted via hardware only.

UNDEFINED SONET OH BYTES

The remaining bytes of the STS-N transport overhead are all currently undefined. The txstoh_cont block inserts all zeros in those bytes in accordance with the SONET standard.

■ A SONET NE shall have the capability to ignore the values contained in all undefined and unused bits and bytes [except for BIP-8 calculations] to prevent misinterpretation of the received patterns.

■ A SONET NE should send an all-zeros pattern (before scrambling) in undefined bits and bytes. All-zero patterns should also be sent in defined bits and bytes if the NE does not support the defined function or if the function has been disabled by the user.

AIS-L CONTROL

The txstoh_cont provides AIS-L insertion capabilities according to the SONET standard:

■ STE shall generate AIS-L downstream within 125μs of detecting an LOS or LOF defect on the incoming signal or the failure of LTE supporting provisioned line origination functions. The AIS-L shall be generated as an STS-N electrical signal that contains valid section overhead and a scrambled all-ones pattern for the remainder of the signal.

The txstoh_cont allows software to insert an AIS-L condition on the transmitted data by writing to an appropriate bit in the register file. The AIS-L condition is set/unset on frame boundaries. AIS-L insertion overrides all other frame data insertion schemes with the exception of LOS insertion.

LOS INSERTION

The txstoh_cont block allows software to specify an LOS condition on the transmitted data which sets all data bytes to zero after scrambling. LOS insertion is enabled by writing a "1" to the appropriate register file bit. LOS insertion, if specified, overrides all other transmit frame data insertion schemes.

TXSTOH_PROC BLOCK

The txstoh_proc has one 8 bit internal data bus interface. The txstoh_proc multiplexes Transport overhead data from the txstoh_cont block and SPE data from the txspoh_proc block and inserts them into the data stream. The txstoh_proc block generates timing and location signals for the other transmitter blocks and performs primitive SONET tasks such as scrambling, B1/B2 calculation and insertion, and start of frame (A1/A2) insertion using control signals from the txstoh_cont block.

LOCATION STROBE GENERATION

The txstoh_proc block maintains the location of the current byte (byte lanes) being transmitted and outputs time-advanced row, column, and time slot numbers of the data on the byte lane(s) for the other SONET transmitter blocks. The time-advanced location signals allow for pipeline delays necessary to move the data from the other transmit blocks to the txstoh_proc block.

A1/A2 INSERTION

During normal operation, the txstoh_proc block inserts the SONET framing pattern F628 (hex) for the A1 and A2 bytes respectively. This can be overridden by non-zero values from the tx_toh_data input from the txstoh_cont block at the time of insertion.

B1 CALCULATION AND INSERTION

The txstoh_proc block calculates the BIP-8 B1 error code on the scrambled data of the current frame and inserts it into the B1 byte of the next frame before scrambling. Errors can be inserted for diagnostic purposes from the tx_toh_data input from the txstoh_proc block.

B2 CALCULATION AND INSERTION

The txstoh_proc block calculates the BIP-8 B2 error code on the unscrambled data of the current frame except for the Section overhead bytes and inserts it into the B2 bytes of the next frame before scrambling. Errors can be inserted for diagnostic purposes from the tx_toh_data input from the txstoh_proc block.

Two memories are used in the B2 error code calculations for the txstoh_proc block. One memory is used to store the running value of the B2 error calculations. This memory is a 12x8 dual port RAM with one port for reads and one port for writes. This is necessary because as the hardware is calculating the B2 code for each STS, it needs to store the new value into the memory and at the same time fetch the current code for the next STS from memory. The second memory is a single port 12x8 RAM used to store the final B2 codes for all the STS's. This memory is read at the B2 byte locations for comparisons and written into in the A1 byte locations to store the final B2 codes for the previous frame. For the 8 bit version of the rxstoh_proc block, the B2 RAM widths are 8 bits.

SCRAMBLING

The txstoh_proc block scrambles all the bytes of the SONET frame except for the A1, A2, and J0/Z0 bytes. Scrambling may be disabled by software. Scrambling is controlled on frame boundaries. That is, the txstoh_proc block will sample the scram_enable input at the beginning of each frame and scrambling is performed on the entire frame if the scram_enable is "High".

SONET OH DATA INSERTION

For the rest of the SONET OH bytes, the txstoh_proc simply takes the data on the TxOH input at the time of transmission, and inserts it into the corresponding location in the SONET frame. The SONET OH bytes intended to be inserted in this manner are: M0/M1, J0, S1, K1, K2, F1, E1, E2, the data communication bytes (D1-D12) and the undefined and growth bytes.

SPE DATA INSERTION

The txspoh_proc block places SPE data on the tx_path_data input of the txstoh_proc according to the location signals generated by the txstoh_proc block. The txstoh_proc takes the SPE data and inserts it into the transmit SONET frame at the appropriate instances in time.

AIS-L/LOS INSERTION

The txstoh_proc can apply either an AIS-L or a LOS condition as described in previous sections according to control signals from the txstoh_cont block.

4.9   TELECOM BUS INTERFACE

The device's Telecom Bus interface supports the following features:

Option to enable/disable parity generation.

Option to select if parity is generated over data only or data and PL and C1J1 and Alarm signals.

Option to select if odd or even parity is used.

Accepts 8 kHz transmit frame pulse and complementary transmit reference clock to synchronize transmit data.

4.9.1   TRANSMIT TELECOM BUS

The Tansmit Telecom Bus interface consists of the following outputs: 8-bit data bus TxD_D[7:0], clock TxD_CLK, payload indication TxD_PL, timing indication TxD_C1J1V1_FP, parity TxD_DP, and a alarm indication TxD_ALARM. The device also allows a common set of reference timing signals for synchronizing the data input to each of the Telecom Bus ports for the cases where transmit re-phase is not available on the other side. The Telecom Bus port operates at 19.44 MHz on STS3 and 6.28 Mhz on STS1.

The subsections below summarize the functionality of the Telecom Bus interface signals. Tx51_19Mhz is provided as a reference clock to put data out onto the Telecom Bus ports. These signals are 19.44/6.28 MHz. This clock must be used to source the data to be transmitted on the appropriate Telecom Bus.

An 8kHz pulse (TxSBFP_IN_OUT) is input on the falling edge of Tx51_19Mhz once every frame period and is one Tx51_19Mhz clock cycle wide. It is used to synchronize the data arriving at the TxD_D[7:0] outputs. A 16-bit latency counter can be configured to determine the latency between the frame pulse and the associated input data (C1). **Figure 24** shows the relationship between the Input Telecom Bus Data and the TxSBFP_IN_OUT signal.

FIGURE 24. TRANSMIT TELECOM BUS INTERFACE TIMING
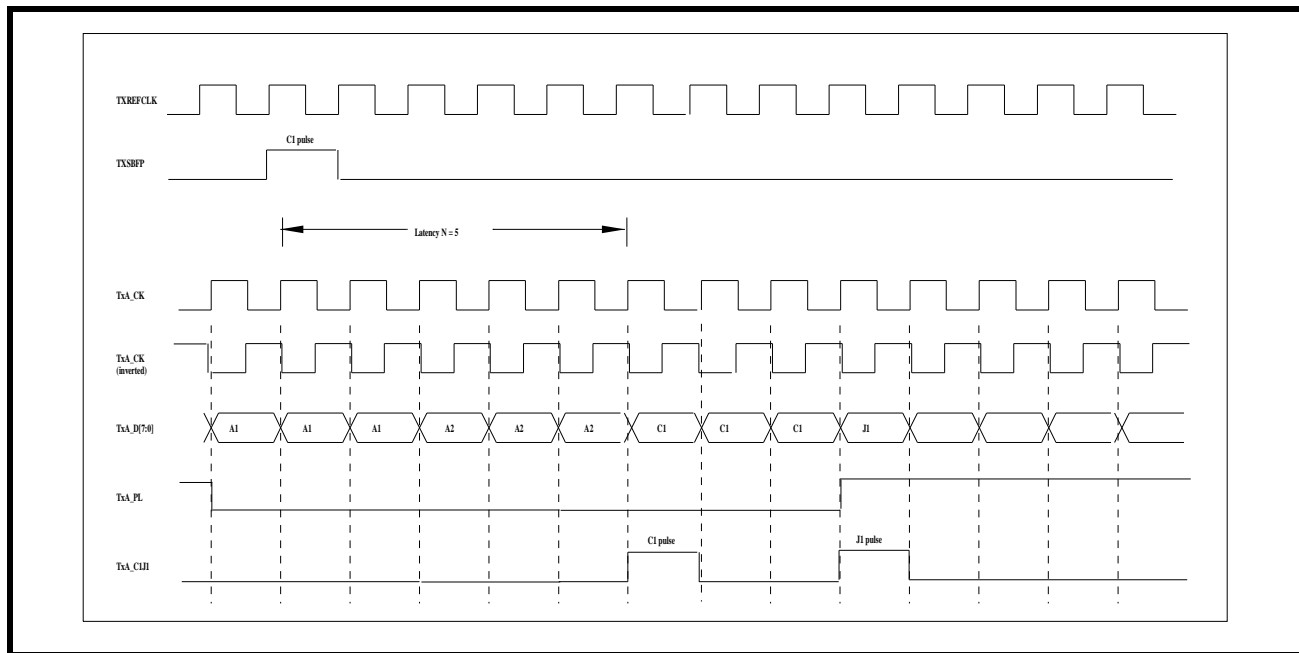
The transmit Telecom Bus clock output (TxD_CLK) is used to clock the transmit Telecom Bus output signals. It must be synchronous with the Tx51_19Mhz clock. Also, no phase relationship is required between Tx51_19Mhz and the TxD_CLK. The TxD_D[7:0] stream must contain valid Pointer Bytes and the POH.

The Telecom Bus also generates the value of the transmit Telecom Bus parity output (TxD_DP). The parity calculations can be configured through the use of the control bits in the interface control registers. The

transmit Telecom Bus Alarm output (TxA_Alarm) is generated to tell the external device to generate AIS-P in the STS1/STS3 for which the alarm occurs.

4.9.2   2kHz Mode in STS3

To align the V1 bytes with H4 in STS3, the part must be configured for 2kHz. With a 2kHz frame pulse applied to each of the Voyager devices, the parts can align VT Superframe boundaries. This will allow V1 bytes within each device to match one another. The TxD_C1J1V1_FP will pulse "High" for all C1J1 bytes. However, it will only pulse "High" during the V1 byte. V2, V3, and V4 will not be indicated by the external frame pulse.

FIGURE 25. C1J1V1 PULSE IN STS3 2KHZ MODE
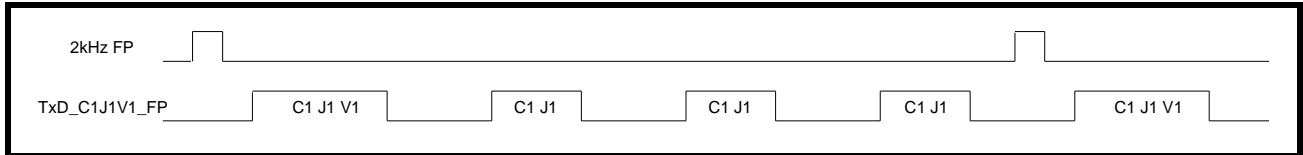
4.9.3   RECEIVE TELECOM BUS

The receive Telecom Bus interface consists of the following inputs: 8-bit data bus RxD_D[7:0], clock (RxD_CLK), SPE indication (RxD_PL), C1J1 indication (RxD_C1J1V1_FP), parity (RxD_DP), and a alarm indication (RxD_ALARM). All of the receive Telecom Bus ports operate at 19.44/6.28 MHz.

The subsections below summarize the functionality of the receive Telecom Bus interface signals. The receive Telecom Bus clock input RxD_CLK is used to clock in the receive Telecom Bus input signals from an external device. The clock edge on which the Telecom Bus signals are clocked is programmable via the CKINV control bits. **Figure 26** shows the functional relationship of the receive Telecom Bus signals.

FIGURE 26. RECEIVE TELECOM BUS INTERFACE TIMING
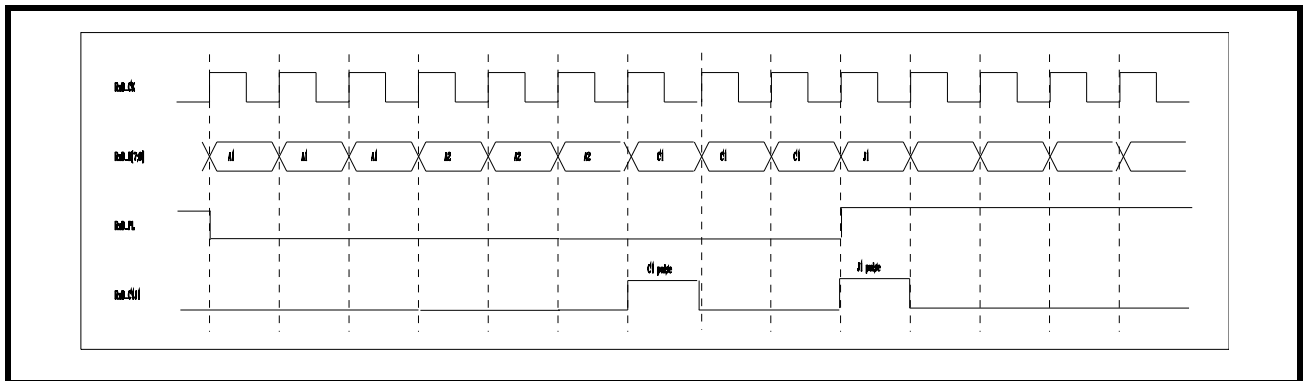
Each receive Telecom Bus port has an 8-bit wide data bus that inputs the STS1/STS3 data from an external device. The receive Telecom Bus data is byte-aligned and the entire payload, including SONET TOH and POH, is passed in the device. The receive Telecom Bus C1J1 input (RxD_C1J1V1_FP) can be provisioned to provide two different types of indications, depending on the register setting. When CPOS is set to "1", the corresponding RxD_C1J1V1_FP signal provides two pulses.

For all sub-frames, the receive Telecom Bus PL input (RxD_PL) is "Low" during the SONET OH bytes in the RxD_D[7:0] stream and is "High" during the SPE bytes. This includes cases where pointer adjustments are performed and the SPE needs to be adjusted about the H3 bytes. For example, the H3 bytes are payload bytes during the frame in which a pointer decrement occurs, therefore the RxD_PL signal will be "High" coincident with the H3 bytes for that frame. Also in the frame where a pointer increment occurs, the three bytes after the H3 bytes become stuff, therefore the RxD_PL signal will be "Low" for those bytes. The parity checking can be configured through the use of the control bits in the interface control registers.

The receive Telecom Bus alarm output (RxD_ALARM) is generated by an external device in response to an alarm condition that will cause AIS-P to be generated. The RxD_ALARM input will remain active for the duration of the alarm condition that causes it to become set.

4.10   VT MAPPER

INTERFACES AND PROTOCOLS

This block has three interfaces to the outside world:

The Internal Bus interface through which the block communicates with the µP interface block which interfaces to the external processor that controls and monitors the VT Mapper.

The Mid Bus interface through which the block communicates with the blocks processing the higher levels of SONET overhead.

The E1 I/O interface up to 28 T1 or 21 E1 digital signals.

INTERNAL BUS INTERFACE

Figure 27 shows the internal synchronous bus structure. It consists of two 8-bit data buses, an 8-bit address bus, and 5 control lines: clock (clk), select (sel), read (read), data transfer acknowledge (dtack), and interrupt request (irq). All of these lines are active High.

FIGURE 27. INTERNAL BUS STRUCTURE
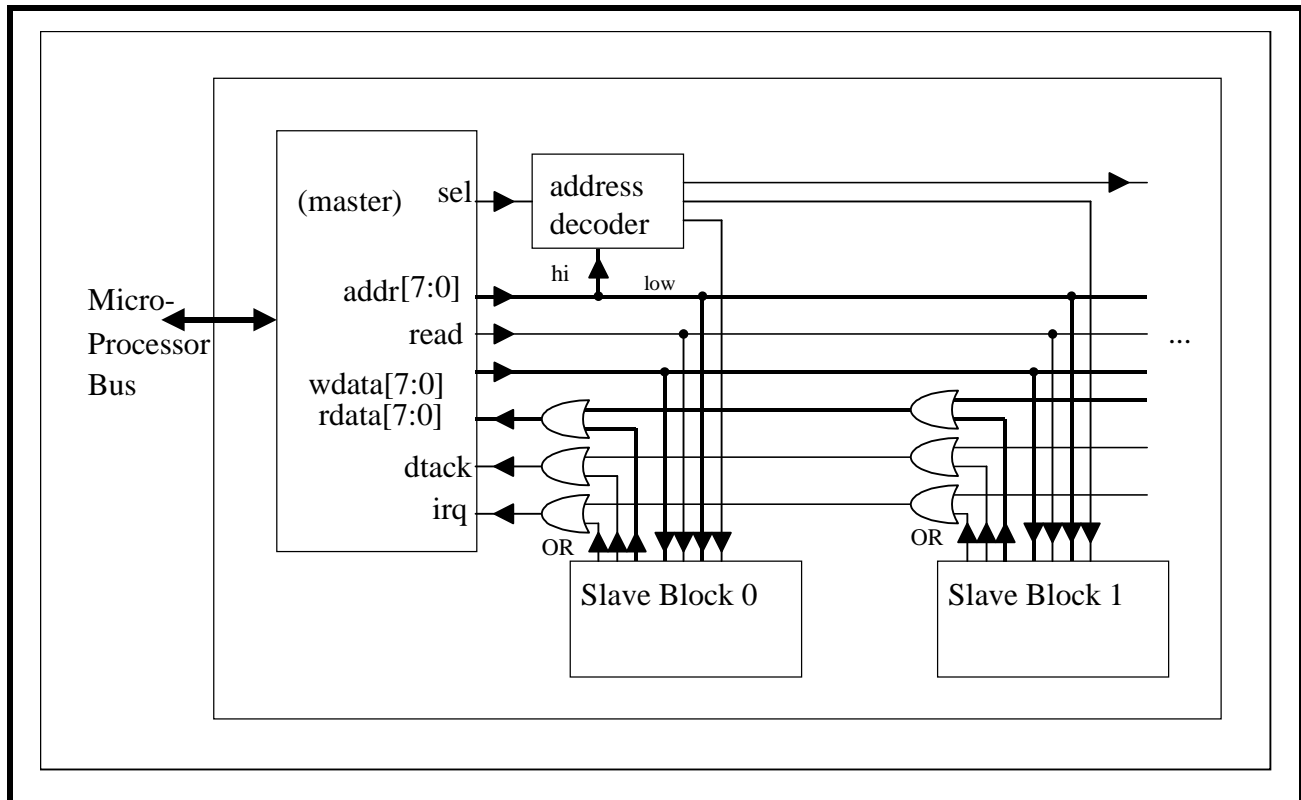
Byte-oriented addressing is used for all of the address maps.

Internal Bus Signals

Signals and their usage are described. **Clk**, **Sel** and **Read** are driven high or low by the pif block, based on the **Clk**, **Chip Select**, and **WE** signals from the microprocessor. irq and dtack are low or high driven by internal registers. addr, rdata and wdata may be undefined as long as no read or write action is taken. All signals are Clk aligned and sensitive to the positive edge of Clk.

SIGNAL	DIRECTION	DESCRIPTION
Clk	input	System clock signal, input from external processor
Sel	input	Select signal, when it goes high, selects internal register
Read	input	Read/write control signalHIGH: read data from data bus.LOW: Write data to data bus.
Dtack	output	Data transfer acknowledge signal, comes from internal registers, indicate internal registers are ready to send or accept data.
addr[7:0]	input	Register address.
Irq	output	Interrupt request signal when it goes to 1 indicates an interrupt request.
rdata[7:0]	output	Reads data signals from internal register.
wdata[7:0]	input	Write Data signals to internal register.

MID BUS INTERFACE

The interface between the VTM and the other SONET blocks is a single edge synchronous interface. It consists of a clock, enable pair, and an 8-bit data bus in each direction. The enable signals are active High and data is transferred on the rising edge of the corresponding clock.

FIGURE 28. MID BUS INTERFACE
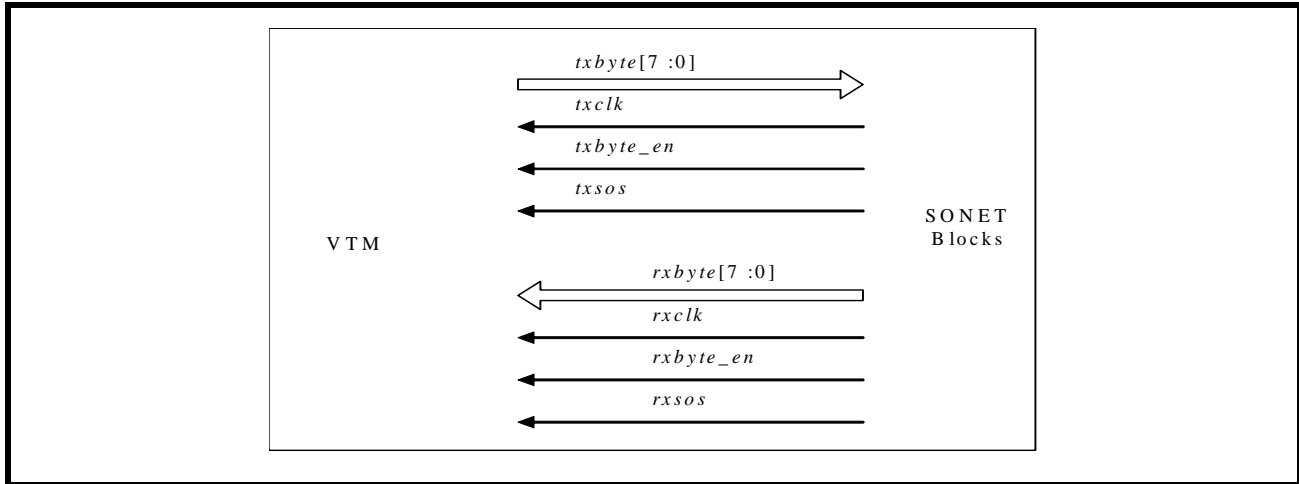
SONET to VTM Direction

In this direction, the higher level SONET block is sending data to the VT Mapper. Data presented on the rxbyte[7:0] data bus of the VTM by the SONET block must be valid to be sampled on the rising edge of rxclk when rxbyte_en is "High". The VTM block samples the rxbyte_en and rxbyte[7:0] lines on each rising edge of rxclk. If rxbyte_en is "High", the data on rxbyte[7:0] is processed as valid data. The transitions on the rxbyte[7:0] and rxbyte_en lines should be timed to satisfy the VTM's setup & hold requirements with respect to rxclk.

For all timing diagrams in this section, it is implied that the data lines can change at every clock cycle. Only when the nature of the data carried on the data lines changes is there a boundary shown on the data line.

FIGURE 29. SONET TO VTM DATA TRANSFER WITH ZERO POINTER OFFSET
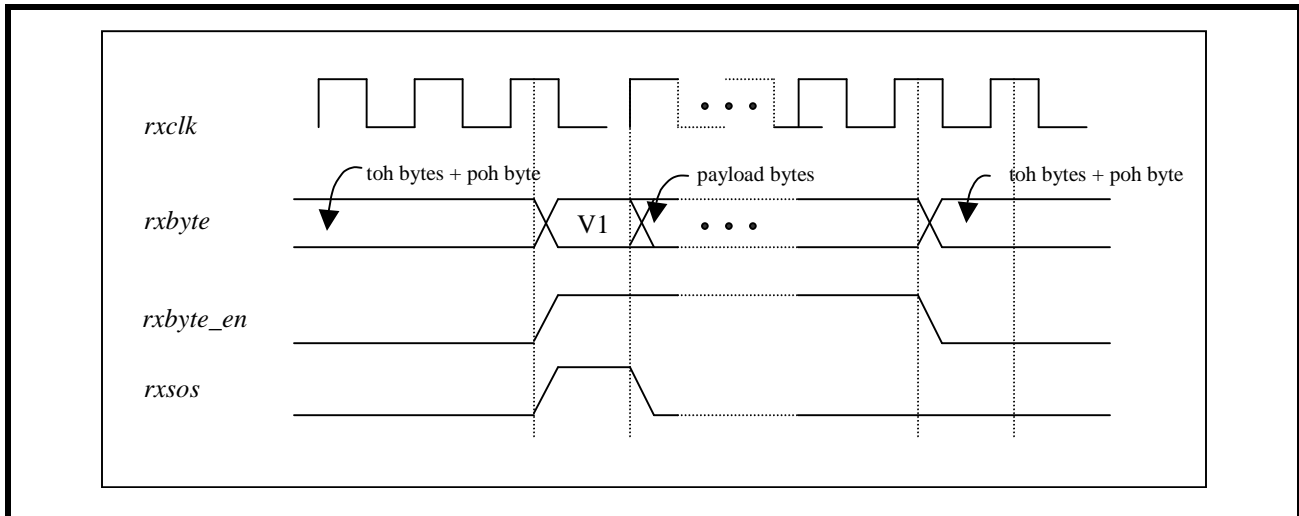
The Start of Superframe signal is asserted while the first V1 byte of the Superframe is present on rxbyte.

VTM to SONET Direction

When the SONET block is receiving data from the VTM, txbyte_en is used as a command signal. When the SONET block asserts txbyte_en "High", data from the VTM is produced on the next rising txclk edge. **Figure 30** gives an example of such a transaction. Transitions of lines txbyte[7:0] and txsos occur on the rising edge of txclk so setup time requirements of up to one txclk period can be satisfied. It is up to the interface designer to make sure that the other timing requirements of circuits connected to the VTM are satisfied.

FIGURE 30. VTM TO SONET DATA TRANSFER
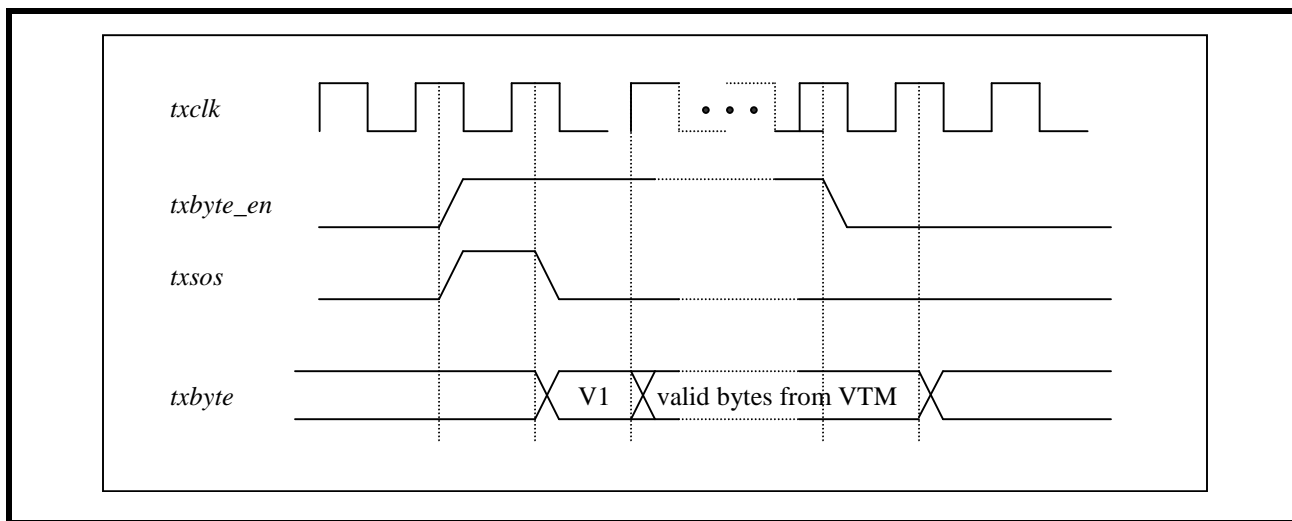
Although a minimum of buffering is done at the VTM Mid Bus output to compensate for the jitter introduced by the transport and path overhead columns (SONET TOH & POH), it is assumed and required that txbyte_en and txclk clock ticks will occur at an average frequency of 6.192MHz (i.e. 6.48MHz txclk with a 86:90 enable ratio) and will be approximately equally spaced (burst reads are not supported).

FIGURE 31. T1/E1 INTERFACE TIMING (INTERNAL TO THE CHIP)
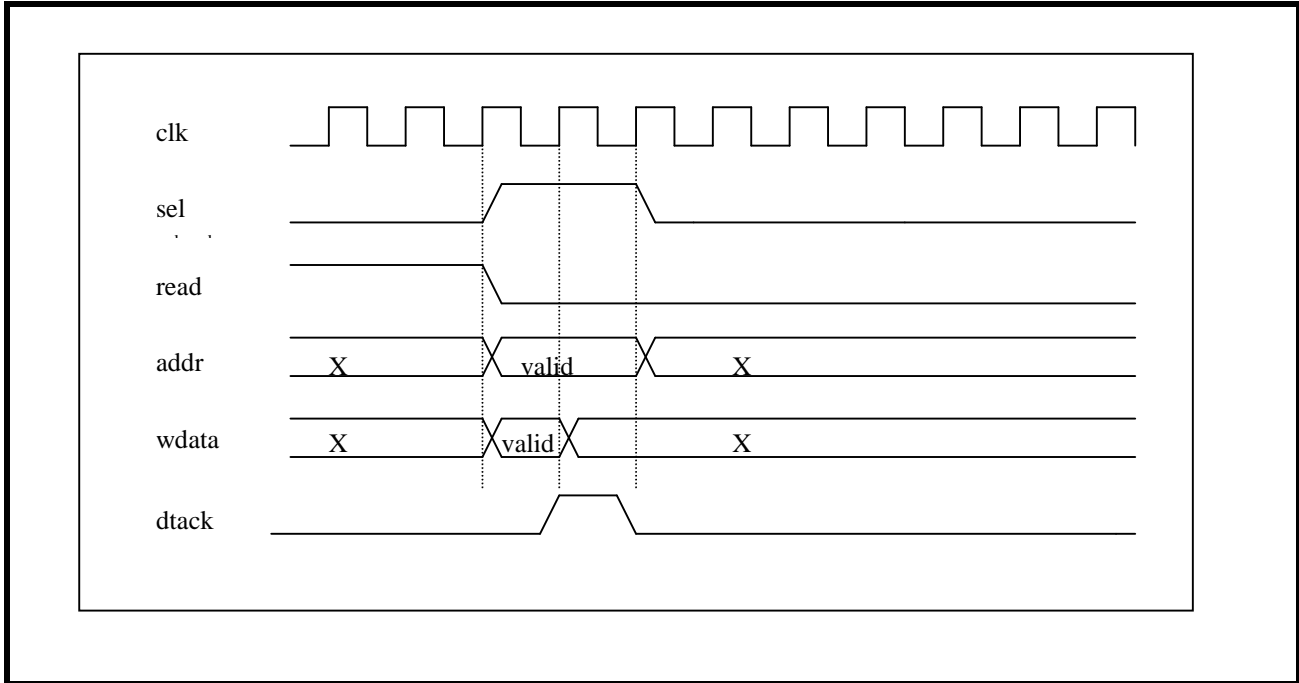
FIGURE 32. T1/E1 INTERFACE TIMING (T1/E1 SYNCHRONOUS MAPPING, INTERNAL TO THE CHIP)
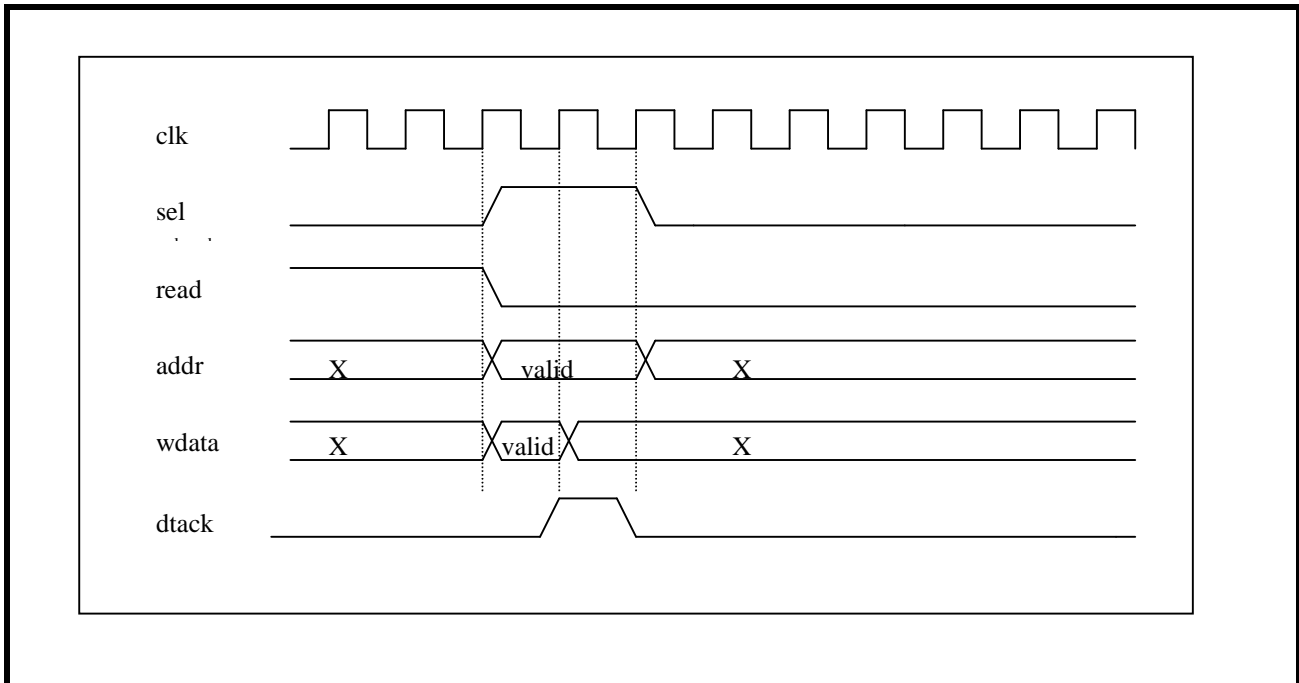
DESIGN DESCRIPTION

The function of this reusable block is limited to the construction and extraction of the VT structured content of the SONET STS1 Payload Capacity / SONET VC-3 as described by Telcordia's GR-253-CORE Generic Requirements and ITU-T's G.707 recommendations. The rest of the work for the higher levels of hierarchy including Transport and Path Overhead is handled by the STS1 SONET blocks.

VT STRUCTURED STS1 PAYLOAD CAPACITY

This section briefly describes the structure of the SONET data stream used to carry lower bit-rate channels. The STS1 Payload Capacity is made up of 84 columns of 9 rows each. The Payload Capacity is divided equally amongst seven Groups. Each Group can contain four VT1.5/TU-11 or three VT2/TU-12 tributaries. VT1.5/TU-11 tributaries are used to carry T1 signals and VT2/TU-12 tributaries are used to carry an E1 signals.

VT Superframe

Four consecutive STS1 frames of Payload Capacity are used to make up a VT Superframe. The first byte of each Tributary in each frame has a special function. These special bytes are called V1 to V4.

V1 & V2 : VT Payload Pointer

The V1 and V2 bytes form the VT Payload Pointer. In asynchronous mappings or on transmission, the VT Payload Pointer is assigned a fixed value by this block such that the V5, J2, Z6/N2 and Z7/K4 bytes immediately follow the V1 to V4 bytes. In synchronous mappings or on reception, the VT Payload Pointer is processed as prescribed in Telcordia and ITU. Each time a received VT Payload Pointer is incremented or decremented, internal counters are available to be read by the processor in registers BIP2CNT1 to BIP2CNT21 and REICNT1 to REICNT21 are incremented.

V3 : VT Pointer Action Byte

This byte is used as a negative stuff byte when required by a pointer decrement. Otherwise, it is Undefined. It is never used by this block on transmission of asynchronously mapped signals. In synchronous mappings or on reception, this byte is processed along with the VT Payload Pointer bytes as prescribed in the Telcordia and ITU documents.

V4 : Undefined

This byte is reserved for future growth and is treated as Undefined. It is ignored on reception and is transmitted as all zeros.

VT Path Overhead

Each Virtual Tributary has it's own set of Path Overhead bytes which are processed as described in the following paragraphs.

V5 : VT Path Error Checking, Signal Label and Path Status

The bit assignments for the V5 byte are shown in **Table 7**.

TABLE 7: V5 - VT PATH ERROR CHECKING, SIGNAL LABEL AND PATH STATUS

7 (MSB)	6	5	4	3	2	1	0 (LSB)
BIP-2		REI-V	RFI-V		Signal Label		RDI-V

Bits [7:6] of V5 are used for error performance monitoring. A BIP-2 scheme is defined as follows. When generating a tributary, bit 7 is set to the exclusive-or of all the odd numbered bits (bits 7,5,3 and 1) of the previous VT SPE (including the V5, J2, Z6/N2 or Z7/K4 byte but not the V1 to V4 bytes, except V3 when it is used as a negative stuff byte), bit 6 is set to the exclusive-or of all the even numbered bits (bits 6, 4, 2 and 0) of the previous VT SPE. When terminating a tributary, bit 7 is compared to the exclusive-or of all the odd numbered bits of the previous VT SPE, bit 6 is compared to the exclusive-or of all the even numbered bits of the previous VT SPE. If there is any difference, bit 5 of V5 (REI-V) of the peer tributary generator is set to "1",

otherwise it is set to "0". Detected errors are tallied in the BIP2CNTx counters that can be read by the processor in registers BIP2CNT1 to BIP2CNT21

Bit 4 of V5 is used for VT Path Remote Failure Indication (RFI-V). As described in GR-253-CORE, when automatic RFI-V insertion is enabled by writing "1" to bit VTRFIEN of registers INS1 to INS21, RFI-V will be signalled by inserting a "1" in the RFI-V bit of byte V5 when LOP-V, AIS-V, UNEQ-V or PLM-V is detected for more than 2½±½ seconds on the received tributary in the corresponding time slot. The RFI-V signalling is removed, and bit RFI-V of byte V5 is cleared if the condition that triggered it is absent for 10±½ seconds.

Bits [3:1] of V5 are used for VT Path Signal Label and indicate the contents of the tributary. Only the following codes are generated by the tributary generator or expected by the VT PTE:

000 : Unequipped or not provisioned

010 : Asynchronous Mapping of E1

100 : Byte Synchronous Mapping E1

Bit 0 of V5 is used for one-bit VT Path Remote Defect Indication (RDI-V) As described in GR-253-CORE. When automatic RDI-V insertion is enabled by writing "1" to bit VTRDIEN of registers INS1 to INS21, RDI-V will be signalled by inserting a "1" in the RDI-V bit of byte V5 when LOP-V, AIS-V, UNEQ-V or PLM-V is detected on the received tributary in the corresponding time slot.

VT1.5/VT2 Path Remote Loopback Signaling

Voyager supports in-band signaling within the Virtual Tributary VT1.5/VT2 Path overhead to request VT1.5/VT2 path Remote Loopback (E1 payloads) provisioning at down-stream equipment. Signaling will be sent on the STS1/STS3 transmit output from the request originating system (sending system) and received on the STS1/STS3 input of the far-end system (receiving system). Once the receiving system detects this in-band message, a status flag is set to indicate the Remote Loopback request detection. The system software will detect this flag through interrupts and subsequently provision the appropriate VT path for Remote Loopback. The sending system shall continue sending the in-band message until such time that the Remote Loopback should be removed. At this time, the VT1.5/VT2 Path Overhead/Payload content within the STS1/STS3 transmit output of the sending system shall resume normal function. Upon detecting termination of the Remote Loopback request, the receiving equipment shall set a status flag to indicate the clearance of the Remote Loopback request. The system software can detect this flag and subsequently remove the Remote Loopback provisioning for the appropriate VT path. This function is provided on a per VT1.5/VT2 basis.

The LSB of the bit stuff byte immediately following V5 is used as the location for the Remote Loopback request messaging. During normal operation, this bit will contain the usual stuff bits. However, during Remote Loopback request transmission, this bit shall transmit a continuous, alternating pattern of 1's and 0's. The pattern shall always begin with a "1" and terminate immediately upon release of the software control bit for the remote loopback request enable. The receiving equipment shall monitor this bit location for the pattern of "1010101010", or exactly ten bits of alternating 1's and 0's with the first bit having a value of "1". Once the stated pattern is detected, the receiver sets a status flag indicating detection of the Remote Loopback request. This bit should be reset upon read and should not be set again until clearance of the Remote Loopback request is detected, and a new Remote Loopback request message is received.

Detection and cancellation examples:

J2 : VT Path Trace

Byte J2 is used to transmit repetitively a Virtual Tributary Path Access Point Identifier so that a Path receiving terminal can verify its continued connection to the intended transmitter. The Path Access Point Identifier supports both 16-byte and 64-byte frame as the J0 byte defined in the earlier section.

The 64 byte RAM is used on a shared basis with J2 and N2 bytes. When the 64 byte J2 message mode is configured, the N2 tandem connection feature is disabled. When the J2 message mode is configured as 16 byte, two 16 byte segments are used for TC (tandem connection) and J2.

Z6/N2 : VT PATH GROWTH (TANDEM CONNECTION, TC)

N2 is allocated for Tandem Connection Monitoring for the VT1.5 and VT2 level. The structure of the N2 byte is given in **Table 8**.

- Bits 1-2 are used as an even BIP-2 for the Tandem Connection.

- Bit 3 is fixed to "1". This guarantees that the contents of N2 are not all zeroes at the TC source. This enables the detection of an unequipped or supervisory unequipped signal at the Tandem Connection sink without the need for monitoring further OH-bytes.

- Bit 4 operates as an "incoming AIS" indicator.

- Bit 5 operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.

- Bit 6 operates as the OEI to indicate errored blocks of the egressing VT-n.

- Bits 7-8 operate in a 76 multiframe as:
    - the access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format of J0;
    - the TC-RDI, indicates to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink; An 8-bit ounter is provided for counting the number of REI bits received as 1 in bit 5 of N2. An REI indicates that the distant end has detected one or two errors between the BIP-2 calculation of the previous frame (all the bytes) and the BIP-2 value carried in the N2 byte in the current frame.
    - the ODI, indicates to the far end that VT-AIS has been inserted at the TC-sink into the egressing VT-n due to defects before or within the Tandem Connection; An 8-bit counter is provided for counting the number of OEI bits received as equal to 1 in bit 6 of N2. An OEI indication (a1) indicates that the distant end has detected one or two errors when, the BIP-2 calculated for the previous frame is compared against the BIP-2 value carried in the V5 byte in the current frame.
    - reserved capacity (for future standardization).
    - The structure of the multiframe is given in **Table 9** and **Table 10**.

TCM Functionality - Source

- If no valid VT-n is entering the Tandem Connection at the TC-source, a valid pointer is inserted. This results in a VT-AIS signal and bit 4 is set to "1". Even BIP-2 parity is calculated over the inserted VT-AIS signal and written into bits 1-2 of N2.

- If a valid VT-n is entering the Tandem Connection at the TC source, then even BIP-2 parity is calculated over the incoming valid VT-n or the inserted VT-AIS signal and written into bits 1-2 of N2.
    - The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
    - The original BIP-2 is compensated according to the algorithm described below.

NOTE: *In an unequipped or supervisory unequipped signal entering a Tandem Connection, the N2 and V5 bytes are overwritten with values not equal to all zeroes.*

TABLE 8: N2 BYTE STRUCTURE

B1	B2	B3	B4	B5	B6	B7	B8
BIP-2		"1"	"Incoming AIS"	TC-REI	OEI	TC-APId, TC-RDI ODI, reserved	

TABLE 9: B7-B8 MULTIFRAME STRUCTURE

FRAME #	B7-B8 DEFINITION
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 C1C2C3C4C5C6C7]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
:	:
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved

TABLE 10: STRUCTURE OF FRAMES # 73 - 76 OF THE B7-B8 MULTIFRAME

TC-RDI, ODI AND RESERVED CAPACITY		
FRAME #	B7 DEFINITION	B8 DEFINITION
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

TCM FUNCTIONALITY - SINK

If no valid VT-n is present at the TC-sink, a defect caused within the Tandem Connection is stated and the TC-RDI and ODI conditions apply.

If a valid VT-n is present at the TC-sink, the N2 byte is monitored:

- ·An "all-zeroes" N1-byte indicates a miss or disconnection within the Tandem Connection. In this case, the TC-RDI and ODI-bits are set to "1" in the reverse direction and VT-AIS is inserted in the egressing VT-n.

- Bit 4 of the received N2 is set to "1" to indicate that a defect has already occurred before the Tandem Connection. In this case, the ODI bit is set to "1" in the reverse direction and VT-AIS is inserted in the egressing VT-n.

- The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found, the TC-RDI and ODI bits are set to "1" in the reverse direction and VT-AIS is inserted in the egressing VT-n.

- The TC-APId is recovered and compared with the expected TC-APId. In the case of a mismatch, the TC-RDI and ODI bits are set to "1" in the reverse direction and VT-AIS is inserted in the egressing VT-n.

The even BIP-2 is computed for each bit pair of every byte of the preceding VT-n including V5 and compared with the BIP-2 retrieved from the V5 byte. A difference not equal to zero indicates that the VT-n has been corrupted and, then the OEI bit is set to "1" in the reverse direction. Furthermore the actual BIP-2 is compared

with the BIP-2 retrieved from the N2-byte. A difference not equal to zero indicates that the VT-n has been corrupted within the Tandem Connection and, then the TC-REI is set to "1" in the reverse direction.

If VT-AIS is not inserted at the Tandem Connection sink, then the N2-Byte is set to all zeroes and the BIP is compensated according to the algorithm described below.

Multiframe Generation and Synchronization

Loss of multiframe occurs when two consecutive Frame Alignment Signals (1111 1111 1111 1110) are detected in error (i.e., one or more errors in each FAS). Multiframe alignment is recovered when one consecutive non-errored FAS are found. Two status bits are used to indicate the Loss Of MultiFrame (TXAnLOMF, RXDnLOMF).

The TC trace identifier message comparison is based on the same state machine as that used for the 16-byte J2 message. The TC lock is removed (instable, INV) when 3 messages are received in error and the TC_INV alarm is declared. The TC lock is established when 3 valid, identical messages are received. A comparison is performed between the microprocessor-written TC and the contents of the incoming message. The message consists of TC Trace ID bytes 0 to 15. A TC Trace Identifier Mismatch (TC_MIS) alarm is declared when any byte does not match. Recovery occurs when there is a match between the expected message and the accepted message.

Bit 8 in frame 73 is defined as a Tandem Connection Remote Defect Indication (TC RDI). A TC RDI alarm occurs when a "1" has been detected in bit 8 in frame 73 for five consecutive multiframes (where each multiframe is 38 ms). The TC RDI alarm state is exited when bit 8 is equal to 0 for five consecutive multiframes. An alarm indication is reported as TC_RDI.

Bit 7 in frame 74 is defined as a Tandem Connection Outgoing Defect Indication (TC ODI). A TC ODI alarm occurs when a "1" has been detected in bit 7 in frame 74 for five consecutive multiframes (where each multiframe is 38 ms). The TC ODI alarm state is exited when bit 7 is equal to 0 for five consecutive multiframes. An alarm indication is reported as TC_ODI.

Tandem Connection Unequipped Status

Unequipped Tandem Connection detection is provided. Five or more consecutive received tandem connection N2 bytes equal to XX00 0000 result in a TC unequipped indication (TC_UNEQ). The alarm state is exited when five or more consecutive received tandem connection N2 (Z6) bytes are not equal to XX00 0000. Note that bits 1 and 2 of the N2 (Z6) byte are masked (shown as X) and do not affect the detection. The XX represents a don't care value and may be equal to a BIP-2 value.

BIP-2 Compensation

Since the BIP-2 parity check is taken over the VT-n (including N2), writing into N2 at the TC-source or TC-sink will affect the VT1.5/VT2 path parity calculation. Unless this is compensated, the error monitoring mechanism of BIP-2 is corrupted. Because the parity should always be consistent with the current state of the VT-n, the BIP has to be compensated each time the N2-byte is modified. Since the BIP-2 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-2 bits in the previous frame shall also be considered in the compensation of BIP-2 in the current frame.

Z7/K4 : VT PATH APS AND VT PATH REMOTE DEFECT INDICATION

Bits [7:4] are used for VT Path APS signalling (APS-V).

Bits [3:1] are for the optional Enhanced VT Path Remote Defect Indication (ERDI-V). Bits 5 to 7 of byte K4 may provide a remote defect indication with additional differentiation between the remote payload defect (LCD), server defects (AIS, LOP), and the remote connectivity defects (TIM, UNEQ). The optional codes from **Table 11** will be used. Use of the "010" code to indicate payload defects does not imply a requirement to use the "101" and "110" codes to distinguish between server and connectivity defects.

TABLE 11: K4 (B5-B7) CODING AND INTERPRETATION

B5/B8 OF V5	B6	B7	MEANING	TRIGGERS
0	0	0	No remote defect	No remote defect
0	0	1	No remote defect	No remote defect
0	1	1	No remote defect	No remote defect
0	1	0	Remotepayload defect	LCD(Note 1)
1	0	0	Remote defect	AIS, LOPTIM, UNEQ(or PLM, LCD)(Note 2)
1	1	1	Remote defect	AIS, LOPTIM, UNEQ(or PLM, LCD)(Note 2)
1	0	1	Remoteserver defect	AIS, LOP(Note 3)
1	1	0	Remoteconnectivity defect	TIM,UNEQ

NOTES:

1. *LCD is the only currently defined payload defect and is applicable to ATM equipment only.*
2. *Old equipment may include LCD or PLM as a trigger condition. PLM and UNEQ have previously been covered by SLM.*
3. *Remote server defect and server signal failure are defined in Recommendation G.783.*

For these optional codes, bit 7 is always set to the inverse of bit 6 to allow equipment which supports this feature to identify that it is interworking with equipment that uses the single bit RDI. In such a case, equipment at both ends will interpret only V5.

Bit 0 is reserved for future growth and is treated as Undefined.

TABLE 12: Z7/K4 - VT PATH GROWTH AND VT PATH REMOTE DEFECT INDICATION

7 (MSB)	6	5	4	3	2	1	0 (LSB)
APS-V				ERDI-V			Undefined

MAKE PAYLOAD BLOCK (MKP)

Figure 33 and **Figure 34** show the internal workings of the Make Payload block.

FIGURE 33. MKP (MAKE PAYLOAD), ONE OF SEVEN MKG : MAKE VT/TU GROUP
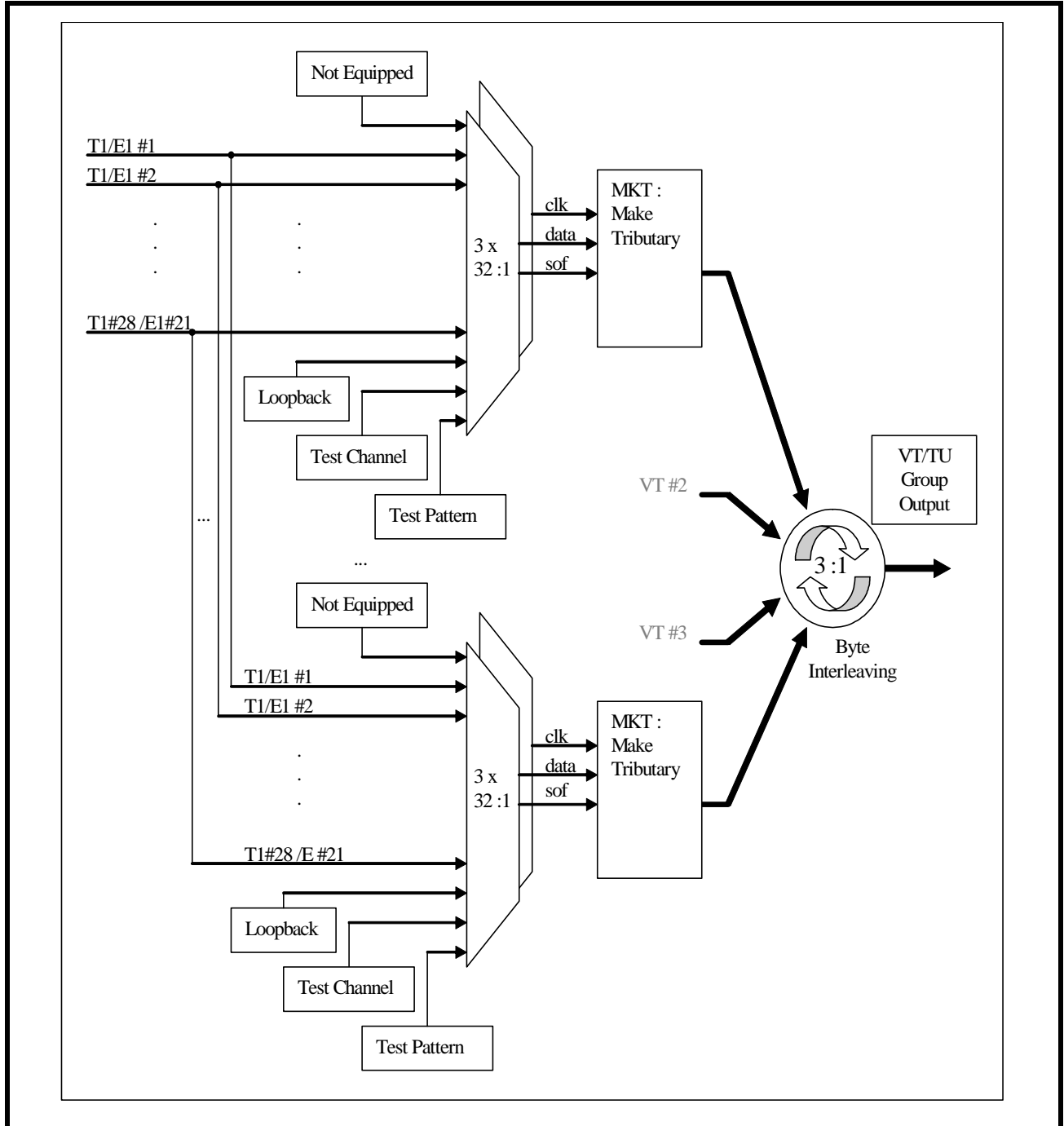
FIGURE 34. MKP (MAKE PAYLOAD), VT/TU GROUP INTERLEAVING.
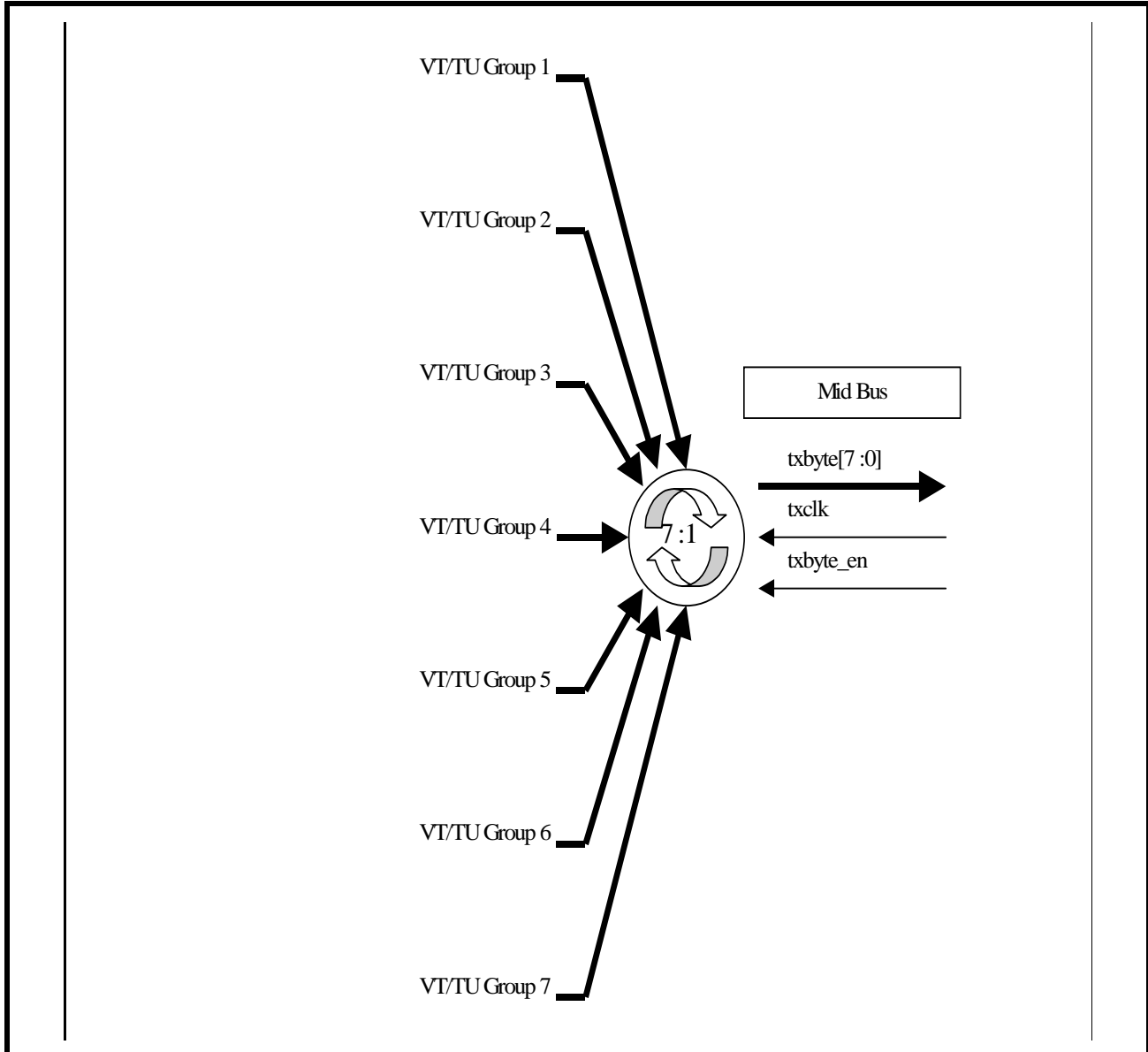
Make Tributary block (MKT)

Each of the 28/21 Make Tributary blocks (MKT) illustrated in **Figure 35** takes the output of its channel multiplexer and builds a tributary suitable for byte interleaving into a Tributary Group. It takes care of deserialization, VT POH generation and stuff bit control. If the Alarm Indication Signal (AIS) is asserted, a tributary made up of all ones is generated.

FIGURE 35. MAKE TRIBUTARY (MKT)
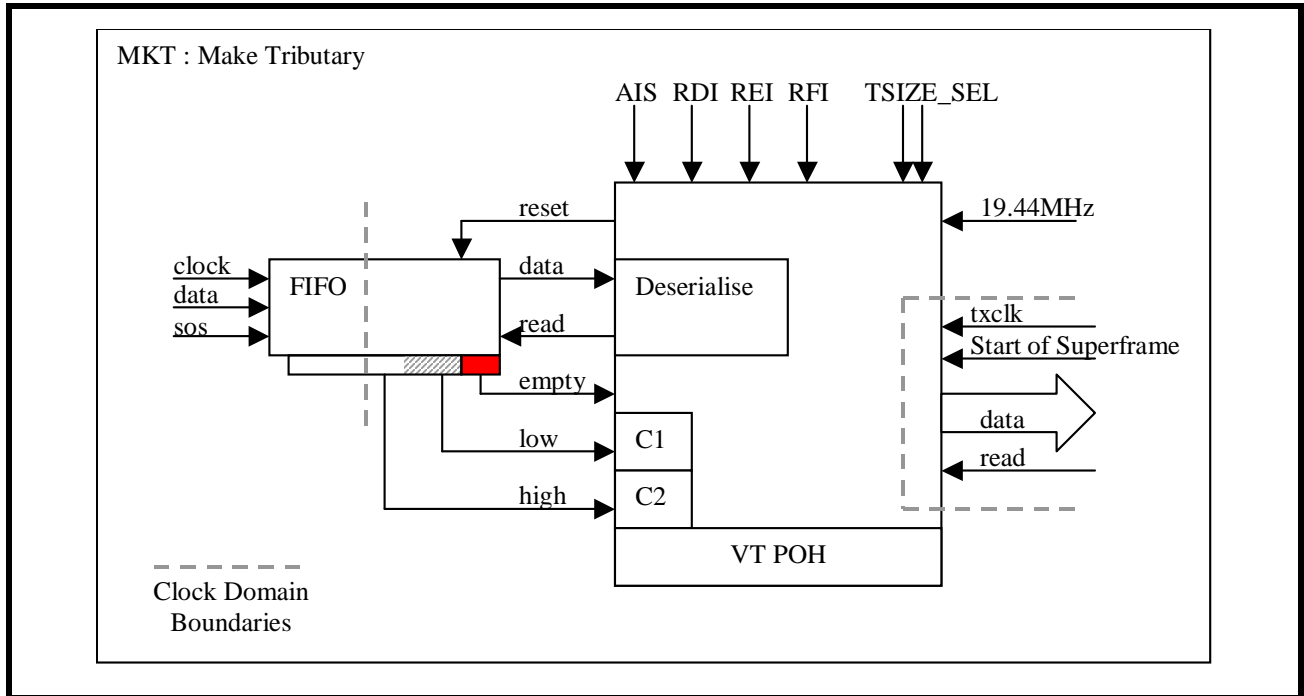
Extract Payload block (XTP)

This block, illustrated in **Figure 36**, extracts the individual T1/E1 channels from the SONET data stream. The Seven Groups are first de-interleaved, Fixed Stuff columns are removed, and then One to Four tributaries are extracted from each Group. This block handles the V1-V2 VT Payload Pointer processing, VT POH, and stuff bits.

FIGURE 36. EXTRACT PAYLOAD (XTP)
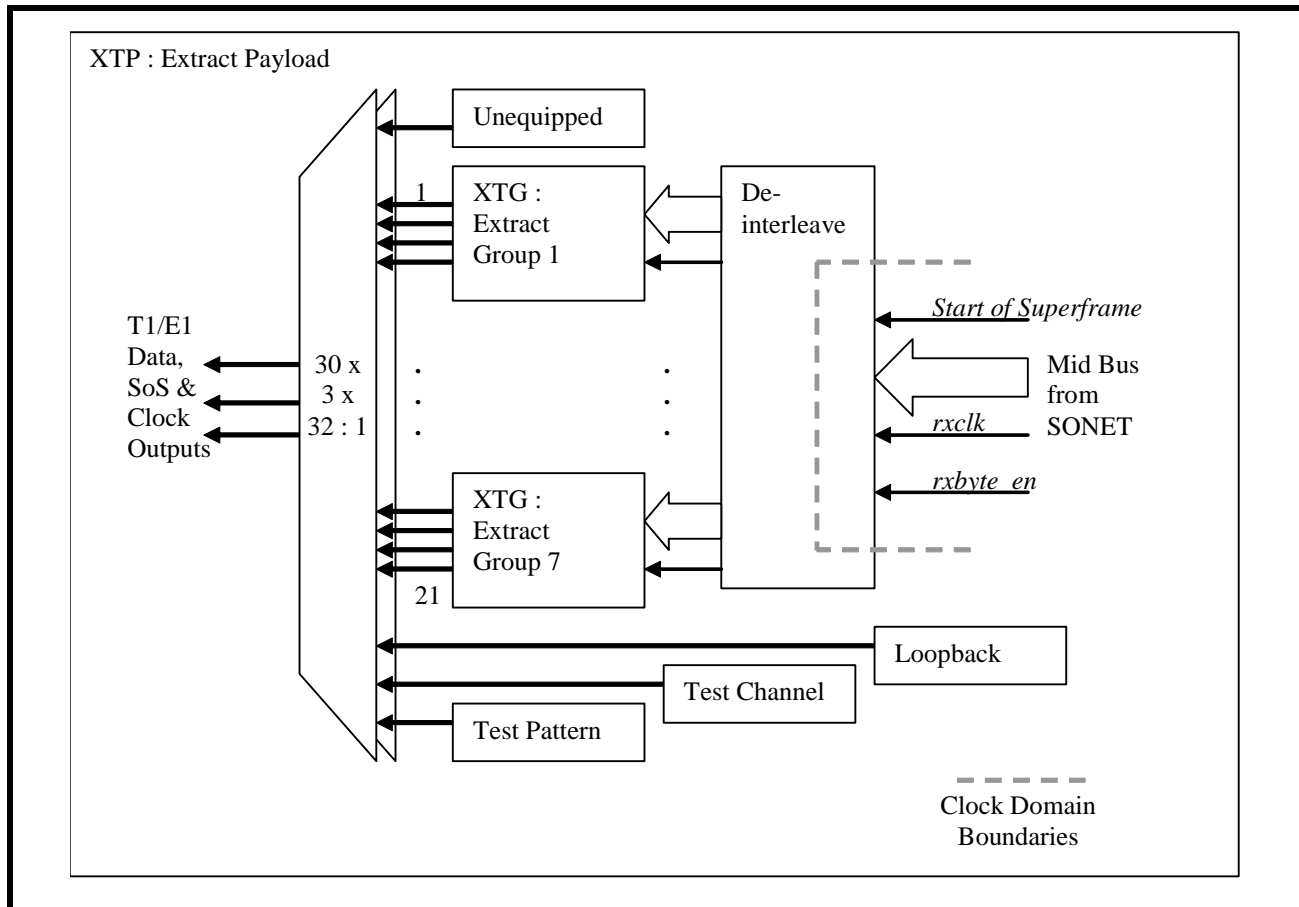
Test Channel

Two extra T1/E1 channels (one input, the other output) are available to be used as a test channel. The test channel's input and output can be used in the same way as any of the 28 T1 /21 E1 signals' inputs and outputs. They can be mapped into or extracted from the SONET stream, they can be looped back, or fed by or compared to the test pattern generator.

Test Pattern Generator (TPG)

The Test Pattern Generator can generate or compare to a pseudo random test pattern of length 2^{15}-1, a fixed pattern of all zeros, all ones, or alternating ones and zeros as recommended in ITU/CCITT Recommendation O.151. The pseudo random pattern is generated by a fifteen stage shift register whose 14th and 15th stage outputs are added in a modulo-two stage, and the result is fed back to the input of the first stage. The fed back bit is inverted before it is used as the next bit in the pseudo random sequence either for output or to be compared to. The test patterns of correct bit rate is made available to each of the Seven Groups according to the size of the tributaries assigned to each Group. In addition to valid clock and data signals, the TPG generates a valid Start of Superframe Pulse one T1/E1 clock tick wide at appropriate intervals, for synchronous T1/E1 mappings. This will emulate four null signalling bits.

Reference Clocks Generation (RCG)

The Reference Clock Generator block (RCG) divides the 19.44MHz input clock to generate clock signals of precise frequencies and signals used in loopback modes. The SONET loopback clock lbclk is simply a 6.48MHz clock obtained by dividing the input frequency by three. The loopback byte enable signal lbbyte_en is asserted for 86 out of every 90 lbclk clock ticks. The loopback Start of Superframe signal lbsos is a single pulse, one lbclk tick wide that occurs once every 4x9x90 lbclk ticks.

FIGURE 37. REFERENCE CLOCKS GENERATOR (RCG)
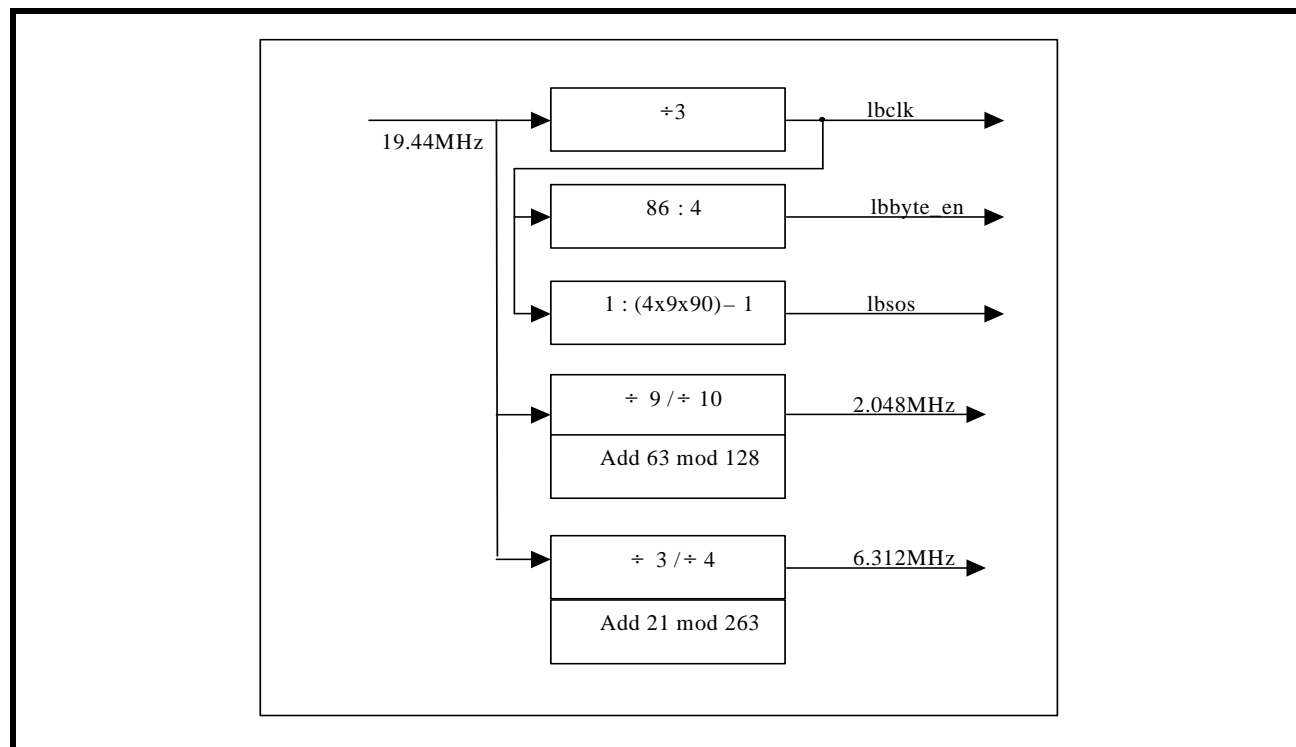
DATA INTERFACE BETWEEN SONET/FRAMER AND MAPPER

The data interface between the SONET and the Mapper blocks consist of three lines/buses in each direction: clk, byte lane, and byte enable. There are 1 byte lanes (8 bits) and 1 byte enable running at a data rate of 6.48MHz.

In the receive direction, the SONET payload data is sent to the receive mapper block. Data is presented on the byte lane on the rising edge of rclk with rbyte_en "High" representing the data is valid. The Mapper block then fetches the data on the next rising edge of rclk.

FIGURE 38. RECEIVE SONET/FRAMER MAPPER INTERFACE
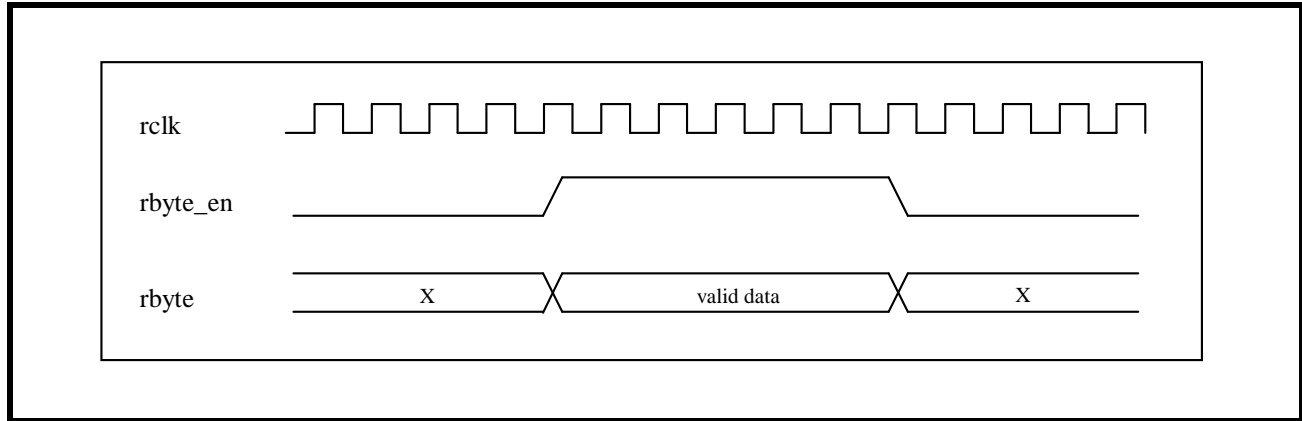
In the transmit direction, the SONET payload data is pulled from the transmit Mapper block. tbyte_en is used as an acknowledge signal indicating that data is recognized. When tbyte_en is asserted "High", data from the Mapper is latched into the SONET block on the next rising tclk edge.

FIGURE 39. TRANSMIT SONET/FRAMER MAPPER INTERFACE
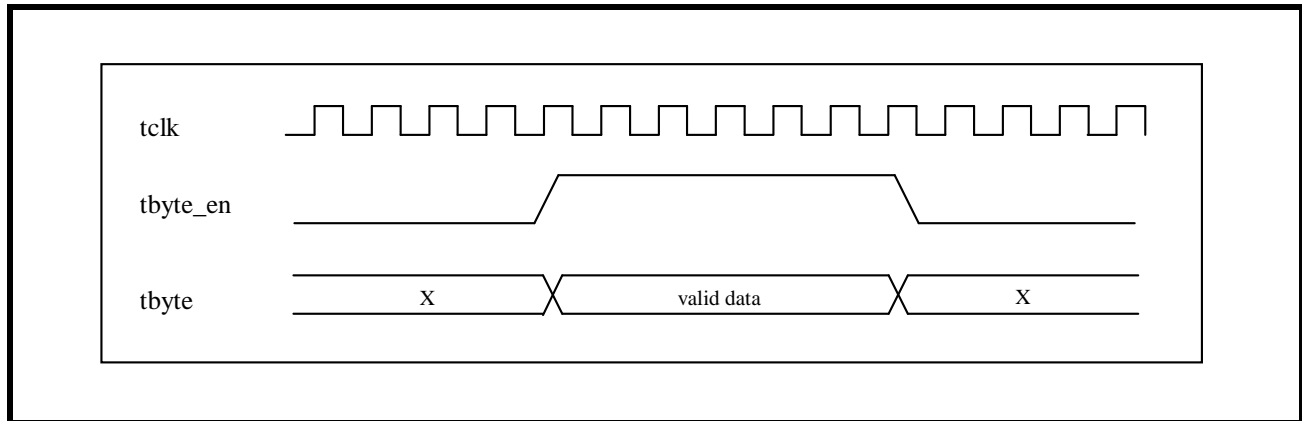
T1/E1 FRAME SYNCHRONIZATION

The T1/E1 framer establishes frame and multiframe boundaries by searching for frame alignment, CRC alignment, and channel associated signaling multiframe alignment in the incoming PCM data stream, and provides an output clock useful for data conditioning and decoding. User access to the T1/E1 framer is via the microprocessor bus interface. The framer incorporates a robust framing algorithm which prevents false synchronization on patterns that mimic the framing bits.

The T1/E1 framer monitors the incoming data stream from the LIU line interface module for loss of frame, loss of multiframe, etc. alignment based on user-selectable criteria, and searches for new frame alignment pattern when sync loss is detected. When sync loss is detected, the framer begins an off-line search for the new alignment and shifts into resync mode; all output timing signals remain at the old alignment during this period. When one and only one candidate is qualified, the output timing will move to the new alignment at the beginning of the next frame (or multiframe). One frame later, the framer resumes the normal sync monitoring mode and outputs the valid sync signal. The general synchronization flow diagram is illustrated in **Figure 40**.

FIGURE 40. T1/E1 FRAMER SYNCHRONIZATION FLOW DIAGRAM
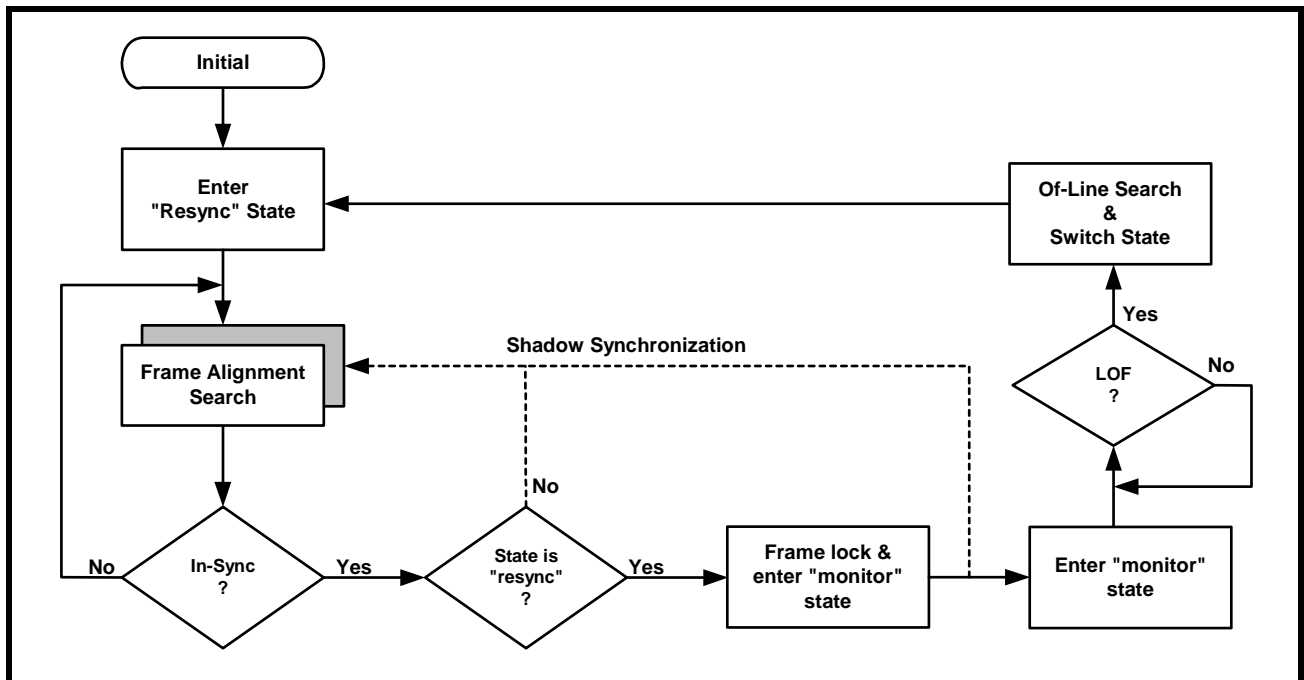
E1 FAS Synchronization

Three steps are involved in the synchronization process. The first one is finding FAS frame alignment. The second one searches for FAS using one of two user selectable algorithms as defined in Recommendation G.706. In addition, a two frame check sequence can be added optionally to either one of these two algorithm to provide protection against false frame alignment in the presence of random mimic patterns.

Algorithm 1:

Step 1: Seach for the presence of the correct 7-bit FAS pattern. Go to step 2 if found;

Step 2: Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timslot 0 byte is a one. Go back to step 1 if verification failed; Otherwise, go to step 3;

Step 3: Check if the FAS is present in the assumed timeslot 0 byte of the third frame. Go back to step 1 if failed.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the errored timeslot 0 byte locaiton. If both conditions are met and frame check sequence is enabled, then an additional check sequence is initiated. The check sequence consists of verifying correct frame alignment for an additional two frames.

Step 4: Once the frame alignment is found, check if the FAS is absent in the following frame by verifying the bit 2 of timeslot 0 being a one. If verification failed, go back to step 1.

Step 5: Check that the FAS is present of the next frame. If not, go back to step 1.

The second algorithm is similar to the first one, but adds a one frame hold-off in the second step to begin a new search in the bit immediately following the second (third frame) assumed FAS. This extra frame hold-off is performed only after the condition in step 2 fails to provide a robust algorithm which allows the framer to operate correctly in the presence of fixed timeslot imitating the FAS pattern.

Algorithm 2:

Step 1: Seach for the presence of the correct 7-bit FAS pattern. Go to step 2 if found;

Step 2: Check if the FAS is absent in the following frame by verifying that bit 2 of the assumed timslot 0 byte is a one. Go to step 4 if varification failed; Otherwise, go to step 3;

Step 3: Check if the FAS is present in the assumed timeslot 0 byte of the third frame. Go back to step 1 if failed; Otherwise start check sequence if enabled.

Step 4: Wait for assumed FAS in next frame, then go back to step 1.

If both conditions are met and frame check sequence is enabled, then an additional check sequence is initiated. The check sequence consists of verifying correct frame alignment for an additional two frames.

Step 5: Once the frame alignment is found, check if the FAS is absent in the following frame by verifying the bit 2 of timeslot 0 being a one. If verification failed, go back to step 4.

Step 6: Check that the FAS is present of the next frame. If not, go back to step 1.

When synchronization is achieved, the framer monitors alignment signals for errors. A Red Alarm (FASRED) is generated if frame alignment is lost. The criteria for loss of frame alignment in FAS framing is dictated by an T1/E1 Framing Control Register (FCR). The MSB of this register is an RSYNC bit which imposes the framer to restart the resync process even if the frame is currently in sync. This bit will be cleared after the framer resumes its normal sync monitoring mode. The FAS criteria bits specify the number of consecutive erred FAS patterns determining the loss of FAS alignment. Note: Loss of FAS alignment forces loss of CAS and loss of CRC alignment.

It is important to note that the off-line searching is conducted by a shadow synchronizer. The shadow synchronizer continuously searches for the frame alignment even if the framer is in the in-sync state. Once the loss of frame is declared and the resync mode is entered, the framer can shift back into monitor mode by moving to the new alignment at the beginning of the next frame as long as the shadow synchronizer is in-sync. This feature dramatically reduces the reframe time required.

CRC Synchronization

After the FAS frame alignment is declared, the second step is to find the CRC-4 multiframe alignment. This is done by observing whether the international bits (bit 1 of timeslot 0) of non-FAS frames match the CRC multiframe alignment pattern. Multiframe alignment is declared if at least the valid CRC multiframe alignment signals are observed within 8ms. The CRC synchronization logic will force a FAS frame search when CRC multiframe alignment has not been found for 8ms.

Once the CRC multiframe alignment is found, the Out Of CRC MultiFame alignment indication is cleared. The CRC synchronizer monitors the multiframe alignment signal, indicates errors occurring in the 6-bit CRC pattern, and indicates the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The loss of CRC multiframe alignment is declared if consecutive CRC multiframe alignment signals have been received in error.

When synchronization is achieved, the framer monitors the multiframe alignment signals for errors. A CRC LOF indication is set to "1" if frame alignment is lost. The criteria for loss of CRC multiframe alignment is dictated by CRCC bits in E1 Framing Control Register.

Annex B compliance

When ModEnb is "1", G.706 Annex B modified CRC-4 multiframe alignment algorithm is implemented. If CRC-4 alignment is enabled and not achieved in 400ms while the basic frame alignment signal is present, it is assumed that the remote end is a non-CRC-4 equipment. The flow chart in **Figure 41** demonstrates this algorithm.

FIGURE 41. FLOW OF CRC-4 MULTIFRAME ALIGNMENT FOR INTERWORKING
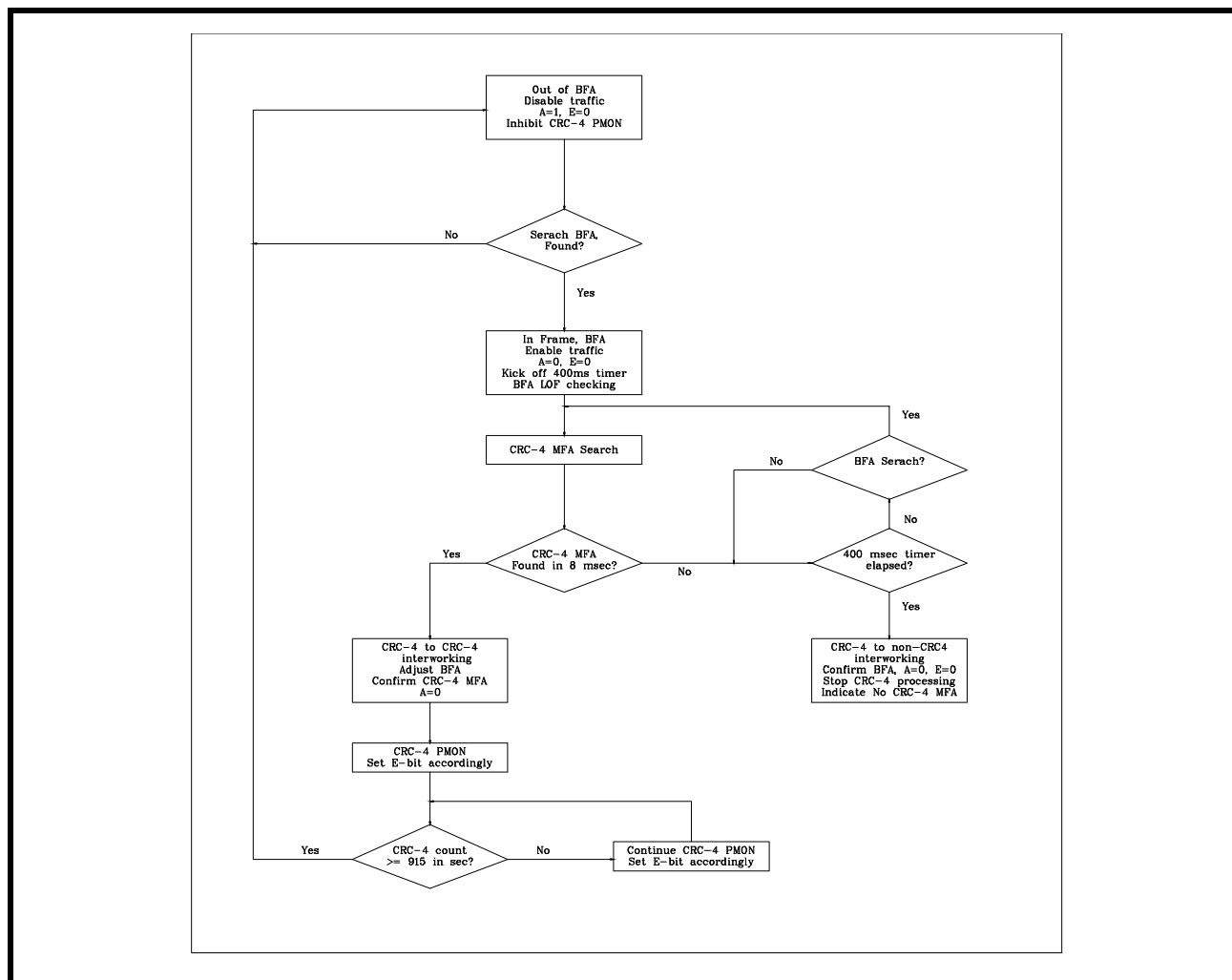
A 400ms CRC-4 multiframe alignment search period is applied for interworking detection. The 400 msec timer is triggered on the initial recovery of basic frame alignment and is not reset until the loss of basic frame alignment occurs. A re-search for FAS will be initiated if CRC-4 multifame alignment can not be found in 8ms and will not reset the 400ms timer or invoke the consequent actions associated with loss of FAS. All subsequent searches for CRC-4 multiframe alignment are associated with each basic FAS found. In order to maintain no disturbance to traffic during the 400ms CRC-4 multiframe search, traffic should be allowed through with synchronization to the initially determined primary basic frame alignment sequence. If a CRC-4 multiframe alinment signal is found befoe the 400ms timer elapses, then the basic FAS associated with the CRC-4 multiframe alignment signal should be the one chosen, i.e. the primary basic FAS should be amended accordingly if the basic FAS alignment changed. If a CRC-4 multiframe alignment sequence can not be found in 400ms, it should be concluded that a condition of interworking between equipments with and without a CRC-4 capability exist, so the traffic should be maintained to the initially determined FAS alignment.

If the path is reconfigured at any time, then it is assumed that the new pair of path will need to re-establish the complete framing process, i.e. the algorithm is reset.

Consequent actions are taken while a non-CRC-4 remote side is detected:

- The Framer will provide an indication that there is no incoming CRC-4 multiframe alignment signal
- The Framer will inhibit further CRC-4 processing
- The Framer will continue to transmit CRC-4 data to the remote side with both E bits set to zero

In this modified framing mode, the framer always sets the return E bits to zero until the interworking relationship has been established. If CRC-4-to-CRC-4 interworking is established, then normal CRC-4 processing of erred CRC-4 block data should commence. If CRC-4-to-non-CRC-4 interworking is established, the E bits should remain at 0.

CAS Synchronization

After the FAS frame alignment is declared, the third step is to find CAS multiframe alignment. Two user-selectable algroithms are available.

Algorthm 1 monitors the sixteenth timeslot of each frame and declares CAS multiframe alignment when 15 consecutive frames with bits 1-4 of timeslot 16 not containing the alignment pattern are observed to precede a frame with timeslot 16 containing the correct alignment pattern.

Algorthm 2 monitors the sixteenth timeslot of each frame and declares CAS multiframe alignment when non-zero bits 1-4 of timeslot 16 are observed to precede a timeslot 16 containing the correct alignment pattern.

Once the CAS multiframe alignment is found, the Out Of CAS MultiFame alignment indication is cleared. The CAS synchronizer monitors the multiframe alignment signal, indicates errors occurring in the 4-bit alignment pattern, and indicates the debounced value of the remote signaling multiframe alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe).

When synchronization is achieved, the framer monitors multiframe alignment signals for errors. The CAS LOF indication turns on if frame alignment is lost. The criteria for loss of CRC multiframe alignment is dictated by the CASC bits in the E1 Framing Control Register.

FRAME COUNTERS AND TIMING GENERATION

Receive Frame and Multiframe counters and timing generators provide timing for frame and multiframe alignment, CRC-4 check, signaling extraction, facility data link extraction, yellow alarm, and all the timing for per-channel parameter fetch. The data extracted from this timing is placed into the appropriate internal storage elements for the microprocessor to access. The information extracted is not valid unless the receive module has achieved valid synchronization.

CRC-4 VERIFICATION

The CRC verification is performed by calculating the 4-bit CRC checksum for each incoming sub-multiframe and comparing this result to the received CRC remainder bits in the subsequent sub-multiframe. The CRC errors are accumulated over one second intervals. Optionally, a CRC frame resync can be initiated when 915 or more CRC errors occur in one second. The number of CRC errors accumulated during the previous second is available by reading the T1/E1 Receive Synchronization Bit Error Counter.

ALARM AND ERROR INDICATION

The Alarm indication logic examines the incoming T1/E1 data for alarm conditions. When the change of an alarm condition is detected, corresponding bits are set in the Alarm and Error Status Register. The Alarm and Error Interrupt Enable Register is used to select the events that generate interrupts on the microprocessor interrupt pin when their state changes.

LOF (Red Alarm) Defect/Alarm

When DEFDET=1, the Loss Of Frame defect is detected when "FASC" (in framing control register) consecutive incorrect frame alignment signals have been received (default is 3 to comply with G.706). It is cleared when 2 consecutive FAS's are detected.

When DEFDET = 0, The red alarm is detected by monitoring the occurrence of Loss Of Frame (LOF) over a 4 ms interval. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 25 valid intervals have been accumulated. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

TRANSMIT SLIP BUFFERING

The Voyager has two-frame (512 bits) elastic stores. This store can be enabled or disabled via programming bits SB_ENB in the Slip Buffer Control and Status Register (SBCSR). If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. If the slip buffer is bypassed (SB_ENB[1:0] = 00 or 11), the slip buffer is used as a regular JA buffer. If SB_ENB = 2, the slip buffer is put into a FIFO mode. In the FIFO mode, the slip buffer is acting like a standard first-in-first-out storage. A fixed read and write latency is maintained in a programmable fashion controlled by the FIFO Latency Register. However, the user should assume the responsibility to phase lock the input clock to the receive clock to avoid either overrun or under-run. A Slip Buffer Control & Status register is used to control the slip buffer operations and control interrupts and report its status.

4.11   T1/E1 PHY LOOPBACK DIAGNOSTICS

This section provides some architectural views and implementation details regarding to the system level integration and performance.

4.11.1   T1/E1 LOOPBACKS

Various controls in the VT Mapper module and T1/E1 framer module allow Voyager to conduct many types of loopbacks for supporting system diagnosis. Three of them are explained here: T1/E1 facility loopback, T1/E1 facility I/O loopback and T1/E1 module loopback.

T1/E1 facility loopback

Figure 42 shows this type of loopback by sending the ingress T1/E1 inputs back to egress T1/E1 outputs.

FIGURE 42. T1/E1 FACILITY LOOPBACK
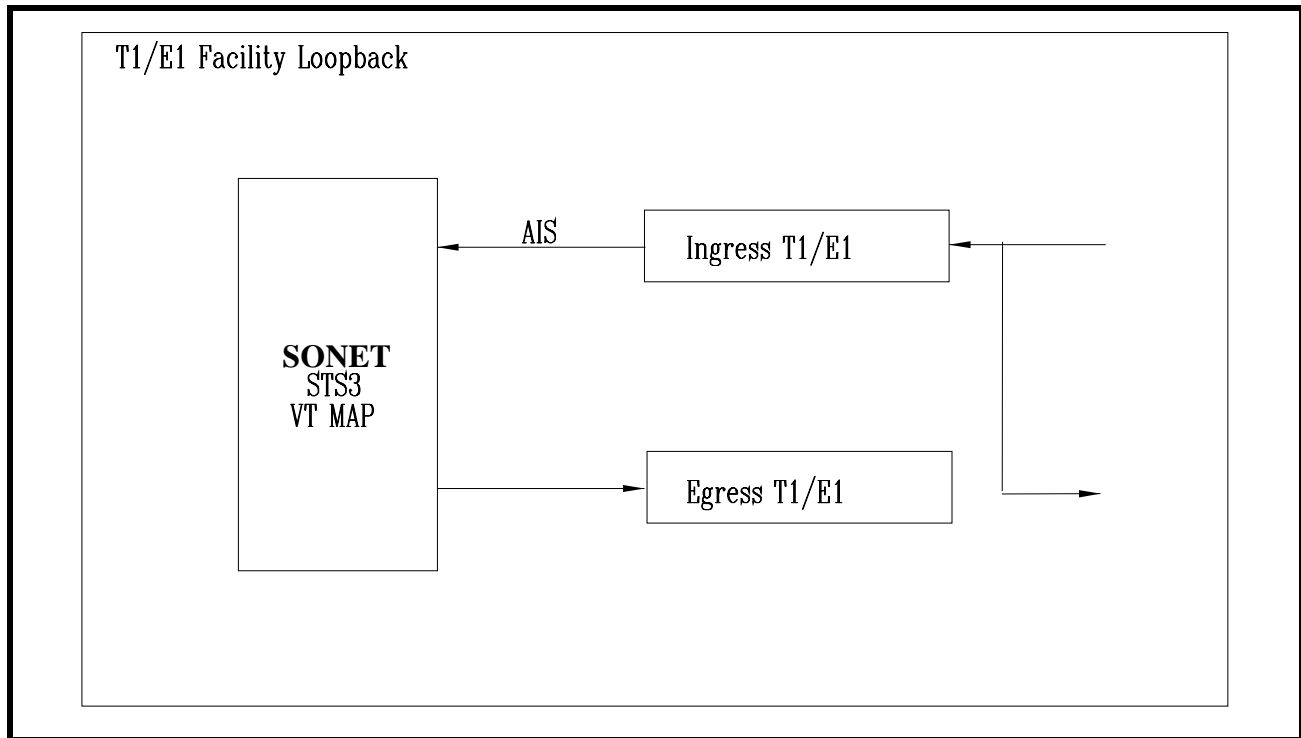
4.11.2   T1/E1 facility I/O loopback

Figure 43 shows the this type of loopback by connecting the egress T1/E1 outputs to the ingress T1/E1 inputs.

FIGURE 43. T1/E1 FACILITY I/O LOOPBACK
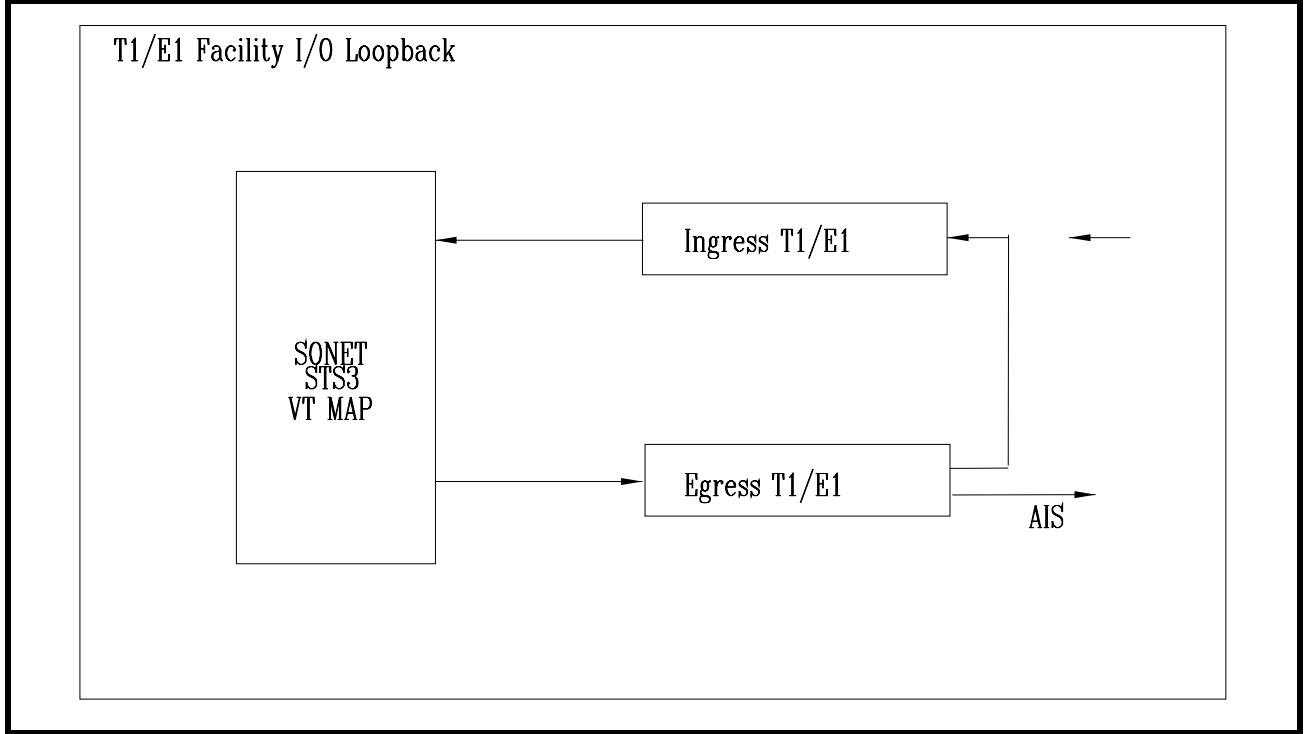
4.11.3   T1/E1 module loopback

Figure 44 shows the this type of loopback by sending the ingress T1/E1 framer outputs back to egress T1/E1 framer inputs.

FIGURE 44. T1/E1 MODULE LOOPBACK
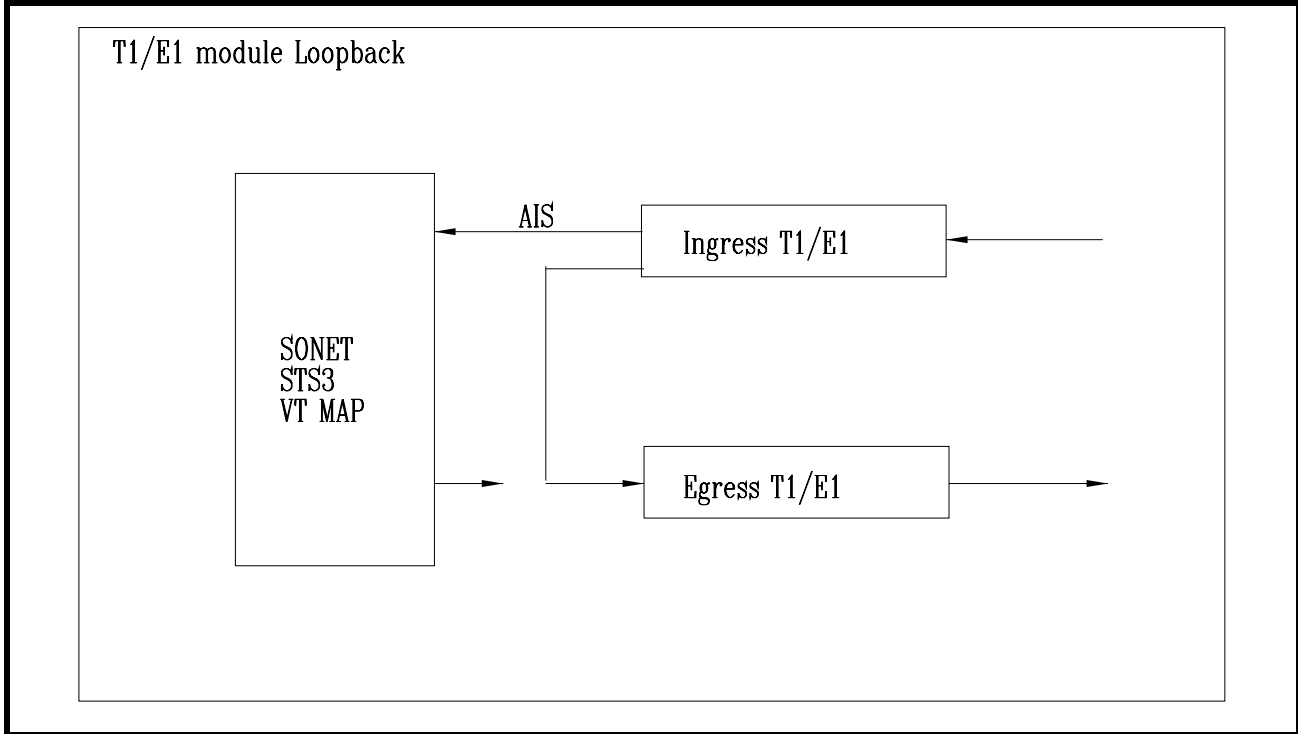
4.11.4 ALARM AND AUTO AIS

Voyager provides the capability to insert alarm, especially AIS, automatically into the data down stream while exceptional conditions occur. **Figure 45** shows the basic structure of the Auto AIS insertion. Note: Each condition is optional

FIGURE 45. T1/E1 AUTO AIS INSERTION
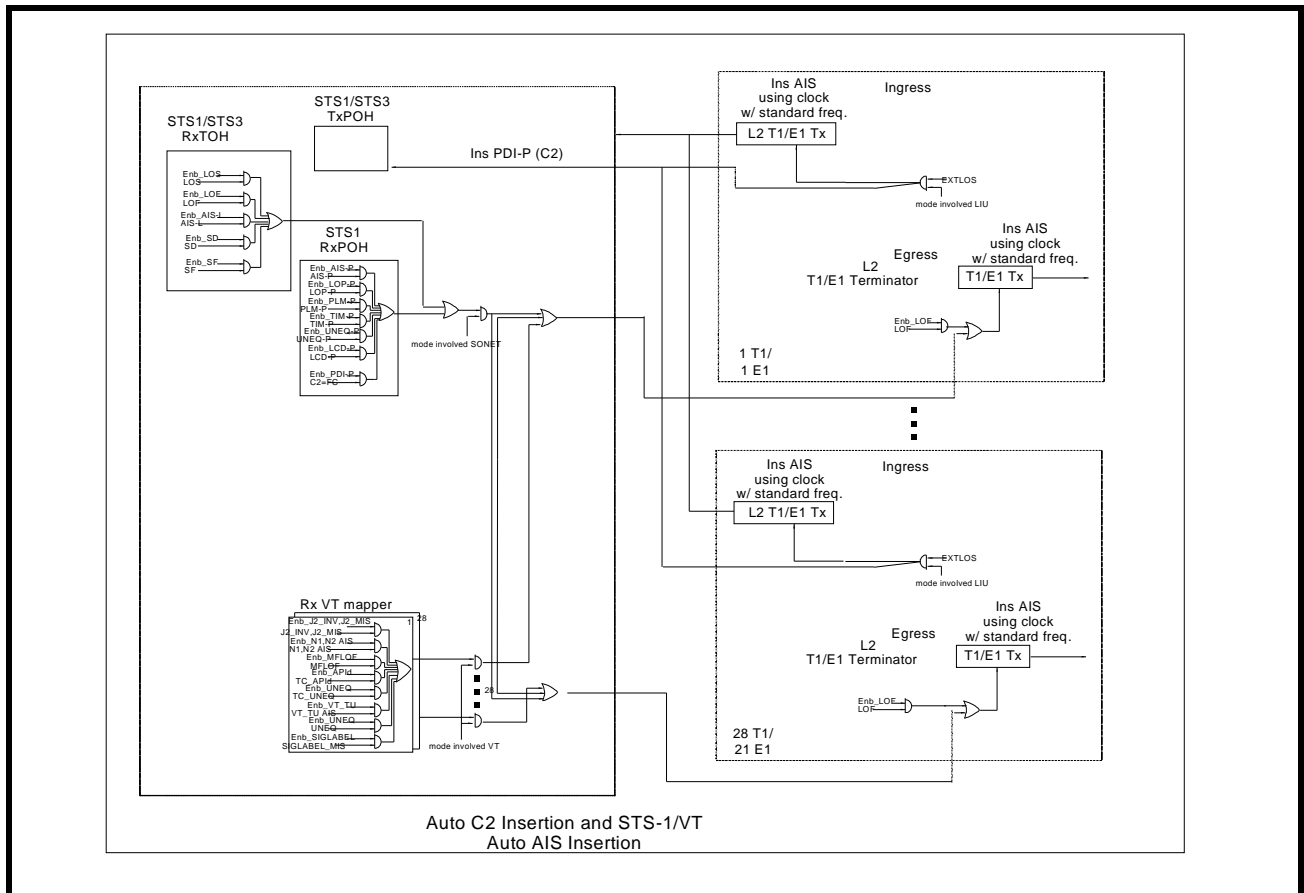
TABLE 13: T1/E1 TO STS1/STS3 - RESPONSE TIME < 125 USEC

T1/E1 CONDITION	STS1/STS3 RESPONSE
LOS	T1/E1-AIS,PDI-P/AIS-P
LOF	PDI-P/AIS-P
AIS-L	PDI-P/AIS-P

TABLE 14: STS1/STS3 TO T1/E1 - RESPONSE TIME < 125 USEC

STS1/STS3 CONDITION	T1/E1 RESPONSE	STS1/STS3 RETURN PATH
LOS	T1/E1 AIS	RDI-L, RDI-P
LOF	T1/E1 AIS	RDI-L, RDI-P
AIS-L	T1/E1 AIS	RDI-L, RDI-P

TABLE 14: STS1/STS3 TO T1/E1 - RESPONSE TIME < 125 USEC

STS1/STS3 CONDITION	T1/E1 RESPONSE	STS1/STS3 RETURN PATH
LOP-P	T1/E1 AIS	RDI-P
AIS-P	T1/E1 AIS	RDI-P
UNEQ-P	T1/E1 AIS	RDI-P
PLM-P	T1/E1 AIS	RDI-P
TIM-P	T1/E1 AIS	RDI-P

5.0   ANALOG FRONT END / LINE INTERFACE UNIT (LIU) SECTION

The analog front end section is a fully integrated, 28-channel T1/ 21-channel E1 LIU for 75Ω or 120Ω applications. With internal termination and an option for high impedance, the LIU uses one bill of materials to support Coax or Twisted Pair medium and supports 1:1 or 1+1 redundancy. Each transmitter has an optional Jitter Attenuator and can provide basic diagnostic features that can be used to send data to the line interface. Each receiver accepts standard T1/E1 pulses, provides clock and data recovery, basic diagnostic detection, and an optional Jitter Attenuator before presenting data to the VT Mapper section. A simplified block diagram of the LIU section can be seen below.

FIGURE 46.   SIMPLIFIED BLOCK DIAGRAM OF THE LIU SECTION

5.1   TRANSMIT LINE INTERFACE UNIT

5.1.1   Jitter Attenuator

The LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1/E1 data, stuffing bits are typically removed which can leave gaps in the incoming data stream. The jitter attenuator can be selected in the transmit path with a 32-Bit or 64-Bit FIFO that is used to smooth the gapped clock into a steady T1/E1 output. The maximum gap width that the jitter attenuator can accept without a disruption in data flow is shown below.

FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: If the LIU is used in a loop timing system, the jitter attenuator can be selected in the receive path. See the Receive LIU Section of this datasheet.

5.1.2   TAOS (Transmit All Ones)

The LIU section has the ability to transmit all ones on a per channel basis by programming the appropriate channel register. This function takes priority over the digital data present on its digital inputs from the VT Mapper section. **Figure 47** is a diagram showing the all ones signal at TTIP and TRING.

FIGURE 47. TAOS (TRANSMIT ALL ONES)

5.1.3   ATAOS (Automatic Transmit All Ones)

If ATAOS is selected by programming the appropriate global register, an AMI all ones signal will be transmitted for each channel that experiences an RLOS condition. If RLOS does not occur, the ATAOS will remain inactive until an RLOS on a given channel occurs. A simplified block diagram of the ATAOS function is shown in **Figure 48**.

FIGURE 48. SIMPLIFIED BLOCK DIAGRAM OF THE ATAOS FUNCTION

5.1.4   QRSS/PRBS Generation

The LIU section can transmit a QRSS/PRBS random sequence to a remote location from TTIP/TRING. To select QRSS or PRBS, see the register map for programming details. The polynomial for each selection is shown below.

RANDOM PATTERN	T1 AND E1
QRSS	2^{20} - 1
PRBS	2^{15} - 1

5.1.5   Transmit Pulse Shaper and Filter

If TCLK is not present from the VT Mapper section, pulled "Low", or pulled "High" the transmitter outputs at TTIP/TRING will automatically send an all ones or an all zero signal to the line by programming the appropriate global register. By default, the transmitters will send all zeros. To send all ones, the TCLKCNL bit must be set "High".

5.1.6   DMO (Digital Monitor Output)

The driver monitor circuit is used to detect transmit driver failures by monitoring the activities at the TTIP/TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit inputs. If the transmitter of a channel has no output for more than 128 clock cycles, DMO goes "High" until a valid transmit pulse is detected. If the DMO interrupt is enabled, the change in status of DMO will cause the interrupt pin to go "Low". Once the status register is read, the interrupt pin will return "High" and the status register will be reset (RUR).

5.2   Line Termination (TTIP/TRING)

The output stage of the transmit path generates standard return-to-zero (RZ) signals to the line interface for T1/E1 twisted pair or E1 coaxial cables. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for 100Ω, 75Ω, and 120Ω reducing the number of external components necessary in system design. The transmitter outputs only require one DC blocking capacitor of 0.68μF. For redundancy applications (or simply to tri-state the transmitters), set TxTSEL to a "0" in the appropriate channel register. A typical transmit interface is shown in **Figure 49**.

FIGURE 49. TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION
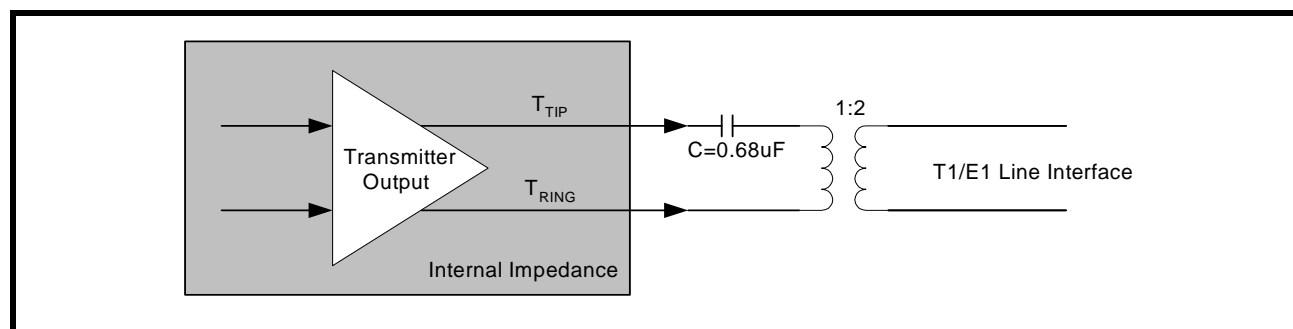
5.3   Receive path line interface

The receive path of the LIU section consists of 28 independent T1 or 21 independent E1 receivers. The following section describes the complete receive path from RTIP/RRING inputs to RCLK/RPOS outputs which are then sent to the VT Mapper interface internal to the chip. A simplified block diagram of the receive path is shown in **Figure 50**.

FIGURE 50.   SIMPLIFIED BLOCK DIAGRAM OF THE RECEIVE PATH
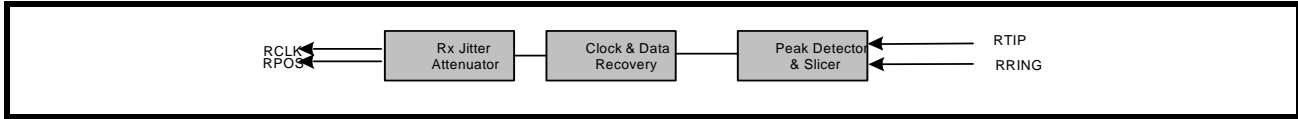
5.3.1   Line Termination (RTIP/RRING)

The input stage of the receive path accepts standard T1/E1 twisted pair or coaxial cable inputs through RTIP and RRING. The physical interface is optimized by placing the terminating impedance inside the LIU. This allows one bill of materials for 100Ω, 110Ω, 75Ω, and 120Ω operation reducing the number of external components necessary in system design. The receive termination impedance (along with the transmit impedance) is selected by programming TERSEL to match the line impedance. Selecting the internal impedance is shown below.

TERSEL[1:0]	LINE TERMINATION
00	100Ω
01	110Ω
10	75Ω
11	120Ω

The LIU section has the ability to switch the internal termination to "High" impedance by programming RxTSEL in the appropriate channel register. For internal termination, set RxTSEL to "1". By default, RxTSEL is set to "0" ("High" impedance). See **Figure 51** for a typical connection diagram using the internal termination.

FIGURE 51.   TYPICAL CONNECTION DIAGRAM USING INTERNAL TERMINATION
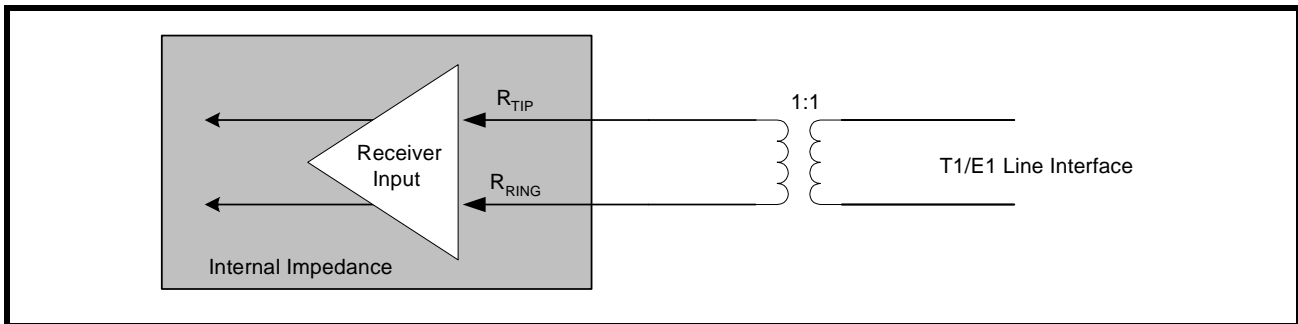
5.3.2   Clock and Data Recovery

The receive clock (RCLK) is recovered by the clock and data recovery circuitry. An internal PLL locks on the incoming data stream and outputs a clock that's in phase with the incoming signal. This allows for multi-channel T1/E1 signals to arrive from different timing sources and remain independent. In the absence of an incoming signal, RCLK maintains its timing by using the internal master clock (64 x MCLK) as its reference (MCLK). Once, RLOS is cleared, the recovered line clock switches back to RCLK. See **Figure 52** for the detailed timing specifications.

FIGURE 52. RECOVERED LINE CLOCK PLL TIMING
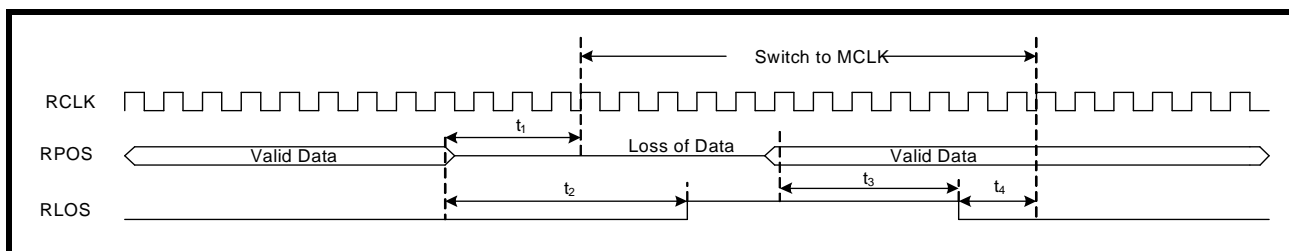
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Switching time from RCLK to MCLK	t_1			14.6	μS
RLOS declares Loss of Signal	t_2		See Note 2.		
RLOS clears Loss of Signal	t_3		See Note 2		
Switching time from MCLK to RCLK	t_4			18.1	μS

NOTE: *1. VDD=3.3V ±5%, T_A=25℃, Unless Otherwise Specified*

NOTE: *2. RLOS declaration and clearance depends on which mode is selected. The LIU supports both G.775 and ETSI-300-233. Refer to the register map for more details.*

5.3.3   Recovered Line Clock Outputs

There are two output pins that can be used to select among the 28 T1/ 21 E1 Recovered Line Clock signals. These signals can be used as a timing reference relative to the two channels chosen. The pins are REF_REC1 and REF_REC0.

FIGURE 53. REF_REC[1:0] RECOVERED LINE CLOCK SELECTION TO OUTPUT PINS
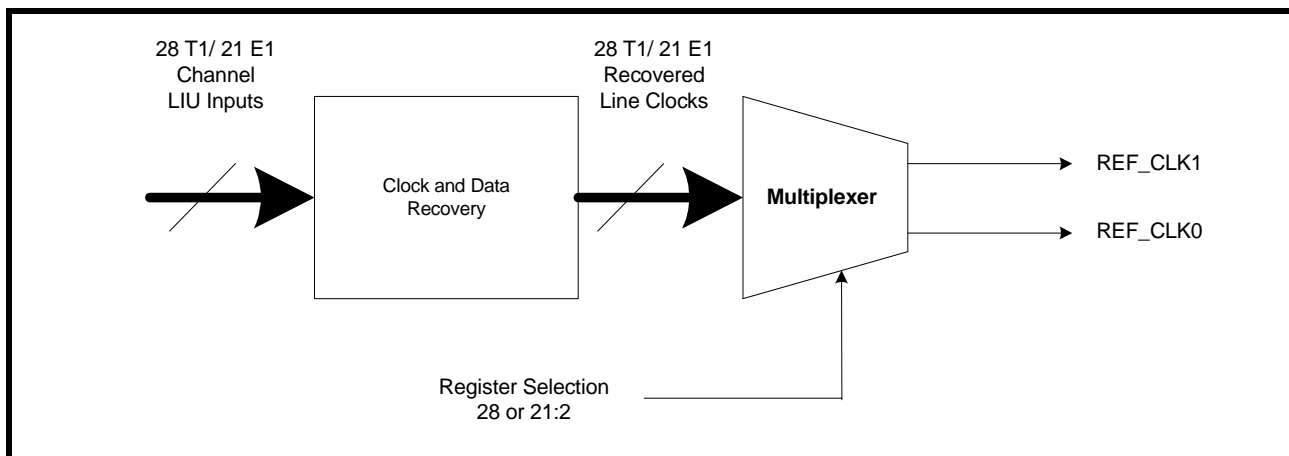
5.3.4 RLOS (Receiver Loss of Signal)

The LIU section supports both G.775 or ETSI-300-233 RLOS detection.

In G.775 mode, RLOS is declared when the received signal is less than 375mV for 32 consecutive pulse periods (typical). The device clears RLOS when the receive signal achieves 12.5% ones density with no more than 15 consecutive zeros in a 32 bit sliding window and the signal level exceeds 425mV (typical).

In ETSI-300-233 mode, the device declares RLOS when the input level drops below 375mV (typical) for more than 2048 pulse periods (1msec).

The device exits RLOS when the input signal exceeds 425mV (typical) and has transitions for more than 32 pulse periods with 12.5% ones density with no more than 15 consecutive zero's in a 32 bit sliding window.

5.3.5 EXLOS (Extended Loss of Signal)

By enabling the extended loss of signal by programming the appropriate channel register, the digital RLOS is extended to count 4,096 consecutive zeros before declaring RLOS. By default, EXLOS is disabled and RLOS operates in normal mode.

5.3.6 Jitter Attenuator

The jitter attenuator reduces phase and frequency jitter in the recovered clock if it is selected in the receive path. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth of 32-bit or 64-bit. If the LIU is used for line synchronization (loop timing systems), the JA should be enabled in the receive path. When the Read and Write pointers of the FIFO are within 2-Bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this condition occurs, the jitter attenuator will not attenuate input jitter until the Read/Write pointer's position is outside the 2-Bit window. The bandwidth is programmable to either 10Hz or 1.5Hz (1.5Hz automatically selects the 64-Bit FIFO depth). The JA has a clock delay equal to ½ of the FIFO bit depth.

NOTE: If the LIU is used in a multiplexer/mapper application where stuffing bits are typically removed, the jitter attenuator can be selected in the transmit path to smooth out the gapped clock. See the Transmit LIU Section of this datasheet.

5.3.7 RxMUTE (Receiver LOS with Data Muting)

The receive muting function can be selected by setting RxMUTE to "1" in the appropriate global register. If selected, any channel that experiences an RLOS condition will automatically pull RPOS "Low" to prevent data chattering to the internal connection to the VT Mapper section. If RLOS does not occur, the RxMUTE will remain inactive until an RLOS on a given channel occurs. The default setting for RxMUTE is "0" which is disabled. A simplified block diagram of the RxMUTE function is shown in **Figure 54**.

FIGURE 54. SIMPLIFIED BLOCK DIAGRAM OF THE RxMUTE FUNCTION
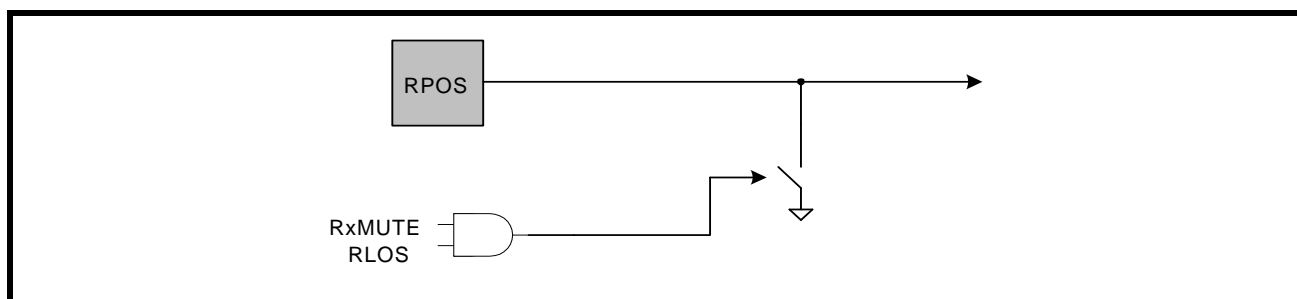
6.0 MICROPROCESSOR INTERFACE TIMING

6.1 *MICROPROCESSOR INTERFACE TIMING - INTEL ASYNCHRONOUS MODE*

In Intel Asynchronous mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, ALE, $\overline{WR}$, $\overline{RD}$ and $\overline{RDY}$. A READ cycle starts with assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus. Inside XRT86SH328 address is latched on the falling edge of the ALE input. Address may change on the ADDR inputs after the falling edge of the ALE.

Multiplexed Address & Data bus is supported in this mode using ALE input. It is possible to pull-up the ALE input if multiplexed address and data mode is not used. In this case the address should be stable through entire read or write instruction cycle.

Following falling edge of ALE, $\overline{RD}$ is asserted for the READ operation. $\overline{RD}$ must remain asserted until $\overline{RDY}$ is asserted by the XRT86SH328 device, which indicates DATA from the addressed location is available on the data bus. RD and CS can be de-asserted when the data has been read by the processor.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{RDY}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that following falling edge of ALE $\overline{WR}$ is asserted. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WR}$ is asserted. $\overline{WR}$ should remain asserted until $\overline{RDY}$ is asserted by the XRT86SH328 device. Following $\overline{RDY}$ assertion $\overline{WR}$ and $\overline{CS}$ may be de-asserted.

FIGURE 55. INTEL-ASYNCHRONOUS MODE TIMING - WRITE OPERATION
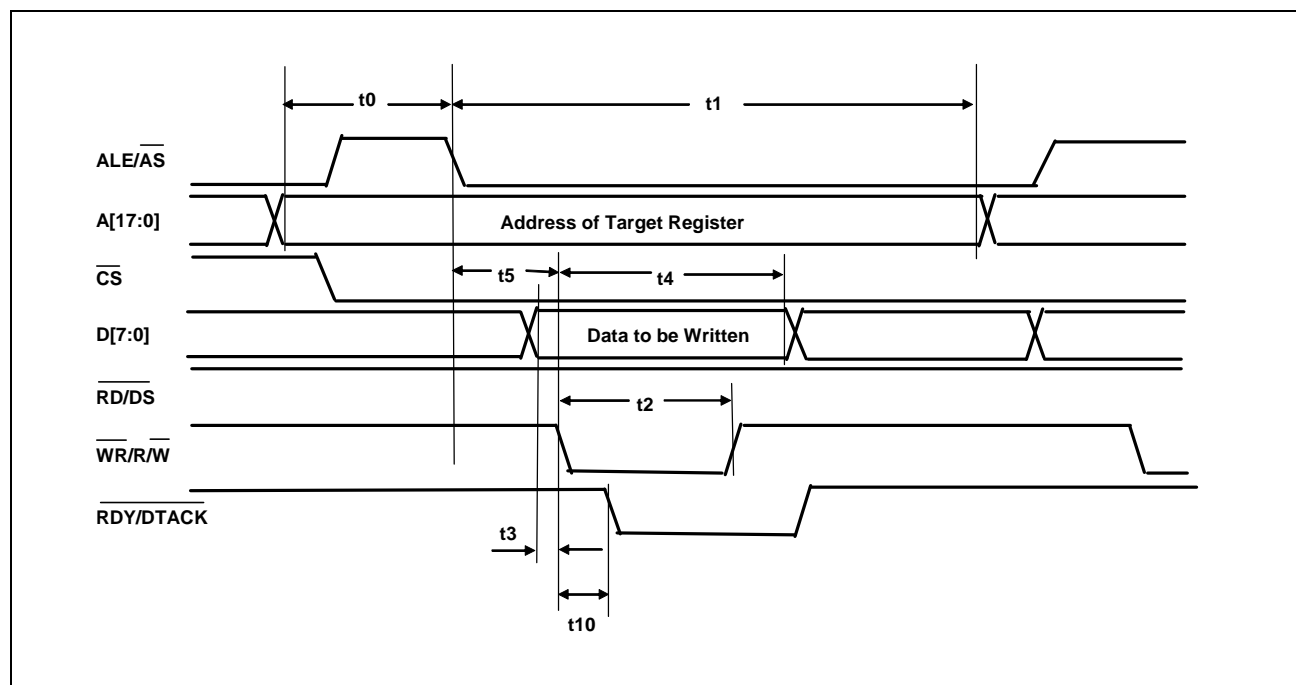
Note: The values for t0 through t10, within this figure can be found in **Table 15**.

Table 15   Intel Asynchronous Mode Timing - Write Operation

TimingSymbol	Description	Min.	Typ.	Max.	Units
	Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified				
t0	Address setup time to ALE "Low"	5	-	-	ns
t1	Address hold time from ALE "Low"	5	-	-	ns
t2	$\overline{WR}$ strobe pulse width	150	-	-	ns
t3	Data setup time to $\overline{WR}$ "Low"	25	-	-	ns
t4	Data hold time from $\overline{WR}$ "Low"	200	-	-	ns
t5	ALE "Low" set-up time to $\overline{WR}$ "Low"	50	-	-	ns
t10	$\overline{WR}$ "Low" to $\overline{RDY}$ "Low" delay time	-	-	125	ns

FIGURE 56. INTEL-ASYNCHRONOUS MODE TIMING - READ OPERATION
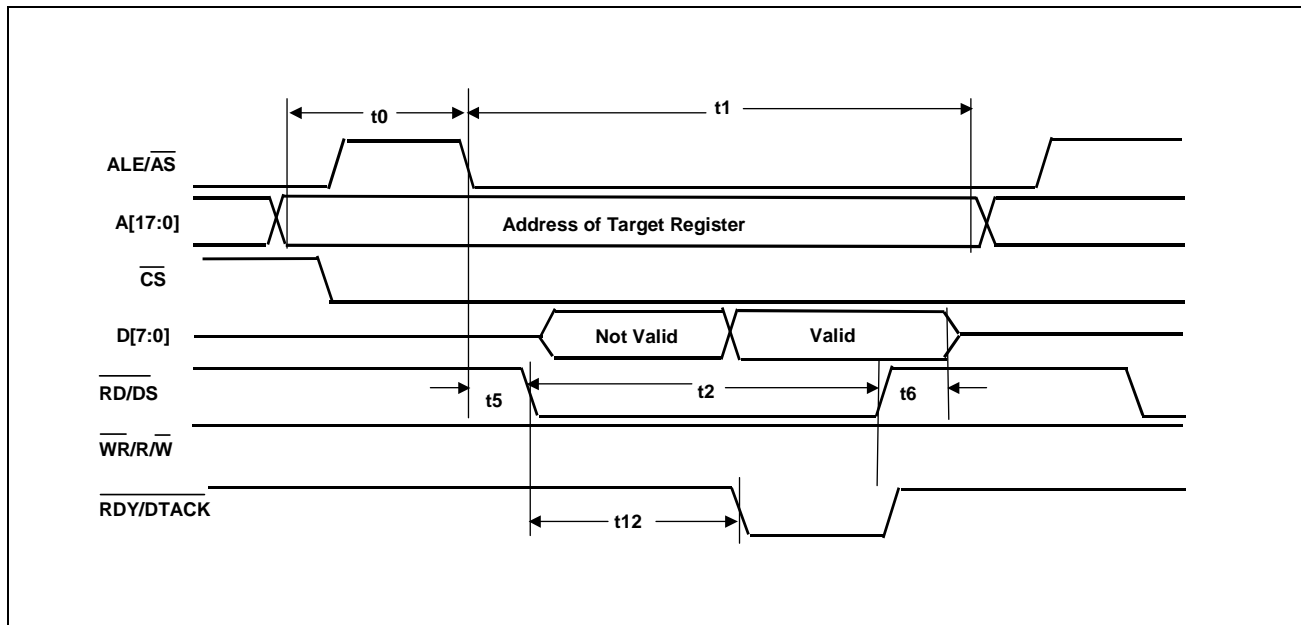
Note: The values for t0 through t10, in this figure can be found in **Table 16**.

Table 16   Intel Asynchronous Mode Timing - Read Operation

TimingSymbol	Description	Min.	Typ.	Max.	Units
	Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified				
t0	Address setup time to ALE "Low"	5	-	-	ns
t1	Address hold time from ALE "Low"	5	-	-	ns
t2	$\overline{RD}$ strobe pulse width	200	-	-	ns
t5	ALE "Low" set-up time to $\overline{RD}$ "Low"	50	-	-	ns
t6	Data Invalid delay from $\overline{RD}$ "High"	-	-	9	ns

Table 16   **Intel Asynchronous Mode Timing - Read Operation**

t12	$\overline{RD}$ "Low" to $\overline{RDY}$ "Low" delay time	-	-	125	ns

6.2 MICROPROCESSOR INTERFACE TIMING - MOTOROLA ASYNCHRONOUS (68K) MODE

In Motorola Asynchronous mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{DS}$ and $\overline{DTACK}$. A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

In this mode the address should be stable through entire read or write instruction cycle.

Following falling edge of $\overline{CS}$, $\overline{DS}$ is asserted for the READ operation. $\overline{DS}$ must remain asserted until $\overline{DTACK}$ is asserted by the XRT86SH328 device, which indicates DATA from the addressed location is available on the data bus. $\overline{DS}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{DTACK}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{DS}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{DS}$ is asserted. $\overline{DS}$ should remain asserted until $\overline{DTACK}$ is asserted by the XRT86SH328 device. Following assertion of $\overline{DTACK}$ $\overline{DS}$ and $\overline{CS}$ may be de-asserted.

FIGURE 57. MOTOROLA-ASYNCHRONOUS MODE TIMING - WRITE OPERATION
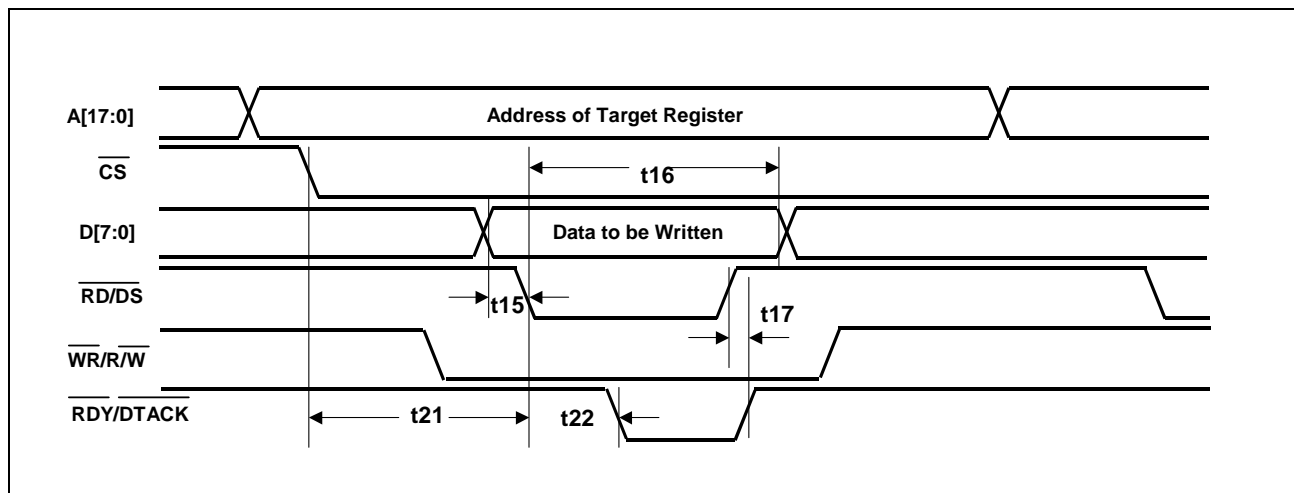
Note: The values for t15 through t22 can be found in **Table 17**.

Table 17   **Motorola (68K) Asynchronous Mode Timing Information - Write Operation**

Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t15	Data setup time to $\overline{DS}$ "Low"	25	-	-	ns
t16	Data hold time to $\overline{DS}$ "Low"	150	-	-	ns
t17	$\overline{DS}$ "High" to $\overline{DTACK}$ "High"	-	-	9	ns
t21	$\overline{CS}$ "Low" to $\overline{DS}$ set-up time	50	-	-	ns

Table 17   Motorola (68K) Asynchronous Mode Timing Information - Write Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified						
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t22	$\overline{DS}$ "Low" to $\overline{DTACK}$ "Low" delay time	130	-	-	ns

6.2.1   Motorola-Asynchronous Mode Timing - Read Operation

FIGURE 58. MOTOROLA-ASYNCHRONOUS MODE TIMING - READ OPERATION
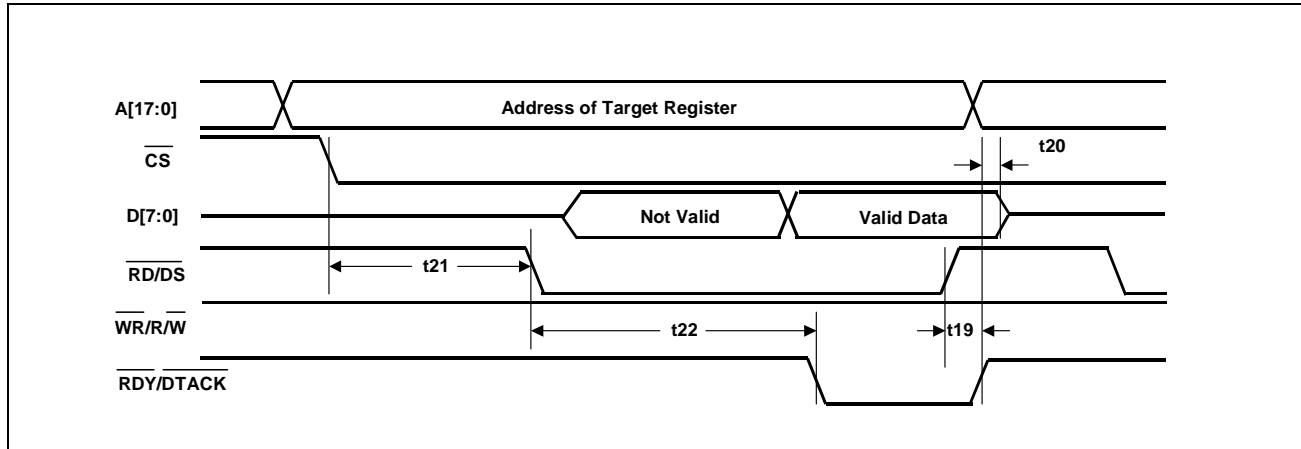
Note: The values for t13 through t24 can be found in **Table 17***.*

Table 18   Motorola (68K) Asynchronous Mode Timing - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified						
Timing	**Description**	**Min.**	**Typ.**	**Max**	**Units**
t19	$\overline{DS}$ "High" to $\overline{DTACK}$ "High"	-	-	8	ns
t20	$\overline{DTACK}$ "High" to Data invalid	-	-	8	ns
t21	$\overline{CS}$ "Low" to $\overline{DS}$ set-up time	50	-	-	ns
t22	$\overline{DS}$ "Low" to $\overline{DTACK}$ "Low" delay time	120	-	-	ns

6.3   PowerPC 403 Synchronous Mode:

In PowerPC mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{WE}$, $\overline{DBEN}$, $\overline{RDY}$ and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 66 MHz.

A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

Following falling edge of $\overline{CS}$, $\overline{DBEN}$ is asserted for the READ operation. $\overline{DBEN}$ must remain asserted until RDY is asserted by the XRT86SH328 device, which indicates DATA from the addressed location is available on the data bus. $\overline{DBEN}$ and $\overline{CS}$ can be de-asserted when the data has been read by the processor. $\overline{WE}$ should be high during the entire read cycle.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of RDY is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{WE}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WE}$ is asserted. $\overline{WE}$ should remain asserted until RDY is asserted by the XRT86SH328 device. Following RDY assertion $\overline{WE}$ and $\overline{CS}$ may be de-asserted. $\overline{DBEN}$ should be high during the entire write cycle.

FIGURE 59. POWERPC 403 MODE TIMING - WRITE OPERATION
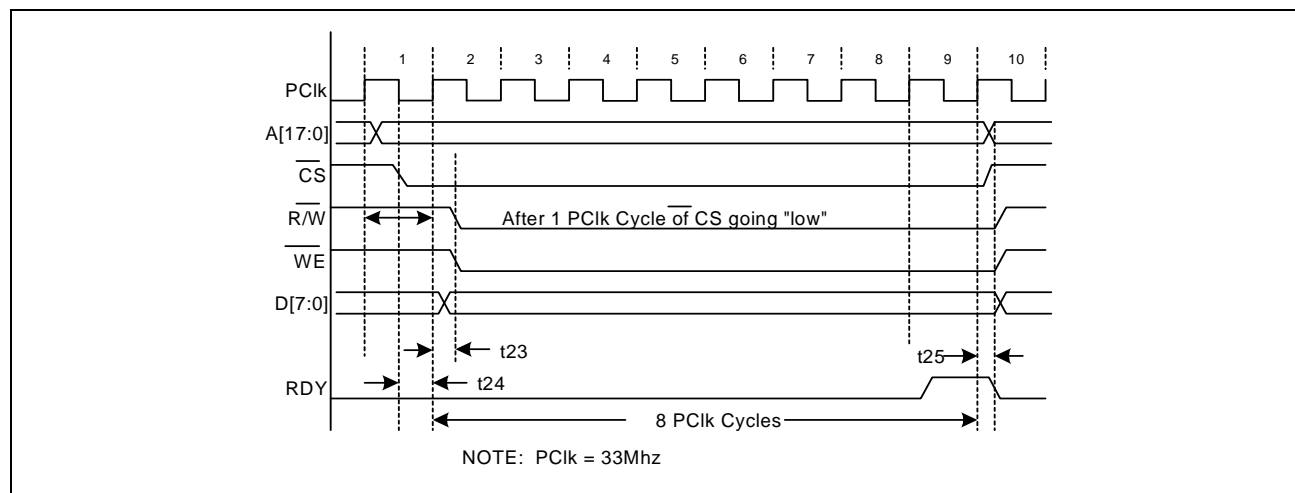
Note: The value for t25 through t38 can be found in **Table 19**.

Table 19   Power PC403 Mode Timing - Write Operation

Timing	Description	Min.	Typ.	Max.	Units
Test Conditions: TA = 25°C, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
t23	R/$\overline{W}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "Low" delay	4	-	-	ns

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FIGURE 60. POWERPC 403 MODE TIMING - READ OPERATION

Note: The value for t25 through t38 can be found in **Table 20***.*

Table 20   Power PC403 Mode Timing - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "Low" delay	4	-	-	ns
t27	R/$\overline{W}$ "High" to rising edge of PCLK set-up time	5	-	-	ns

6.4 MICROPROCESSOR INTERFACE TIMING - MCP860 SYNCHRONOUS MODE

In MPC86x mode the active signals are ADDR[17:0], DATA[7:0], $\overline{CS}$, $\overline{RW}$, $\overline{WE}$, $\overline{DBEN}$, $\overline{TA}$ and PCLK. In this mode all input signals are sampled by the PCLK. For all inputs minimum setup time is 4ns and minimum hold time is 3ns. Maximum PCLK frequency is 66 MHz.

A READ cycle starts with $\overline{RW}$ being 'HIGH' and assertion of $\overline{CS}$, address is assumed to be stable at this time since $\overline{CS}$ is usually derived from the decoding the address bus.

Following falling edge of $\overline{CS}$, $\overline{DBEN}$ is asserted for the READ operation. $\overline{DBEN}$ must remain asserted until $\overline{TA}$ is asserted by the XRT86SH328 device, which indicates DATA from the addressed location is available on the data bus. DBEN and $\overline{CS}$ can be de-asserted when the data has been read by the processor. $\overline{WE}$ should be high during the entire read cycle.

Operation with wait-states is also possible, provided the wait is longer than the minimum cycle time. Use of $\overline{TA}$ is recommended for timing efficiency since the read cycle time can vary depending on the internal address location being accessed.

WRITE operation is identical to read operation except that the cycle starts with $\overline{RW}$ being 'LOW', followed by $\overline{CS}$ assertion further followed by assertion of $\overline{WE}$. Data to be written at the addressed location should be valid on the data bus at the time $\overline{WE}$ is asserted. $\overline{WE}$ should remain asserted until $\overline{TA}$ is asserted by the XRT86SH328 device. Following assertion of $\overline{TA}$ $\overline{WE}$ and $\overline{CS}$ may be de-asserted. DBEN should be high during the entire write cycle.

FIGURE 61. MPC86X MODE TIMING - WRITE OPERATION

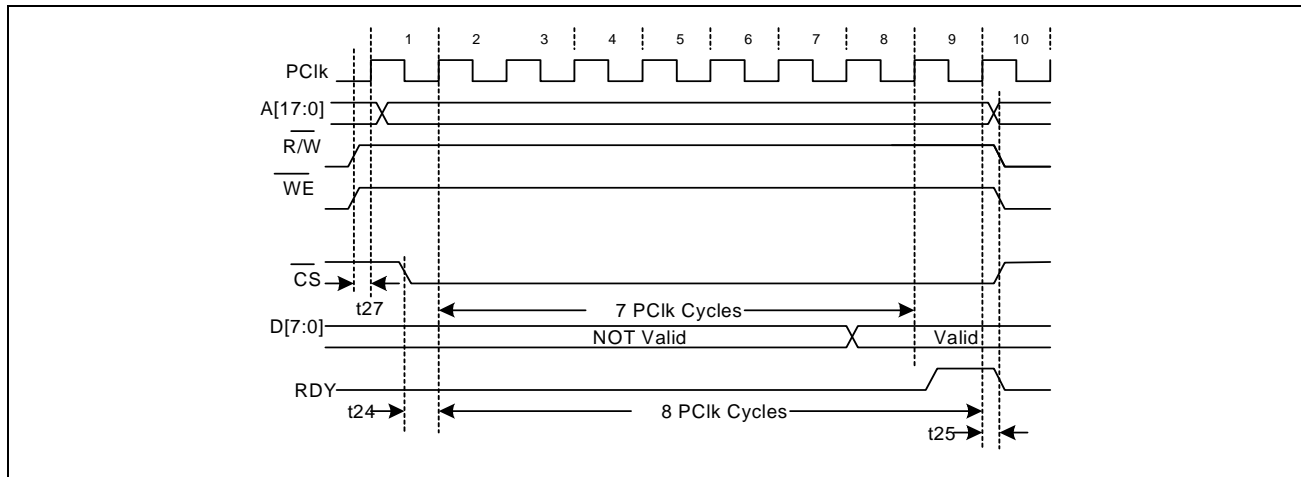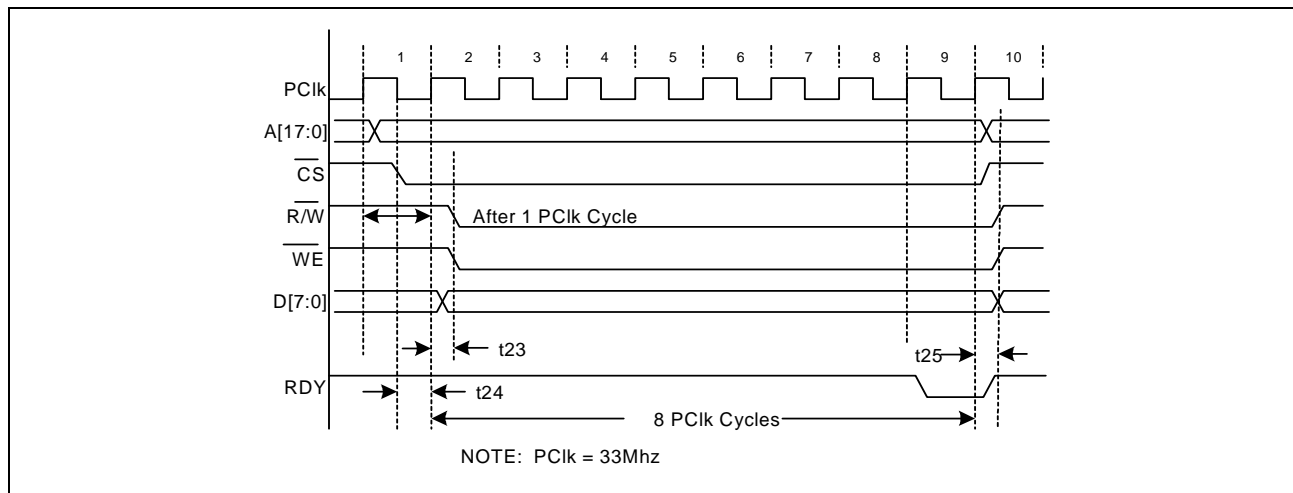**Table 21   MPC86X Mode Timing - Write Operation**

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	**Description**	**Min.**	**Typ.**	**Max.**	**Units**
t23	R/$\overline{W}$ "Low" to rising edge of PCLK set-up time (Write Operation)	5	-	-	ns
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	4	-	-	ns
t25	Rising edge of PCLK to RDY "High"delay	4	-	-	ns

FIGURE 62. MPC86X MODE TIMING - READ OPERATION
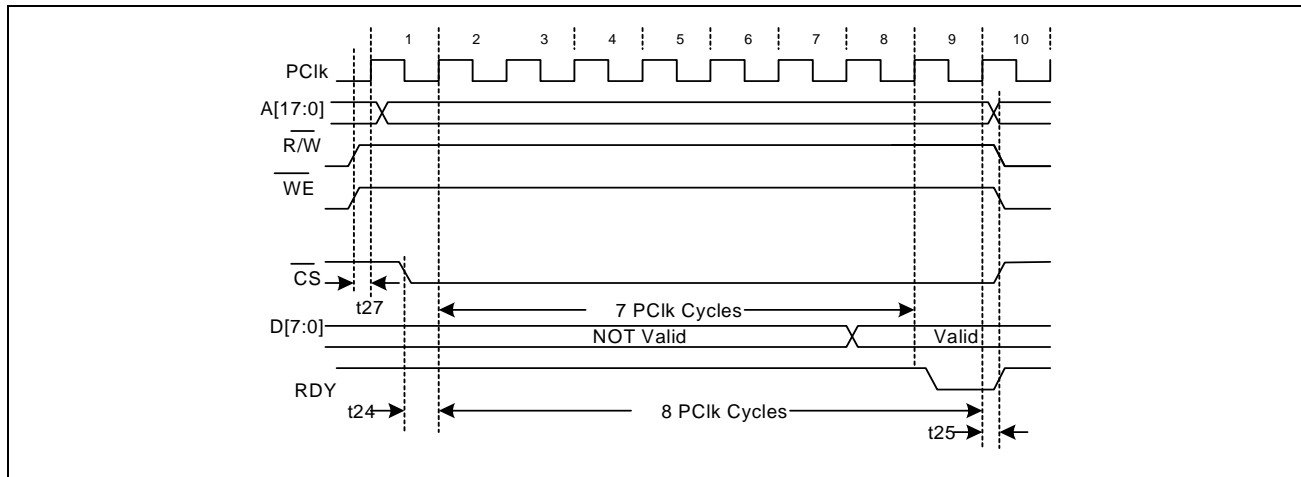
Table 22   MPC86X Timing Information - Read Operation

Test Conditions: TA = 25℃, VCC = 3.3V±5% and 1.8V ±5%, unless otherwise specified					
Timing	Description	Min.	Typ.	Max.	Units
t24	$\overline{CS}$ "Low" to rising edge of PCLK set-up time	5	-	-	ns
t25	Rising edge of PCLK to RDY "High" delay	4	-	-	ns
t27	R/$\overline{W}$ "High" to rising edge of PCLK set-up time	5	-	-	ns

7.0 INTERFACE TIMING SPECIFICATIONS

7.1 STS1/STS3 TELECOM BUS INTERFACE TIMING INFORMATION

This Section presents the timing requirements of the STS1/STS3 Telecom Bus Interface, for the following conditions/modes.

• Whenever the STS1/STS3 Telecom Bus Interface has been configured to operate in the STS1 Mode.

• Whenever the STS1/STS3 Telecom Bus Interface has been configured to operate in the STS3 Slot Master Mode

• Whenever the STS1/STS3 Telecom Bus Interface has been configured to operate in the STS3 Slot Slave Mode

This section presents the timing requirements for the STS1/STS3 Telecom Bus Interface. In particular this section indicates the following.

   a) Identifies which edge of TxA_CLK in which the TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP, TxA_ALARM and TxA_DP output pins are updated on.

   b) The clock to output delays (from the rising edge of TxA_CLK to the instant that the TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP, TxA_ALARM and TxA_DP output pins are updated.

   c) Identifies which edge of RxD_CLK that the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input pins are sampled on.

   d) The set-up time requirements (from an update in the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input signals to the rising edge of RxD_CLK).

   e) The hold-time requirements (from the rising edge of RxD_CLK to a change in the RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP input signals)

7.2 The Transmit STS1/STS3 Telecom Bus Interface Timing - STS1 Applications

Whenever the Transmit STS1/STS3 Telecom Bus Interface has been configured to operate in the STS1 Mode, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (6.48MHz clock signal).

FIGURE 63. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STS1/STS3 TELECOM BUS INTERFACE (FOR STS1 APPLICATIONS)
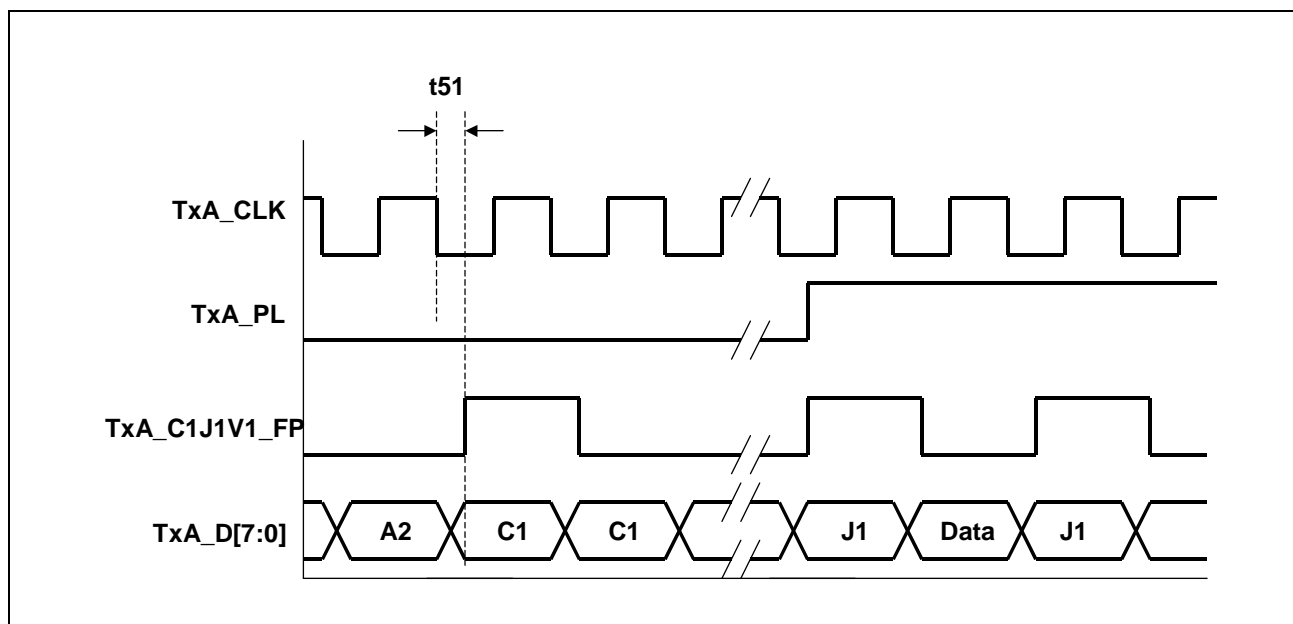
Note: The value for t51 can be found in **Table 23**.

Table 23   Timing Information for the Transmit STS1 Telecom Bus Interface - STS1 Applications

Symbol	Description	Min.	Typ.	Max.
t51	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	2.0ns		3.1ns

7.3   The Transmit STS1/STS3 Telecom Bus Interface Timing - STS3 Slot Master Applications

Whenever the Transmit STS1/STS3 Telecom Bus Interface has been configured to operate in both the STS3 and the Slot Master Mode, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (19.44MHz clock signal).

FIGURE 64. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STS1/ STS3 TELECOM BUS INTERFACE (FOR STS3 APPLICATIONS)
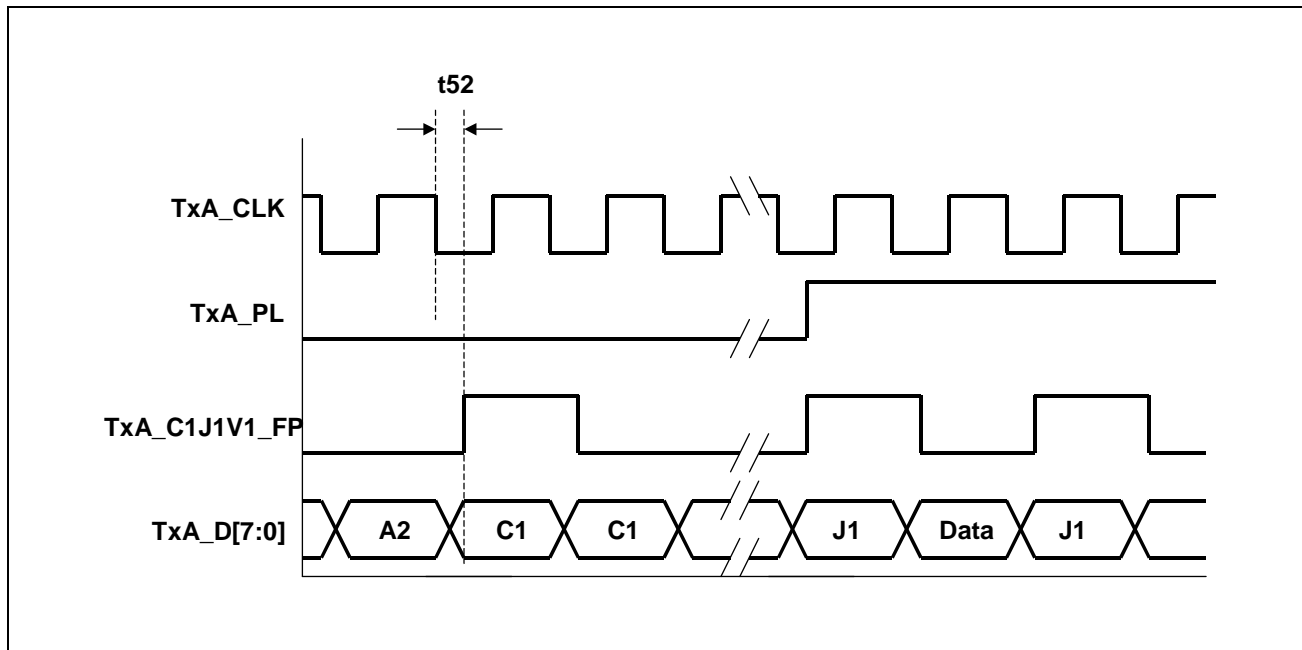
If the XRT86SH328 is configured to operate as the Slot Master, then it will pulse the TxSBFP_IN_OUT output pin "High" coincident to the instant that the chip outputs the very first byte of a given STS3 frame. The XRT86SH328 will update the TxSBFP_IN_OUT output pin upon the falling edge of TxA_CLK.

FIGURE 65. AN ILLUSTRATION OF THE TIMING RELATIONSHIPS BETWEEN THE TxSBFP_IN_OUT OUTPUT PIN, AND THE TxA_CLK OUTPUT PIN, WITHIN THE TRANSMIT STS3 TELECOM BUS INTERFACE (SLOT MASTER MODE APPLICATION)

Table 24   Timing Information for the Transmit STS1/STS3 Telecom Bus Interface - STS3 Slot Master Applications

Symbol	Description	Min.	Typ.	Max.
t52	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	2.0ns		4.0ns
t53	Falling edge of TxA_CLK to update in the TxSBFP_IN_OUT signal	0.1		0.3

7.4   The Transmit STS1/STS3 Telecom Bus Interface Timing - STS3 Slot Slave Applications

Whenever the Transmit STS1/STS3 Telecom Bus Interface has been configured to operate in the STS3, then all of the signals (which are output via this Bus Interface) are updated upon the falling edge of TxA_CLK (19.44MHz clock signal).

FIGURE 66. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE OUTPUT VIA THE TRANSMIT STS1/ STS3 TELECOM BUS INTERFACE (FOR STS3 APPLICATIONS)
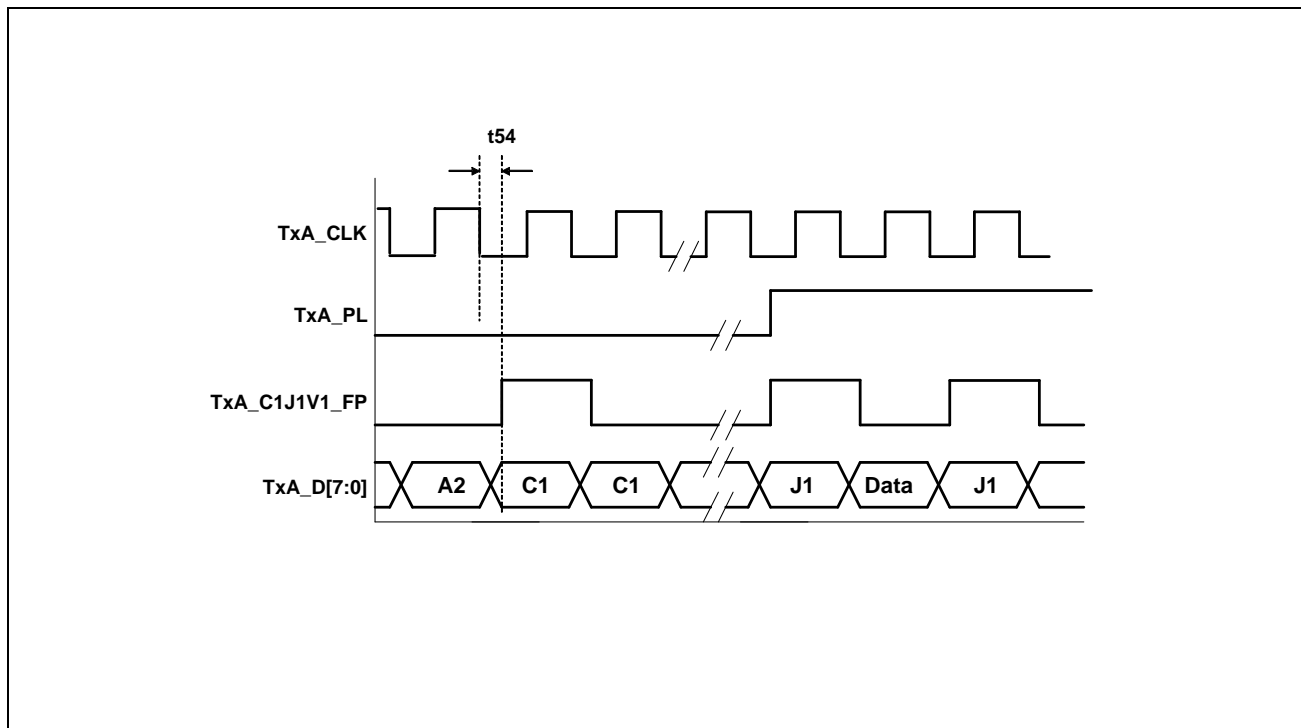
If the XRT86SH328 is configured to operate as the Slot Slave, then it will sample the TxSBFP_IN_OUT signal via an internal clock. The timing relationship between the TxSBFP_IN_OUT signal and the other Transmit STS1/STS3 Telecom Bus Interface signals is presented below in **Figure 67**.

FIGURE 67. AN ILLUSTRATION OF THE TIMING RELATIONSHIPS BETWEEN THE TXSBFP INPUT PIN AND THE TXA_CLK OUTPUT PIN WITHIN THE TRANSMIT STS1/STS3 TELECOM BUS INTERFACE (STS3 SLOT SLAVE APPLICATIONS)
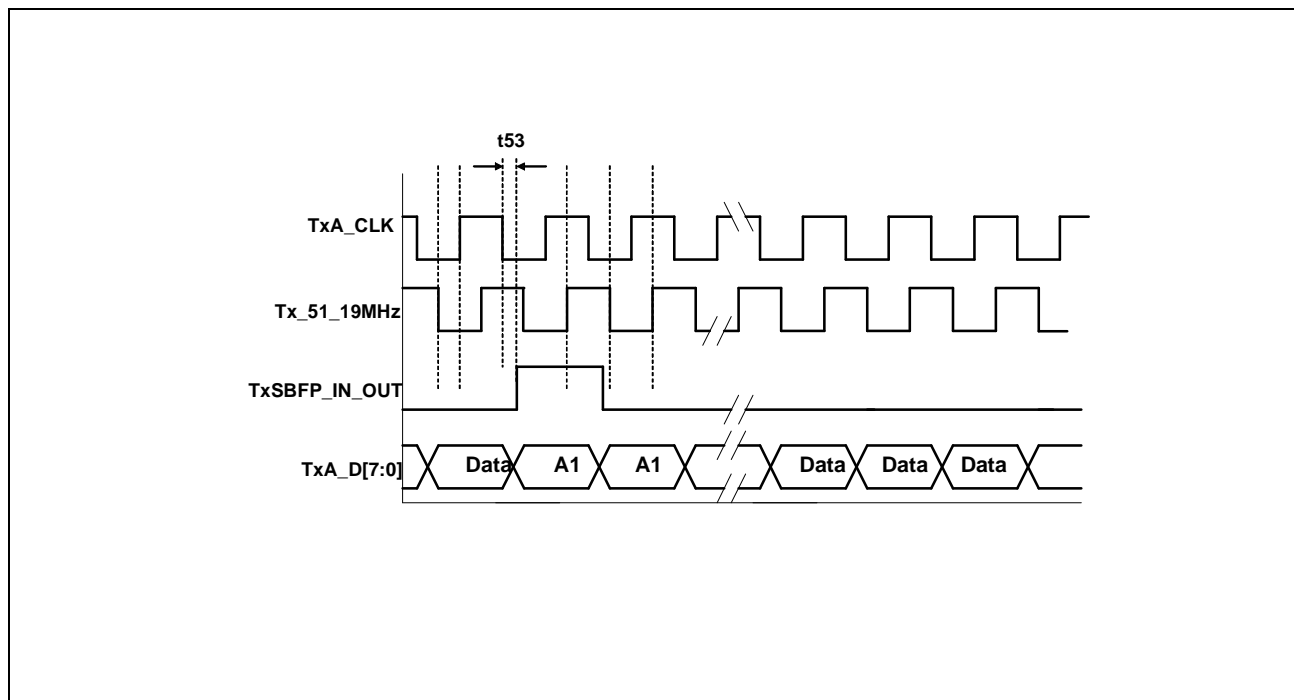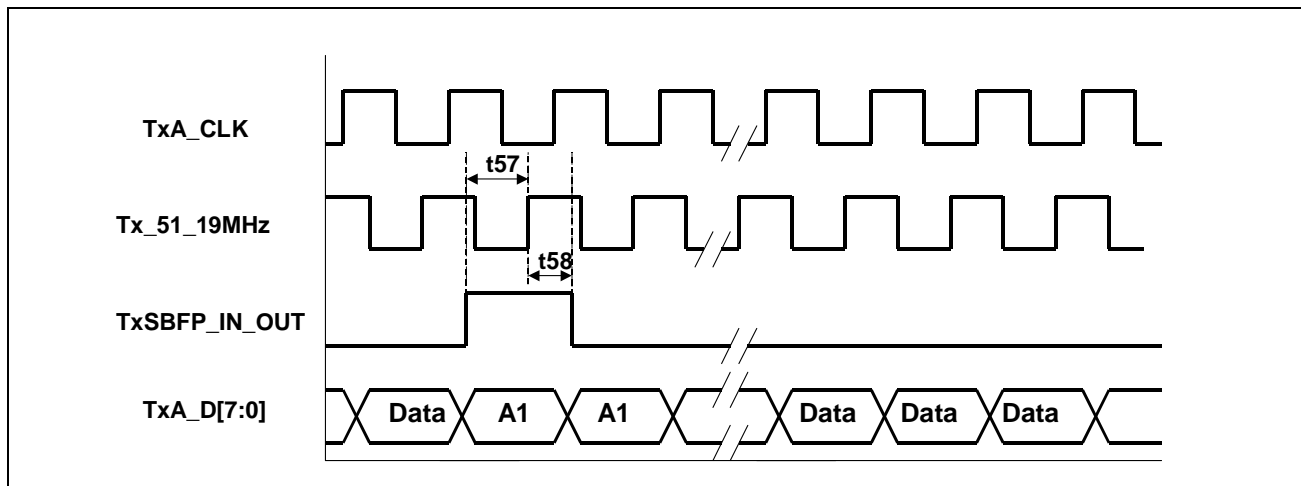
Table 25   Timing Information for the Transmit STS1/STS3 Telecom Bus Interface - STS3 Slot Slave Applications

Symbol	Description	Min.	Typ.	Max.
t54	Falling edge of TxA_CLK to updates in TxA_D[7:0], TxA_PL, TxA_C1J1V1_FP and TxA_DP	1.1ns		2.5ns
t57	TxSBFP Set-up time to rising edge of Tx51_19MHz	6ns		
t58	Rising edge of Tx51_19MHz to TxSBFP_IN_OUT Hold Time	1ns		

Note: In Slave mode, TxSBFP_IN_OUT is input to XRT86SH328. Inputs are applied using input clock Tx_51_19MHz and are sampled on rising edge of Tx_51_19MHz internally. The t57 parameter is referenced to the rising edge of Tx_51_19MHz, which provides the minimum setup and hold time required for TxSBFP_IN_OUT. TxA_CLK should be used to sampe the output signals not the input signals.

7.5   The Receive STS1/STS3 Telecom Bus Interface Timing - STS1 Applications

Whenever the Receive STS1/STS3 Telecom Bus Interface has been configured to operate in the STS1 Mode, then all of the signals (which are accepted via this Bus Interface) are sampled upon the rising edge of RxD_CLK (6.48MHz clock signal).

FIGURE 68. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STS1/STS3 TELECOM BUS INTERFACE
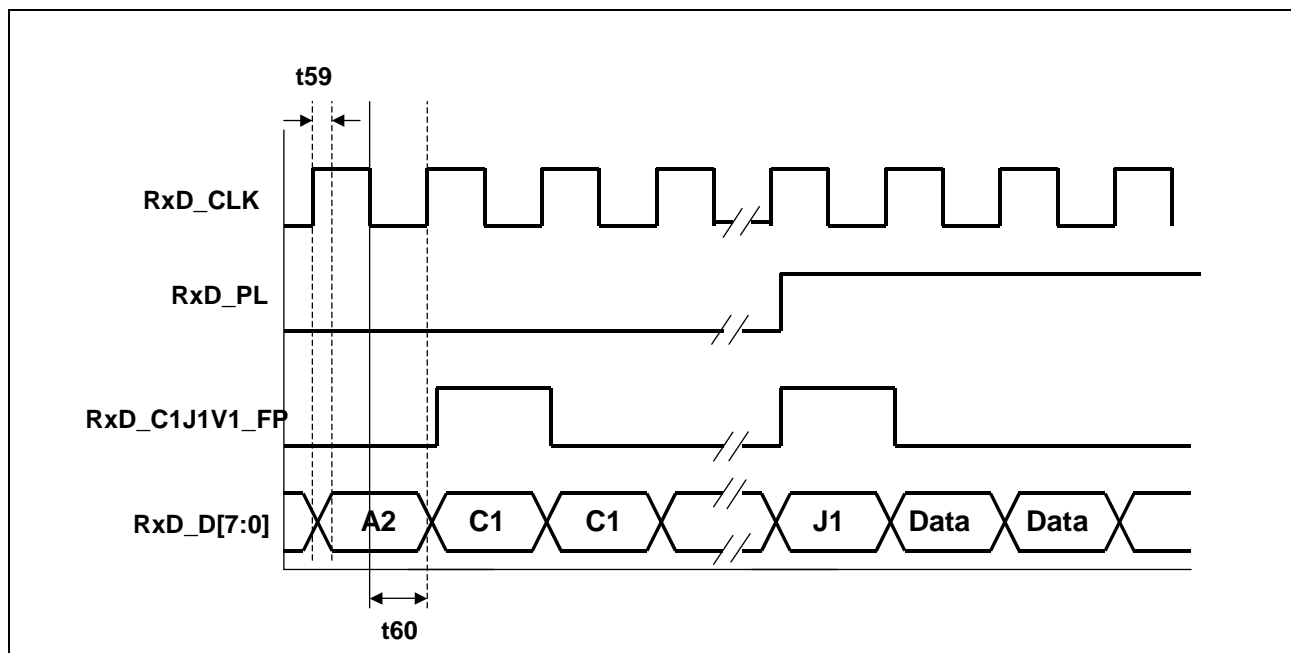
Note: The value for t59 and t60 can be found in Table 26. The data and control signals are applied on the falling edge of RxD_CLK. The XRT86SH328 samples the data and control signals on the rising edge of RxD_CLK.

Table 26   Timing Information for the Receive STS1/STS3 Telecom Bus Interface - STS1 Applications

Symbol	Description	Min.	Typ.	Max.
t59	RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP to rising edge of RxD_CLK set-up time requirements	6 ns		

Table 26   Timing Information for the Receive STS1/STS3 Telecom Bus Interface - STS1 Applications

Symbol	Description	Min.	Typ.	Max.
t60	rising edge of RxD_CLK to RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP hold time requirements	2 ns		

7.6   The Receive STS1/STS3 Telecom Bus Interface Timing - STS3 Applications

Whenever the Receive STS1/STS3 Telecom Bus Interface has been configured to operate in the STS3 Mode, then all of the signals (which are accepted via this Bus Interface) are sampled upon the rising edge of RxD_CLK (19.44MHz clock signal).

FIGURE 69. AN ILLUSTRATION OF THE WAVEFORMS OF THE SIGNALS THAT ARE INPUT VIA THE RECEIVE STS1/ STS3 TELECOM BUS INTERFACE
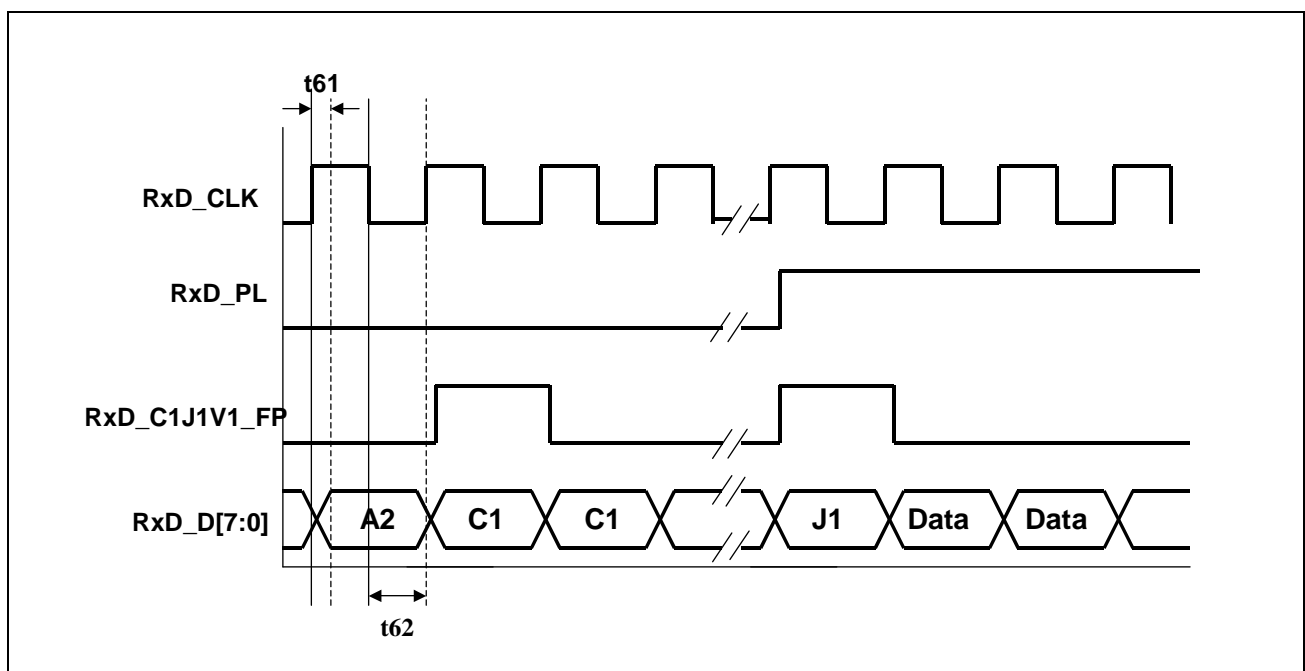
Note: The value for t61 and t62 can be found in **Table 27**.

Table 27   Timing Information for the Receive STS1/STS3 Telecom Bus Interface - STS3 Applications

Symbol	Description	Min.	Typ.	Max.
t61	RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP to rising edge of RxD_CLK set-up time requirements	6 ns		
t62	Rising edge of RxD_CLK to RxD_D[7:0], RxD_PL, RxD_C1J1V1_FP, RxD_ALARM and RxD_DP hold time requirements	2 ns		

7.7 STS1 LIU INTERFACE TIMING INFORMATION

In addition to the Telecom Bus, the XRT86SH328 can be configured for High-Speed STS1 LIU Interface Ports.

7.7.1 Receive STS1 LIU Interface Timing

FIGURE 70. AN ILLUSTRATION OF THE WAVEFORMS OF THE RECEIVE STS1 SIGNALS THAT ARE INPUT TO THE RECEIVE STS1 LIU INTERFACE BLOCK - SHARED PORT
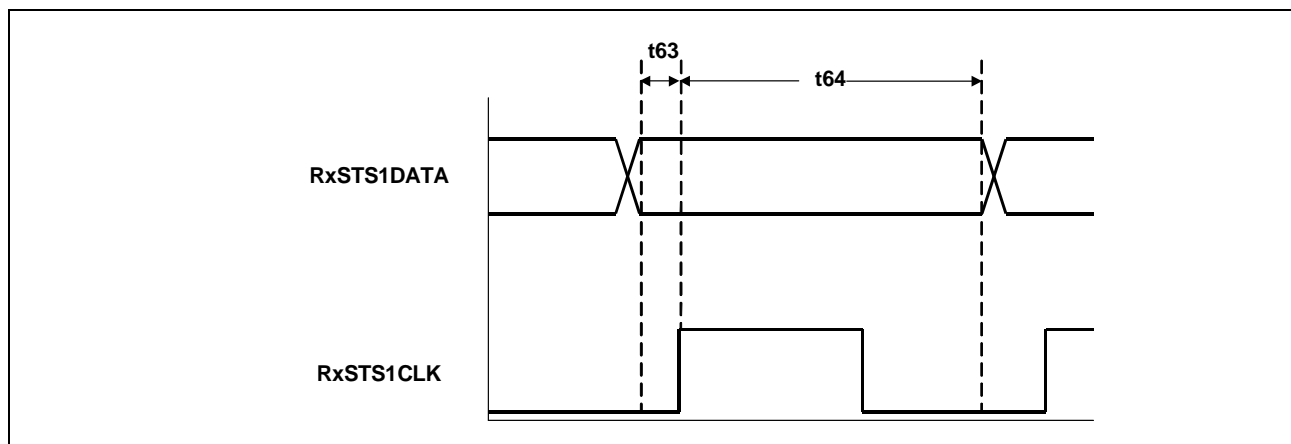
Note: The values for t63 and t64 are presented in **Table 28***.*

Table 28   Timing Information for the Receive STS1 LIU Interface when the Receive STS1 TOH Processor block has been configured to sample the RxSTS1DATA signal upon the rising edge of the RxSTS1CLK signal

Symbol	Description	Min.	Typ.	Max.
t63	RxSTS1DATA to rising edge of RxSTS1CLK set-up time requirements	5ns		
t64	Rising edge of RxSTS1CLK to RxSTS1DATA Hold time requirements	0ns		

7.7.2　Transmit STS1 LIU Interface Timing

FIGURE 71. AN ILLUSTRATION OF THE WAVEFORMS OF THE STS1 SIGNALS THAT ARE OUTPUT FROM THE TRANSMIT STS1 LIU INTERFACE - DEDICATED PORT
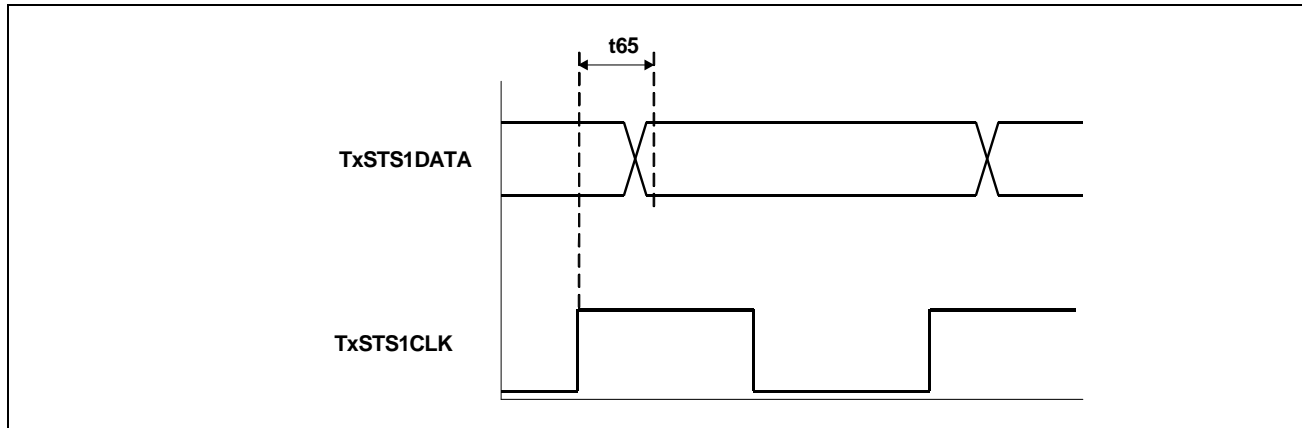
Note: The value for t65 is presented in **Table 29** *.*

Table 29　Timing Information for the Transmit STS1 LIU Interface when the Transmit STS1 TOH Processor block has been configured to update the TxSTS1DATA signal upon the rising edge of the TxSTS1CLK signal

Symbol	Description	Min.	Typ.	Max.
t65	Rising edge of TxSTS1CLK to TxSTS1DATA output delay	2.0ns		5.0ns

7.8   TRANSMIT STS1/STS3 TOH and POH DATA INPUT PORT

The Transmit STS1/STS3 TOH and POH Data Input Port is used to insert a value for the TOH and POH bytes into the outbound STS1/STS3 data-stream.

Note: The TxOHIns and the TxOH input pins are sampled (by the Transmit STS1/STS3 TOH and POH Overhead Input Port) upon the rising edge of TxOHClk. All of the remaining signals (e.g., TxOHFrame and TxOHEnable) are updated upon the falling edge of TxOHClk.

FIGURE 72. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT STS1/STS3 TOH AND POH OVERHEAD DATA INPUT PORT
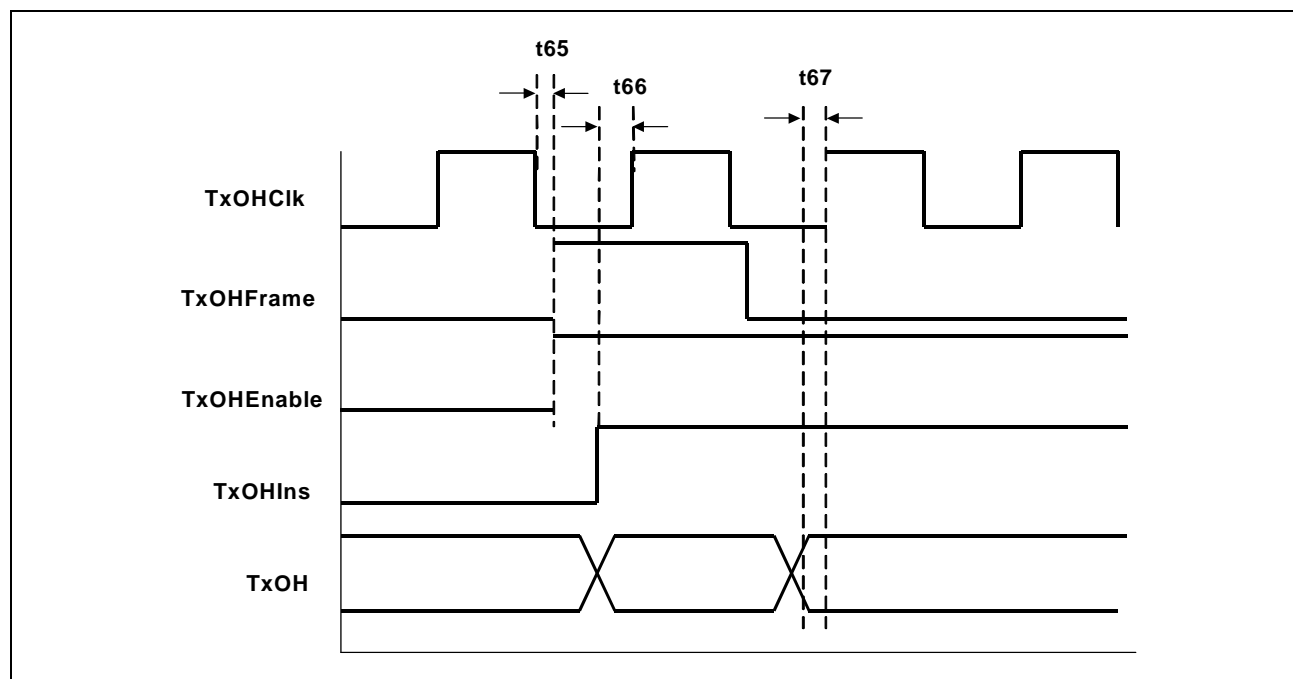
Note: The values for t65, t66 and t67 can be found in **Table 30**.

Table 30   Timing Information for the Transmit STS1/STS3 TOH and POH Overhead Data Input Port

Symbol	Description	Min.	Typ.	Max.
t65	Falling edge of TxOHClk to rising edge of TxOHFrame, TxOHEnable and TxPOHInd output delay	-3.0ns		-2.0ns
t66	TxOHIns to rising edge of TxOHClk set-up time	6.0ns		
t67	TxOH Data to rising edge of TxOHClk set-up time	6.0ns		
F1	TxOHClk Frequency	3.08MHz		

Note: The XRT86SH328 uses faster SYSCLK (49MHz) and enable at STS1 byte rate (6.48MHz) to generate all the outputs including TxOHClk, TxOHEnable and TxOHFrame. This can make t65 have negative min and max times.The rising of TxOHClk should be used to sample TxOHEnable and TxOHFrame which provides enough setup and hold times.

7.9   TRANSMIT VC-4 POH DATA INPUT PORT

The Transmit VC-4 POH Data Input Port is used to insert a value for the VC-4 POH bytes into the outbound VC-4 data-stream (which is output) via the Transmit STM-1 Telecom Bus.

Note: The TxTUPOHIns and the TxTUPOH input pins are sampled (by the Transmit VC-4 POH Data Input Port) upon the rising edge of TxTUPOHClk. All of the remaining signals (e.g., TxTUPOHFrame and TxTUPOHEnable) are updated upon the falling edge of TxTUPOHClk.

FIGURE 73. ILLUSTRATION OF TIMING WAVE-FORM OF THE TRANSMIT VC-4 POH DATA INPUT PORT
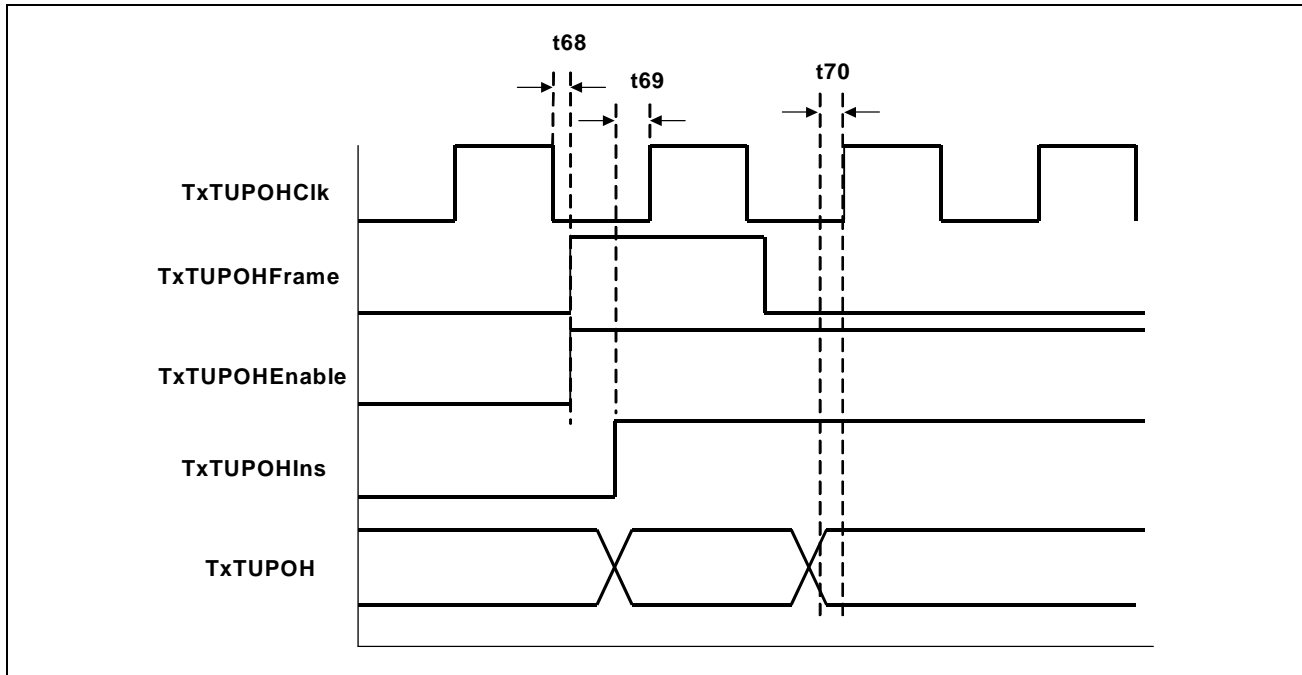
Note: The values for t68, t69 and t70 can be found in **Table 31**.

Table 31   Timing Information for the Transmit VC-4 POH Data Input Port

Symbol	Description	Min.	Typ.	Max.
t68	Falling edge of TxTUPOHClk to rising edge of TxTUPOHFrame and TxTUPOHValid output delay	-0.5ns		0.5ns
t69	TxTUPOHIns to rising edge of TxTUPOHClk set-up time	6ns		
t70	TxTUPOH Data to rising edge of TxTUPOHClk set-up time	6ns		

7.10   *Receive STS1/STS3 TOH and POH Data Output Port*

The Receive STS1/STS3 TOH and POH Data Output port is used to extract out the values of the TOH and POH bytes within the incoming STS1/STS3 data-stream. All of the Receive TOH and POH Data Output port signals are updated upon the falling edge of RxOHClk.

FIGURE 74. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE STS1/STS3 TOH AND POH DATA OUT-PUT PORT
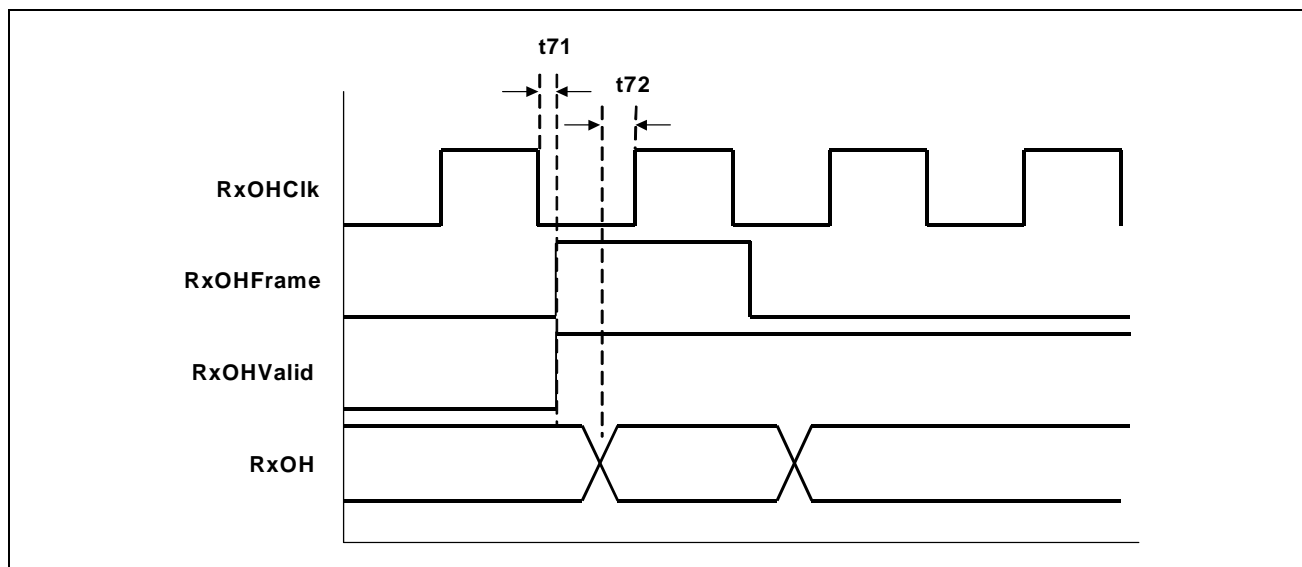
Note: The values for t71 and t72 can be found in **Table 32***.*

Table 32   Timing Information for the Receive STS1/STS3 TOH and POH Data Output Port

Symbol	Description	Min.	Typ.	Max.
t71	Falling edge of RxOHClk to rising edge of RxOHFrame, RxOHValid, and RxPOHInd	-0.2ns		0.2ns
t72	Falling edge of RxOHClk to RxOH output delay	-0.2ns		0.2ns

7.11   RECEIVE VC-4 POH DATA OUTPUT PORT

The Receive VC-4 POH Overhead Output port is used to extract out the values of the VC-4 POH bytes within the incoming STM-1 data-stream. All of the Receive VC-4 POH Overhead Output port signals are updated upon the falling edge of RxTUPOHClk. The timing wave-form and information for the Receive VC-4 POH Data Output Port is presented below.

FIGURE 75. ILLUSTRATION OF THE TIMING WAVE-FORM OF THE RECEIVE VC-4 POH DATA OUTPUT PORT
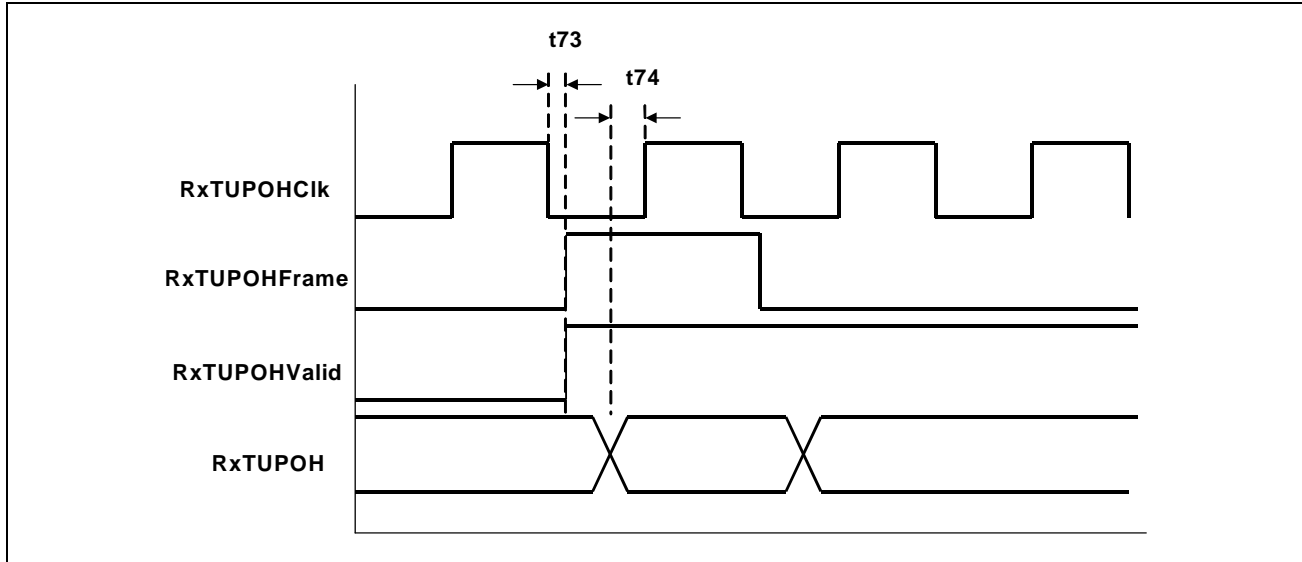
Note: The values for t73 and t74 can be found in **Table 33***.*

Table 33   Timing Information for the Receive VC-4 POH Data Output Port

Symbol	Description	Min.	Typ.	Max.
t73	Falling edge of RxTUPOHClk to rising edge of RxTUPOHFrame and RxTUPOHValid	-0.2ns		0.2ns
t74	Falling edge of RxTUPOHClk to RxTUPOH output delay	-0.2ns		0.2ns

7.12   INGRESS DIRECTION - ADD/DROP PORT TIMING

7.12.1   Ingress Direction - Add Port Timing

FIGURE 76.   ILLUSTRATION OF THE INGRESS-DIRECTION ADD PORT SIGNALS
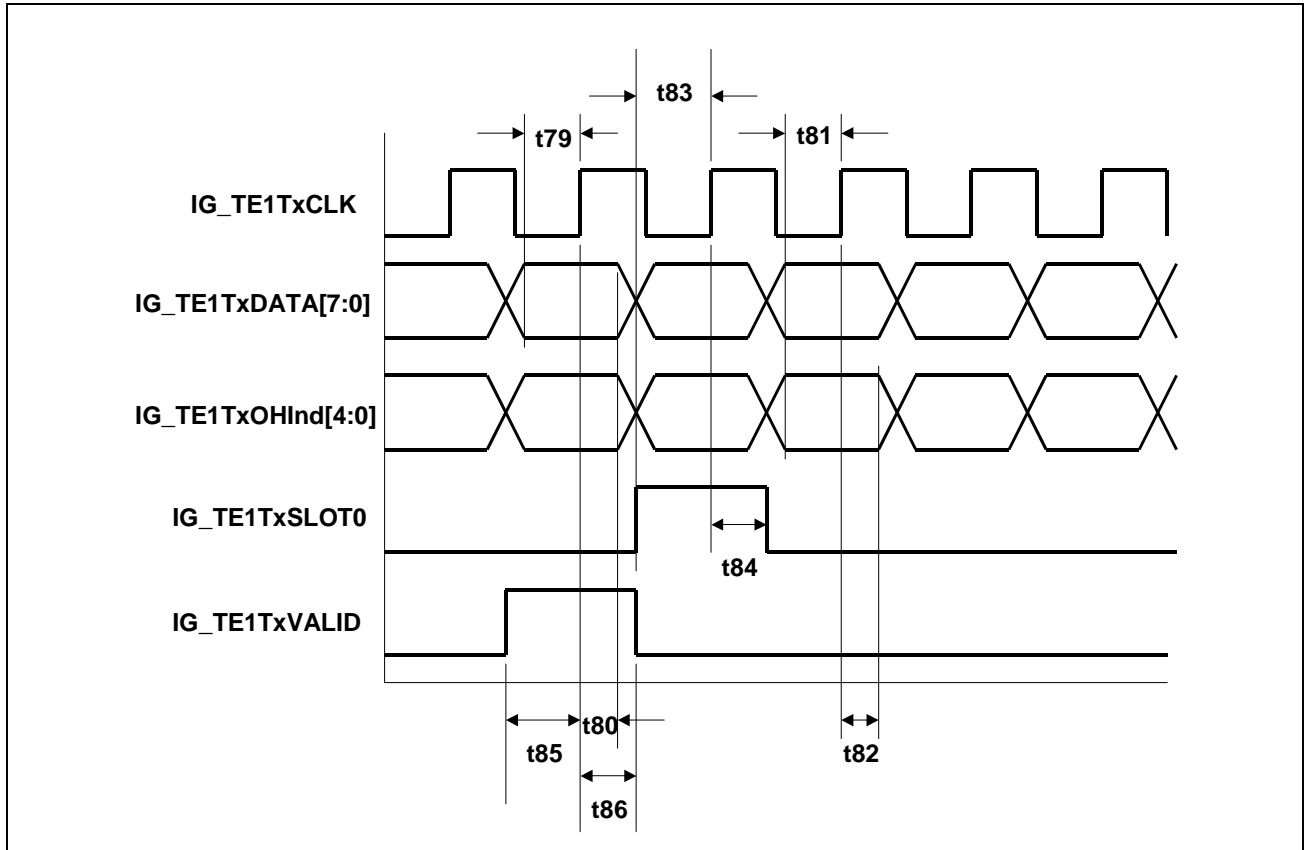
Table 34   Timing Information for the Ingress-Direction Add Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t79	IG_TE1TxDATA[7:0] to rising edge of IG_TE1TxCLK set-up time	4.5			ns
t80	Rising edge of IG_TE1TxCLK to IG_TE1TxDATA[7:0] hold time	3.0			ns
t81	IG_TE1TxOHInd[4:0] to rising edge of IG_TE1TxCLK set up time	4.5			ns
t82	Rising edge of IG_TE1TxCLK to IG_TE1TxOHInd[4:0] hold time	3.0			ns
t83	IG_TE1TxSLOT0 to rising edge of IG_TE1TxCLK set-up time	5.0			ns
t84	Rising edge of IG_TE1TxCLK to IG_TE1TxSLOT0 hold time	3.0			ns
t85	IG_TE1TxVALID to rising edge of IG_TE1TxCLK set-up time	5.0			ns
t86	Rising Edge of IG_TE1TxCLK to IG_TE1TxVALID hold time	3.0			ns

7.12.2   Ingress Direction - Drop Port Timing

FIGURE 77. ILLUSTRATION OF THE INGRESS-DIRECTION DROP PORT SIGNALS
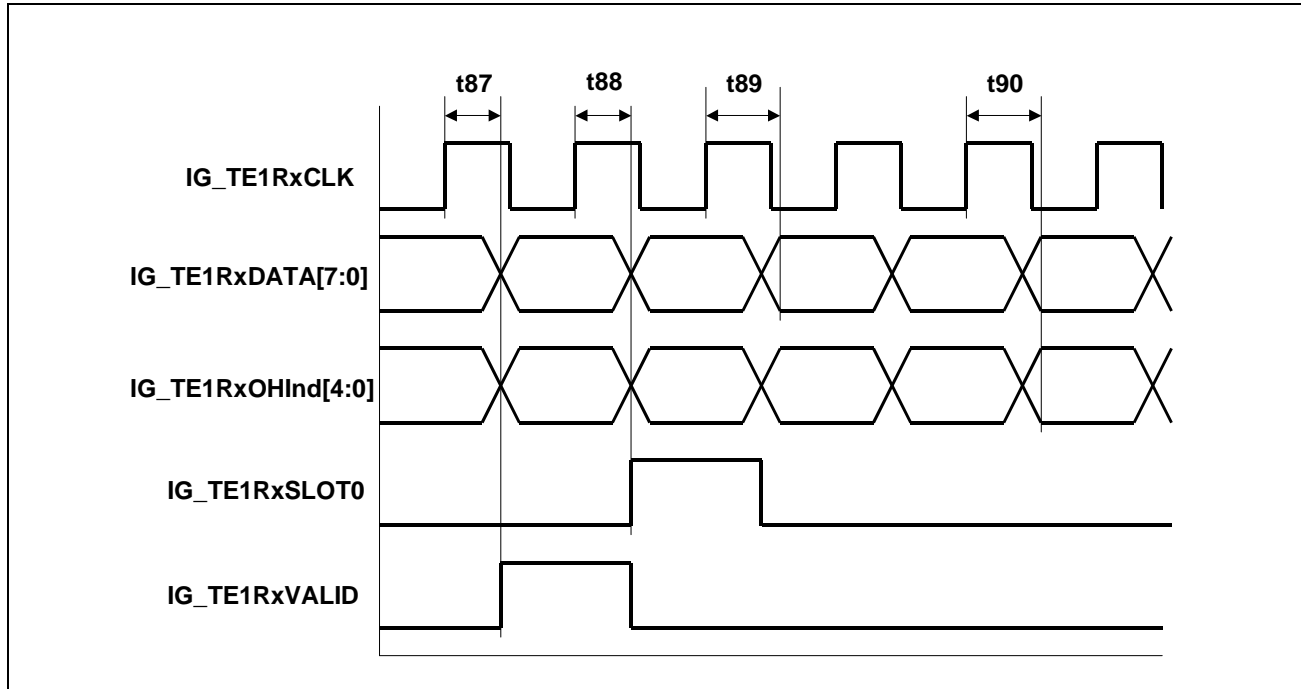
Table 35   Timing Information for the Ingress-Direction Drop Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t87	Falling Edge of IG_TE1RxCLK to IG_TE1RxVALID output delay	-0.2		3.0	ns
t88	Rising edge of IG_TE1RxCLK to IG_TE1RxDATA[7:0] hold time	6.0			ns
t89	IG_TE1RxOHInd[4:0] to rising edge of IG_TE1rxCLK set up time	4.5			ns
t90	Rising edge of IG_TE1RxCLK to IG_TE1RxOHInd[4:0] hold time	6.0			ns

7.13 EGRESS DIRECTION - ADD/DROP PORT TIMING

7.13.1 Egress Direction - Add Port Timing

FIGURE 78. ILLUSTRATION OF THE EGRESS-DIRECTION ADD PORT SIGNALS
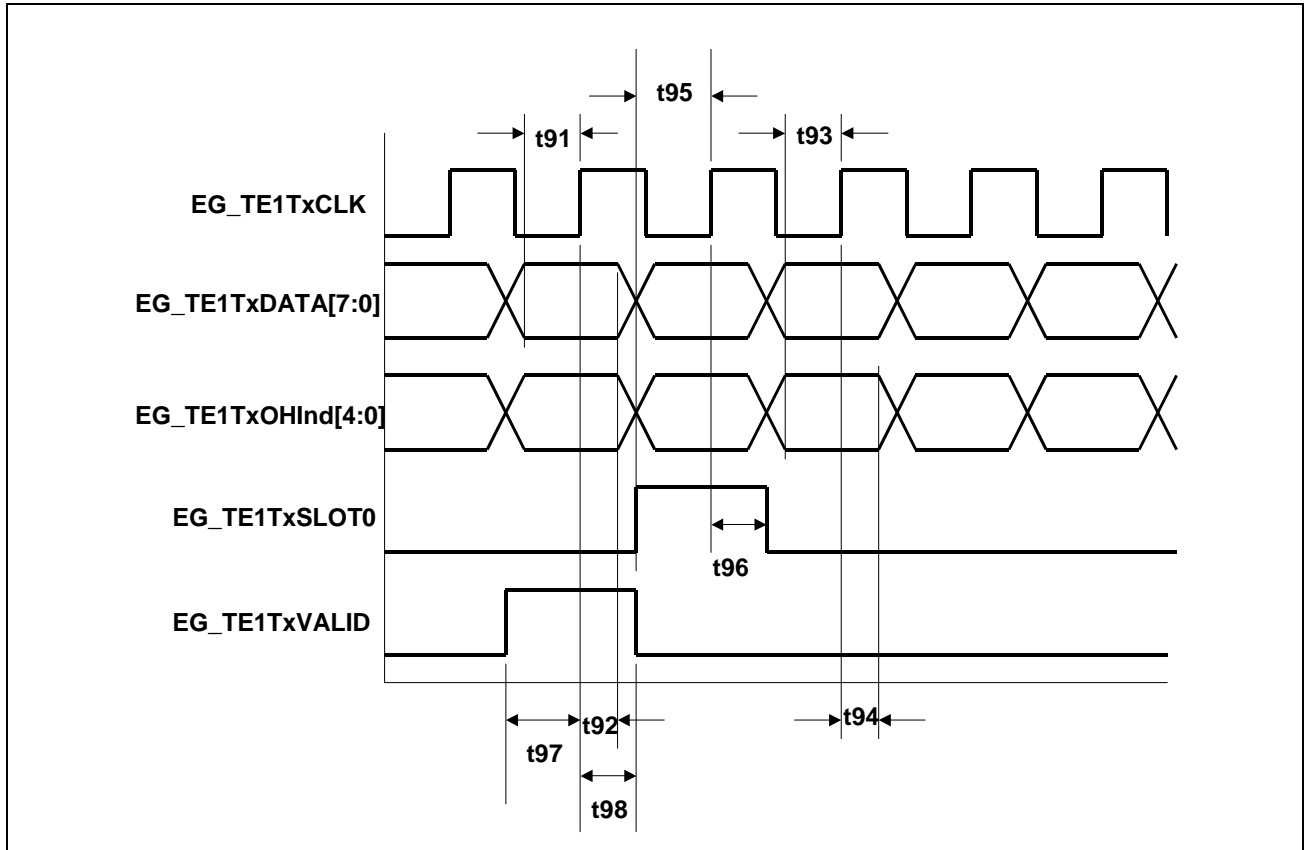
Table 36   Timing Information for the Egress-Direction Add Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t91	EG_TE1TxDATA[7:0] to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t92	Rising edge of EG_TE1TxCLK to EG_TE1TxDATA[7:0] hold time	2.0			ns
t93	EG_TE1TxOHInd[4:0] to rising edge of EG_TE1TxCLK set up time	7.0			ns
t94	Rising edge of EG_TE1TxCLK to EG_TE1TxOHInd[4:0] hold time	2.0			ns
t95	EG_TE1TxSLOT0 to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t96	Rising edge of EG_TE1TxCLK to EG_TE1TxSLOT0 hold time	2.0			ns
t97	EG_TE1TxVALID to rising edge of EG_TE1TxCLK set-up time	7.0			ns
t98	Rising Edge of EG_TE1TxCLK to EG_TE1TxVALID hold time	2.0			ns

7.13.2   Egress Direction - Drop Port Timing

F<small>IGURE</small> 79. I<small>LLUSTRATION OF THE</small> E<small>GRESS-</small>D<small>IRECTION</small> D<small>ROP</small> P<small>ORT</small> S<small>IGNALS</small>
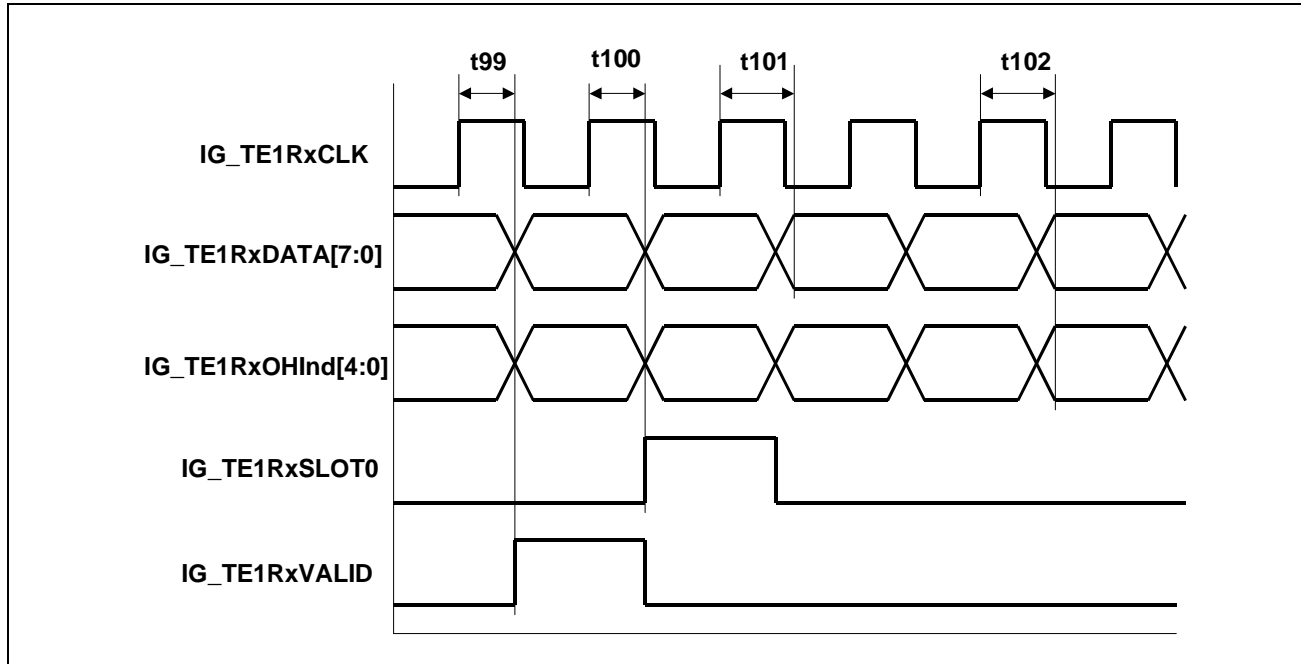
Table 37   Timing Information for the Egress-Direction Drop Port Signals

Timing Symbol	Description	Min	Typ	Max	Units
t99	Falling Edge of EG_TE1RxCLK to EG_TE1RxVALID output delay	-0.2		3.0	ns
t100	Rising edge of EG_TE1RxCLK to EG_TE1RxDATA[7:0] hold time	6.0			ns
t101	EG_TE1RxOHInd[4:0] to rising edge of EG_TE1RxCLK set up time	4.5			ns
t102	Rising edge of EG_TE1RxCLK to EG_TE1RxOHInd[4:0] hold time	6.0			ns

8.0 ELECTRICAL CHARACTERISTICS

TABLE 38: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	3.465	v	Note 1
V_{DD18}	Supply Voltage	-0.5	1.890	v	Note 1
V_{In}	Input Voltage	-0.5	5.5	V	Note 1
S_{TEMP}	Storage Temperature	-65	+150	°C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	+85	°C	Industrial Tem p Grade
$ThetaJA_0$	Thermal Resistance (without heatsink)		11.6	°C/W	0 lfpm airflow
$ThetaJA_{200}$	Thermal Resistance (without heatsink)		10.7	°C/W	200 lf pm airflow
$ThetaJA_{400}$	Thermal Resistance (without heatsink)		9.2	°C/W	400 lfp m airflow
$ThetaJA_{0H}$	Thermal Resistance (with ext fin-type heatsink)		9.5	°C/W	0 lfpm airflow
$ThetaJA_{100H}$	Thermal Resistance (with ext fin-type heatsink)		8.1	°C/W	100 lfpm airflow
$ThetaJA_{200H}$	Thermal Resistance (with ext fin-type heatsink)		7.5	°C/W	200 lfpm airflow
$ThetaJA_{400H}$	Thermal Resistance (with ext fin-type heatsink)		6.2	°C/W	400 lfpm airflow
$LFPM_{MIN}$	Minimum Airflow Required for Operation	--		lfpm	Maximum Ambient Operating Temperature Dependent
$JTEMP_{MAX}$	Maximum Junction Temperature		+125	°C	Note 1
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-8
ESD	ESD Rating - HBM		2000	v	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended periods may cause permanent failure and impair reliabilty of the device.*
2. *ESD testing method is per JESD22-A114.*

TABLE 39: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VDD$_{IO}$ = 3.3V $\pm$ 5% , VDD$_{CORE}$ = 1.8V $\pm$ 5%, T$_A$=25℃, unless otherwise specified					
Power Supply Voltage (3.3V)	VDD33	3.13	3.3	3.46	V
Power Supply Voltage (1.8V)	VDD18	1.71	1.8	1.89	V
Current Consumption (3.3V) PRBS pattern	IDD33$_{100\Omega-PRBS}$		980		mA
Current Consumption (1.8V) PRBS pattern	IDD18$_{100\Omega-PRBS}$		840		mA
Power Consumption (3.3V) - PRBS pattern	P33$_{100\Omega-PRBS}$		3.23		W
Power Consumption (1.8V) - PRBS pattern	P18$_{100\Omega-PRBS}$		1.52		W
Total Power Consumption- PRBS pattern	Ptotal$_{100\Omega-PRBS}$		4.75		W
Current Consumption (3.3V) all "ones" patt	IDD33$_{100\Omega-ONES}$		1330		mA
Current Consumption (1.8V) all "ones" patt	IDD18$_{100\Omega-ONES}$		840		mA
Power Consumption (3.3V) - all "ones" patt	P33$_{100\Omega-ONES}$		4.39		W
Power Consumption (1.8V) - all "ones" patt	P18$_{100\Omega-ONES}$		1.52		W
Total Power Consumption- all "ones" patt	Ptotal$_{100\Omega-ONES}$		5.91		W
Input High Voltage	V$_{IH}$	2.0	-	5.0	V
Input Low Voltage	V$_{IL}$	-0.5	-	0.8	V
Output High Voltage IOH=-2.0mA	V$_{OH}$	2.4	-		V
Output Low Voltage IOL=2.0mA	V$_{OL}$	-	-	0.4	V
Input Leakage Current	I$_L$	-	-	±10	µA
Input Capacitance	C$_I$	-	5.0		pF
Output Load Capacitance	C$_L$	-	-	25	pF

NOTES:

1. *Current and Power Consumption values are taken for 100Ω internal terminations and under load.*
2. *Input leakage current excludes pins that are internally pulled "Low" or "High".*

TABLE 40: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD$_{IO}$ = 3.3V $\pm$ 5% , VDD$_{CORE}$ = 1.8V $\pm$ 5%, T$_A$=-40°to 85°C, unless otherwise specified

PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Receiver loss of signal: Number of consecutive zeros before RLOS is set		175			
Input signal level at RLOS	15	20	-	dB	Cable attenuation @772kHz
RLOS Clear	12.5	-	-	% ones	ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss) Normal Extended	 0 0	- 	 36 45	 dB dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Input Impedance		15	-	kΩ	
Jitter Tolerance: 1Hz 10kHz - 100kHz	 138 0.4	 - -	 - -	UIpp	AT&T Pub 62411
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 - -	 10 	 - 0.1	 KHz dB	TR-TSY-000499
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		Hz	AT&T Pub 62411
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 - - -	 14 20 16	 - - -	 dB dB dB	

TABLE 41: E1 RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
VDD_{IO} = 3.3V ± 5% , VDD_{CORE} = 1.8V ± 5%, T_A=25℃, unless otherwise specified					
Receiver loss of signal:					
Number of consecutive zeros before LOS is set	-	32	-	bit	Cable attenuation @1024KHz ITU-G.775, ETS1 300 233
Input signal level at LOS	13	16	-	dB	
RLOS Clear	12.5	-	-	% ones	
Receiver Sensitivity Cable + Flat Loss	6+6	-	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application.
Interference Margin	-18	-14	-	dB	With 6dB cable loss
Input Impedance	15		-	KΩ	
Jitter Tolerance: 1 Hz 10KHz---100KHz	37 0.3	- -	- -	UIpp UIpp	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	-	20	36 0.5	KHz dB	ITU G.736
Jitter Attenuator Corner Frequency(-3dB curve) JABW=0 JSBW=1	- -	10 1.5	- -	Hz Hz	ITU G.736
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	12 18 14	- - -	- - -	dB dB dB	ITU G.703

TABLE 42: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
VDD$_{IO}$ = 3.3V ± 5% , VDD$_{CORE}$ = 1.8V ± 5%, T$_A$=-40°to 85°C, unless otherwise specified					
AMI Output Pulse Amplitude:	2.4	3.0	3.60	V	1:2 transformer measured at DSX-1.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	- - -	17 12 10	- - -	dB dB dB	

TABLE 43: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITION
VDD$_{IO}$ = 3.3V ± 5% , VDD$_{CORE}$ = 1.8V ± 5%, T$_A$=25°C, unless otherwise specified					
AMI Output Pulse Amplitude 75Ω 120Ω	2.13 2.70	2.37 3.00	2.60 3.30	V V	1:2 Transformer
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05		ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05		ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UI$_{p-p}$	Broad Band with jitter free TCLK applied to the input.
Output Return Loss 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	15 9 8	- - -	- - -	dB dB dB	ETSI 300 166

9.0 BACKGROUND AND PROTOCOLS

This section intends to provide a background coverage of the theory of communication protocols involved in Voyager development. Only brief descriptions of their formats, control flows, and application-specific features are presented here.

9.1 SYNCHRONOUS OPTICAL NETWORK (SONET) STANDARD

This section intends to provide a background coverage of the theory of communication protocols involved in SONET standard. Only brief descriptions of their rates, formats, control flows, and application-specific features are presented here.

Synchronous Optical Network (SONET): The SONET is a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks.

Synchronous Transport Signal (STS): An STS is the information structure used to support Transport layer connections in the SONET. It consists of the information payload along with the Path Overhead (POH) and Transport Overhead (SOH) information fields organized in a block frame structure which repeats every 125 μs. The information is suitably conditioned for serial transmission on the selected media at a rate which is synchronized to the network. A basic STS is defined at 51 840 kbit/s. This is termed STS1. Higher capacity STS-n are formed at rates equivalent to N times this basic rate. STS capacities for N=3, N=12, N=48 and N=192 are defined; higher values are under consideration.

The STS1 comprises a single SPE (Synchronous Payload Envelope) along with the Transport Overhead (TOH) Bytes. The STS-N, N = 1, is the smallest unit structure in the SONET transmission protocol.

STS-n Synchronous Payload Envelope (STS-n SPE): A Synchronous Payload Envelope is the information structure used to support Path layer connections in the SONET. It consists of the Information Payload and Path Overhead (POH) information fields organized in a block frame structure which repeats every 125 or 500 us. Alignment information to identify STS-n SPE frame start is provided by the server network layer.

Two types of Synchronous Payload Envelope have been identified.

- Non-concatenate/Channelized STS-n SPE: STS-n SPE (n=1, 3, 12, 48). This element comprises of byte interleaved or multiplexed STS1 SPE's including the Path Overhead Bytes of each STS1 payload container. This channelized STS-n SPE's (n=12, 48) element could also compromise of byte interleaved or multiplexed Concatenate STS-nc SPE's (n=3, 12).

- Concatenate STS-nc SPE: STS-nc SPE (n=3, 12, 48). This element comprises either a single bulk payload container-n (n=3, 12, 48) along with a single set of Path Overhead Bytes.

H1, H2 Pointer Bytes (H1, H2): The H1, H2 pointer bytes are central to SONET's ability in asynchronously mapping payload. These two bytes are located on the Line Overhead bytes in the Transport section of the overhead bytes. The H1 and H2 contain the location of the first POH byte (J1) of the channelized STS1 SPE or the concatenate STS-nc SPE (n=3, 12) and in some cases the channelized concatenated STS-nc SPE (n=3, 12) within the payload portion of the SONET frame structure. These pointer bytes also indicate pointer justifications and NDF (New Data Flag) events.

Virtual Tributaries-n (VT-n): The Virtual Tributary framing structure is the vehicle medium which provides the mapping structure for lower rate asynchronous/plesiochronous digital signal format such as DS1, E1, and DS2. There are specific VT-n mapping structures for each targeted digital signal format payload. For DS1, the VT-n mapping structure is referred to as VT1.5 and for E1, the VT mapping structure is referred to as VT2. These VT-n mapping structures are essentially similar in structure with each type containing four VT POH bytes called V5, J2, Z6(N2), and Z7(K4). The VT-n frame always begins with the V5 VT POH byte. Each VT-n frame is straddled accross four STS1 frames with the H4 byte value in the POH denoting the specific VT POH present and the VT-n phase. A VT1.5 straddled accross four STS1 frames will have 27 bytes allocated per STS1 frame with one byte used for the VT POH byte and the other two bytes used for stuffing and stuffing control leaving an ending balance of 24 bytes for DS1 payload per STS1 frame. Similarly, a VT2 straddled accross four STS1 frames will have 36 bytes allocated per STS1 frame with one byte used for a VT POH byte and the other three bytes used for stuffing and stuffing control leaving an ending balance of 32 bytes for E1 payload per STS1 frame.

Virtual Tributary Group (VT Group): The are seven VT Group per STS1 SPE. An STS1 SPE structure consist of a fixed 9 rows by 87 byte-wide columns space. One column is reserved for the SONET STS1 SPE POH bytes and VT mapping requires 2 columns for fixed stuffing (Column 30 and 59), leaving 84 columns for the seven VT Groups. Each VT Group can consist of VT1.5, VT2, VT3 and VT6 tributaries. However, each VT Group must contain a homogenous mapping of VT-n. Therefore each VT Group in the STS1 SPE is allocated 9 rows deep by 12 columns byte-wide space that can containing either four channelized VT1.5, or three channelized VT2, or two channelized VT3, or a single mapping of VT6. A VT Group containing four VT1.5 has 27 bytes (3 byte-wide columns) allocated for each of the channelized VT1.5. Proportionately, a VT Group carrying three VT2 has 36 bytes (4 byte-wide colums) allocated for each of the channelized VT2.

9.2 BASIC FRAME STRUCTURE

STS-N frame structure is shown in **Figure 81**. The three main areas of the STS-N frame are indicated:

• SOH (Section Overhead) - SOH and LOH collectively known as TOH (Transport Overhead);

• LOH (Line Overhead) - SOH and LOH collectively known as TOH (Transport Overhead);

• STS-N SPE (Synchronous Payload Envelope) containing POH (Path Overhead) and Information Payload.

FIGURE 80. STS-N FRAME STRUCTURE
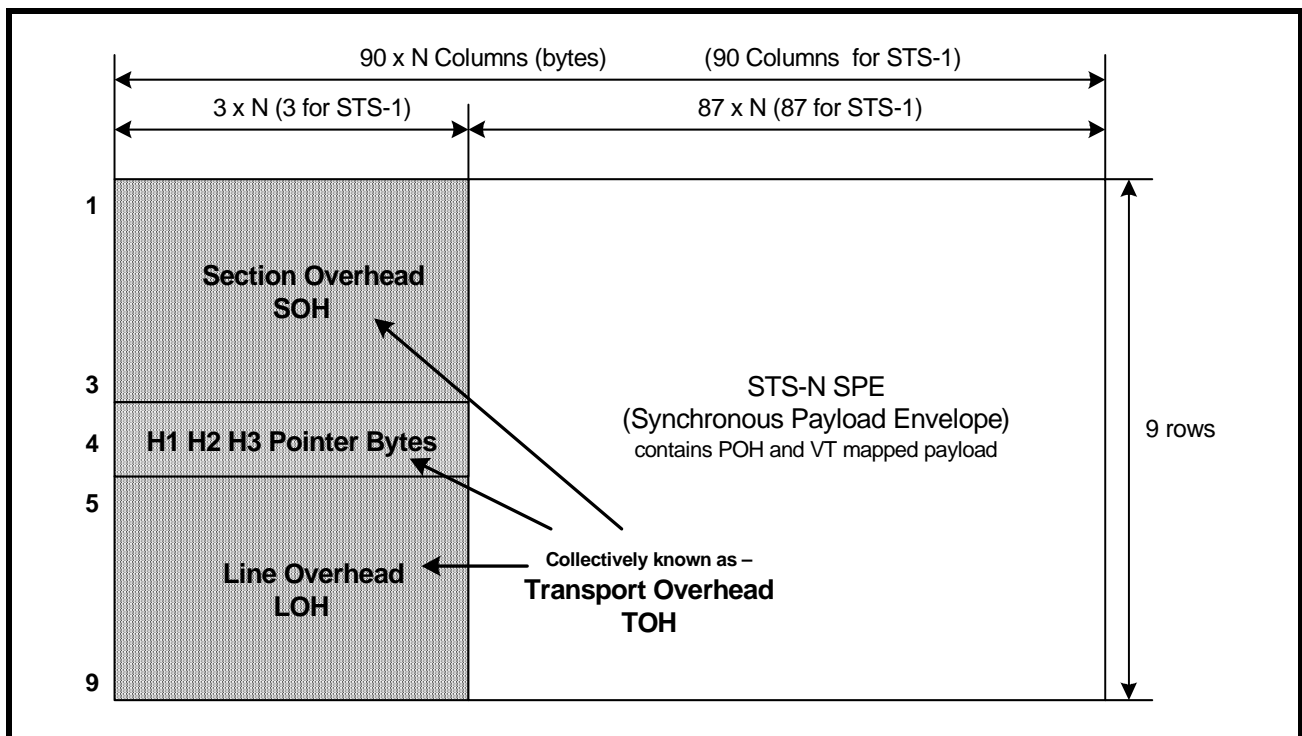
Section overhead (TOH)

Rows 1-3 of columns 1 to 3 x N of the STS-N in **Figure 80** are dedicated to the SOH.

Line Overhead (TOH)

Rows 5-9 of columns 1 to 3 x N of the STS-N in **Figure 80** are dedicated to the LOH.

H1, H2, and H3 Pointer Bytes (TOH)

Row 4 of columns 1 to 3 × N in **Figure 80** are dedicated for H1, H2, and H3 pointer bytes.

Transport Overhead

Collectively, rows 1-9 of columns 1 to 3 × N in **Figure 80** is referred to as the Transport Overhead bytes - TOH.

Synchronous Payload Envelope in the STS-N

The STS-N payload supports STS-N SPE where the:

A. STS-192 may consist of:

   1. one hundred ninety-two channelized STS1 SPE;
   2. sixty-four channelized STS3c SPE;
   3. sixteen channelized STS12c SPE;
   4. four channelized STS48c SPE;
   5. one STS192c SPE.

B. STS-48 SPE may consist of:

   1. forty-eight channelized STS1 SPE;
   2. sixteen channelized STS3c SPE;
   3. four channelized STS12c SPE
   4. one STS48c SPE.

C. STS-12 SPE may consist of:

   1. twelve channelized STS1 SPE;
   2. four channelized STS3c SPE
   3. one STS12c SPE.

D. STS-3 SPE may consist of:

   1. three channelized STS1 SPE;
   2. one STS3c SPE.

E. STS-1 SPE may consist of:

   1. seven VT Group consisting of 28 VT1.5 (4 VT1.5 per VT Group);
   2. seven VT Group consisting of 21 VT2 (3 VT2 per VT Group);
   3. seven VT Group consisting of a combination of VT1.5 and VT2 (4 VT1.5 or 3 VT2 per VT Group).

The VT-n (n = 1.5, 2, etc.) associated with each VT Group does not have a fixed phase with respect to the STS1 SPE. The location of the first byte of the VT-n (V5 VT POH) is indicated by the V1, V2 pointer. The VT-n sets of V1 and VT-n sets of V2 pointer bytes is in a fixed location immediately following the J1 POH Path Trace byte within the STS-1 SPE.

In an STS-M application carrying channelized STS1, the STS1 SPE associated with each STS-1 TOH does not have a fixed relationship with respect to the start of the STS-M SPE. The STS1 SPE pointer is in a fixed location in the STS-1 LOH and the location of the first byte of the respective STS1 SPE within the STS-M SPE is indicated by the H1, H2 pointer bytes of the respective STS-1 TOH.

Likewise in an STS-M application carrying channelized STS-Nc, the STS-Nc SPE associated with each STS-Nc TOH does not have a fixed relationship with respect to the start of the STS-M SPE. The STS-Nc SPE pointer is in a fixed location in the STS-Nc LOH and the location of the first byte of the respective STS-Nc SPE within the STS-M SPE is indicated by the H1, H2 pointer bytes of the respective STS-Nc TOH.

10.0 BACKGROUND AND PROTOCOLS

This section intends to provide a background coverage of the theory of communication protocols involved in Voyager development. Only brief descriptions of their formats, control flows, and application-specific features are presented here.

10.1 SYNCHRONOUS DIGTIAL HIERARCHY (SDH) STANDARD

This section intends to provide a background coverage of the theory of communication protocols involved in SDH standard. Only brief descriptions of their rates, formats, control flows, and application-specific features are presented here.

Synchronous digital hierarchy (SDH): The SDH is a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks.

Synchronous transport module (STM): An STM is the information structure used to support section layer connections in the SDH. It consists of information payload and Section Overhead (SOH) information fields organized in a block frame structure which repeats every 125 μs. The information is suitably conditioned for serial transmission on the selected media at a rate which is synchronized to the network. A basic STM is defined at 155 520 kbit/s. This is termed STM-1. Higher capacity STMs are formed at rates equivalent to N times this basic rate. STM capacities for N=4, N=16, N=64 and N=256 are defined; higher values are under consideration.

The STM-0 comprises a single Administrative Unit of level 3. The STM-N, N = 1, comprises a single Administrative Unit Group of level N (AUG-N) together with the SOH.

Virtual container-n (VC-n): A Virtual Container is the information structure used to support path layer connections in the SDH. It consists of information payload and Path Overhead (POH) information fields organized in a block frame structure which repeats every 125 or 500 us. Alignment information to identify VC-n frame start is provided by the server network layer.

Two types of Virtual Containers have been identified.

• Lower order Virtual Container-n: VC-n (n=1, 2, 3). This element comprises a single Container-n

    (n=1, 2, 3) plus the lower order Virtual Container POH appropriate to that level.

• Higher order Virtual Container-n: VC-n (n=3, 4). This element comprises either a single

    Container-n (n=3, 4) or an assembly of Tributary Unit Groups (TUG-2s or TUG-3s), together with Virtual Container POH appropriate to that level.

Administrative unit-n (AU-n): An Administrative Unit is the information structure which provides adaptation between the higher order path layer and the multiplex section layer. It consists of an information payload (the higher order Virtual Container) and an Administrative Unit pointer which indicates the offset of the payload frame start relative to the multiplex section frame start.

Two Administrative Units are defined. The AU-4 consists of a VC-4 plus an Administrative Unit pointer which indicates the phase alignment of the VC-4 with respect to the STM-N frame. The AU-3 consists of a VC-3 plus an Administrative Unit pointer which indicates the phase alignment of the VC-3 with respect to the STM-N frame. In each case the Administrative Unit pointer location is fixed with respect to the STM-N frame.

One or more Administrative Units occupying fixed, defined positions in an STM payload are termed

an Administrative Unit Group (AUG). An AUG-1 consists of a homogeneous assembly of AU-3s or an AU-4.

Tributary unit-n (TU-n): A Tributary Unit is an information structure which provides adaptation between the lower order path layer and the higher order path layer. It consists of an information payload (the lower order Virtual Container) and a Tributary Unit pointer which indicates the offset of the payload frame start relative to the higher order Virtual Container frame start.

The TU-n (n=1, 2, 3) consists of a VC-n together with a Tributary Unit pointer. One or more Tributary Units, occupying fixed, defined positions in a higher order VC-n payload is termed a Tributary Unit Group (TUG). TUGs are defined in such a way that mixed capacity payloads made up of different size Tributary Units can be

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constructed to increase flexibility of the transport network. A TUG-2 consists of a homogeneous assembly of identical TU-1s or a TU-2. A TUG-3 consists of a homogeneous assembly of TUG-2s or a TU-3.

Container-n (n=1-4): A container is the information structure which forms the network synchronous information payload for a Virtual Container. For each of the defined Virtual Containers there is a corresponding container. Adaptation functions have been defined for many common network rates into a limited number of standard containers.

10.2 *BASIC FRAME STRUCTURE*

STM-N frame structure is shown in **Figure 81**. The three main areas of the STM-N frame are indicated:

- RSOH and MSOH;

- Administrative Unit pointer(s);

- Information payload.

FIGURE 81. STM-N FRAME STRUCTURE
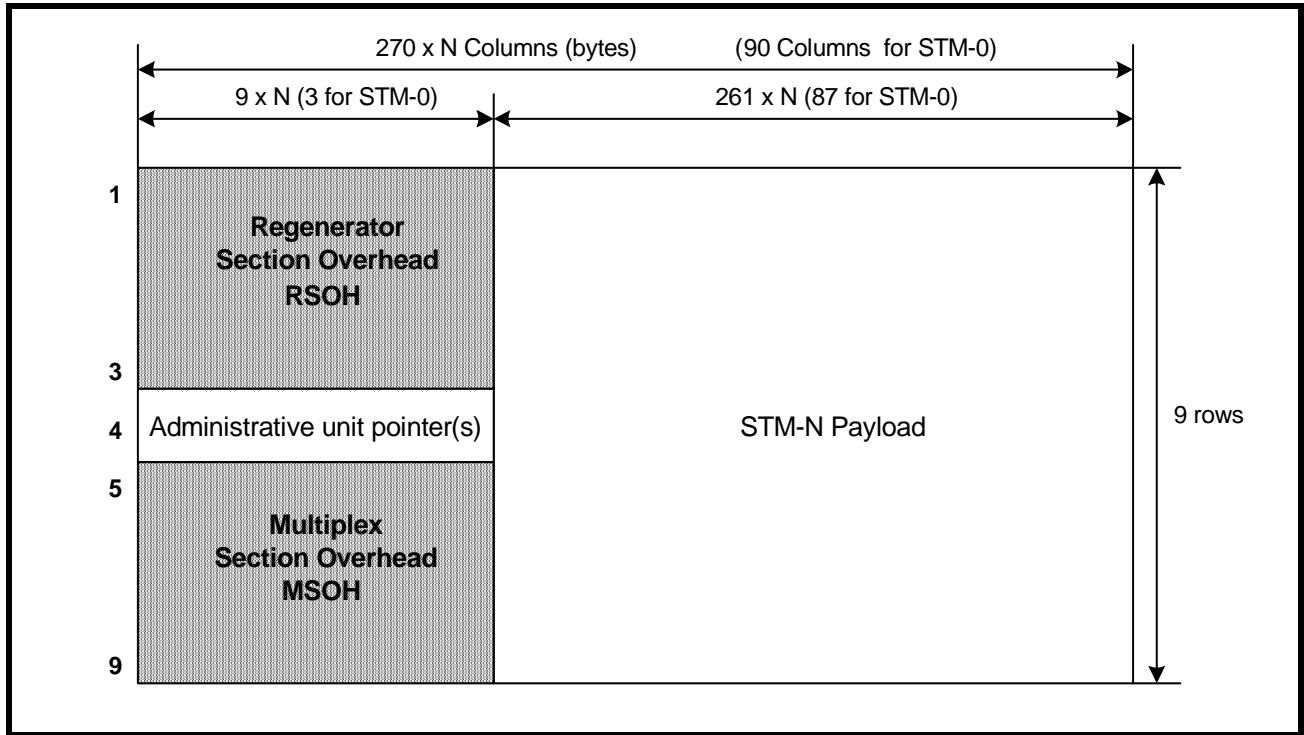
Regenerator Section Overhead

Rows 1-3 of columns 1 to 9 x N of the STM-N in **Figure 81** are dedicated to the RSOH.

Administrative Unit pointers

Row 4 of columns 1 to 9 × N in **Figure 81** is available for Administrative Unit pointers.

Multiplex Section Overhead

Rows 5-9 of columns 1 to 9 x N of STM-N in **Figure 81** are dedicated to the MSOH

Administrative Units in the STM-N

The STM-N payload supports one AUG-N where the:

A. AUG-256 may consist of:

    1. four AUG-64;

    2. one AU-4-256c.

B. AUG-64 may consist of:

    1. four AUG-16;

    2. one AU-4-64c.

C. AUG-16 may consist of:

    1. four AUG-4;

    2. one AU-4-16c.

D. AUG-4 may consist of:

    1. four AUG-1;

    2. one AU-4-4c.

E. AUG-1 may consist of:

    1. one AU-4;

    2. three AU-3s.

The VC-n associated with each AU-n does not have a fixed phase with respect to the STM-N frame. The location of the first byte of the VC-n is indicated by the AU-n pointer. The AU-n pointer is in a fixed location in the STM-N frame.

The AU-4 may be used to carry, via the VC-4, a number of TU-ns (n=1, 2, 3) forming a two-stage multiplex. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-4. The TU-n pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

The AU-3 may be used to carry, via the VC-3, a number of TU-ns (n=1, 2) forming a two-stage multiplex. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-3. The TU-n pointer is in a fixed location in the VC-3 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

11.0 REFERENCE DOCUMENTATION

- Telcordia, Transport Systems Generic Requirements (TSGR): Common Requirements GR-499-CORE Issue 2, December 1998

- ITU-T Recommendation G.707 Network Node Interface for the Synchronous Digital Hierarchy (SDH) (03/96)

- ITU-T Recommendation G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks (01/94)

- ITU/CCITT Recommendation O.151 Error Performance Measuring Equipment Operating at the Primary Rate and Above (10/92)

- ANSI T1.107, "Digital Hierarchy - Formats Specifications", 1988.

- ANSI 1.107a, Addendum to ANSI T1.107, 1988", 1990.

- ANSI T1.403 - 1999, Network-to-Customer Installation - DS1 Metallic Interface

- ANSI T1.408-1990, Integrated Services Digital Network (ISDN) Primary Rate - Customer Installation Metallic Interfaces Layer 1 Specification

- ETS 300 011, ISDN primary rte user-network interface layer 1 specification and test principles, April 1992

- ETS 300 233, ISDN; Access digital section for ISDN primary rate, May 1994

- Intel i750, i860, i960 Processors and Related Products Data Book, 1994

- Intel 8-bit Embedded Controllers Data Book

- Motorola MC68302, Integrated Multi-Protocol Processor User's Manual

11.1 TERMINOLOGY

11.1.1 NOMENCLATURE

"Transmit" refers to the flow of data from the user interface to the physical line interface.

"Receive" refers to the flow of data from the physical line interface to the user interface.

"Ingress" refers to the flow of data from the E1 LIU's to the SDH interface.

"Egress" refers to the flow of data from the SDH interface to the E1 LIU's.

11.1.2 SIGNAL NAME PREFIXES AND SUFFIXES

The following lists the convention used in this design for naming distinguished signals.

Tx	Signals pertaining to the DS1 transmit framer
Rx	Signals pertaining to the DS1 receive framer
Li	Signals pertaining to LIU interface module
p	Signals pertaining to microprocessor interface

11.1.3 ABBREVIATIONS

AIS	Alarm Indication Signal
AMI	Alternate Mask Inversion
AU	Administrative Unit
AUG	Administrative Unit Group
BIP	Bit Interleaved Parity
BPV	Bipolar Violation
CRC	Cyclic Redundancy Check

DSn	Digital Signal n (any of DS1, DS1A, DS1C or DS2)
DL	Data Link
FA	Frame Alignment
FAS	Frame Alignment Signal
FCS	Frame Check Sequence
FIFO	First In First Out
FPS	Framing Pattern Sequence
HDLC	High level Data Link Control protocol
ITU	The International Telecommunications Union
LAPD	Link Access Protocol D
LCV	Line Code Violation
LIU	Line Interface Unit
LOF	Loss Of Frame synchronization
LOP	Loss Of Pointer
LOS	Loss Of Signal
LTE	Line Terminating Equipment
MSOH	Multiplex Section Overhead
NRZ	Non Return to Zero
OH	OverHead
OOF	Out Of Frame synchronization
OC	Optical Carrier
PLM	Payload Label Mismatch
POH	Path Overhead
PM	Performance Monitor
PMDL	Path Maintenance Data Link
PMON	Performance Monitor
PTE	Path Terminating Equipment
RAI	Remote Alarm Indication
RDI	Remote Defect Indication
REI	Remote Error Indication
RFI	Remote Failure Indication
RSOH	Regenerator Section Overhead
SDH	Synchronous Digital Hierarchy
Rx	Receive
SF	Super Frame
SDH	Synchronous Digtial Hierarchy
SPE	Synchronous Payload Envelop

STM	Synchronous Transport Module
TU	Tributary Unit
TUG	Tributary Unit Group
Tx	Transmit
T1DM	T1 Data Multiplexer
mp(uP)	Microprocessor
VC	Virtual Container
VT	Virtual Tributary

1   Package Mechanical Specifications

Table 44   Ordering Information

Product Number	Package Type	Operating Temperature Range
XRT86SH328IB	568 Ball PBGA-TEP	-40℃ to +85℃

Figure 1   568 Ball PBGA Plastic Ball Grid Array (31 x 31 mm, 30 x 30 matrix, w/ Exposed Heat Slug)
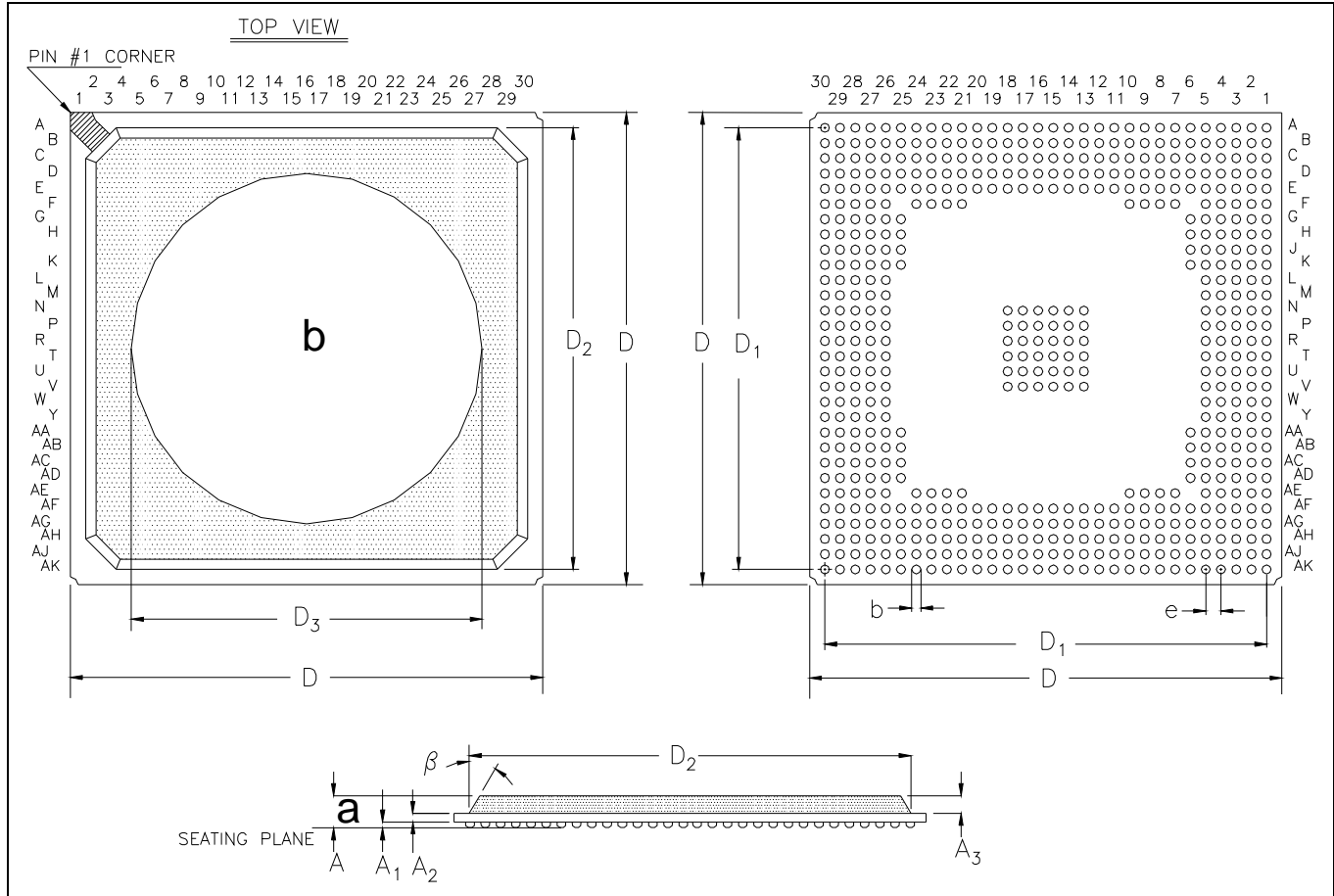
Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.067	0.106	1.70	2.70
A1	0.020	0.028	0.50	0.70
A2	0.016	0.028	0.40	0.70
A3	0.039	0.051	1.00	1.30
D	1.213	1.228	30.80	31.20
D1	1.142 BSC		29.00 BSC	
D2	1.134	1.150	28.80	29.20
D3	0.886	0.925	22.50	23.50
b	0.020	0.028	0.50	0.70
e	0.0394 BSC		1.00 BSC	
β	30° TYP.		30° TYP.	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
1.0.0	May 2008	Final release datasheet of the XRT86SH328 Pin and Architecture Description.
1.0.1	August 2008	Removed LVPECL reference and corrected with LVCMOS/LVTTL.

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