AKD4125-A
AK4125 Evaluation Board Rev.1

GENERAL DESCRIPTION

The AKD4125-A is an evaluation board for AK4125, the digital sample rate converter. The AKD4125-A has the digital audio interface and can achieve the interface with digital audio system via opt-connector.

■ **Ordering guide**

AKD4125-A --- AK4125 Evaluation Board

FUNCTION

- **DIR/DIT with optical input/output**
- **10pin Header for AKM AD/DA evaluation board**

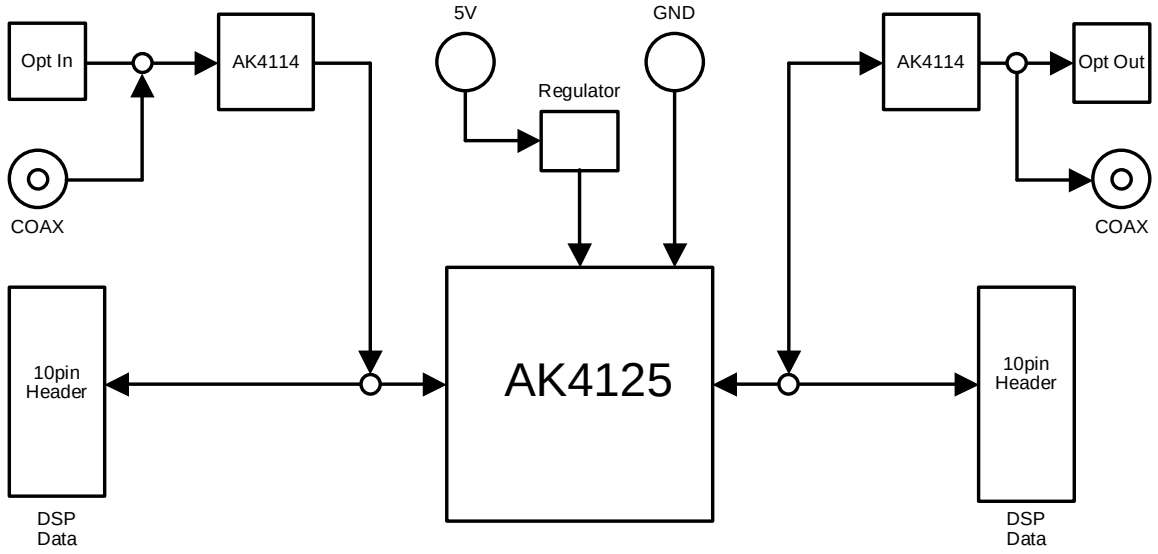


Figure 1. AKD4125-A Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supply lines.
[VCC] (red) = +5V (for regulator)
[DGND] (black) = 0V

Each supply line should be distributed from the power supply unit.
The regulator can be supplied 3.3V to all circuits.

2) Set up the evaluation mode, jumper pins. (See the followings.)

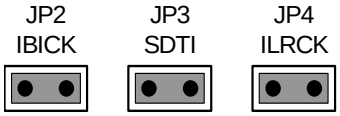
3) Power on.
The AK4125 should be reset once bringing SW1 (PDN) "L" upon power-up.

■ Evaluation mode

(1) Setting for Input port

(1) When using DIR function of AK4114 (U3)

When using PORT1 (DIR) or J1 (COAX), nothing should be connected to PORT2 (INPUT).



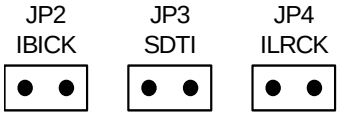
- SW3 setting (See Table 1)
Upper-side is "H" and lower-side is "L".
The audio interface format of the AK4114 is fixed to 24bit, MSB justified. IDIF2-0 and PLL2-0 of SW3 should be used by default setting.

SW3 No.	Name	ON ("H")	OFF ("L")	Default
1	DITH	Dither ON	Dither OFF	L
2	PLL2	PLL Mode Setting Fixed to default		H
3	PLL1			L
4	PLL0			H
5	IDIF0	AK4125 Audio I/F Format Setting Fixed to default		L
6	IDIF1			H
7	IDIF2			L

Table 1. SW3 Setting

(2) All clocks are fed through the 10pin port

When using PORT2 (INPUT), nothing should be connected to J1 (COAX) and PORT1 (DIR).



- SW3 setting (See Table 2)
  Upper-side is "H" and lower-side is "L".

SW3 No.	Name	ON ("H")	OFF ("L")	Default
1	DITH	Dither ON	Dither OFF	L
2	PLL2	PLL Mode Setting Refer to Table 3		H
3	PLL1			L
4	PLL0			H
5	IDIF0	AK4125 Audio I/F Format Setting Refer to Table 4		L
6	IDIF1			H
7	IDIF2			L

Table 2. SW3 Setting

Mode	Master / Slave	PLL2	PLL1	PLL0	ILRCK Freq	IBICK Freq	IMCLK	SMUTE (Note 4)
0	Slave IMCLK = DVSS IBICK = Input ILRCK = Input	L	L	L	8k ~ 96kHz	Depending on IDIF2-0	Not needed.	Manual
1		L	L	H	8k ~ 216kHz 16k ~ 216kHz (Note 1)			
2		L	H	L				Semi-Auto
3		L	H	H	Reserved			
4		H	L	L	8k ~ 216kHz (Note 2)	32fsi (Note 3)	Not needed.	Manual
5		H	L	H		64fsi		
6		H	H	L		128fsi		
7		H	H	H		64fsi		Semi-Auto
8	Master IMCLK = Input IBICK = Output ILRCK = Output	L	L	L	8k ~ 216kHz	64fs	128fs	Manual
9		L	L	H	8k ~ 108kHz		256fs	
10		L	H	L	8k ~ 54kHz		512fs	
11		L	H	H	8k ~ 216kHz		128fs	Semi-Auto
12		H	L	L	8k ~ 216kHz		192fs	Manual
13		H	L	H	8k ~ 108kHz		384fs	
14		H	H	L	8k ~ 54kHz		768fs	
15		H	H	H	8k ~ 216kHz		192fs	Semi-Auto

Table 3. PLL Setting (Input PORT)

Note 1. PLL lock rage is changed by the value of R and C connected FILT pin. Refer to "PLL Loop Filter" in the datasheet. 470Ω, 0.22μF and 1nF are implemented on the evaluation board.
Note 2. The IBCIK must be continuous except when the clocks are changed.
Note 3. IBCIK = 32fsi is supported only 16bit LSB justified and I^2S Compatible.
Note 4. Refer to "Soft Mute Operation" for Manual mode and Semi-Auto mode in the datasheet.

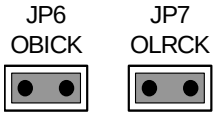
Mode	IDIF2	IDIF1	IDIF0	SDTI Format	ILRCK	IBICK	IBICK Freq	Master / Slave
0	L	L	L	16bit, LSB justified	Input	Input	≥ 32fsi	Slave
1	L	L	H	20bit, LSB justified			≥ 40fsi	
2	L	H	L	24/20bit, MSB justified			≥ 48fsi	
3	L	H	H	24/16bit, I^2S Compatible			≥ 48fsi or 32fsi	
4	H	L	L	24bit, LSB justified			≥ 48fsi	
5	H	L	H	24bit, MSB justified	Output	Output	64fs	Master
6	H	H	L	24bit, I^2S Compatible			64fs	
7	H	H	H	Reserved				

Table 4. Input Audio Interface Format (Input PORT)

(2) Setting for Output port

(1) When using DIT function of AK4114 (U4)

When using PORT4 (DIT) or J2 (TX), nothing should be connected to PORT3 (OUTPUT). When BICK and LRCK frequencies are changed, the value of X'tal (X1) frequency should be changed.



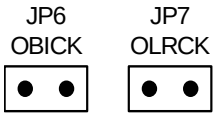
- SW4 setting (See Table 5)
  Upper-side is "H" and lower-side is "L".
  The audio interface format of the AK4114 is fixed to 24bit, MSB justified. ODIF2-0, CMODE2-0 and OBIT1-0 of SW3 should be used by default setting.

SW4 No.	Name	ON ("H")	OFF ("L")	Default
1	ODIF1	AK4125 Output Audio I/F Format Setting		H
2	ODIF0	Fixed to default		L
3	CMODE2	AK4125 Mode Setting		H
4	CMODE1	Fixed to default		L
5	CMODE0			L
6	OBIT1	AK4125 Output bit Length Setting		H
7	OBIT0	Fixed to default		H

Table 5. SW4 Setting

(2) All clocks are fed through the 10pin port

When using PORT3 (OUTPUT), nothing should be connected to J2 (TX) and PORT4 (DIT).



- SW4 setting (See Table 6)
  Upper-side is "H" and lower-side is "L".

SW4 No.	Name	ON ("H")	OFF ("L")	Default
1	ODIF1	AK4125 Output Audio I/F Format Setting Refer to Table 7		H
2	ODIF0			L
3	CMODE2	AK4125 Mode Setting Refer to Table 8		H
4	CMODE1			L
5	CMODE0			L
6	OBIT1	AK4125 Output bit Length Setting Refer to Table 9		H
7	OBIT0			H

Table 6. SW4 Setting

Mode	ODIF1	ODIF0	SDTO Format
0	L	L	LSB justified
1	L	H	(Reserved)
2	H	L	MSB justified
3	H	H	I^2S Compatible

Table 7. Output Audio Interface Format 1 (Output PORT)

Mode	CMODE2	CMODE1	CMODE0	Master / Slave	OMCLK	fso
0	L	L	L	Master	256fso	8k ~ 108kHz
1	L	L	H	Master	384fso	8k ~ 108kHz
2	L	H	L	Master	512fso	8k ~ 54kHz
3	L	H	H	Master	768fso	8k ~ 54kHz
4	H	L	L	Slave	Not used. Set to DVSS.	8k ~ 216kHz
5	H	L	H	Master	128fso	8k ~ 216kHz
6	H	H	L	Master	192fso	8k ~ 216kHz
7	H	H	H	Master (Bypass)	Not used. Set to DVSS.	8k ~ 216kHz

Table 8. Master/Slave Control (Output PORT)

Mode	OBIT1	OBIT0	SDTO Output
0	L	L	16bit
1	L	H	18bit
2	H	L	20bit
3	H	H	24bit

Table 9. Output Audio Interface Format 2 (Output PORT)

■ Other jumper pins set up

1. JP1 (RX) : Select of RX input
   COAX: COAX input.
   RX: Optical input. <Default>

2. JP5 (CKSO) : AK4114 BICK and LRCK setting
   H: BICK: 2.048MHz ~ 12.288MHz, LRCK: 32kHz ~ 192kHz
   L: BICK: 2.048MHz ~ 6.144MHz, LRCK: 32kHz ~ 96kHz <Default>
   When BICK and LRCK frequencies are changed, the value of X'tal (X1) frequency should be changed.

3. JP8 (TX) : Select of TX output
   BNC: BNC connector (J2) output.
   OPT: Optical (PORT4) output. <Default>

■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Resets the AK4125 and the AK4114. Keep "H" during normal operation.
The AK4125 and the AK4114 should be resets once bringing "L" upon power-up.

[SW2] (SMUTE): Soft mute of AK4125

■ Indication for LED

[LED1] (UNLOCK): Monitor UNLOCK pin of the AK4125. LED turns on when unlock occurs.

[LED2] (ERF): Monitor INT0 pin of the AK4114 (U3). LED turns on when unlock or parity error occurs.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
- Power Supply : AVDD = DVDD = 3.3V
- Band width : 10Hz ~ FSO/2
- Temperature : Room

[Measurement Result]

SRC Characteristics	Result	Unit
THD+N (Input = 1kHz, 0dBFS)		
FSO/FSI = 44.1kHz/48kHz	130.2	dB
FSO/FSI = 48kHz/44.1kHz	124.9	dB
FSO/FSI = 48kHz/192kHz	130.6	dB
FSO/FSI = 192kHz/48kHz	124.3	dB
Worst Case (FSO/FSI = 44.1kHz/8kHz)	116.7	dB
Dynamic Range (Input = 1kHz, –60dBFS)		
FSO/FSI = 44.1kHz/48kHz	136.2	dB
FSO/FSI = 48kHz/44.1kHz	136.4	dB
FSO/FSI = 48kHz/192kHz	136.1	dB
FSO/FSI = 192kHz/48kHz	132.3	dB
Worst Case (FSO/FSI = 192kHz/192kHz)	132.2	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted)		
FSO/FSI = 44.1kHz/48kHz	139.6	dB

[Plot]

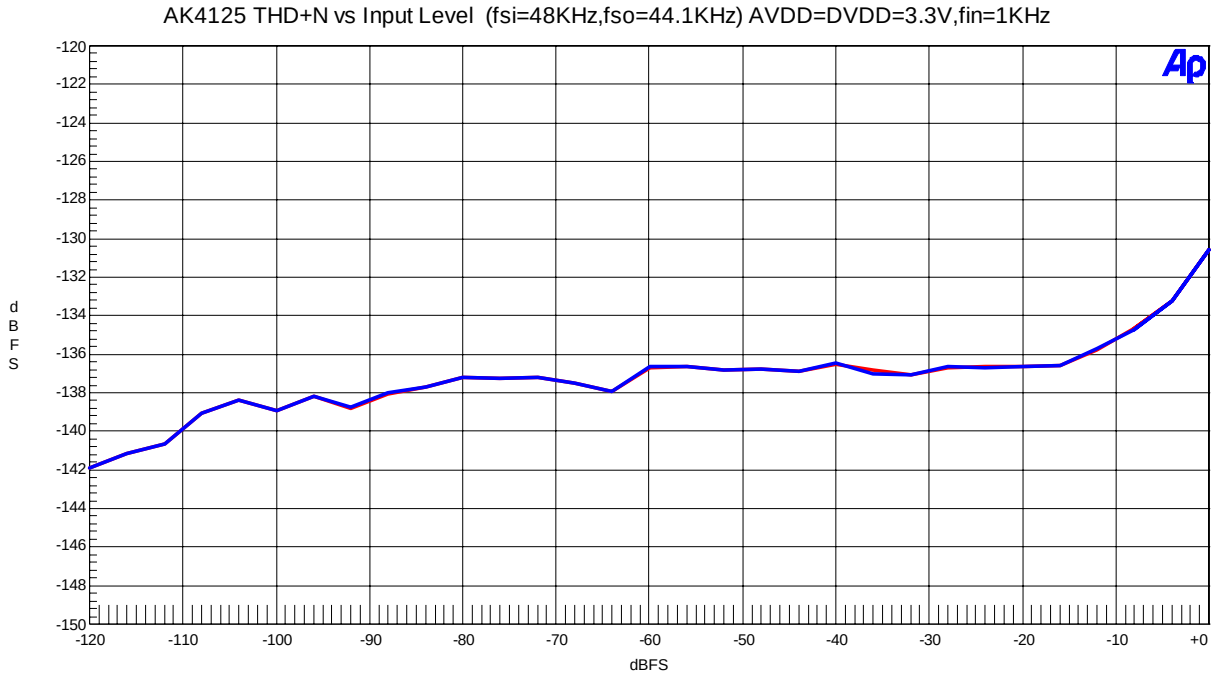


Fig 1. THD+N vs. Input Level

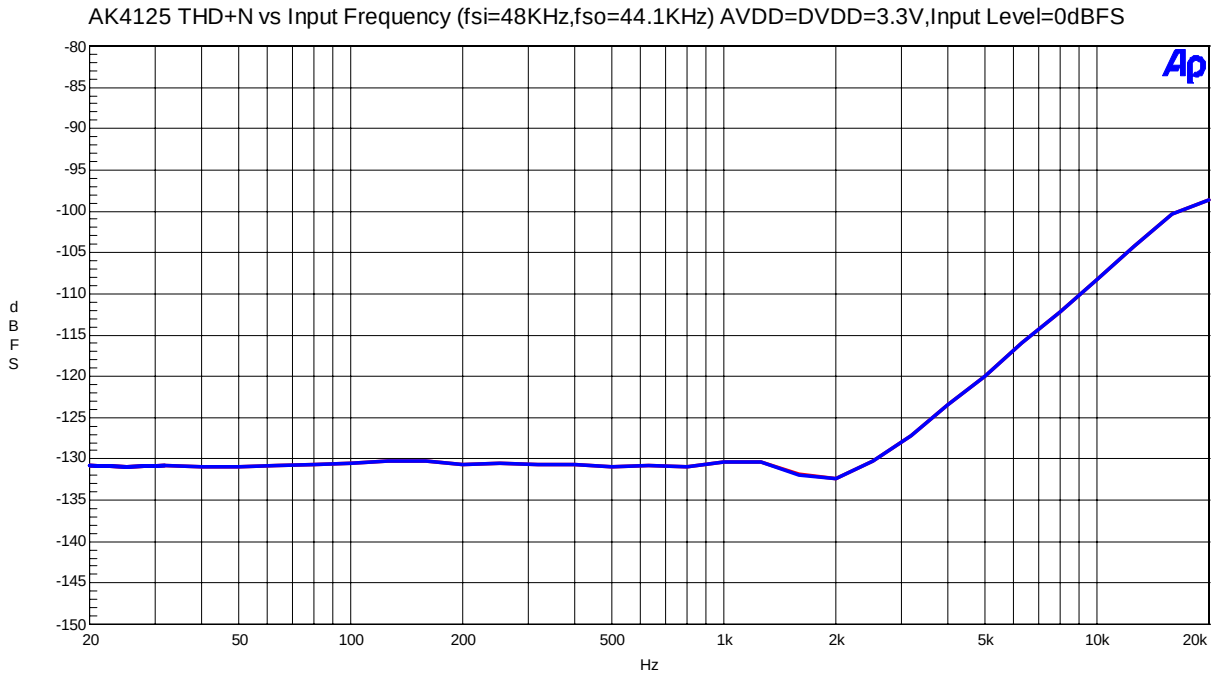


Fig 2. THD+N vs. Input Frequency (Input = 0dBFS)

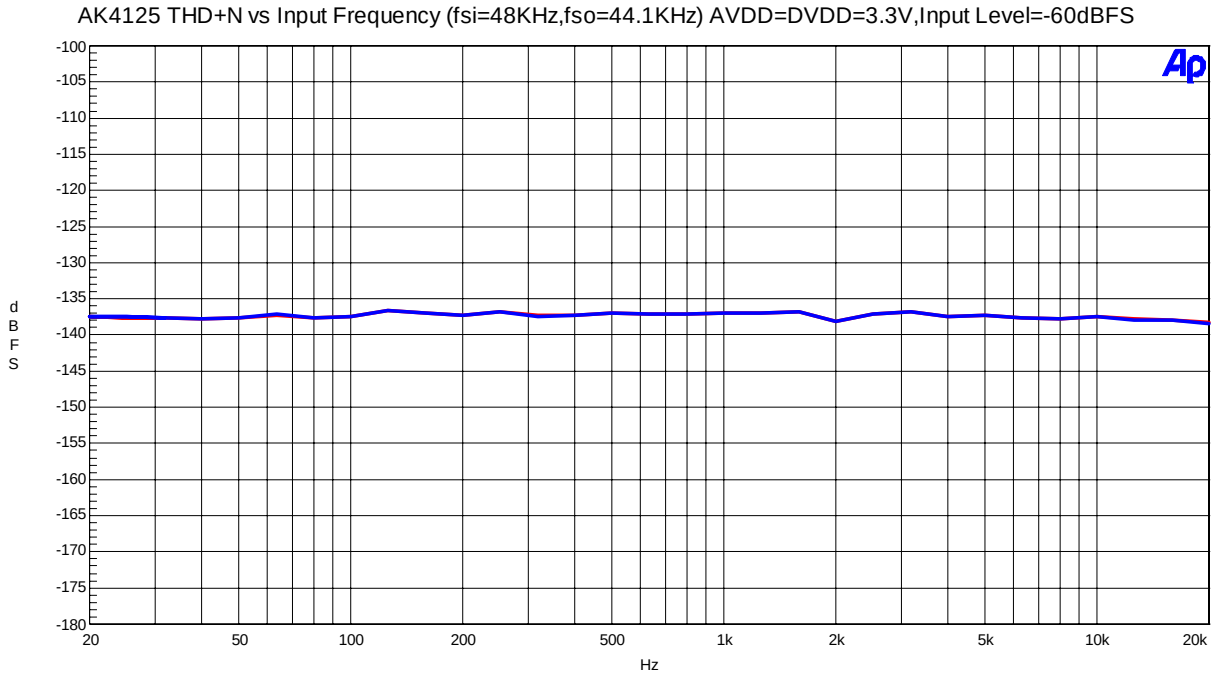


Fig 3. THD+N vs. Input Frequency (Input = –60dBFS)

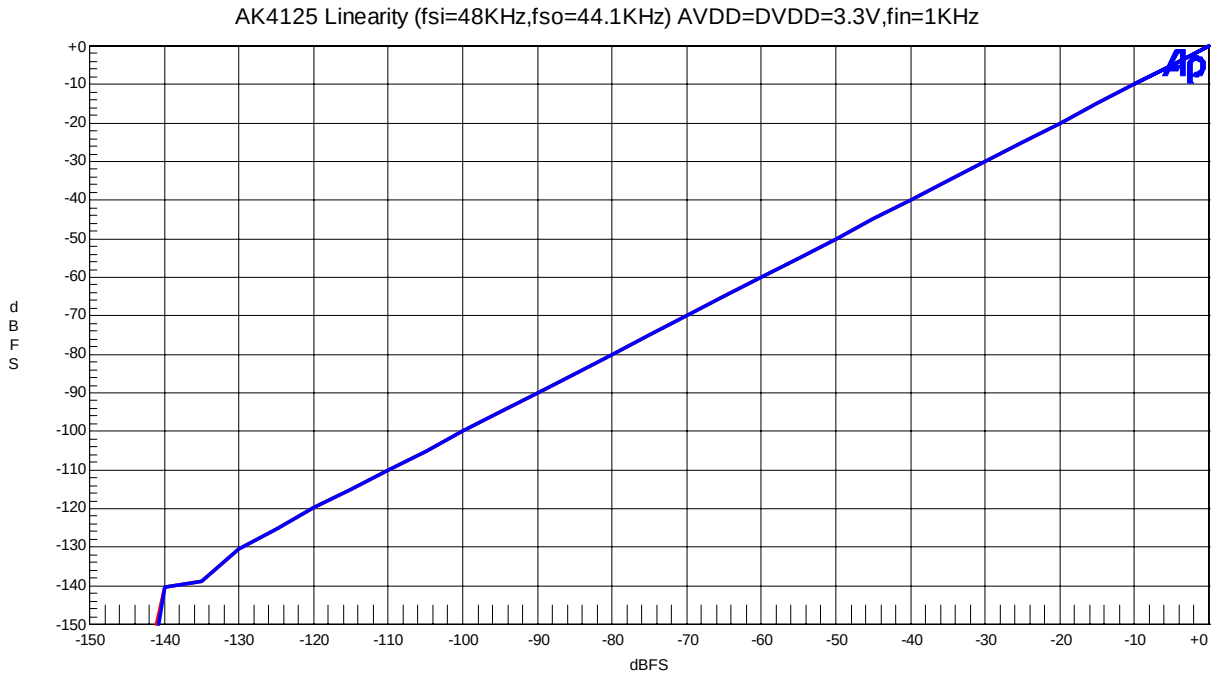


Fig 4. Linearity

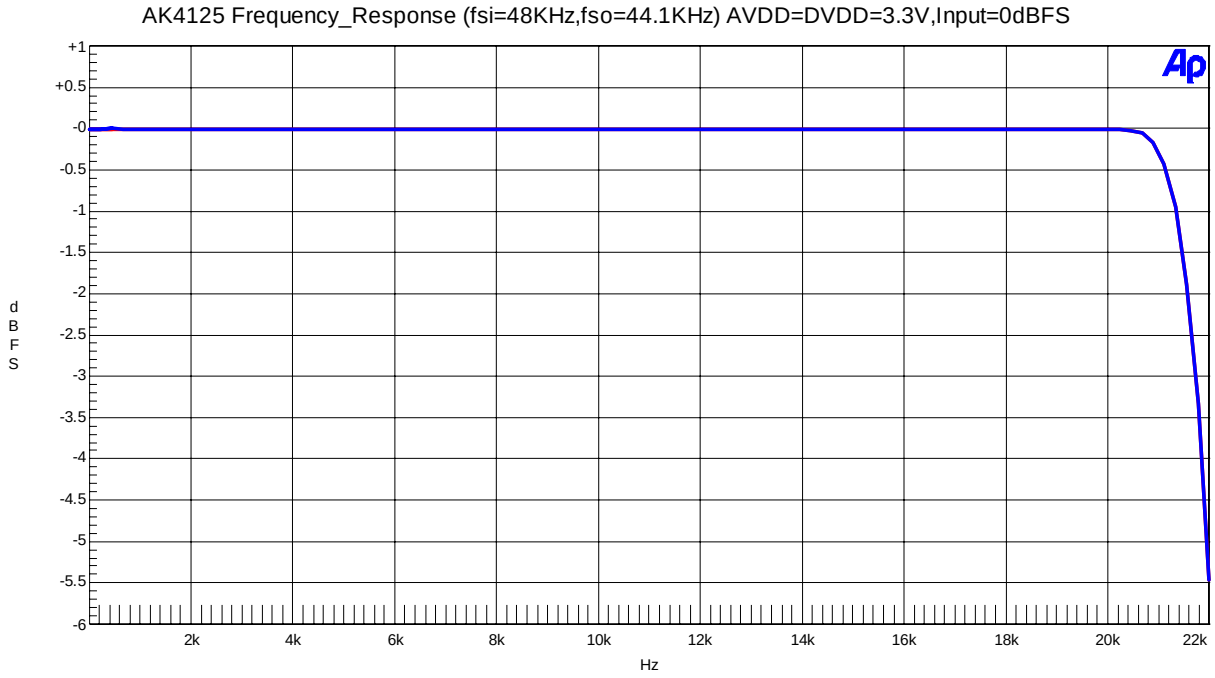


Fig 5. Frequency Response

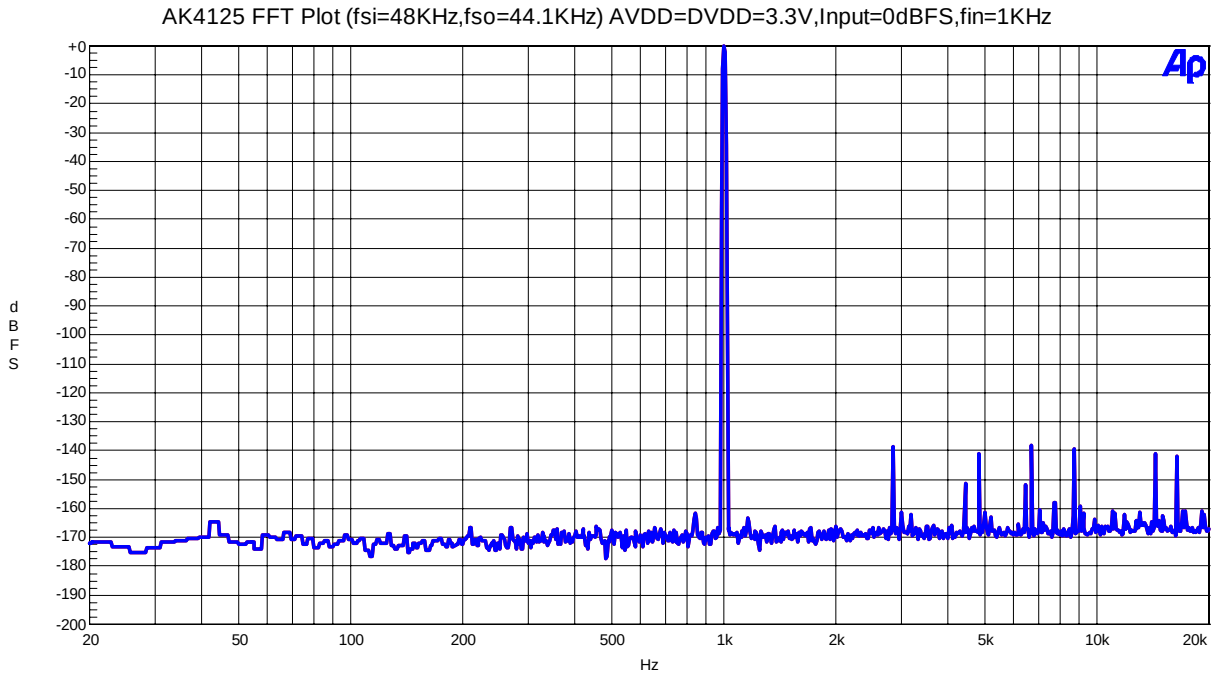


Fig 6. FFT Plot (Input = 0dBFS)

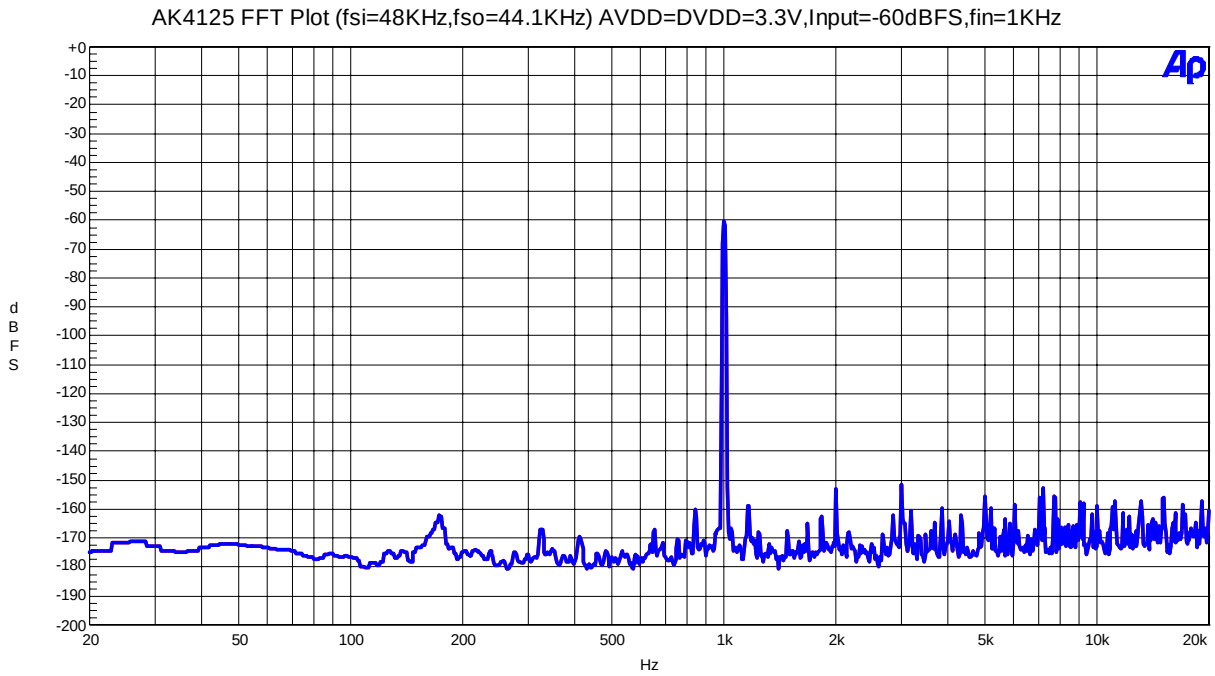


Fig 7. FFT Plot (Input = –60dBFS)

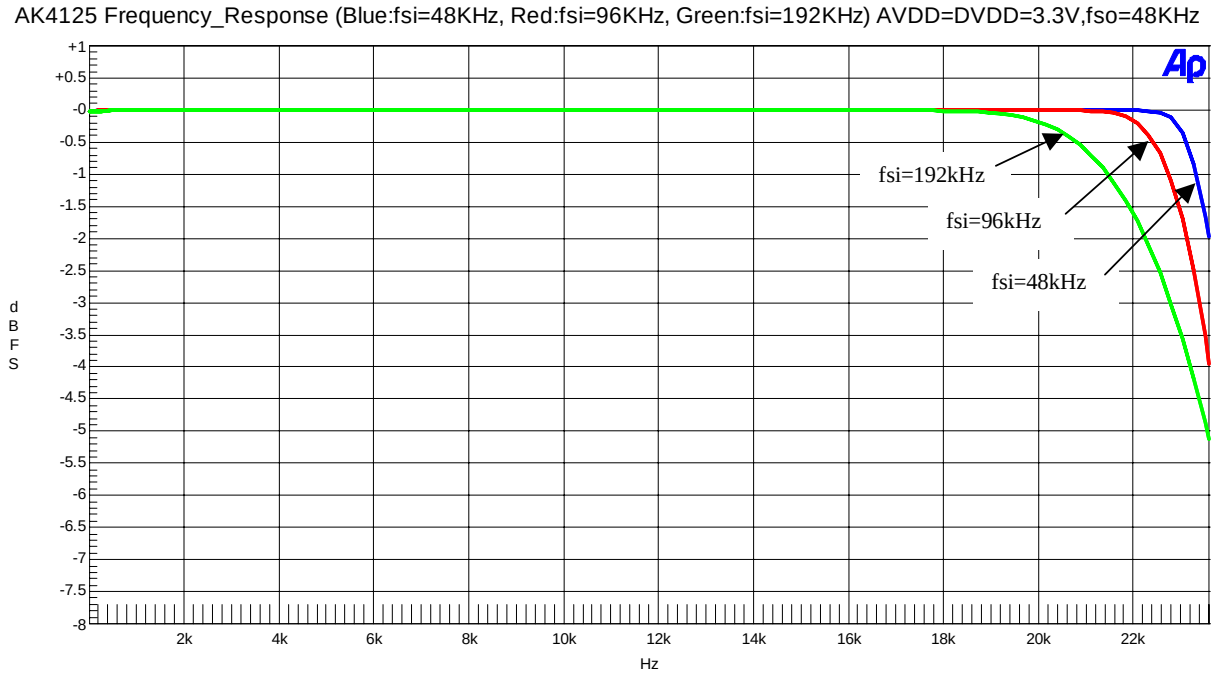


Fig 8. Frequency Response

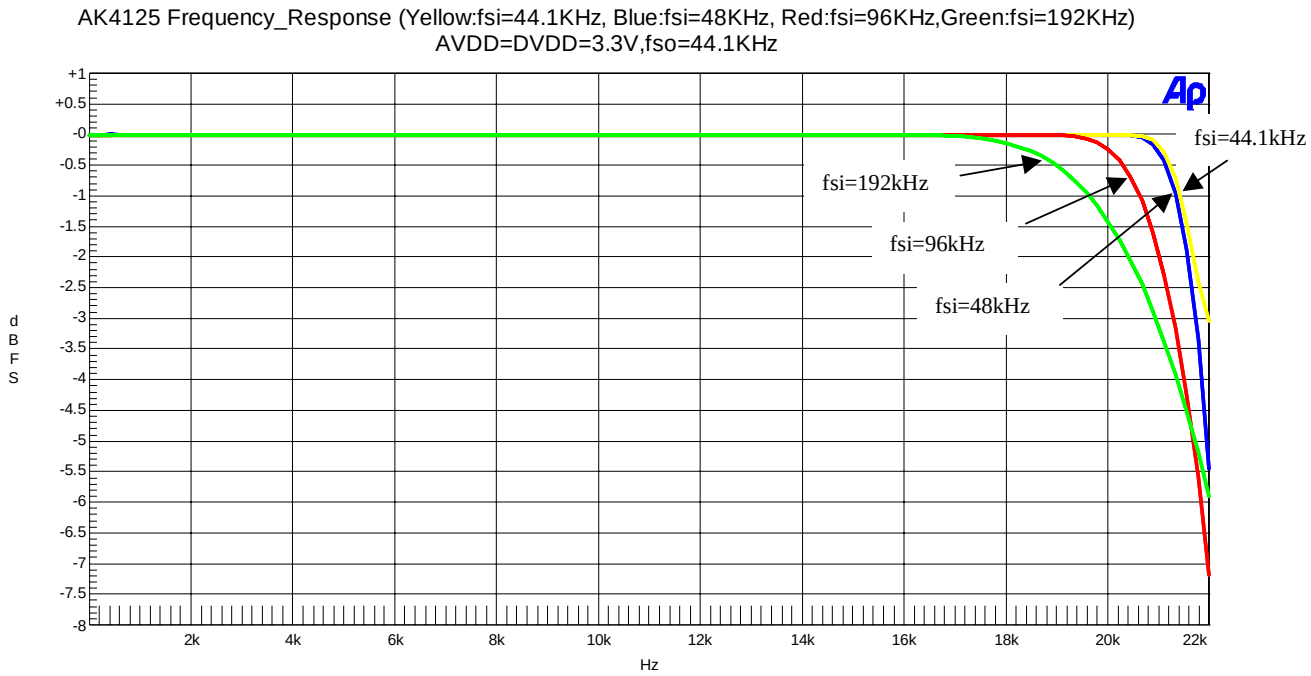


Fig 9. Frequency Response

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
05/06/30	KM078700	0	First Edition	
06/04/18	KM078701	1	Circuit Change	Condenser C24, C25: Value Change: open→5p

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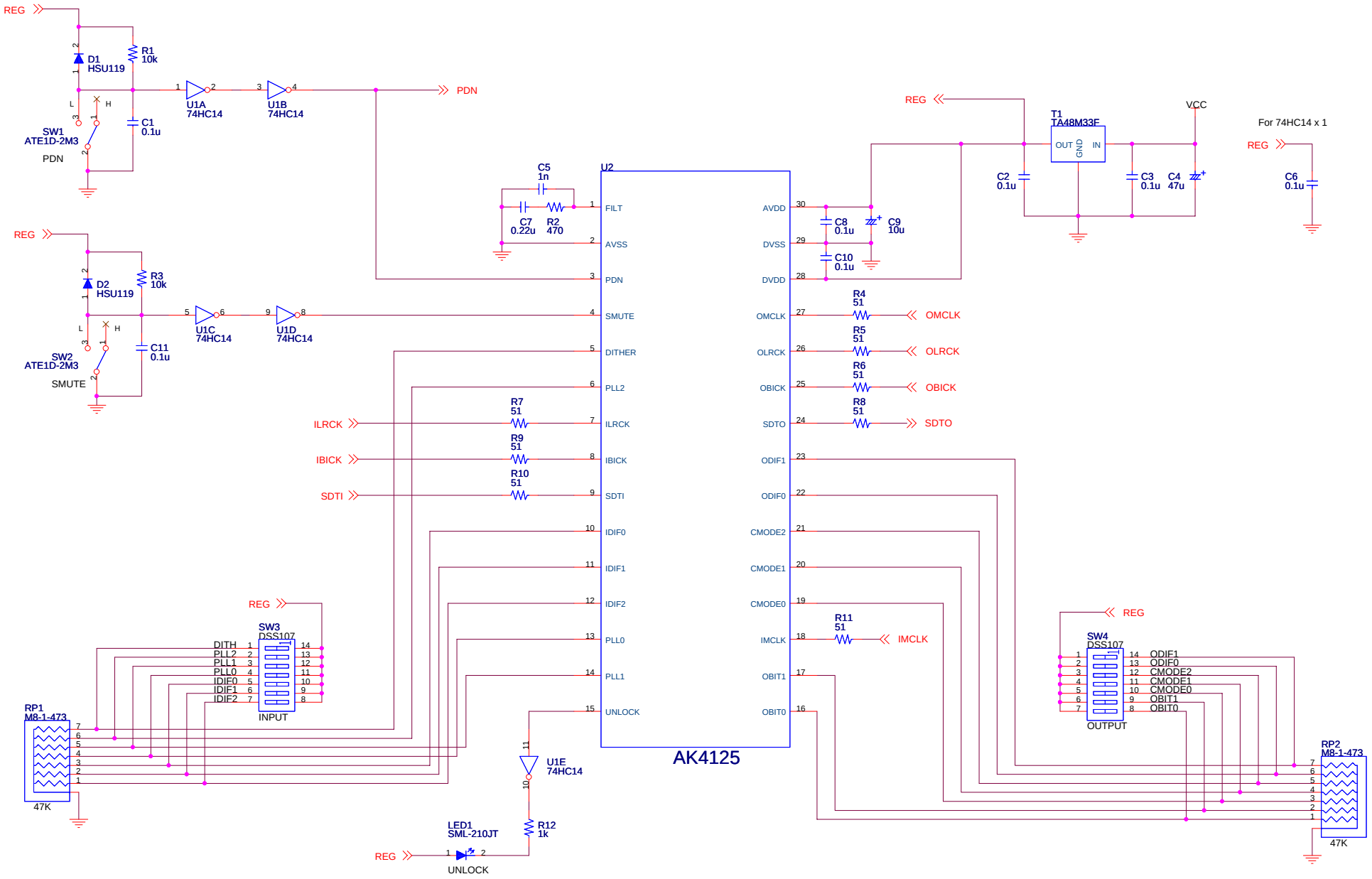

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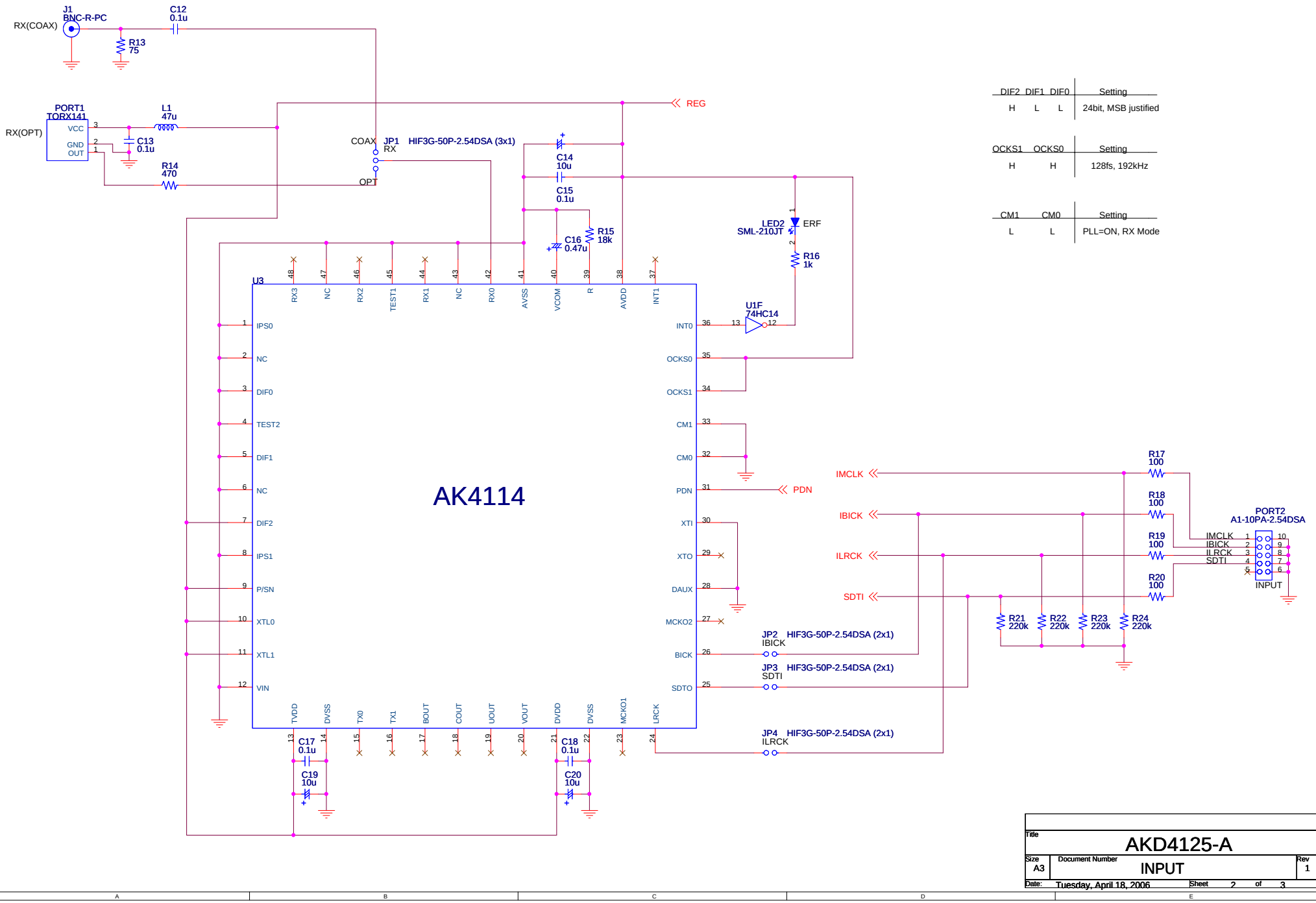
Date: Tuesday, April 18, 2006	Sheet 1 of 3	

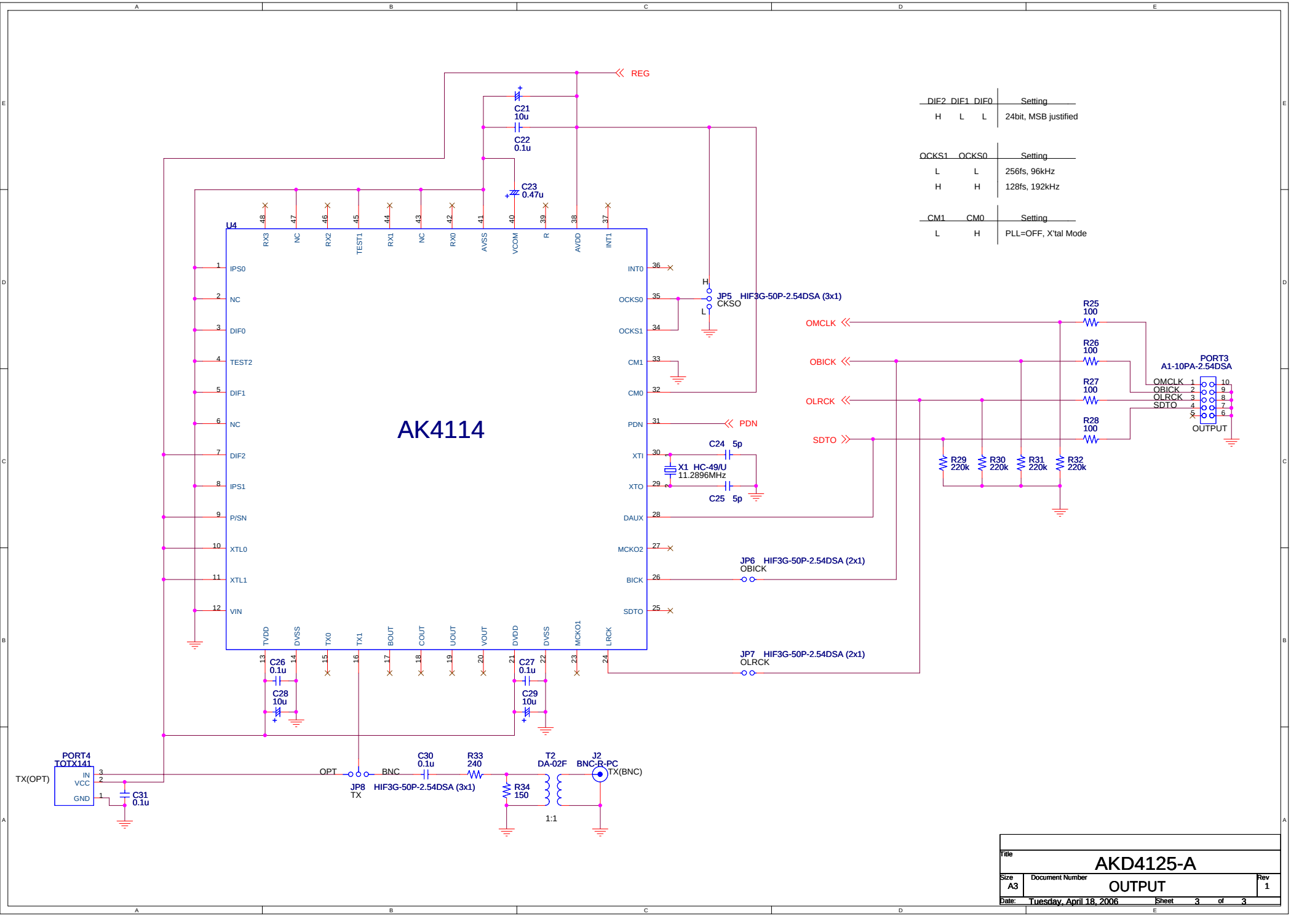


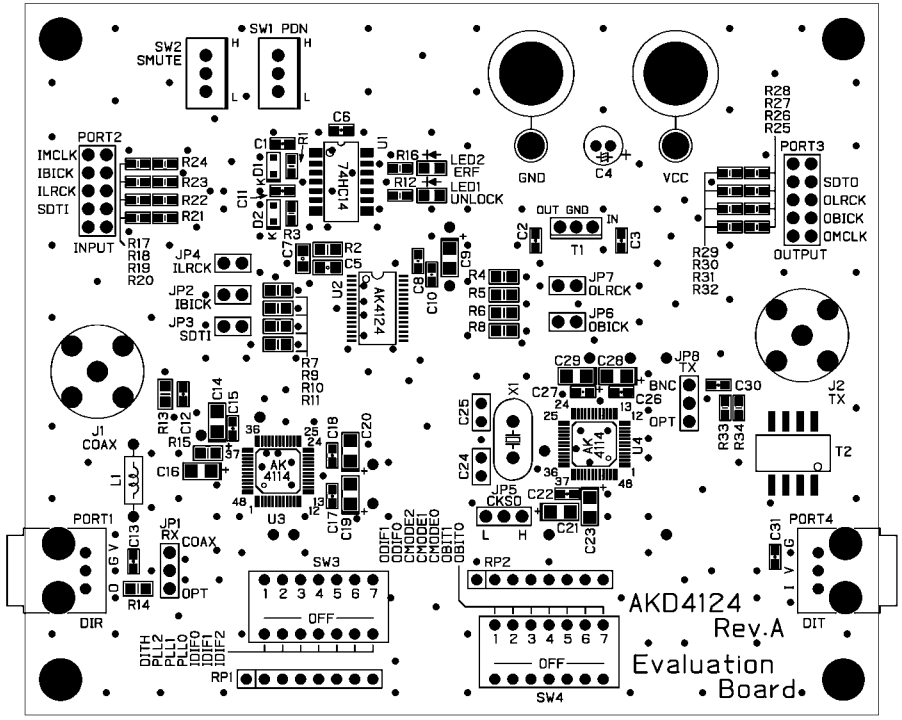
DIF2	DIF1	DIF0	Setting
H	L	L	24bit, MSB justified

OCKS1	OCKS0	Setting
H	H	128fs, 192kHz

CM1	CM0	Setting
L	L	PLL=ON, RX Mode

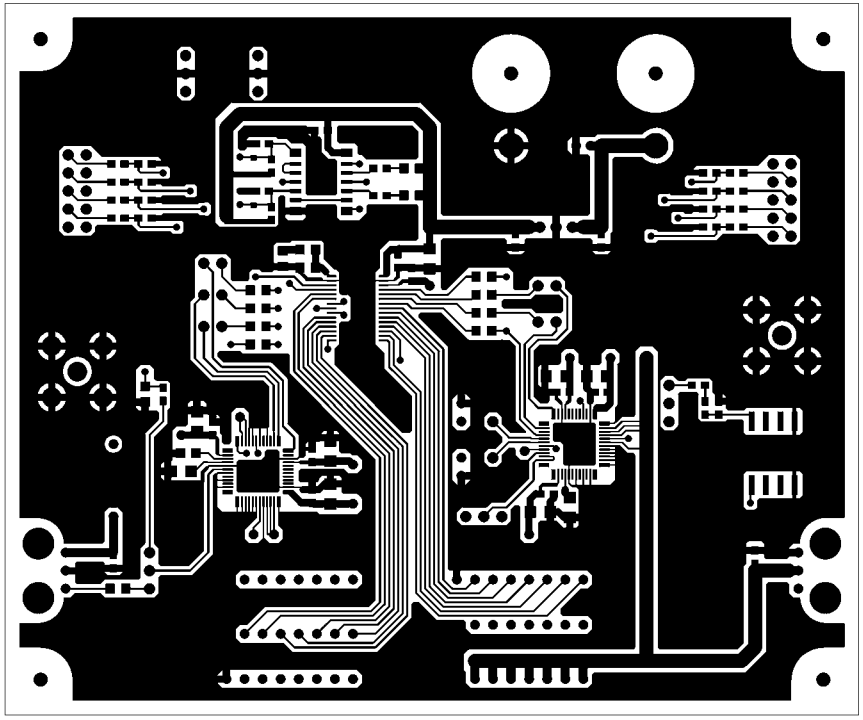
Title	AKD4125-A	
Size A3	Document Number INPUT	Rev 1
Date: Tuesday, April 18, 2006	Sheet 2 of 3	


AK4114
U4
REG
C21 10u
C22 0.1u
C23 0.47u
C24 5p
C25 5p
X1 HC-49/U 11.2896MHz
PDN
JP5 HIF3G-50P-2.54DSA (3x1) CKSO
JP6 HIF3G-50P-2.54DSA (2x1) OBICK
JP7 HIF3G-50P-2.54DSA (2x1) OLRCK
JP8 HIF3G-50P-2.54DSA (3x1) TX
OMCLK
OBICK
OLRCK
SDTO
R25 100
R26 100
R27 100
R28 100
R29 220k
R30 220k
R31 220k
R32 220k
PORT3 A1-10PA-2.54DSA
OUTPUT
C26 0.1u
C27 0.1u
C28 10u
C29 10u
C30 0.1u
C31 0.1u
R33 240
R34 150
T2 DA-02F
1:1
J2 BNC-R-PC
TX(BNC)
PORT4 TOTX141
TX(OPT)
OPT
BNC
DIF2 DIF1 DIF0 Setting
H L L 24bit, MSB justified
OCKS1 OCKS0 Setting
L L 256fs, 96kHz
H H 128fs, 192kHz
CM1 CM0 Setting
L H PLL=OFF, X'tal Mode
Title AKD4125-A
Size A3
Document Number OUTPUT
Rev 1
Date: Tuesday, April 18, 2006
Sheet 3 of 3



AKD4124 Rev.A L1 SR SILK

AKD4124 Rev.A L2 SR



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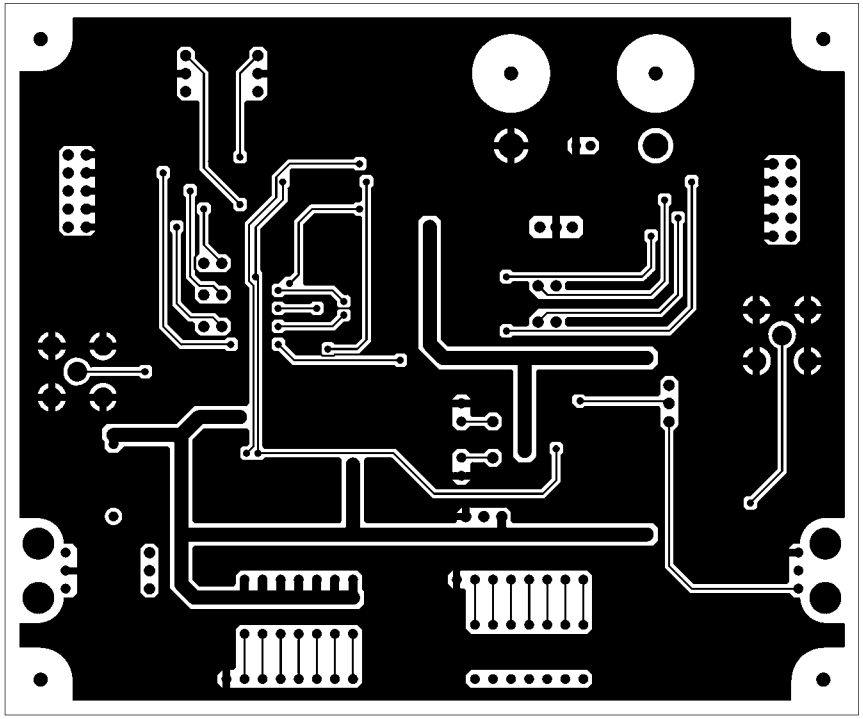

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