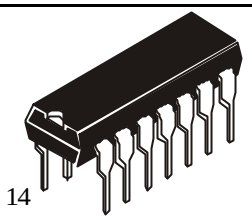
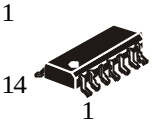
IN74LV74

Dual D-type flip-flop with set and reset; positive-edge trigger



N SUFFIX
PLASTIC



D SUFFIX
SOIC

ORDERING INFORMATION

IN74LV74N	Plastic DIP
IN74LV74D	SOIC
IZ74LV74	chip

T_A = -40° to 125° C for all packages

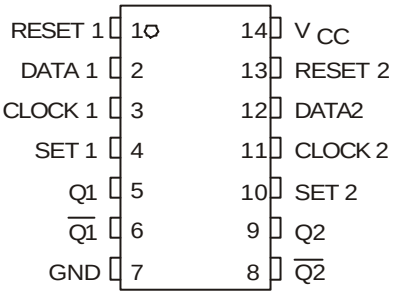
The IN74LV74 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT74.

The IN74LV74 is a dual positive edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set (S_D) and (R_D) inputs; also complementary Q and $\overline{Q}$ outputs.

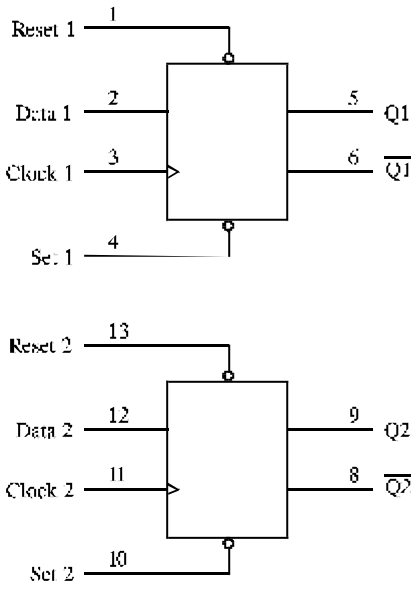
The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition, for predictable operation. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 1.2 to 3.6 V
- Low input current: 1.0 µÀ; 0.1 µÀ at Ò = 25 °Ñ
- High Noise Immunity Characteristic of CMOS Devices

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

FUNCTION TABLE

Inputs				Outputs	
Set	Reset	Clock	Data	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

H= high level L = low level
X = don't care Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.5 to +5.0	V
I_{IK} *1	Input diode current	±20	mA
I_{OK} *2	Output diode current	±50	mA
I_O *3	Output source or sink current	±35	mA
I_{CC}	V_{CC} current	±70	mA
I_{GND}	GND current	±70	mA
P_D	Power dissipation per package: Plastic DIP *4 SO *4	 750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
*1 $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V.
*2 $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V.
*3 -0.5 V $< V_O < V_{CC} + 0.5$ V.
*4 Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C
SO Package: - 8 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		1.2	3.6	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-40	+125	°C
t_r, t_f	Input Rise and Fall Time except for Schmitt-trigger inputs (Figure 1)	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0 0 0 0	1000 700 500 400	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage		1.2 2.0 3.0 3.6	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	0.9 1.4 2.1 2.5	- - - -	V
V_{IL}	LOW level output voltage		1.2 2.0 3.0 3.6	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	- - - -	0.3 0.6 0.9 1.1	V
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -50 µÀ	1.2 2.0 3.0 3.6	1.1 1.92 2.92 3.52	- - - -	1.0 1.9 2.9 3.5	- - - -	1.0 1.9 2.9 3.5	- - - -	V
		$V_I = V_{IH}$ or V_{IL} I_O = -6mÀ	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 50 µÀ	1.2 2.0 3.0 3.6	- - - -	0.09 0.09 0.09 0.09	- - - -	0.1 0.1 0.1 0.1	- - - -	0.1 0.1 0.1 0.1	V
		$V_I = V_{IH}$ or V_{IL} I_O = 6 mÀ	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	*	-	±0.1	-	±1.0	-	±1.0	µÀ
I_{CC}	Supply current	$V_I = V_{CC}$ or 0 V I_O = 0 µÀ	*	-	4.0	-	40	-	80	µÀ

* V_{CC} = 3.3 ± 0.3 V

AC ELECTRICAL CHARACTERISTICS (C_L=50 pF, t_r=t_f=6.0 ns)

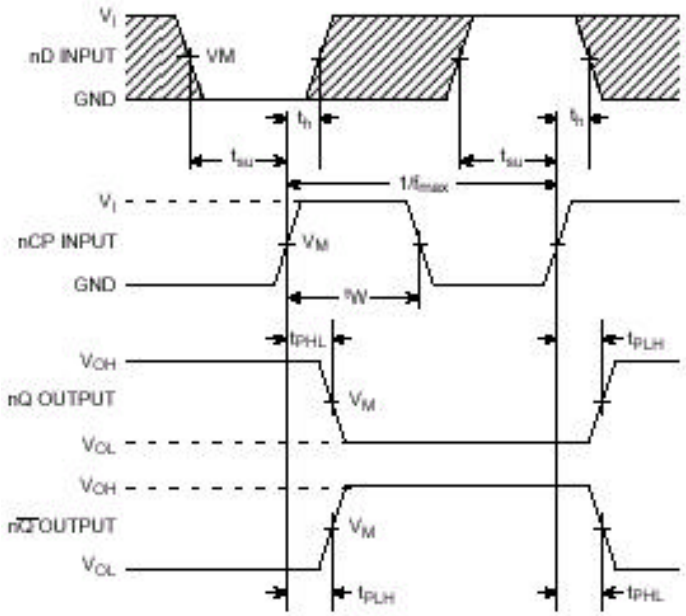
Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH}	Propagation delay , Clock to Q or $\overline{Q}$	V_I = 0 V or V_{CC} Figures 1,3	1.2 2.0 *	- - -	140 45 28	- - -	160 56 35	- - -	180 67 42	ns
t_{PHL}, t_{PLH}	Propagation delay , $\overline{Set}$ to Q or $\overline{Q}$	V_I = 0 V or V_{CC} Figures 2,3	1.2 2.0 *	- - -	150 44 27	- - -	170 54 34	- - -	190 65 41	ns
t_{PHL}, t_{PLH}	Propagation delay , $\overline{Reset}$ to Q or $\overline{Q}$	V_I = 0 V or V_{CC} Figures 2,3	1.2 2.0 *	- - -	160 47 29	- - -	180 58 37	- - -	200 70 44	ns
t_{THL}, t_{TLH}	Output Transition Time, Any Output	V_I = 0 V or V_{CC} Figures 1,3	1.2 2.0 *	- - -	90 20 15	- - -	110 25 19	- - -	130 30 23	ns
C_I	Input capacitance		3.0	-	7.0	-	-	-	-	pF

C_{PD}	Power dissipation capacitance (per flip-flop)	V_I = 0 V or V_{CC}		-	48	-	-	-	-	pF

TIMING REQUIREMENTS (C_L=50 pF, t_r=t_f=6.0 ns)

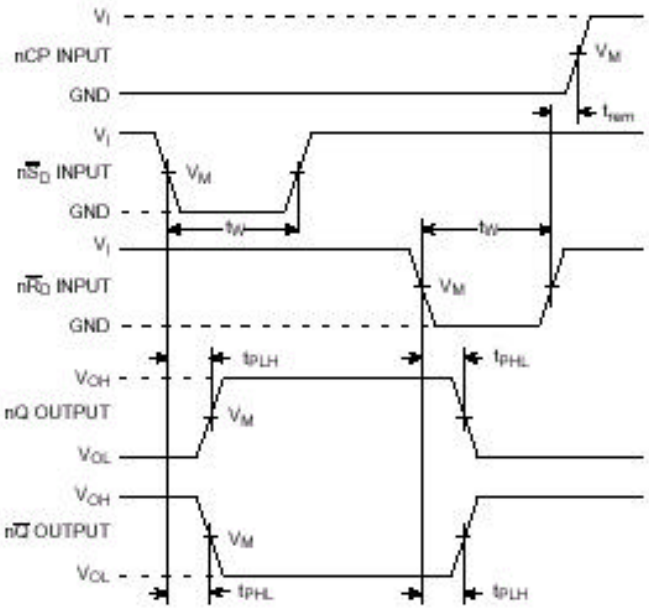
Symbol	Parameter	Test conditions	V_{CC} V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_w	Pulse Width, Clock, Set or Reset	V_I = 0 V or V_{CC} Figures 1,2,3	1.2	75	-	96	-	114	-	ns
			2.0	25	-	32	-	38	-	
			*	16	-	20	-	24	-	
t_{su}	Setup Time, Data to Clock	V_I = 0 V or V_{CC} Figures 1,3	1.2	25	-	32	-	40	-	ns
			2.0	16	-	20	-	24	-	
			*	10	-	13	-	15	-	
t_{rem}	Removal Time, Set or Reset to Clock	V_I = 0 V or V_{CC} Figures 2,3	1.2	18	-	24	-	30	-	ns
			2.0	9	-	12	-	15	-	
			*	6	-	8	-	9	-	
t_h	Hold Time, Clock to Data	V_I = 0 V or V_{CC} Figures 1,3	1.2	3	-	5	-	5	-	ns
			2.0	3	-	3	-	3	-	
			*	3	-	3	-	3	-	
f_c	Clock Frequency	V_I = 0 V or V_{CC} Figures 1,3	1.2	8	-	6	-	4	-	MHz
			2.0	18	-	15	-	12	-	
			3.0	30	-	24	-	20	-	

* V_{CC} = 3.3 ± 0.3 V



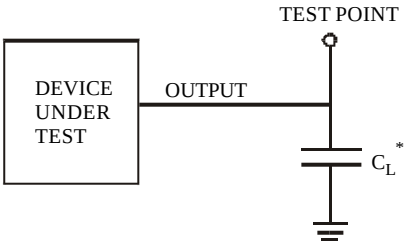
V_M = 0.5 * V_{CC}
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Figure 1. Switching Waveforms



$V_M = 0.5 * V_{CC}$

Figure 2. Switching Waveforms

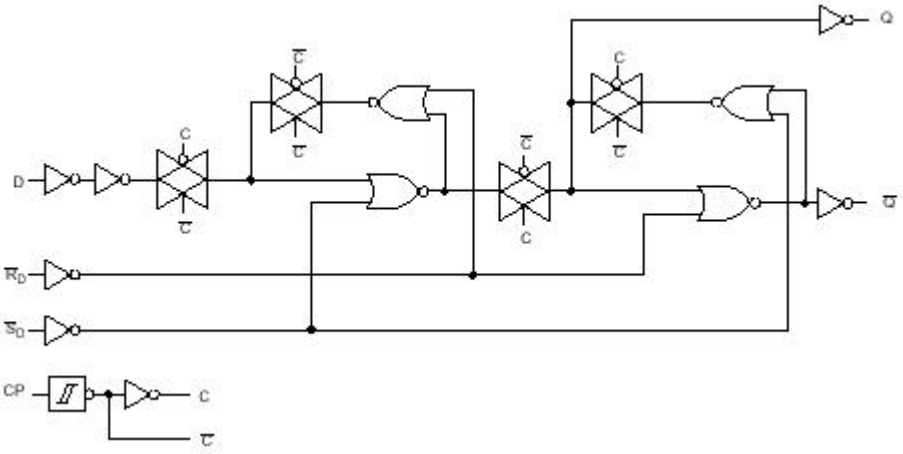


* Includes all probe and jig capacitance

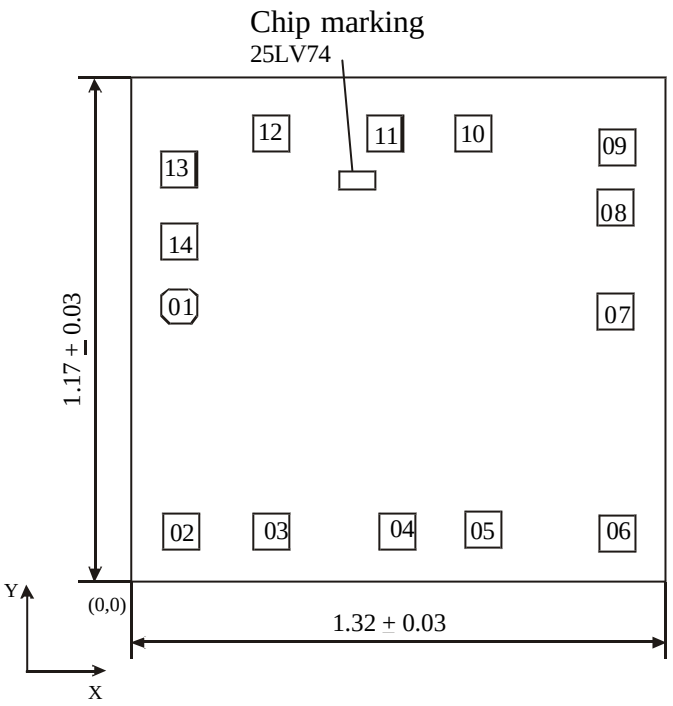
Figure 3. Test Circuit

EXPANDED LOGIC DIAGRAM

(ONE FLIP-FLOP)



CHIP PAD DIAGRAM



Location of marking (mm): left lower corner x=0.520, y=0.865.

Chip thickness: 0.46 ± 0.02 mm.

PAD LOCATION

Pad No	Symbol	Location (left lower corner), mm		Pad size, mm
		X	Y	
01	Reset 1	0.118	0.436	0.108 x 0.108
02	Data 1	0.118	0.125	0.108 x 0.108
03	Clock 1	0.286	0.125	0.108 x 0.108
04	Set 1	0.597	0.125	0.108 x 0.108
05	$\overline{Q}$ 1	0.895	0.125	0.108 x 0.108
06	Q 1	1.100	0.125	0.108 x 0.108
07	GND	1.100	0.423	0.108 x 0.108
08	$\overline{Q}$ 2	1.100	0.721	0.108 x 0.108
09	Q 2	1.100	0.930	0.108 x 0.108
10	Set 2	0.851	0.949	0.108 x 0.108
11	Clock 2	0.540	0.949	0.108 x 0.108
12	Data 2	0.297	0.949	0.108 x 0.108
13	Reset 2	0.118	0.830	0.108 x 0.108
14	V_{CC}	0.118	0.604	0.108 x 0.108

Note: Pad location is given as per metallization layer