

1x, 4x, 128x, and 256x Clock Multiplier with Internal LCO

Features

- ◆ Clock Multiplier / Jitter Reduction
 - Generates a Low Jitter 6 - 75 MHz Clock from a Jittery 23 kHz to 30 MHz Clock Source
- ◆ Internal LCO Reference Clock
- ◆ 128 Hz Loop Filter Bandwidth
- ◆ Selectable Multiplication Factors
 - 1x, 4x, 128x, and 256x
- ◆ Selectable Aux Output Pin
- ◆ Minimal Board Space Required
 - No External Analog Loop-filter Components

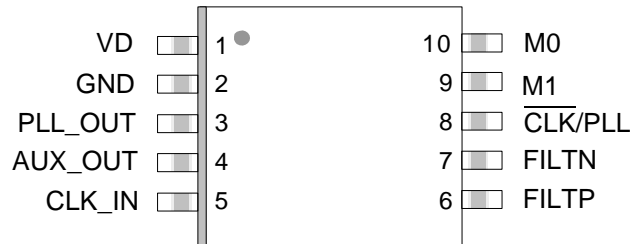
General Description

The CS2300-03 is an extremely versatile system clocking device that utilizes a programmable phase lock loop. The CS2300-03 is based on a hybrid analog-digital PLL architecture comprised of a unique combination of a Delta-Sigma Fractional-N Frequency Synthesizer and a Digital PLL. This architecture allows for generation of a low-jitter clock relative to an external noisy synchronization clock with frequencies as low as 23 kHz. The CS2300-03 is a CS2300-OTP device that has been pre-configured at the factory. There are three hardware configuration pins available for mode and feature selection.

Ordering Information

The CS2300-03 is available in a 10-pin MSOP package in Commercial (-10°C to +70°C) grade. Customer development kits are also available for custom device prototyping and device evaluation. Please see “[Ordering Information](#)” on page 2 for complete details.

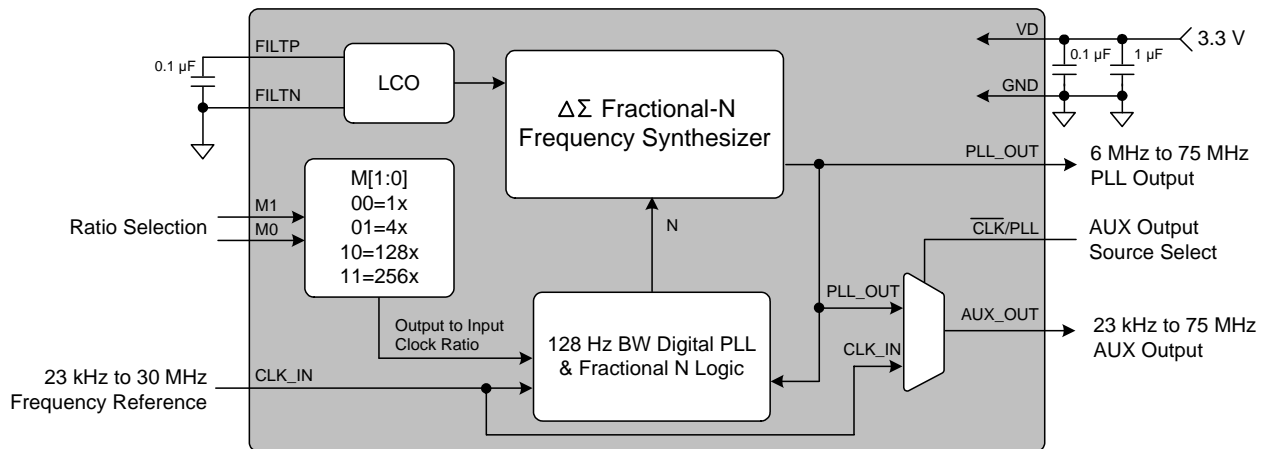
Pin-Out Diagram



Hardware Controls Settings

M1	M0	PLL_OUT
0	0	1x CLK_IN
0	1	4x CLK_IN
1	0	128x CLK_IN
1	1	256x CLK_IN

CLK/PLL	AUX_OUT Source
0	CLK_IN
1	PLL_OUT



1. PIN DESCRIPTIONS

Pin Name	#	Pin Description
VD	1	Digital Power
GND	2	Ground
PLL_OUT	3	PLL Clock Output
AUX_OUT	4	AUX Output
CLK_IN	5	Clock Input
FILTP	6	LCO Filter Connections
FILTN	7	
CLK/PLL	8	AUX Output Source Selection Input
M1	9	Mode Selection Inputs
M0	10	

See the CS2300-OTP datasheet for additional pin description information.

2. SPECIFICATIONS

Please see the CS2300-OTP datasheet for package information, device characteristics, and specifications except where noted due to specific programming options.

3. OPERATIONAL INFORMATION

Complete operational information can be found in the CS2300-OTP datasheet. Specific operational details dictated by the programming of the CS2300-03 are included below.

- The PLL clock output is forced to 0 when the PLL is unlocked, both upon loss of the CLK_IN signal or briefly when switching mode pin configurations.
- The minimum loop filter bandwidth once locked is 128 Hz.

4. CONFIGURATION INFORMATION

The CS2300-03 has been factory pre-programmed with a unique configuration. The following table outlines the specific configuration profile which can be compared to the CS2300-OTP datasheet for detailed functional descriptions.

<i>OTP Modal and Global Configuration Parameters Form</i>							
	Mode 0		Mode 1		Mode 2		Mode 3
Ratio 0 (dec)	1		4		128		256
Ratio 0 (hex)	00:10:00:00		00:40:00:00		08:00:00:00		10:00:00:00
RModSel1	0		0		0		0
RModSel0	0		0		0		0
AuxOutSrc1	0		0		0		0
AuxOutSrc0	1		1		1		1
AutoRMod	0		0		0		0
Global Configuration Set							
ClkSkipEn	AuxLockCfg	ClkOutUnl	LFRatioCfg	M2Cfg2	M2Cfg1	M2Cfg0	
0	0	0	1	1	1	1	
ClkIn_BW2	ClkIn_BW1	ClkIn_BW0					
1	1	1					

5. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS2300-03	Clocking Device	10L-MSOP	Yes	Commercial	-10° to +70°C	Rail	CS230003-CZZ
						Tape and Reel	CS230003-CZZR
CDK-2000	Evaluation Platform	-	Yes	-	-	-	CDK-2000-LCO

6. REVISION HISTORY

Release	Changes
A1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.

IMPORTANT NOTICE

"Advance" product information describes products that are in development and subject to development changes. Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.