256-Kbit (32K x 8) nvSRAM

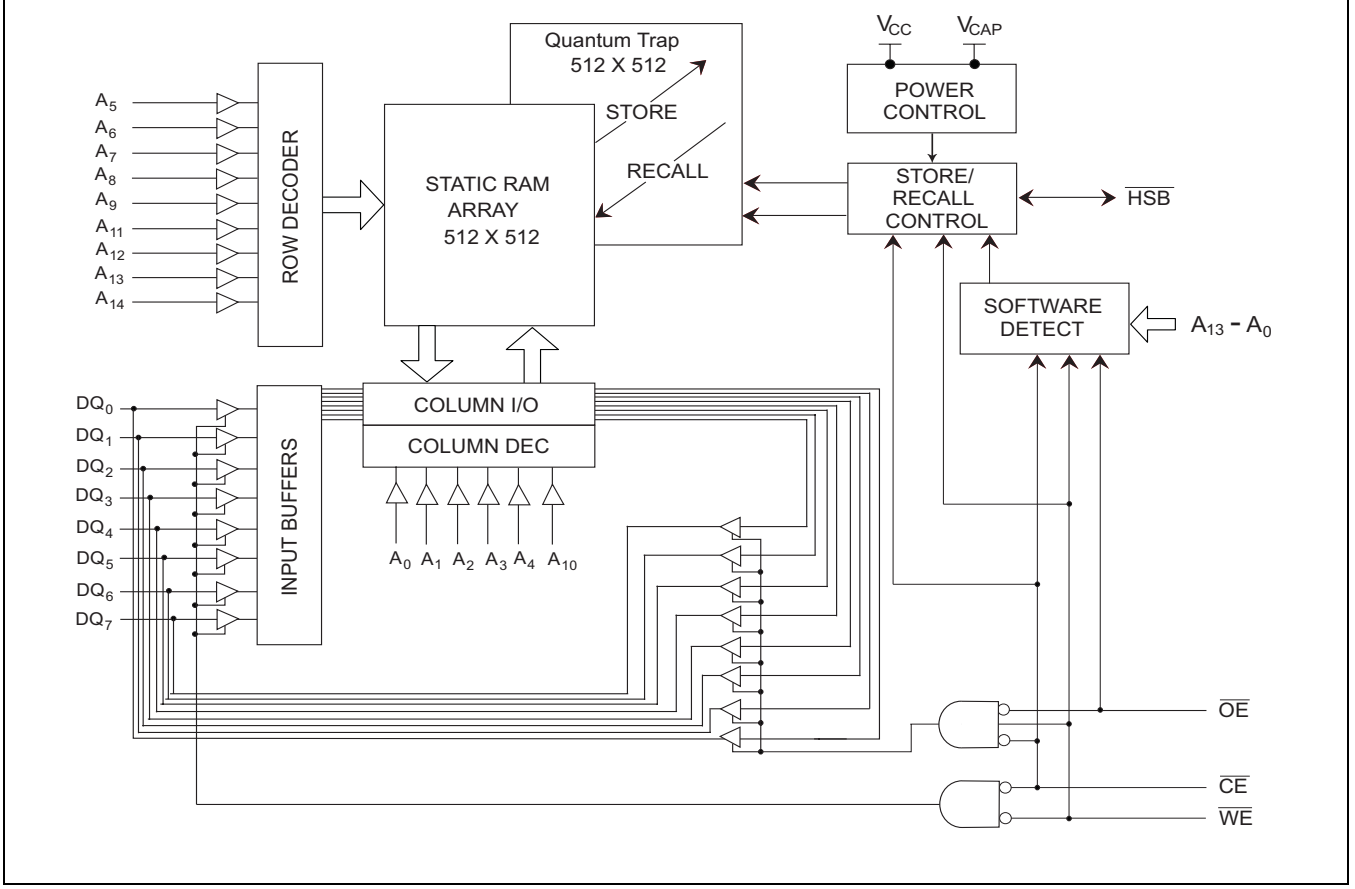
Features

- **25 ns and 45 ns Access Times**
- **"Hands-off" Automatic *STORE* on Power Down with external 68µF capacitor**
- ***STORE* to QuantumTrap® Nonvolatile Elements is initiated by Software, Hardware or Autostore® on Power-down**
- ***RECALL* to SRAM Initiated by Software or Power-up**
- **Infinite *READ, WRITE* and *RECALL* Cycles**
- **15 mA Typical I_{CC} at 200 ns Cycle Time**
- **1,000,000 *STORE* Cycles to QuantumTrap**
- **100-Year Data Retention to QuantumTrap**
- **Single 5V Operation ±10%**
- **Commercial Temperature**
- **SOIC Package**
- **RoHS Compliance**

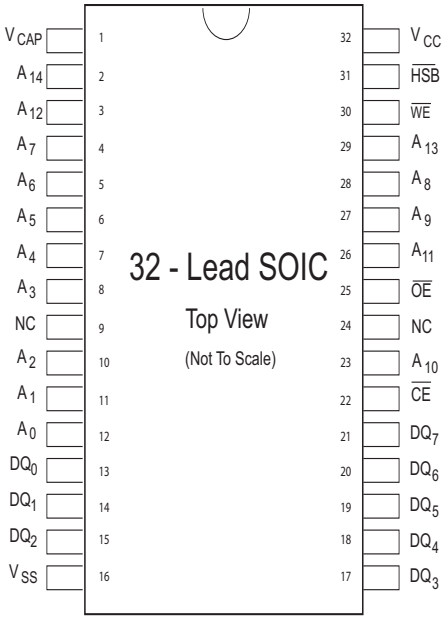
Functional Description

The Cypress CY14E256L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides Infinite read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control. A hardware STORE may be initiated with HSB pin.

Logic Block Diagram



Pin Configurations



Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{14}	Input	**Address Inputs used to select one of the 32,768 bytes of the nvSRAM**.
DQ0-DQ7	Input/Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable Input, active LOW**. When selected LOW, enables data on the I/O pins to be written to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable Input, active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting $\overline{OE}$ HIGH causes the I/O pins to tri-state.
V_{SS}	Ground	**Ground for the device**. Should be connected to ground of the system.
V_{CC}	Power Supply	**Power Supply inputs to the device**.
$\overline{HSB}$	Input/Output	**Hardware Store Busy**. When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull-up resistor keeps this pin high if not connected. (Connection Optional)
V_{CAP}	Power Supply	**Autostore® Capacitor**. Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	**No Connects**. This pin is not connected to the die.

Device Operation

The CY14E256L nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14E256L supports Infinite reads and writes just like a typical SRAM. In addition, it provides Infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations.

SRAM Read

The CY14E256L performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are low while $\overline{WE}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AA} (READ cycle #1). If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs will be valid at t_{ACE} or at t_{DOE}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AA} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought high, or $\overline{WE}$ or $\overline{HSB}$ is brought low.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes high at the end of the cycle. The data on the common I/O pins I/O_{0-7} will be written into the memory if it is valid t_{SD} before the end of a $\overline{WE}$ controlled WRITE or before the end of an $\overline{CE}$ controlled WRITE. It is recommended that $\overline{OE}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{OE}$ is left low, internal circuitry will turn off the output buffers t_{HZWE} after $\overline{WE}$ goes low.

AutoStore Operation

The CY14E256L stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by $\overline{HSB}$, Software Store, activated by an address sequence, and AutoStore, on device power down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14E256L.

During normal operation, the device will draw current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CC}. A STORE operation will be initiated with power provided by the V_{CAP} capacitor.

Figure 1 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to the DC Characteristics table for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to 5V by a charge pump internal to the chip. A pull-up should be placed on $\overline{WE}$ to hold it inactive during power-up.

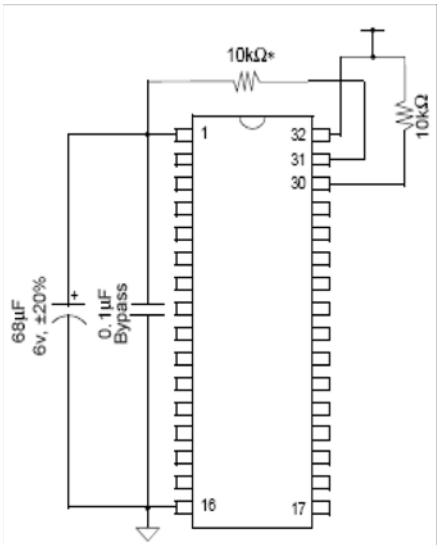


Figure 1. AutoStore® Mode

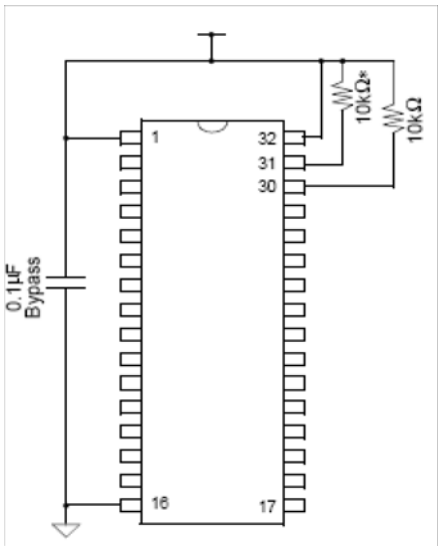


Figure 2. System Power Mode

In system power mode (*Figure 2*), both V_{CC} and V_{CAP} are connected to the +5V power supply without the 68-µF capacitor. In this mode the AutoStore function of the CY14E256L will operate on the stored system charge as power goes down. The user must, however, guarantee that V_{CC} does not drop below 3.6V during the 10-ms STORE cycle.

If an automatic STORE on power loss is not required, then V_{CC} can be tied to ground and + 5V applied to V_{CAP} (*Figure 3*). This is the AutoStore Inhibit mode, in which the AutoStore function is disabled. If the CY14E256L is operated in this configuration, references to V_{CC} should be changed to V_{CAP} throughout this data sheet. In this mode, STORE operations may be triggered through software control or the HSB pin. It is not permissible to change between these three options “on the fly”.

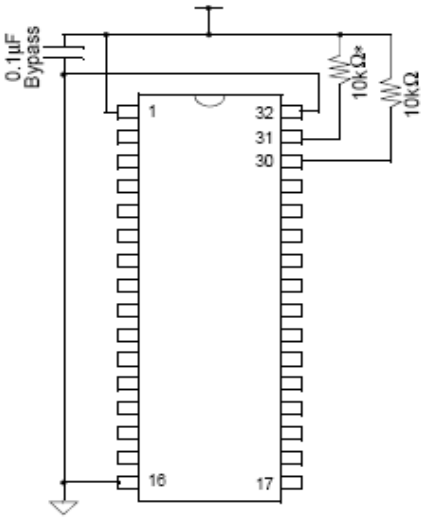


Figure 3. AutoStore Inhibit Mode

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The HSB signal can be monitored by the system to detect an AutoStore cycle is in progress. (In the above *Figures 1*, *2* and *3* * indicates that If HSB is not used, it should be left unconnected.)

Hardware STORE ($\overline{HSB}$) Operation

The CY14E256L provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin can be used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the CY14E256L will conditionally initiate a STORE operation after t_{DELAY}. An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open-drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low by any means are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the CY14E256L will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after $\overline{HSB}$ goes low will be inhibited until $\overline{HSB}$ returns high.

The $\overline{HSB}$ pin can be used to synchronize multiple CY14E256L while using a single larger capacitor. To operate in this mode the $\overline{HSB}$ pin should be connected together to the $\overline{HSB}$ pins from the other CY14E256L. An external pull-up resistor to +5V is required since $\overline{HSB}$ acts as an open-drain pull-down. The V_{CAP} pins from the other CY14E256L parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the CY14E256L detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a STORE cycle (a STORE will take place in those CY14E256L that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the CY14E256L will continue to drive the $\overline{HSB}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14E256L will remain disabled until the $\overline{HSB}$ pin returns high.

If $\overline{HSB}$ is not used, it should be left unconnected.

Hardware RECALL (Power-up)

During power-up, or after any low-power condition (V_{CC} < V_{SWITCH}), an internal RECALL request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{HRECALL}$ to complete.

If the CY14E256L is in a WRITE state at the end of power-up RECALL, the SRAM data will be corrupted. To help avoid this situation, a 10-Kohm resistor should be connected either between $\overline{WE}$ and system V_{CC} or between $\overline{CE}$ and system V_{CC}.

Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14E256L software STORE cycle is initiated by executing sequential $\overline{CE}$-controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0FC0, Initiate STORE cycle

The software sequence may be clocked with $\overline{CE}$-controlled READs or $\overline{OE}$-controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{OE}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

Software RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of $\overline{CE}$-controlled READ operations must be performed:

1. Read address 0x0E38, Valid READ
2. Read address 0x31C7, Valid READ
3. Read address 0x03E0, Valid READ
4. Read address 0x3C1F, Valid READ
5. Read address 0x303F, Valid READ
6. Read address 0x0C63, Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

Data Protection

The CY14E256L protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when $V_{CC} < V_{SWITCH}$. If the CY14E256L is in a WRITE mode (both $\overline{CE}$ and $\overline{WE}$ low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on $\overline{CE}$ or $\overline{WE}$ is detected. This protects against inadvertent writes during power-up or brown-out conditions.

Noise Considerations

The CY14E256L is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground, and signals will reduce circuit noise.

Low Average Active Power

CMOS technology provides the CY14E256L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. *Figure 4* shows the relationship between

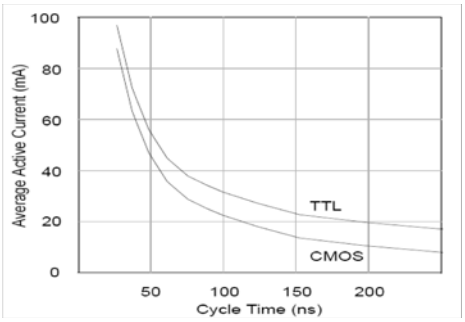


Figure 4. Current vs. Cycle Time (READ)

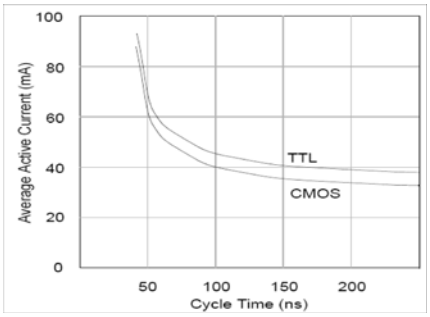


Figure 5. Current vs. Cycle Time (WRITE)

I_{CC} and READ/WRITE cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, VCC = 5.5V, 100% duty cycle on chip enable).Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14E256L depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITEs.
4. CMOS vs. TTL Input Levels.
5. The operating temperature.
6. The V_{CC} level.
7. I/O loading.

Preventing STOREs

The STORE function can be disabled on the fly by holding $\overline{HSB}$ high with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2V, as it will have to overpower the internal pull-down device that drives $\overline{HSB}$ low for 20 µs at the onset of a STORE. When the CY14E256L is connected for AutoStore operation (system V_{CC} connected to V_{CC} and a 68-µF capacitor on V_{CAP}) and V_{CC} crosses V_{SWITCH} on the way down, the CY14E256L will attempt to pull $\overline{HSB}$ low; if $\overline{HSB}$ doesn't actually get below V_{IL},the part will stop trying to pull $\overline{HSB}$ low and abort the STORE attempt.

Table 1. Hardware Mode Selection

$\overline{CE}$	$\overline{WE}$	$\overline{HSB}$	A13–A0	Mode	I/O	Power
H	X	H	X	Not Selected	Output High-Z	Standby
L	H	H	X	Read SRAM	Output Data	Active
L	L	H	X	Write SRAM	Input Data	Active
X	X	L	X	Nonvolatile STORE	Output High-Z	I_{CC2}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND..... –0.5V to 7.0V

Voltage Applied to Outputs in High-Z State ..... –0.5V to V_{CC} + 0.5V

Input Voltage ..... –0.5V to Vcc+0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Lead Soldering Temperature (3 Seconds) ..... +260°C

Output Short Circuit Current [1] ..... 15 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	4.5V to 5.5V

DC Electrical Characteristics Over the Operating Range (V_{CC} = 4.5V to 5.5V) [2]

Parameter	Description	Test Conditions		Min.	Max.	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 25 ns t_{RC} = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I_{OUT} = 0mA.	Commercial		97 70	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			3	mA
I_{CC3}	Average V_{CC} Current at t_{AVAV} = 200 ns, 5V, 25°C typical	$\overline{WE}$ > (V_{CC} – 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads.			15	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care, V_{CC} = Max. Average current for duration t_{STORE}			2	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE}$ > (V_{CC} – 0.2). All others V_{IN} < 0.2V or > (V_{CC} – 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0MHz.			1.5	mA
I_{IX}	Input Leakage Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$		-1	+1	µA
I_{OZ}	Off-State Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{IN} \le V_{CC}$, $\overline{CE}$ or $\overline{OE}$ > V_{IH}		-5	+5	µA
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V

Capacitance [3]

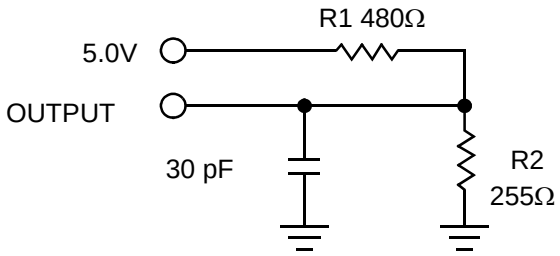
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. Outputs shorted for no more than one second. No more than one output shorted at a time.
2. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and V_{CC} = 5V. Not 100% tested.
3. These parameters are guaranteed but not tested.

Thermal Resistance [3]

Parameter	Description	Test Conditions	32-SOIC	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

AC Test Loads



AC Test Conditions

Input Pulse Levels ..... 0 V to 3 V
Input Rise and Fall Times (10% - 90%) ..... ≤5 ns
Input and Output Timing Reference Levels ..... 1.5 V

AC Switching Characteristics

Parameter		Description	25ns part		45ns part		Unit
Cypress Parameter	Alt. Parameter		Min.	Max.	Min.	Max.	
SRAM Read Cycle							
t_{ACE}	t_{ACS}	Chip Enable Access Time		25		45	ns
t_{RC} [4]	t_{RC}	Read Cycle Time	25		45		ns
t_{AA} [5]	t_{AA}	Address Access Time		25		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		10		20	ns
t_{OHA} [5]	t_{OH}	Output Hold After Address Change	5		5		ns
t_{LZCE} [6]	t_{LZ}	Chip Enable to Output Active	5		5		ns
t_{HZCE} [6]	t_{HZ}	Chip Disable to Output Inactive		10		15	ns
t_{LZOE} [6]	t_{OLZ}	Output Enable to Output Active	0		0		ns
t_{HZOE} [6]	t_{OHZ}	Output Disable to Output Inactive		10		15	ns
t_{PU} [3]	t_{PA}	Chip Enable to Power Active	0		0		ns
t_{PD} [3]	t_{PS}	Chip Disable to Power Standby		25		45	ns
SRAM Write Cycle							
t_{WC}	t_{WC}	Write Cycle Time	25		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	20		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	20		30		ns
t_{SD}	t_{DW}	Data Set-Up to End of Write	10		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		ns
t_{AW}	t_{AW}	Address Set-Up to End of Write	20		30		ns
t_{SA}	t_{AS}	Address Set-Up to Start of Write	0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		ns
t_{HZWE} [6,7]	t_{WZ}	Write Enable to Output Disable		10		14	ns
t_{LZWE} [6]	t_{OW}	Output Active after End of Write	5		5		ns

AutoStore/Power-Up RECALL

Parameter	Description	CY14E256L		Unit
		Min.	Max.	
$t_{HRECALL}$ [8]	Power-Up RECALL Duration		550	µs
t_{STORE} [9]	STORE Cycle Duration		10	ms
V_{SWITCH}	Low Voltage Trigger Level	4.0	4.5	V
$t_{VCCRISE}$	V_{CC} Rise Time	150		µs

Notes:
4. $\overline{WE}$ must be HIGH during SRAM Read Cycles.
5. Device is continuously selected with $\overline{CE}$ and $\overline{OE}$ both Low.
6. Measured ±200mV from steady state output voltage.
7. If $\overline{WE}$ is Low when $\overline{CE}$ goes Low, the outputs remain in the high-impedance state.
8. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
9. If an SRAM Write has not taken place since the last non-volatile cycle, no STORE will take place.

Software Controlled STORE/RECALL Cycle [10,11]

Parameter	Description	25ns part		45ns part		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	STORE/RECALL Initiation Cycle Time	25		45		ns
t_{AS}	Address Set-Up Time	0		0		ns
t_{CW}	Clock Pulse Width	20		30		ns
t_{GLAX}	Address Hold Time	20		20		ns
t_{RECALL}	RECALL Duration		20		20	µs

Hardware STORE Cycle

Parameter	Description	CY14E256L		Unit
		Min	Max	
t_{STORE} [6]	STORE Cycle Duration		10	ms
t_{DELAY} [12]	Time allowed to complete SRAM Cycle	1		µs
$t_{RESTORE}$ [13]	Hardware STORE High to Inhibit Off		700	ns
t_{HLHX}	Hardware STORE Pulse Width	15		ns
t_{HLBL}	Hardware STORE Low to STORE Busy		300	ns

Switching Waveforms

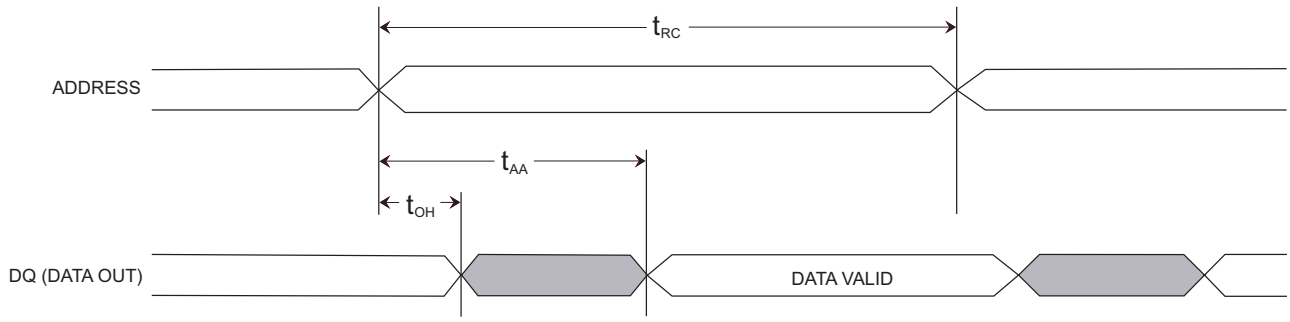


Figure 6. SRAM Read Cycle #1: Address Controlled [4, 5, 14]

Notes:
10. The software sequence is clocked with $\overline{CE}$ controlled READs.
11. The six consecutive addresses must be read in the order listed in the Mode Selection table. $\overline{WE}$ must be HIGH during all six consecutive cycles.
12. Read and Write cycles in progress before $\overline{HSB}$ are given this amount of time to complete.
13. $t_{RESTORE}$ is only applicable after t_{STORE} is complete.
14. $\overline{HSB}$ must remain HIGH during READ and WRITE cycles.

Switching Waveforms (continued)

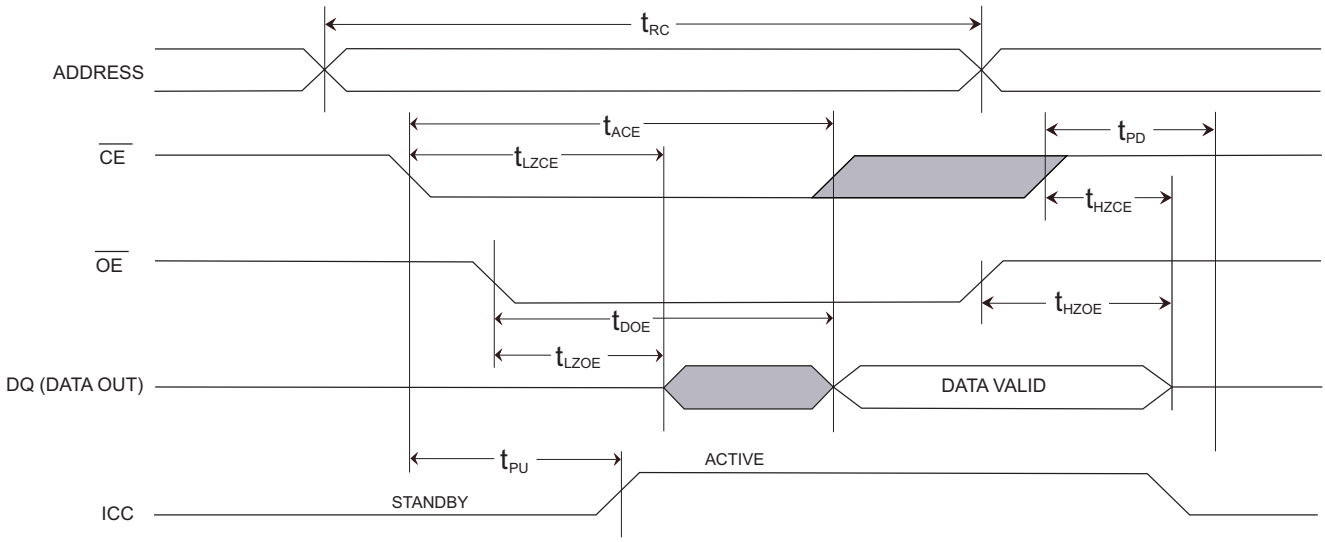


Figure 7. SRAM Read Cycle #2: $\overline{CE}$ Controlled [4,14]

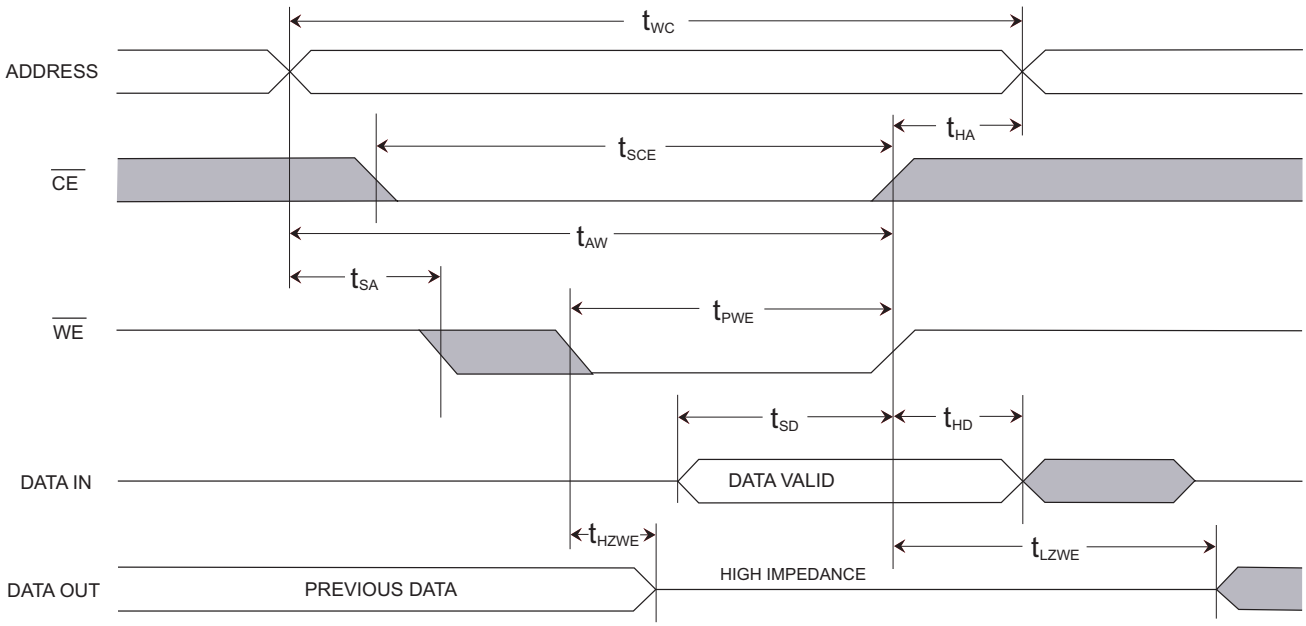


Figure 8. SRAM Write Cycle #1: $\overline{WE}$ Controlled [14,15]

Note:
15. $\overline{CE}$ or $\overline{WE}$ must be > V_{IH} during address transitions.

Switching Waveforms (continued)

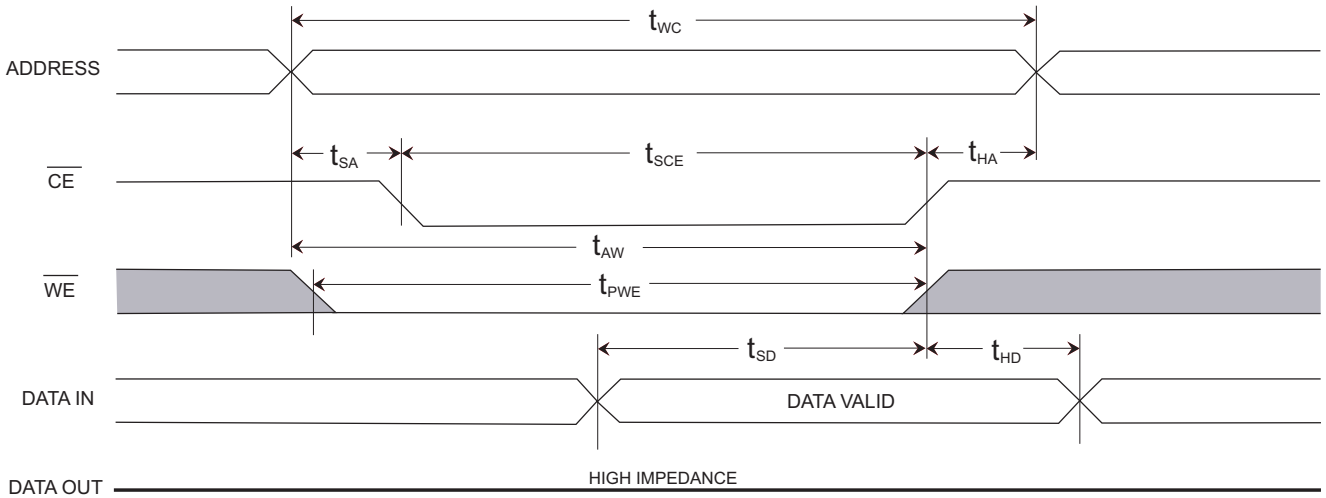


Figure 9. SRAM Write Cycle #2: $\overline{CE}$ Controlled

Switching Waveforms (continued)

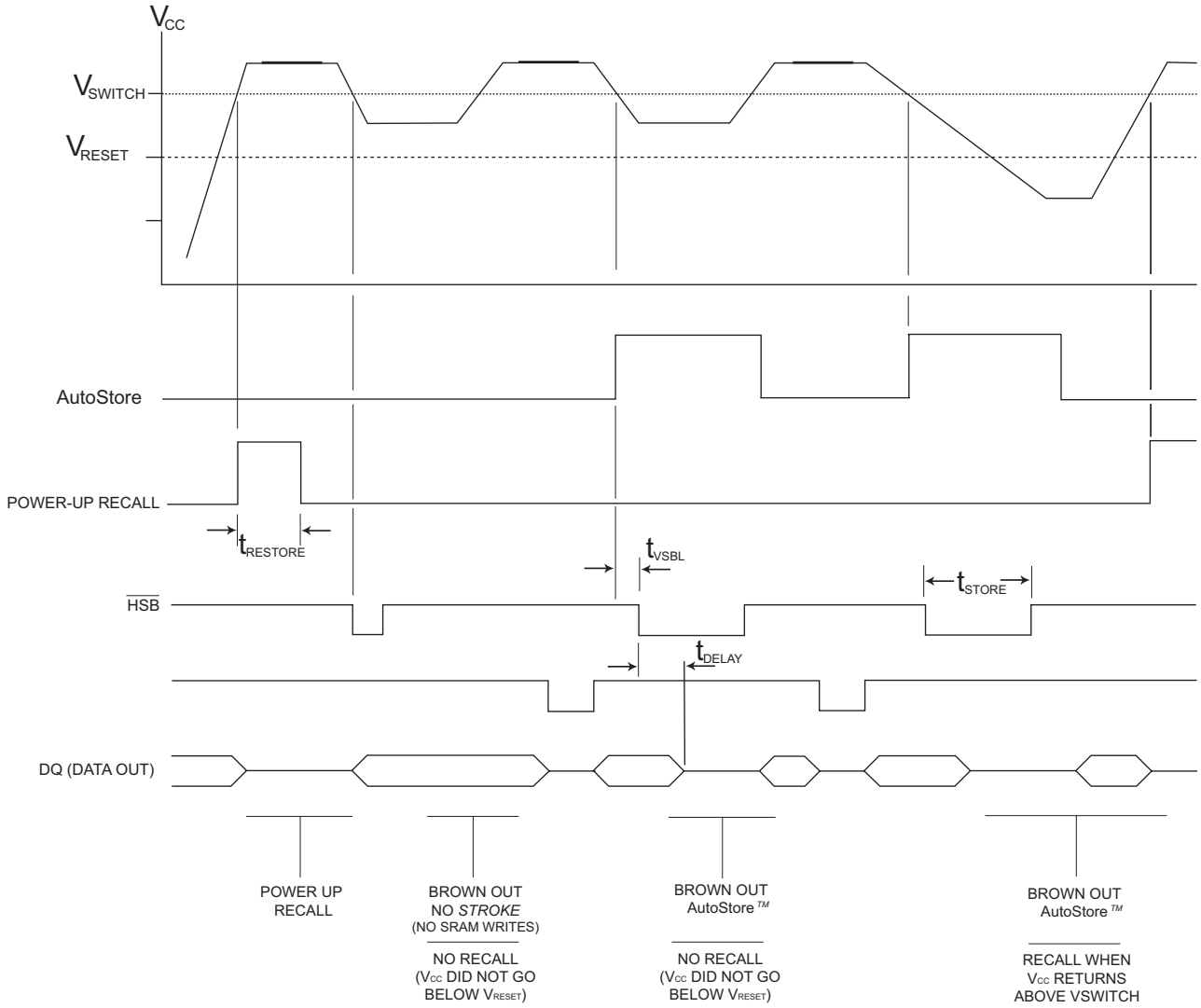


Figure 10. AutoStore/Power-Up RECALL

Switching Waveforms (continued)

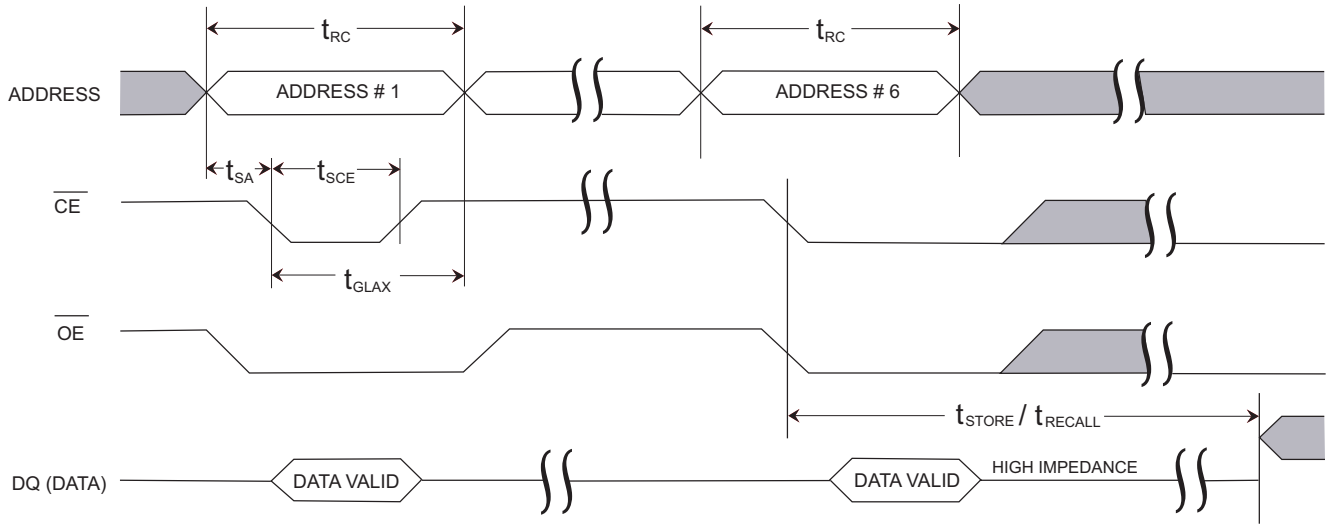


Figure 11. $\overline{CE}$-controlled Software STORE/RECALL Cycle [11]

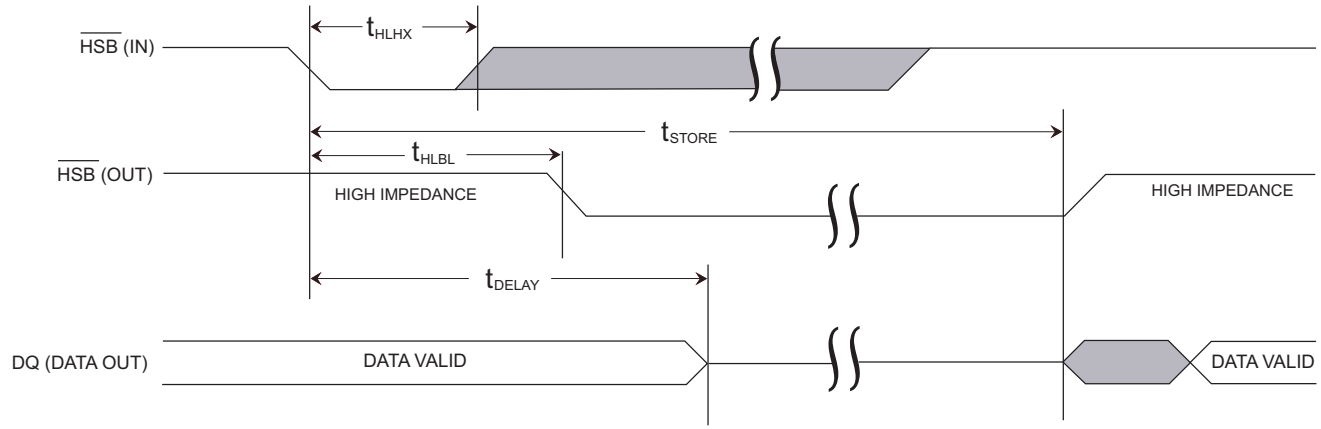
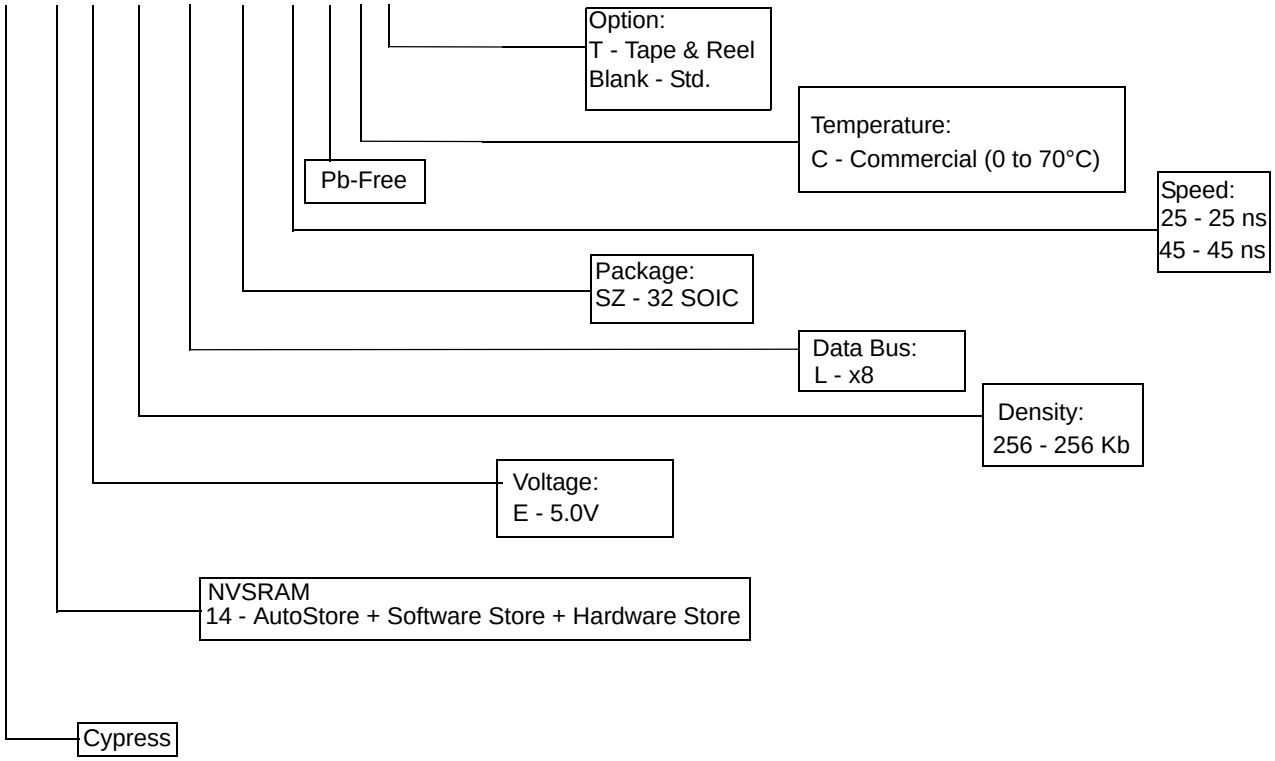


Figure 12. Hardware STORE Cycle

PART NUMBERING NOMENCLATURE

CY 14 E 256 L- SZ 25 X C T

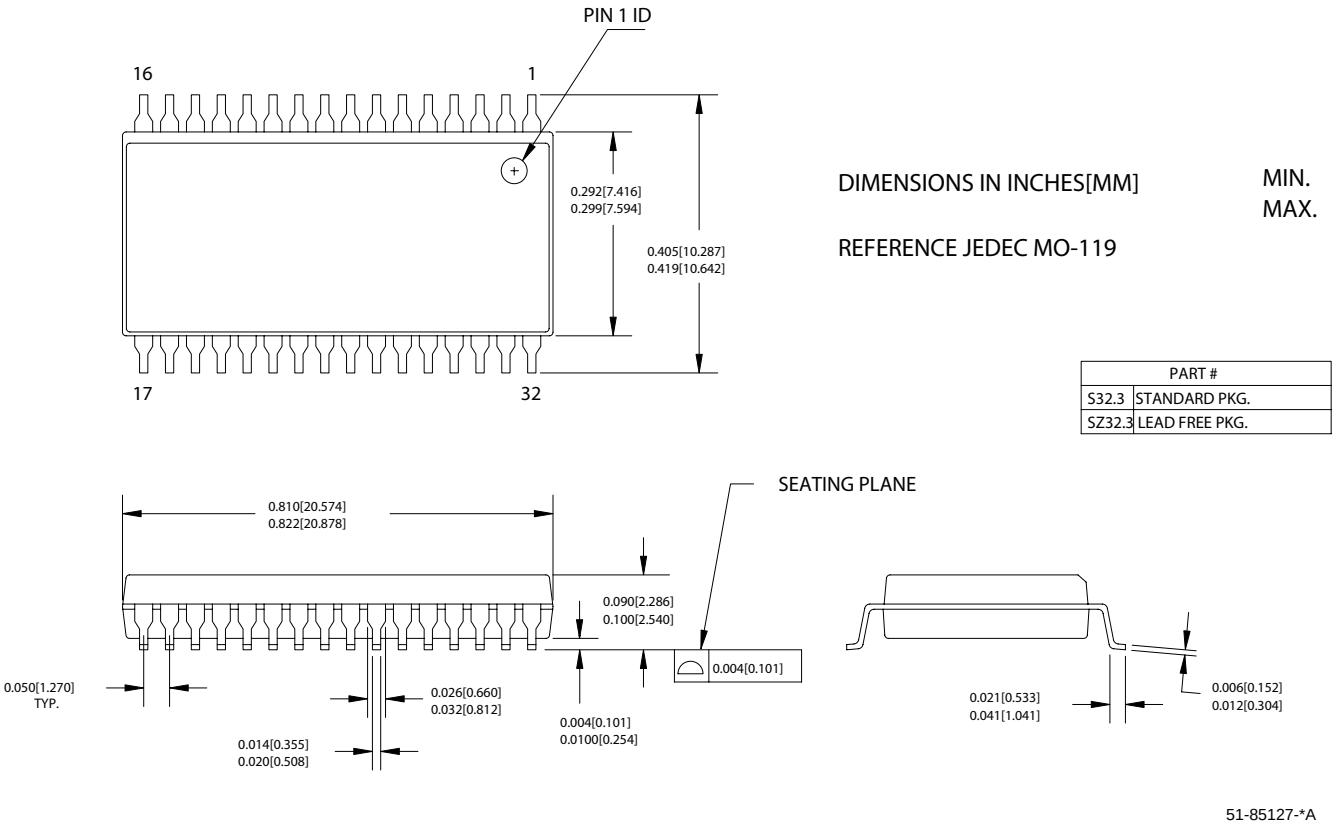


Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14E256L-SZ25XCT	51-85127	32-pin SOIC (Pb-Free)	Commercial
45	CY14E256L-SZ45XCT	51-85127	32-pin SOIC (Pb-Free)	Commercial

Package Diagrams

32-pin (300-Mil) SOIC (51-85127)



Document History Page

Document Title: CY14E256L 256-Kbit (32K x 8) nvSRAM Document Number: 001-06968				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	427789	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on external Web
*B	472053	See ECN	TUP	Updated Part Numbering Nomenclature and Ordering Information
*C	503290	See ECN	PCI	Changed from “Advance” to “Preliminary” Changed the term “Unlimited” to “Infinite” Changed I_{CC3} value from 10mA to 15mA Removed Industrial Grade mention Removed 35ns speed bin Removed Icc1 values from the DC table for 35 ns Industrial Grade Corrected V_{IL} min. spec from (V_{CC} - 0.5) to (V_{SS} - 0.5) Removed all references pertaining to OE controlled “Software STORE and RECALL” operation Changed the address locations of the software STORE/RECALL command Updated “Part Nomenclature Table” and “Ordering InformationTable”