# 10/100 LAN Interface Module with Common Mode Termination

## EPF8001GM

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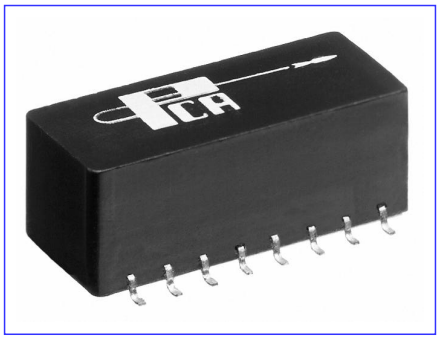


- Optimized for DP83840A/DP83223 Chip Set
- Recommended for use with ICS 1890 Series and SS578Q2120 when connected per appropriate schematic
- Guaranteed to operate with 8 mA DC bias at 70°C
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards

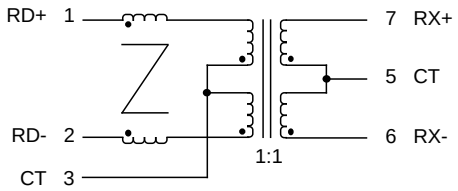
### Electrical Parameters @ 25° C

| **OCL** @ 70°C | **Insertion Loss** (dB Max.) | | | | | | **Return Loss** (dB Min.) | | | | | | **Common Mode Rejection** (dB Min.) | | | | | | **Crosstalk** (dB Min.) [Between Channels] | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 KHz, 0.1 Vrms 8 mA DC Bias | 1-80 MHz | | 80-100 MHz | | 100-150 MHz | | 1-30 MHz | | 30-60 MHz | | 60-100 MHz | | 1-30 MHz | | 100 MHz | | 200 MHz | | 5-10 MHz | 10-100 MHz |
| **Cable Side** | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | Xmit | Rcv | | |
| 350µH | -1 | -1 | -2 | -2 | -3.5 | -3 | -18 | -18 | -12 | -12 | -10 | -10 | -38 | -38 | -35 | -30 | -25 | -25 | -35 | -35 |

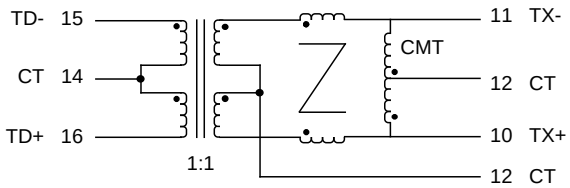
• **Isolation** : 1500 Vrms • **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

### Schematic

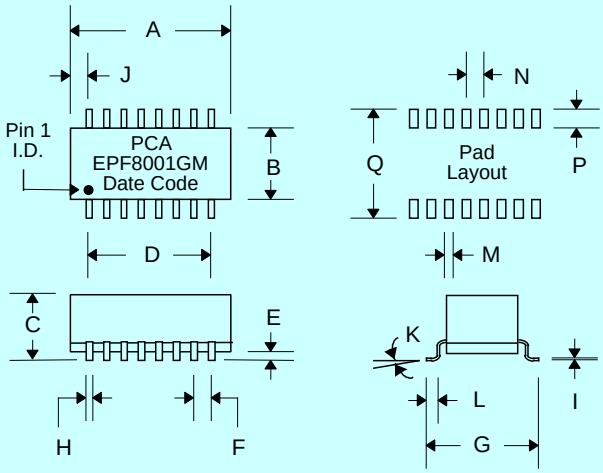
**Receive Channel**




**Transmit Channel**




### Package




### Dimensions

| Dim. | (Inches) Min. | Max. | Nom. | (Millimeters) Min. | Max. | Nom. |
|---|---|---|---|---|---|---|
| A | .880 | .900 | | 22.35 | 22.86 | |
| B | .365 | .385 | | 9.27 | 9.78 | |
| C | .355 | .375 | | 9.02 | 9.52 | |
| D | .700 | Typ. | | 17.78 | Typ. | |
| E | .003 | .020 | | .076 | .508 | |
| F | .100 | Typ. | | 2.54 | Typ. | |
| G | .490 | .510 | | 12.45 | 12.95 | |
| H | .016 | .022 | | .406 | .559 | |
| I | .008 | .012 | | .203 | .305 | |
| J | .085 | Typ. | | 2.16 | Typ. | |
| K | 0° | 8° | | 0° | 8° | |
| L | .025 | .045 | | .635 | 1.14 | |
| M | | | .030 | | | .762 |
| N | | | .100 | | | 2.54 |
| P | | | .055 | | | 1.40 |
| Q | | | .540 | | | 13.72 |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The circuit below is a guideline for interconnecting PCA's EPF8001GM with National DP83840A and DP83223(A) twister chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes. Please consult PCA for applications help regarding the SSI78Q2120 or ICS1890 series parts or consult with the respective application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the TXREF resistor of the twister chip to get at least 2.12V pk-pk across pins 16-15.
Note that this part only has one series common mode choke and a shunt choke with `its center tap available at pin 12 for the "common mode termination" via an external 75Ω. This shunting effect may not meet the system EMI containment needs; in such a case, system designers are highly encouraged to investigate the use of EPF8017GM, a part built specifically with better common mode attenuation for applications with DP83840A and DP83223(A). Designers of the TSC or the ICS parts may look into EPF8010GM for similar enhanced common mode attenuation.
System designers need not take the receiver side center tap to ground, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

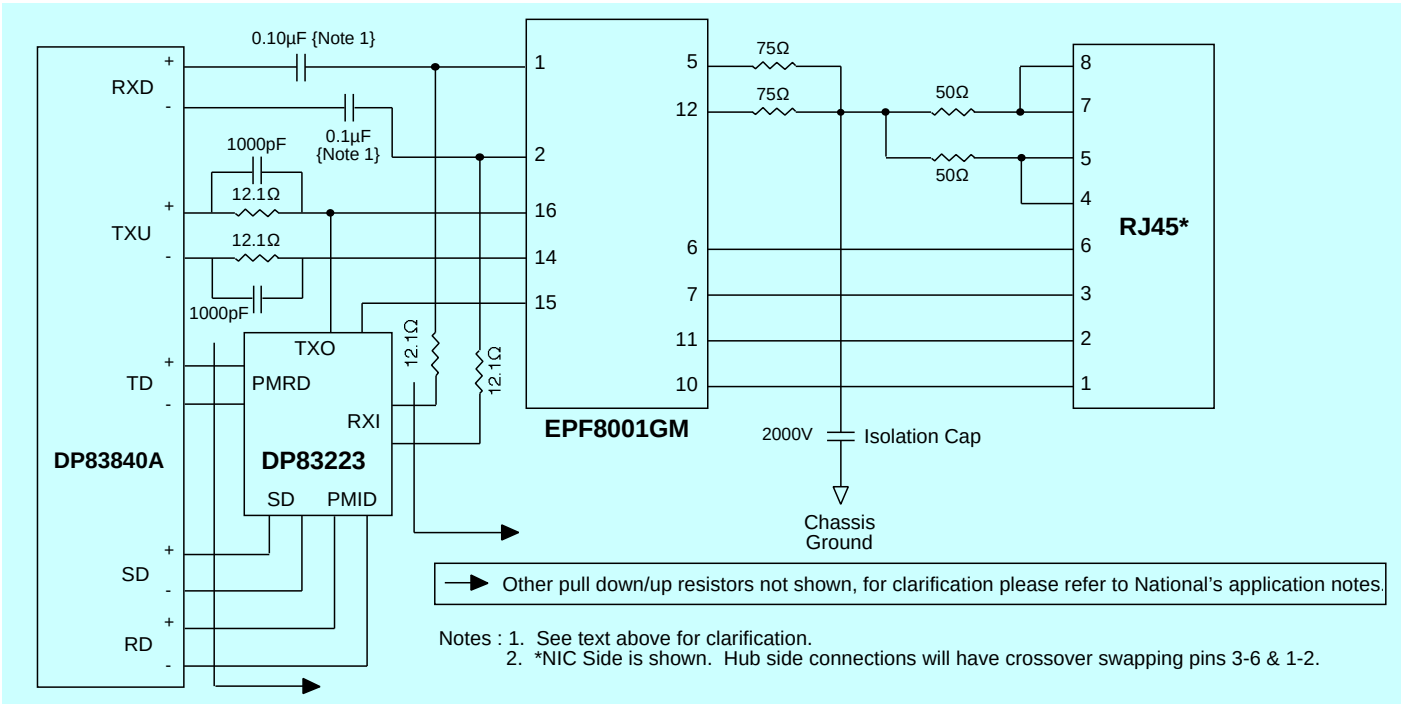
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8001GM. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

**Typical Application Circuit for UTP (Excerpts from NSC DP83840A application notes)**





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