74AVC4T245

4-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 01 — 20 July 2009 Product data sheet

1. General description

The 74AVC4T245 is an 4-bit, dual supply transceiver that enables bidirectional level translation. The device can be used as two 2-bit transceivers or as a 4-bit transceiver. It features two data input-output ports (nAn and nBn), a direction control input (nDIR), a output enable input ($n\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins nAn, $n\overline{OE}$ and nDIR are referenced to $V_{CC(A)}$ and pins nBn are referenced to $V_{CC(B)}$. A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input ($n\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both nAn and nBn are in the high-impedance OFF-state.

2. Features

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3B exceeds 8000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Maximum data rates:
  - 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 3.3 V translation)
  - 200 Mbit/s (≥ 1.1 V to 2.5 V translation)
  - 200 Mbit/s (≥ 1.1 V to 1.8 V translation)
  - 150 Mbit/s (≥ 1.1 V to 1.5 V translation)

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- ◆ 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC4T245D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AVC4T245PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AVC4T245BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

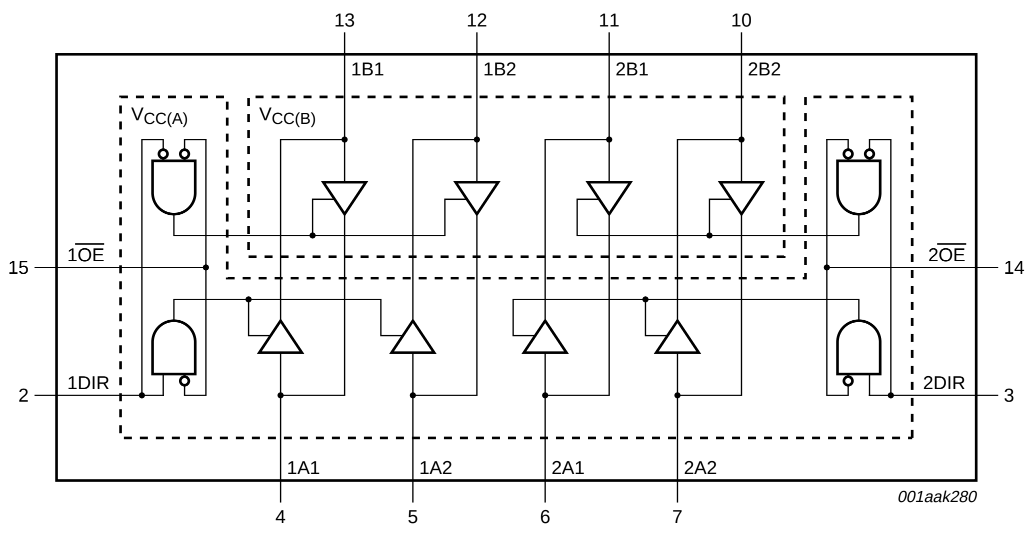


Fig 1. Logic symbol

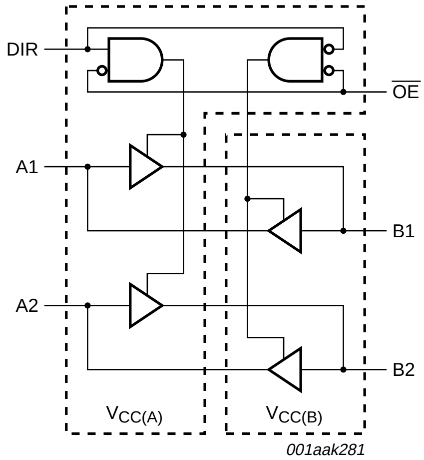


Fig 2. Logic diagram (one 2-bit transceiver)

5. Pinning information

5.1 Pinning

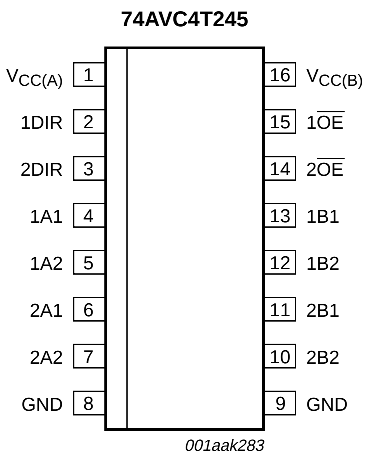


Fig 3. Pin configuration SOT109-1 (SO16)

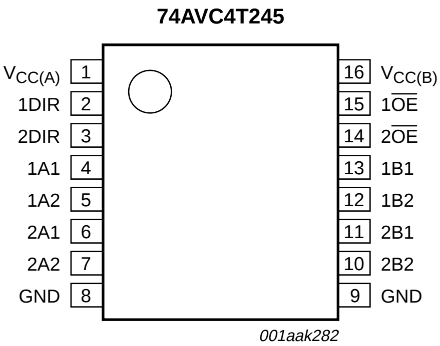
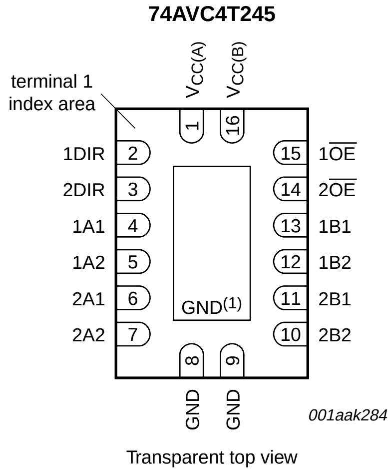


Fig 4. Pin configuration SOT403-1 (TSSOP16)



(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as a supply pin or input.

Fig 5. Pin configuration SOT763-1 (DHVQFN16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (nAn, n$\overline{OE}$ and nDIR inputs are referenced to $V_{CC(A)}$)
1DIR, 2DIR	2, 3	direction control
1A1, 1A2	4, 5	data input or output
2A1, 2A2	6, 7	data input or output
GND[1]	8, 9	ground (0 V)
2B2, 2B1	10, 11	data input or output
1B2, 1B1	12, 13	data input or output
2$\overline{OE}$, 1$\overline{OE}$	14, 15	output enable input (active LOW)
$V_{CC(B)}$	16	supply voltage B (nBn inputs are referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table[1]

Supply voltage	Input		Input/output[3]	
$V_{CC(A)}$, $V_{CC(B)}$	$n\overline{OE}$[2]	nDIR[2]	nAn[2]	nBn[2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND[3]	X	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] The nAn, nDIR and $n\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The nBn input circuit is referenced to $V_{CC(B)}$.

[3] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
V_O	output voltage	Active mode	[1][2][3]	–0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	–0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output port.

[3] V_{CCO} + 0.5 V should not exceed 4.6 V.

[4] For SO16 package: above 70 °C derates linearly with 8 mW/K.
For TSSOP16 package: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN16 package: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.8	3.6	V
$V_{CC(B)}$	supply voltage B			0.8	3.6	V
V_I	input voltage			0	3.6	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	3.6	V
T_{amb}	ambient temperature			–40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CCI} =0.8 V to 3.6 V	[2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at T_{amb} = 25 °C[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.07	-	V
I_I	input leakage current	nDIR, $n\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.025	±0.25	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)} = V_{CC(B)}$ = 3.6 V	[3]	-	±0.5	±2.5	μA
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	[3]	-	±0.5	±2.5	μA
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	[3]	-	±0.5	±2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
C_I	input capacitance	nDIR, $n\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V		-	1.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; V_O = 3.3 V or 0 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V		-	4.0	-	pF

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 7. Static characteristics [1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		V_{CCI} = 0.8 V	0.70V_{CCI}	-	0.70V_{CCI}	-	V
		V_{CCI} = 1.1 V to 1.95 V	0.65V_{CCI}	-	0.65V_{CCI}	-	V
		V_{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V_{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, n$\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	0.70$V_{CC(A)}$	-	0.70$V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	0.65$V_{CC(A)}$	-	0.65$V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	data input					
		V_{CCI} = 0.8 V	-	0.30V_{CCI}	-	0.30V_{CCI}	V
		V_{CCI} = 1.1 V to 1.95 V	-	0.35V_{CCI}	-	0.35V_{CCI}	V
		V_{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, n$\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	-	0.30$V_{CC(A)}$	-	0.30$V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	-	0.35$V_{CC(A)}$	-	0.35$V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA; $V_{CC(A)}$ = $V_{CC(B)}$ = 0.8 V to 3.6 V	V_{CCO} − 0.1	-	V_{CCO} − 0.1	-	V
		I_O = −3 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.1 V	0.85	-	0.85	-	V
		I_O = −6 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.4 V	1.05	-	1.05	-	V
		I_O = −8 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 1.65 V	1.2	-	1.2	-	V
		I_O = −9 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 2.3 V	1.75	-	1.75	-	V
		I_O = −12 mA; $V_{CC(A)}$ = $V_{CC(B)}$ = 3.0 V	2.3	-	2.3	-	V

Table 7. Static characteristics *...continued*[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100\ \mu A$; $V_{CC(A)} = V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	0.1	-	0.1	V
		$I_O = 3\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.1\ V$		-	0.25	-	0.25	V
		$I_O = 6\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.4\ V$		-	0.35	-	0.35	V
		$I_O = 8\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.65\ V$		-	0.45	-	0.45	V
		$I_O = 9\ mA$; $V_{CC(A)} = V_{CC(B)} = 2.3\ V$		-	0.55	-	0.55	V
		$I_O = 12\ mA$; $V_{CC(A)} = V_{CC(B)} = 3.0\ V$		-	0.7	-	0.7	V
I_I	input leakage current	nDIR, $n\overline{OE}$ input; $V_I = 0\ V$ or $3.6\ V$; $V_{CC(A)} = V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	±1	-	±5	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = V_{CC(B)} = 3.6\ V$	[3]	-	±5	-	±30	μA
		suspend mode A port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = 3.6\ V$; $V_{CC(B)} = 0\ V$	[3]	-	±5	-	±30	μA
		suspend mode B port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = 0\ V$; $V_{CC(B)} = 3.6\ V$	[3]	-	±5	-	±30	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC(A)} = 0\ V$; $V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	±5	-	±30	μA
		B port; V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC(B)} = 0\ V$; $V_{CC(A)} = 0.8\ V$ to $3.6\ V$		-	±5	-	±30	μA

Table 7. Static characteristics *...continued*[1][2]

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	µA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	8	-	50	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	−2	-	−12	-	µA
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	µA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	−2	-	−12	-	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-	8	-	50	µA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	20	-	70	µA
		A plus B port ($I_{CC(A)} + I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	16	-	65	µA

[1] V_{CCO} is the supply voltage associated with the output port.

[2] V_{CCI} is the supply voltage associated with the data input port.

[3] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Typical total supply current ($I_{CC(A)} + I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	µA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	µA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	µA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	µA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	µA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	µA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	µA

10. Dynamic characteristics

Table 9. Typical power dissipation capacitance at $V_{CC(A)} = V_{CC(B)}$ and $T_{amb} = 25\ °C$ [1][2]

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction nAn to nBn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nAn to nBn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction nBn to nAn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction nBn to nAn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nAn to nBn); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction nAn to nBn); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction nBn to nAn); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction nBn to nAn); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

Table 10. Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and T_{amb} = 25 °C [1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.5	7.3	6.5	6.2	5.9	6.0	ns
		nBn to nAn	14.5	12.7	12.4	12.3	12.1	12.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	14.3	14.3	14.3	14.3	14.3	14.3	ns
		$n\overline{OE}$ to nBn	17.0	9.9	9.0	9.4	9.0	9.7	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	18.2	18.2	18.2	18.2	18.2	18.2	ns
		$n\overline{OE}$ to nBn	19.2	10.7	9.8	9.6	9.7	10.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 11. Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and T_{amb} = 25 °C [1]
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	nAn to nBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		nBn to nAn	14.5	7.3	6.5	6.2	5.9	6.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	14.3	5.5	4.1	4.0	3.0	3.5	ns
		$n\overline{OE}$ to nBn	17.0	13.8	13.4	13.1	12.9	12.7	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	18.2	5.6	4.0	3.2	2.4	2.2	ns
		$n\overline{OE}$ to nBn	19.2	14.6	14.1	13.9	13.7	13.6	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

Table 12. Dynamic characteristics for temperature range −40 °C to +85 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	1.8	10.9	ns
		n$\overline{OE}$ to nBn	1.9	12.4	1.9	9.6	1.9	9.5	1.4	8.1	1.2	9.1	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	1.4	12.8	ns
		n$\overline{OE}$ to nBn	1.1	13.3	1.1	10.0	1.1	8.9	1.0	7.9	1.0	7.7	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	nAn to nBn	0.3	8.9	0.3	6.3	0.3	5.2	0.3	4.2	0.3	4.2	ns
		nBn to nAn	0.7	7.1	0.7	6.3	0.5	6.0	0.4	5.7	0.3	5.6	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.8	10.2	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
		n$\overline{OE}$ to nBn	1.9	11.3	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.1	9.4	1.4	9.4	1.1	9.4	0.7	9.4	0.4	9.4	ns
		n$\overline{OE}$ to nBn	1.4	12.1	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	nAn to nBn	0.1	8.7	0.1	6.0	0.1	4.9	0.1	3.9	0.3	3.9	ns
		nBn to nAn	0.6	6.2	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.8	8.6	1.6	8.6	1.8	8.6	1.3	8.6	1.6	8.6	ns
		n$\overline{OE}$ to nBn	1.7	10.9	1.7	9.9	1.6	8.7	1.2	6.9	1.0	6.9	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	1.0	7.2	1.0	7.2	1.0	7.2	0.6	7.2	0.4	7.2	ns
		n$\overline{OE}$ to nBn	1.2	11.7	1.2	9.2	1.0	7.4	0.8	5.3	0.8	4.6	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	nAn to nBn	0.1	8.4	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
		nBn to nAn	0.6	5.2	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	1.0	6.2	ns
		n$\overline{OE}$ to nBn	1.5	10.4	1.5	8.8	1.3	8.2	1.1	6.2	0.9	5.2	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.7	4.8	0.7	4.8	0.7	4.8	0.6	4.8	0.4	4.8	ns
		n$\overline{OE}$ to nBn	0.9	11.3	0.9	8.8	0.8	7.0	0.6	4.8	0.6	4.0	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	nAn to nBn	0.1	8.2	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
		nBn to nAn	0.6	5.1	0.6	4.2	0.4	3.4	0.2	3.0	0.1	2.8	ns
t_{dis}	disable time	n$\overline{OE}$ to nAn	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	0.7	5.6	ns
		n$\overline{OE}$ to nBn	1.4	10.2	1.4	9.3	1.2	8.1	1.0	6.4	0.8	6.2	ns
t_{en}	enable time	n$\overline{OE}$ to nAn	0.6	3.8	0.6	3.8	0.6	3.8	0.6	3.8	0.4	3.8	ns
		n$\overline{OE}$ to nBn	0.8	11.3	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

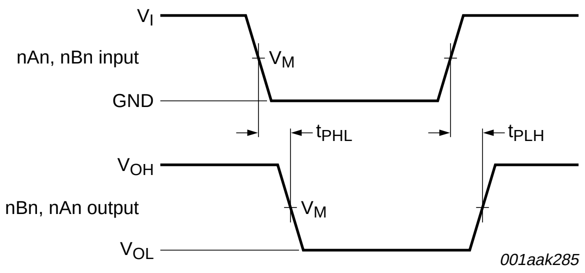
Table 13. Dynamic characteristics for temperature range −40 °C to +125 °C [1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	1.8	12.0	ns
		$n\overline{OE}$ to nBn	1.9	13.7	1.9	10.6	1.9	10.5	1.4	9.0	1.2	10.1	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	1.4	14.1	ns
		$n\overline{OE}$ to nBn	1.1	14.7	1.1	11.0	1.1	9.8	1.0	8.7	1.0	8.5	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	nAn to nBn	0.3	9.8	0.3	7.0	0.3	5.8	0.3	4.7	0.3	4.7	ns
		nBn to nAn	0.7	7.9	0.7	7.0	0.5	6.6	0.4	6.3	0.3	6.2	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	1.8	11.3	1.8	11.3	1.5	11.3	1.3	11.3	1.6	11.3	ns
		$n\overline{OE}$ to nBn	1.9	12.5	1.9	11.4	1.9	10.1	1.4	8.2	1.2	8.4	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	1.1	10.4	1.4	10.4	1.1	10.4	0.7	10.4	0.4	10.4	ns
		$n\overline{OE}$ to nBn	1.4	13.3	1.4	10.6	1.1	8.5	0.9	6.4	0.9	6.2	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	nAn to nBn	0.1	9.6	0.1	6.6	0.1	5.4	0.1	4.3	0.3	4.3	ns
		nBn to nAn	0.6	6.9	0.6	5.9	0.5	5.4	0.3	5.1	0.3	5.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	1.8	9.5	1.6	9.5	1.8	9.5	1.3	9.5	1.6	9.5	ns
		$n\overline{OE}$ to nBn	1.7	12.0	1.7	10.9	1.6	9.6	1.2	7.6	1.0	7.6	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	1.0	8.0	1.0	8.0	1.0	8.0	0.6	8.0	0.4	8.0	ns
		$n\overline{OE}$ to nBn	1.2	12.9	1.2	10.2	1.0	8.2	0.8	5.9	0.8	5.1	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	nAn to nBn	0.1	9.3	0.1	6.3	0.1	5.1	0.2	4.0	0.1	4.0	ns
		nBn to nAn	0.6	5.8	0.6	4.7	0.4	4.3	0.2	3.9	0.2	3.8	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	1.0	6.9	ns
		$n\overline{OE}$ to nBn	1.5	11.5	1.5	10.4	1.3	9.1	1.1	6.9	0.9	5.8	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	0.7	5.3	0.7	5.3	0.7	5.3	0.6	5.3	0.4	5.3	ns
		$n\overline{OE}$ to nBn	0.9	12.4	0.9	9.7	0.8	7.7	0.6	5.3	0.6	4.4	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	nAn to nBn	0.1	9.1	0.1	6.2	0.1	5.0	0.1	3.8	0.1	3.3	ns
		nBn to nAn	0.6	5.7	0.6	4.7	0.4	3.9	0.2	3.4	0.1	3.3	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	0.7	6.2	ns
		$n\overline{OE}$ to nBn	1.4	11.3	1.4	10.3	1.2	9.0	1.0	7.1	0.8	6.9	ns
t_{en}	enable time	$n\overline{OE}$ to nAn	0.6	4.2	0.6	4.2	0.6	4.2	0.6	4.2	0.4	4.2	ns
		$n\overline{OE}$ to nBn	0.8	12.4	0.8	9.6	0.6	7.5	0.5	5.2	0.5	4.2	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.

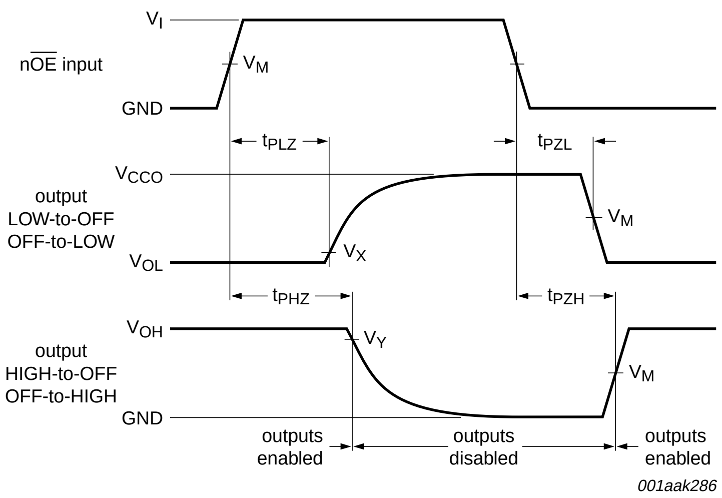
11. Waveforms



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

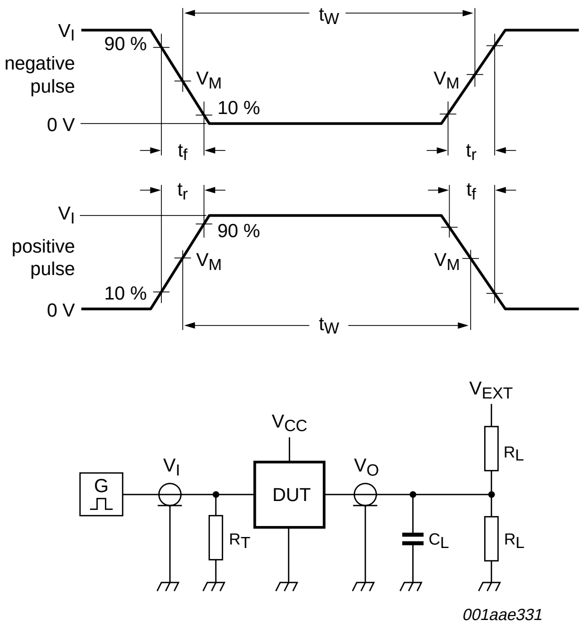
Fig 7. Enable and disable times

Table 14. Measurement points

Supply voltage	Input[1]	Output[2]		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 15.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Load circuit for switching times

Table 15. Test data

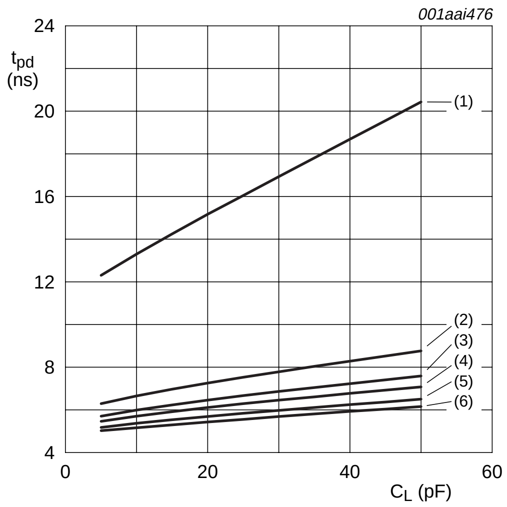
Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I[1]	$\Delta t/\Delta V$[2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
0.8 V to 1.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] dV/dt ≥ 1.0 V/ns

[3] V_{CCO} is the supply voltage associated with the output port.

12. Typical propagation delay characteristics



a. Propagation delay (A to B); $V_{CC(A)}$ = 0.8 V

(1) $V_{CC(B)}$ = 0.8 V.

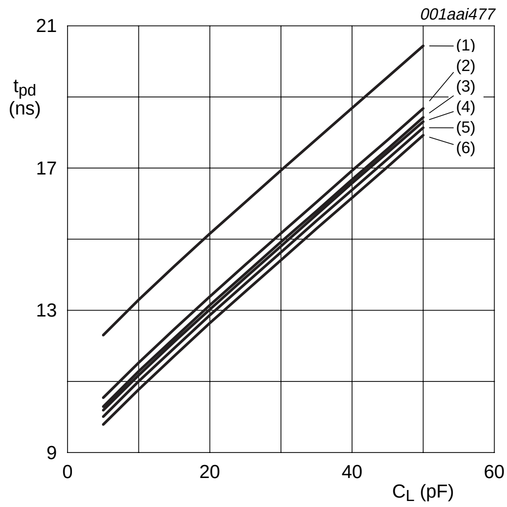
(2) $V_{CC(B)}$ = 1.2 V.

(3) $V_{CC(B)}$ = 1.5 V.

(4) $V_{CC(B)}$ = 1.8 V.

(5) $V_{CC(B)}$ = 2.5 V.

(6) $V_{CC(B)}$ = 3.3 V.



b. Propagation delay (A to B); $V_{CC(B)}$ = 0.8 V

(1) $V_{CC(A)}$ = 0.8 V.

(2) $V_{CC(A)}$ = 1.2 V.

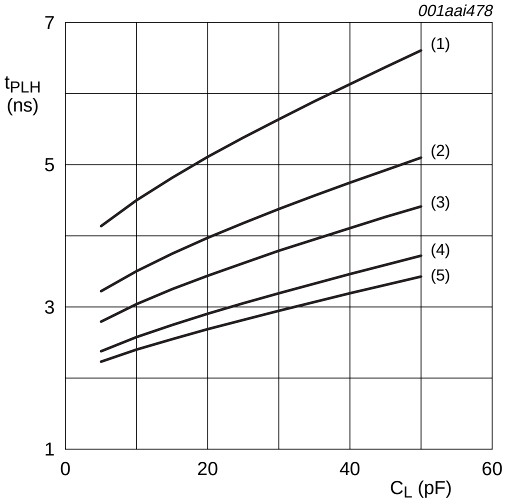
(3) $V_{CC(A)}$ = 1.5 V.

(4) $V_{CC(A)}$ = 1.8 V.

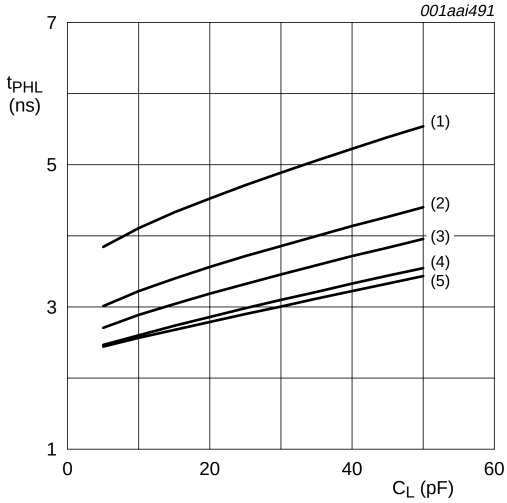
(5) $V_{CC(A)}$ = 2.5 V.

(6) $V_{CC(A)}$ = 3.3 V.

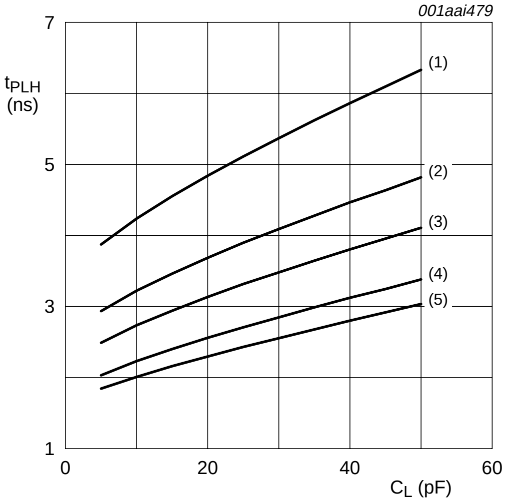
Fig 9. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



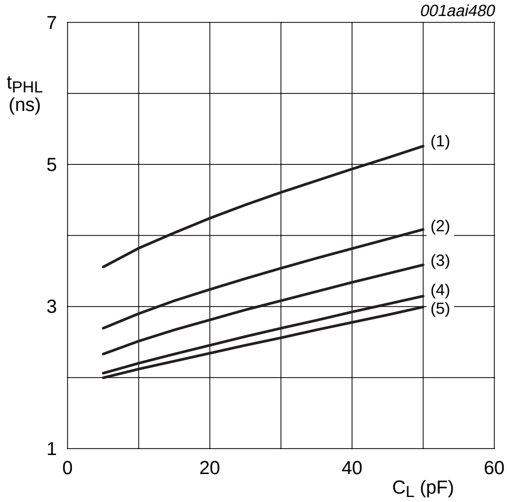
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.2 V



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.2 V



c. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.5 V



d. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.5 V

(1) $V_{CC(B)}$ = 1.2 V.

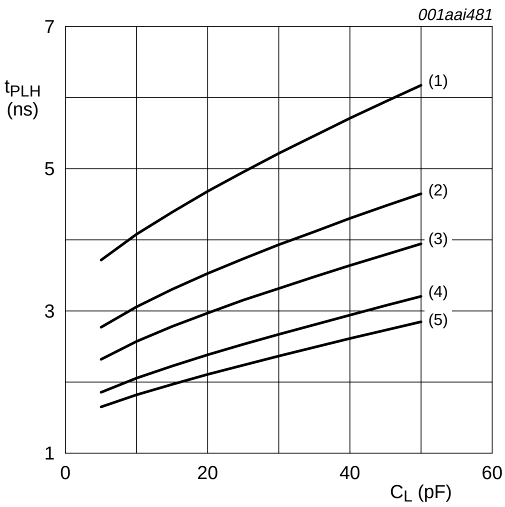
(2) $V_{CC(B)}$ = 1.5 V.

(3) $V_{CC(B)}$ = 1.8 V.

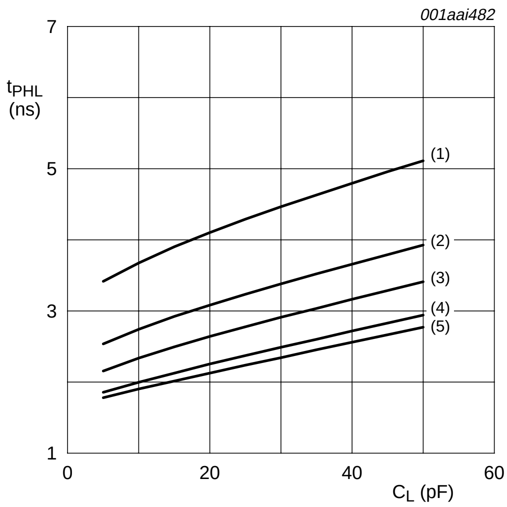
(4) $V_{CC(B)}$ = 2.5 V.

(5) $V_{CC(B)}$ = 3.3 V.

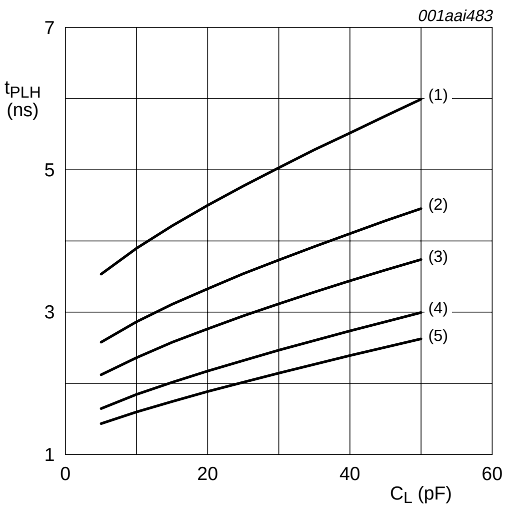
Fig 10. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



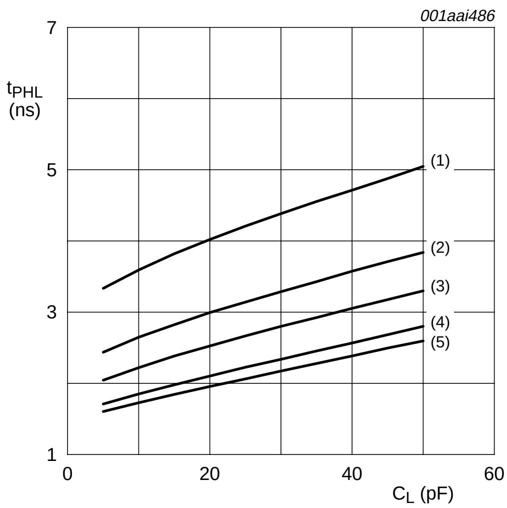
a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 1.8 V



b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 1.8 V



c. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 2.5 V



d. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 2.5 V

(1) $V_{CC(B)}$ = 1.2 V.

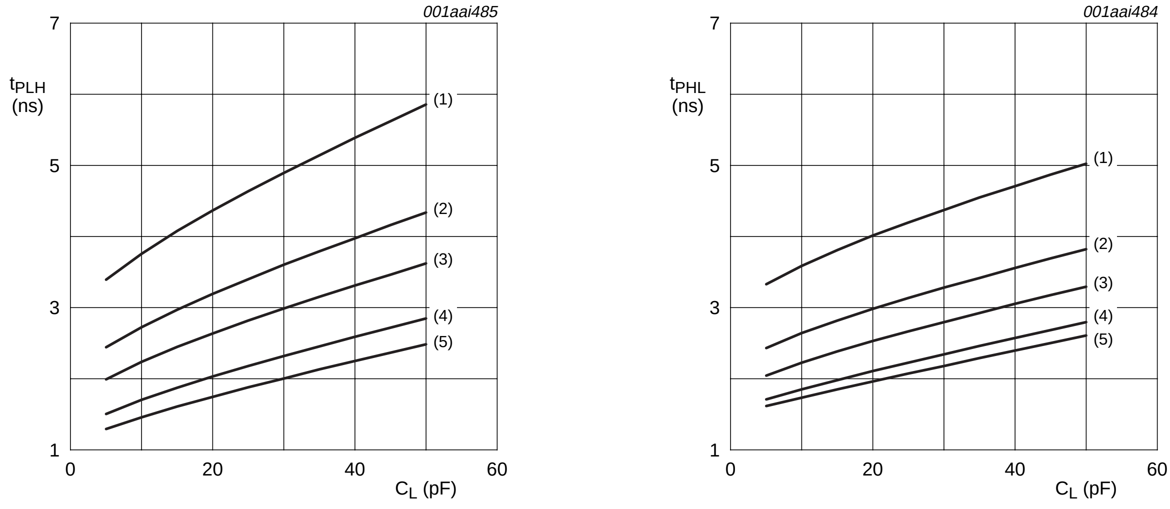
(2) $V_{CC(B)}$ = 1.5 V.

(3) $V_{CC(B)}$ = 1.8 V.

(4) $V_{CC(B)}$ = 2.5 V.

(5) $V_{CC(B)}$ = 3.3 V.

Fig 11. Typical propagation delay versus load capacitance; T_{amb} = 25 °C



a. LOW to HIGH propagation delay (A to B); $V_{CC(A)}$ = 3.3 V

b. HIGH to LOW propagation delay (A to B); $V_{CC(A)}$ = 3.3 V

(1) $V_{CC(B)}$ = 1.2 V.

(2) $V_{CC(B)}$ = 1.5 V.

(3) $V_{CC(B)}$ = 1.8 V.

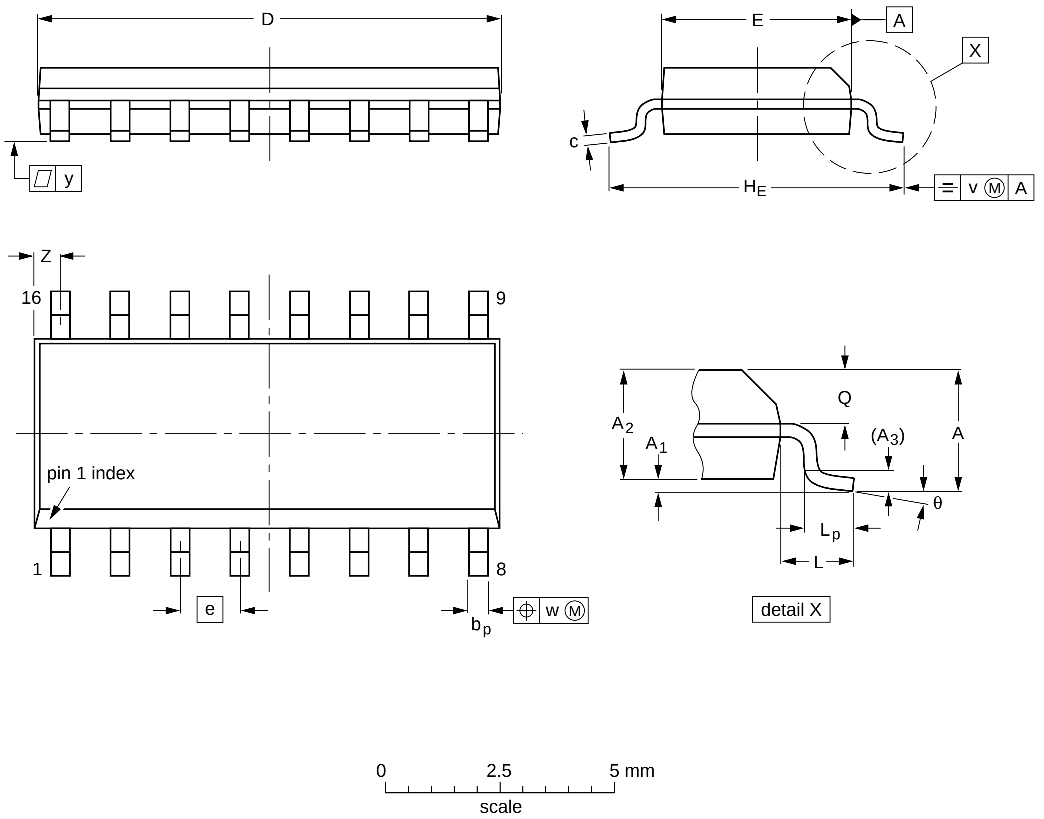
(4) $V_{CC(B)}$ = 2.5 V.

(5) $V_{CC(B)}$ = 3.3 V.

Fig 12. Typical propagation delay versus load capacitance; T_{amb} = 25 °C

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

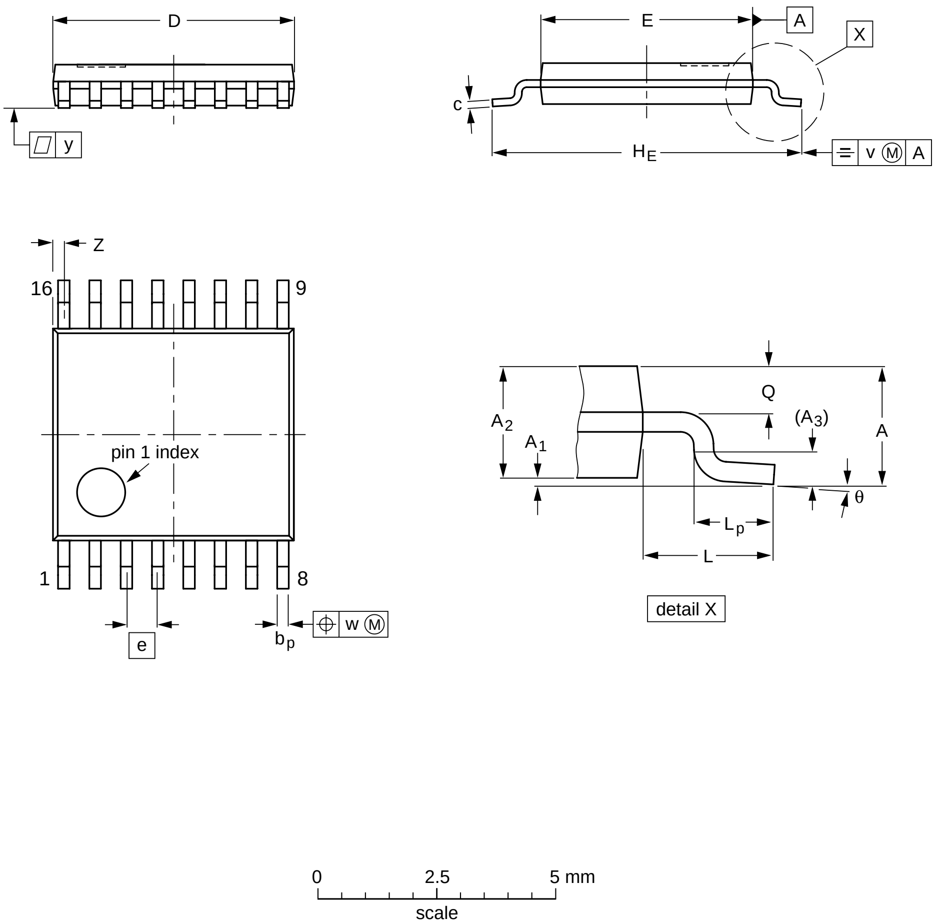
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

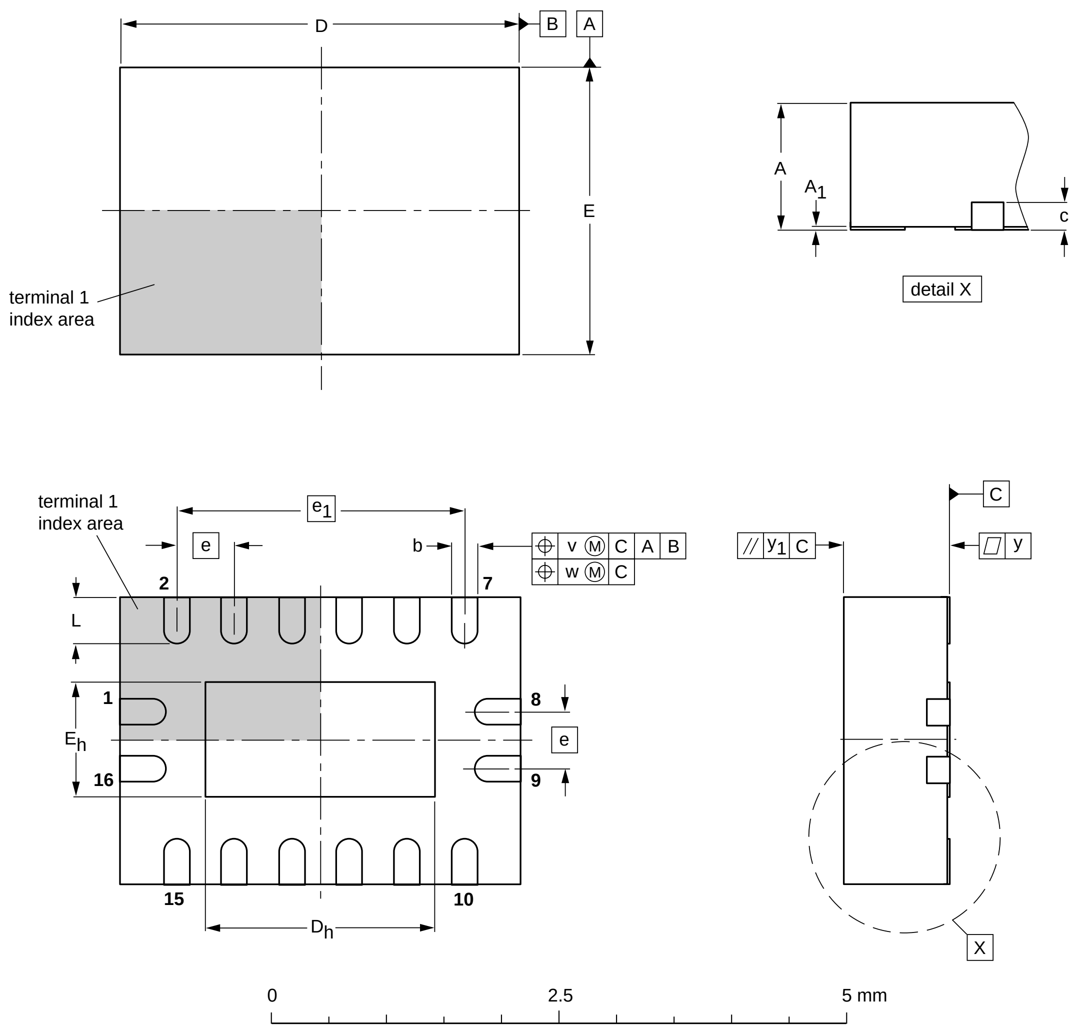
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 14. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 15. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC4T245_1	20090720	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

Date of release: 20 July 2009
Document identifier: 74AVC4T245_1