# **74AUP1G57**

# Low-power configurable multiple function gate Rev. 4 — 20 July 2010 P

**Product data sheet** 

#### **General description** 1.

The 74AUP1G57 provides configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and buffer. All inputs can be connected to  $\ensuremath{V_{\text{CC}}}$  or GND.

This device ensures a very low static and dynamic power consumption across the entire V<sub>CC</sub> range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74AUP1G57 has Schmitt trigger inputs making it capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

The inputs switch at different points for positive and negative-going signals. The difference between the positive voltage  $V_{T+}$  and the negative voltage  $V_{T-}$  is defined as the input hysteresis voltage V<sub>H</sub>.

#### **Features and benefits** 2.

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption;  $I_{CC} = 0.9 \mu A$  (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



#### Low-power configurable multiple function gate

# 3. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range Name		Description	Version					
74AUP1G57GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363					
74AUP1G57GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1.45 $\times$ 0.5 mm	SOT886					
74AUP1G57GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1 $\times$ 0.5 mm	SOT891					
74AUP1G57GN	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115					
74AUP1G57GS	–40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 $\times$ 1.0 $\times$ 0.35 mm	SOT1202					

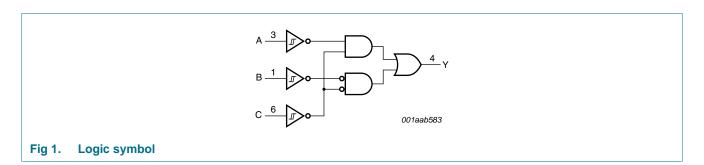
## 4. Marking

#### Table 2. Marking

Type number	Marking code <sup>[1]</sup>
74AUP1G57GW	aC
74AUP1G57GM	aC
74AUP1G57GF	aC
74AUP1G57GN	aC
74AUP1G57GS	aC

<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

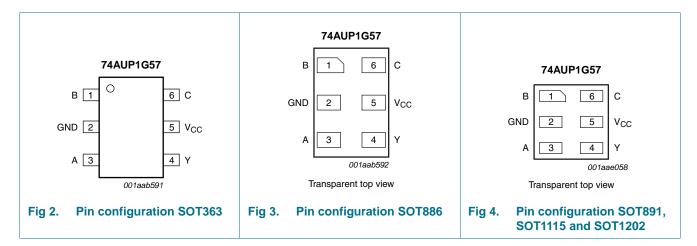
# 5. Functional diagram



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# 6. Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
В	1	data input
GND	2	ground (0 V)
A	3	data input
Υ	4	data output
V <sub>CC</sub>	5	supply voltage
С	6	data input

# 7. Functional description

Table 4. Function table[1]

Input			Output
С	В	Α	Υ
L	L	L	Н
L	L	Н	L
L	Н	L	Н
L	Н	Н	L
Н	L	L	L
Н	L	Н	L
Н	Н	L	Н
Н	Н	Н	Н

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level.

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#### Low-power configurable multiple function gate

## 7.1 Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input AND	see Figure 5
2-input AND with both inputs inverted	see Figure 8
2-input NAND with inverted input	see Figure 6 and Figure 7
2-input OR with inverted input	see Figure 6 and Figure 7
2-input NOR	see Figure 8
2-input NOR with both inputs inverted	see Figure 5
2-input XNOR	see Figure 9
Inverter	see Figure 10
Buffer	see Figure 11

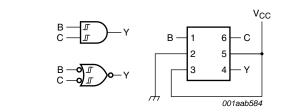


Fig 5. 2-input AND gate or 2-input NOR gate with both inputs inverted

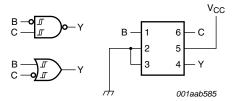


Fig 6. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input

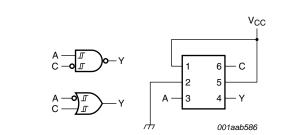


Fig 7. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input

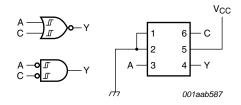
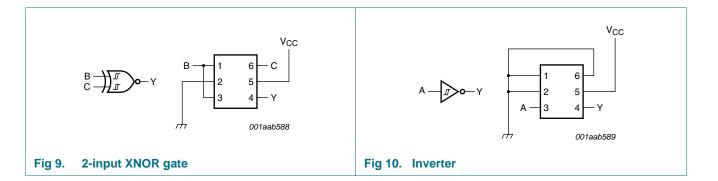
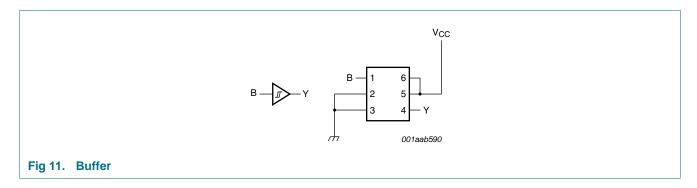


Fig 8. 2-input NOR gate or 2-input AND gate with both inputs inverted



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#### Low-power configurable multiple function gate



# 8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
VI	input voltage		<u>[1]</u> –0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	Active mode and Power-down mode	[ <u>1</u> ] -0.5	+4.6	V
I <sub>O</sub>	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±20	mA
I <sub>CC</sub>	supply current		-	50	mA
I <sub>GND</sub>	ground current		-50	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2] _	250	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	$V_{CC}$	V
		Power-down mode; V <sub>CC</sub> = 0 V	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C

<sup>[2]</sup> For SC-88 packages: above 87.5 °C the value of P<sub>tot</sub> derates linearly with 4.0 mW/K. For XSON6 packages: above 118 °C the value of P<sub>tot</sub> derates linearly with 7.8 mW/K.

## Low-power configurable multiple function gate

## 10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Uni
T <sub>amb</sub> = 2	5 °C					
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_{O} = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.1	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.75 \times V_{CC}$	-	-	V
		$I_{O} = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.11	-	-	V
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.32	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	2.05	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.72	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_O = 20 \mu A$ ; $V_{CC} = 0.8 \text{ V}$ to 3.6 V	-	-	0.1	V
		I <sub>O</sub> = 1.1 mA; V <sub>CC</sub> = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.31	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.31	V
		$I_O = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	V
		$I_O = 2.7 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.31	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	V
l <sub>l</sub>	input leakage current	$V_{I} = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.1	μΑ
l <sub>OFF</sub>	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.2	μΑ
$\Delta I_{OFF}$	additional power-off leakage current	$V_1 \text{ or } V_0 = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.2	μΑ
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.5	μΑ
Δl <sub>CC</sub>	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	-	-	40	μΑ
Cı	input capacitance	$V_I = GND \text{ or } V_{CC}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	1.1	-	pF
Co	output capacitance	$V_O = GND; V_{CC} = 0 V$	-	1.7	-	pF
	40 °C to +85 °C					<u> </u>
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_O = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> – 0.1	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	1.03	-	-	V
		$I_O = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.30	-	-	V
		$I_O = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.97	-	-	V
		$I_{O} = -3.1 \text{ mA; } V_{CC} = 2.3 \text{ V}$	1.85	-	-	V
		$I_O = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.67	-	-	V
		$I_0 = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.55	-	-	V
4AUP1G57		All information provided in this document is subject to legal disclaimers.			© NXP B.V. 2010. All rig	hts reser

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**Table 8. Static characteristics** ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{OL}$	LOW-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_O$ = 20 $\mu$ A; $V_{CC}$ = 0.8 $V$ to 3.6 $V$	-	-	0.1	V
		$I_{O} = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_{O} = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	V
		$I_{O} = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_{O} = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.45	V
l <sub>l</sub>	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.5	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.5	μΑ
Δl <sub>OFF</sub>	additional power-off leakage current	$V_1 \text{ or } V_O = 0 \text{ V to } 3.6 \text{ V};$ $V_{CC} = 0 \text{ V to } 0.2 \text{ V}$	-	-	±0.6	μΑ
lcc	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.9	μΑ
Δl <sub>CC</sub>	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	-	-	50	μΑ
T <sub>amb</sub> = -	40 °C to +125 °C					
V <sub>OH</sub>	HIGH-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_{O} = -20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> – 0.11	-	-	V
		$I_{O} = -1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	$0.6 \times V_{CC}$	-	-	V
		$I_{O} = -1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	0.93	-	-	V
		$I_{O} = -1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.17	-	-	V
		$I_{O} = -2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.77	-	-	V
		$I_{O} = -3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.67	-	-	V
		$I_{O} = -2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.40	-	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.30	-	-	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{T+}$ or $V_{T-}$				
		$I_O = 20 \mu A$ ; $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.11	V
		$I_{O} = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.33 \times V_{CC}$	V
		$I_{O} = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		$I_{O} = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.39	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.50	V
		$I_O = 2.7 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.50	V
l <sub>l</sub>	input leakage current	$V_1 = GND \text{ to } 3.6 \text{ V}; V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.75	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V			±0.75	μΑ

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 Table 8.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$\Delta I_{OFF}$	additional power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μΑ
I <sub>CC</sub>	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	1.4	μΑ
$\Delta I_{CC}$	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A};$ $V_{CC} = 3.3 \text{ V}$	-	-	75	μΑ

# 11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 13.

Symbol	Parameter	Conditions		25 °C			-40 °C to +125 °C			Unit
			N	lin	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$C_L = 5 p$	F									
t <sub>pd</sub>	propagation delay	A, B and C to Y; see Figure 12	1							
		$V_{CC} = 0.8 \text{ V}$		-	22.6	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	2	2.8	6.5	12.6	2.5	13.0	13.2	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	2	2.2	4.6	7.6	2.5	8.2	8.6	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2	2.1	3.9	6.2	2.0	6.8	7.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2	2.0	3.1	4.5	1.8	5.1	5.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1	8.1	2.8	3.9	1.5	4.1	4.3	ns
C <sub>L</sub> = 10	ρF									
t <sub>pd</sub>	propagation delay	A, B and C to Y; see Figure 12	1							
		$V_{CC} = 0.8 \text{ V}$		-	26.1	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	3	3.2	7.3	14.4	2.8	14.9	15.2	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	2	2.6	5.2	8.7	2.8	9.3	9.8	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2	2.5	4.5	7.0	2.2	7.8	8.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2	2.4	3.7	5.2	2.1	5.9	6.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2	2.3	3.4	4.6	1.9	4.9	5.1	ns
C <sub>L</sub> = 15	pF									
t <sub>pd</sub>	propagation delay	A, B and C to Y; see Figure 12	1							
		$V_{CC} = 0.8 \text{ V}$		-	31.6	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$	3	3.4	8.0	15.7	3.1	16.7	17.0	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$	2	2.8	5.7	9.4	3.1	10.4	10.9	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	2	2.6	4.9	7.7	2.5	8.7	9.2	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2	2.6	4.1	5.7	2.4	6.5	6.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2	2.5	3.8	5.0	2.2	5.5	5.7	ns

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 Table 9.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 13.

Symbo	I Parameter	Conditions		25 °C			-4	l0 °C to +1	25 °C	Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C <sub>L</sub> = 30	pF					•			'	
t <sub>pd</sub>	propagation delay	A, B and C to Y; see Figure 12	[2]							
		$V_{CC} = 0.8 \text{ V}$		-	37.8	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		4.6	10.4	20.9	3.9	21.8	22.3	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		3.6	7.4	12.2	3.8	13.4	14.1	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		3.5	6.2	9.9	3.1	11.1	11.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		3.4	5.2	7.4	3.1	8.3	8.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		3.2	4.9	6.6	2.8	7.0	7.4	ns
C <sub>L</sub> = 5 p	oF, 10 pF, 15 pF and	30 pF								
$C_{PD}$	power dissipation	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$	[3][4]							
	capacitance	$V_{CC} = 0.8 \text{ V}$		-	2.6	-	-	-	-	pF
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		-	2.8	-	-	-	-	pF
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		-	2.9	-	-	-	-	pF
		$V_{CC}$ = 1.65 V to 1.95 V		-	3.1	-	-	-	-	pF
		$V_{CC}$ = 2.3 V to 2.7 V		-	3.7	-	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	4.3	-	-	-	-	pF

<sup>[1]</sup> All typical values are measured at nominal  $V_{CC}$ .

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$$
 where:

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}{}^2 \times f_o)$  = sum of the outputs.

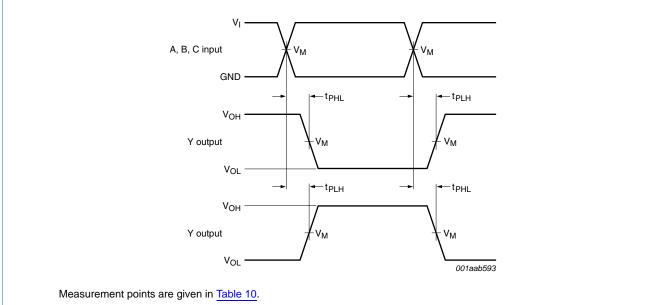
<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

<sup>[3]</sup> All specified values are the average typical values over all stated loads.

<sup>[4]</sup>  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

#### Low-power configurable multiple function gate

## 12. Waveforms



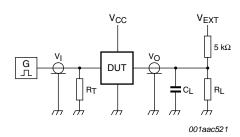
 $\ensuremath{V_{OL}}$  and  $\ensuremath{V_{OH}}$  are typical output voltage drops that occur with the output load.

Fig 12. Input A, B and C to output Y propagation delay times

Table 10. Measurement points

Supply voltage	Output	Input			
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>I</sub>	$t_r = t_f$	
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>CC</sub>	≤ 3.0 ns	

#### Low-power configurable multiple function gate



Test data is given in Table 11.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

 $V_{\text{EXT}}$  = External voltage for measuring switching times.

Fig 13. Test circuit for measuring switching times

#### Table 11. Test data

Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	CL	R <sub>L</sub> [1]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k $\Omega$ or 1 M $\Omega$	open	GND	$2 \times V_{CC}$

<sup>[1]</sup> For measuring enable and disable times,  $R_L$  = 5 k $\Omega$ . For measuring propagation delays, set-up and hold times, and pulse width,  $R_L$  = 1 M $\Omega$ .

#### Low-power configurable multiple function gate

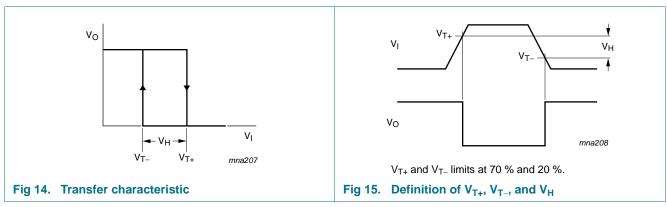
## 13. Transfer characteristics

Table 12. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 13.

Symbol Pa	Parameter	Conditions		25 °C		−40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max (85 °C)	Max (125 °C)	
V <sub>T+</sub> positive-going threshold voltage		see <u>Figure 14</u> and <u>Figure 15</u>							
		$V_{CC} = 0.8 \text{ V}$	0.30	-	0.60	0.30	0.60	0.62	V
		V <sub>CC</sub> = 1.1 V	0.53	-	0.90	0.53	0.90	0.92	V
		V <sub>CC</sub> = 1.4 V	0.74	-	1.11	0.74	1.11	1.13	V
		V <sub>CC</sub> = 1.65 V	0.91	-	1.29	0.91	1.29	1.31	V
		V <sub>CC</sub> = 2.3 V	1.37	-	1.77	1.37	1.77	1.80	V
		V <sub>CC</sub> = 3.0 V	1.88	-	2.29	1.88	2.29	2.32	V
$V_{T-}$	V <sub>T-</sub> negative-going threshold voltage	see <u>Figure 14</u> and <u>Figure 15</u>							
		V <sub>CC</sub> = 0.8 V	0.10	-	0.60	0.10	0.60	0.60	V
		V <sub>CC</sub> = 1.1 V	0.26	-	0.65	0.26	0.65	0.65	V
		V <sub>CC</sub> = 1.4 V	0.39	-	0.75	0.39	0.75	0.75	V
	V <sub>CC</sub> = 1.65 V	0.47	-	0.84	0.47	0.84	0.84	V	
	$V_{CC} = 2.3 \text{ V}$	0.69	-	1.04	0.69	1.04	1.04	V	
		V <sub>CC</sub> = 3.0 V	0.88	-	1.24	0.88	1.24	1.24	V
$V_{H}$	hysteresis voltage	(V <sub>T+</sub> – V <sub>T-</sub> ); see <u>Figure 14</u> , <u>Figure 15</u> , <u>Figure 16</u> and <u>Figure 17</u>							
		$V_{CC} = 0.8 \text{ V}$	0.07	-	0.50	0.07	0.50	0.50	V
		V <sub>CC</sub> = 1.1 V	0.08	-	0.46	0.08	0.46	0.46	V
	V <sub>CC</sub> = 1.4 V	0.18	-	0.56	0.18	0.56	0.56	V	
		V <sub>CC</sub> = 1.65 V	0.27	-	0.66	0.27	0.66	0.66	V
		V <sub>CC</sub> = 2.3 V	0.53	-	0.92	0.53	0.92	0.92	V
		V <sub>CC</sub> = 3.0 V	0.79	-	1.31	0.79	1.31	1.31	V

## 14. Waveform transfer characteristics



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## Low-power configurable multiple function gate

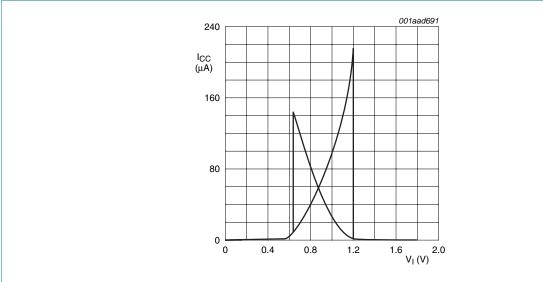


Fig 16. Typical transfer characteristics;  $V_{CC} = 1.8 \text{ V}$ 

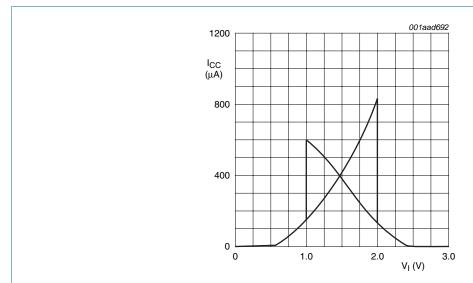


Fig 17. Typical transfer characteristics;  $V_{CC} = 3.0 \text{ V}$ 

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#### Low-power configurable multiple function gate

# 15. Package outline

#### Plastic surface-mounted package; 6 leads

**SOT363** 

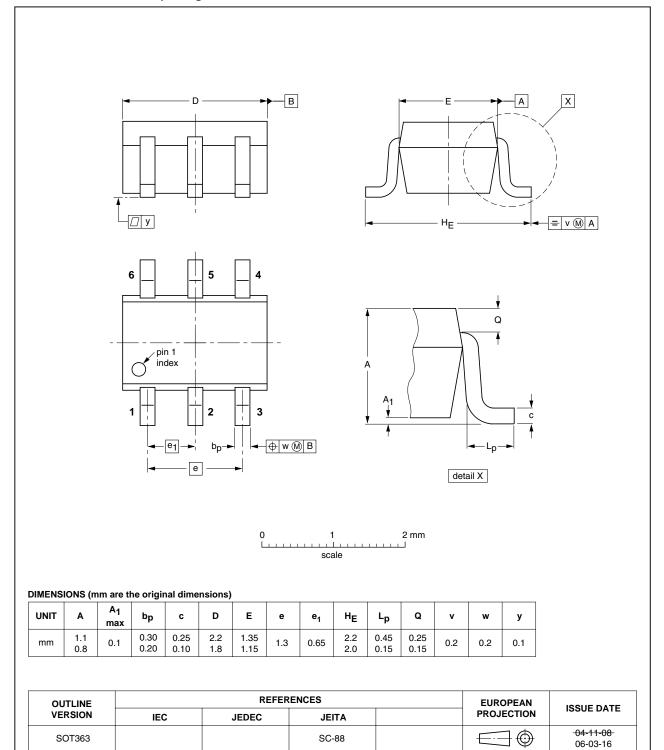


Fig 18. Package outline SOT363 (SC-88)

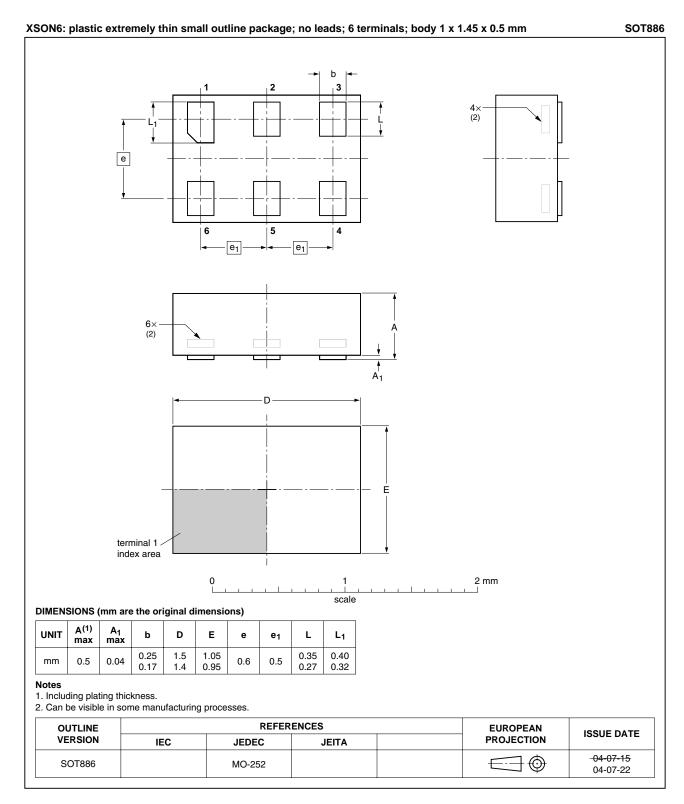


Fig 19. Package outline SOT886 (XSON6)

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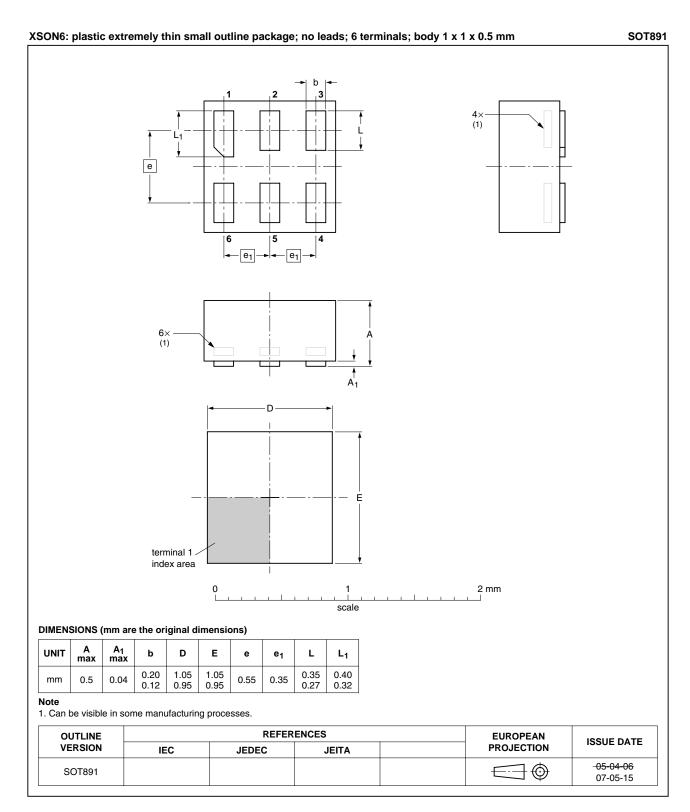


Fig 20. Package outline SOT891 (XSON6)

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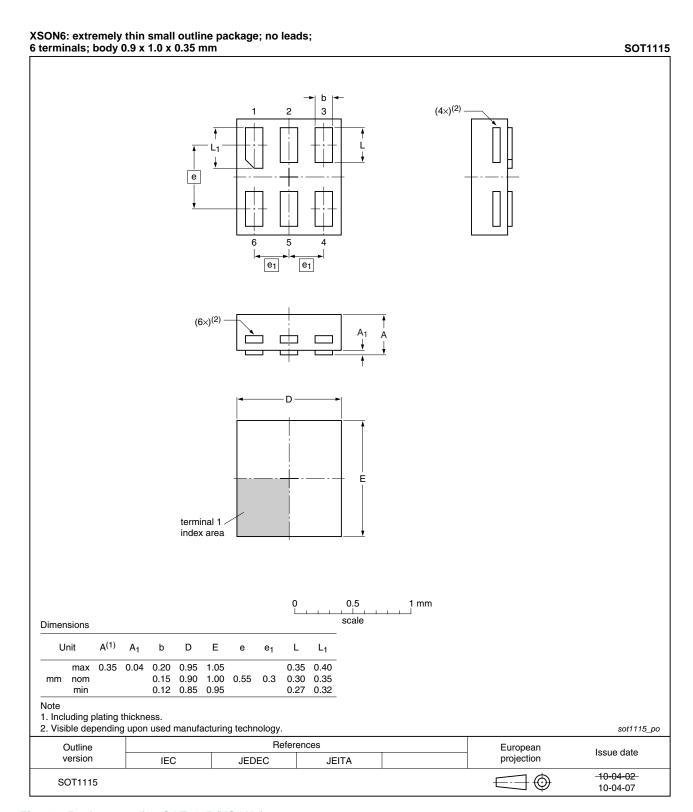


Fig 21. Package outline SOT1115 (XSON6)

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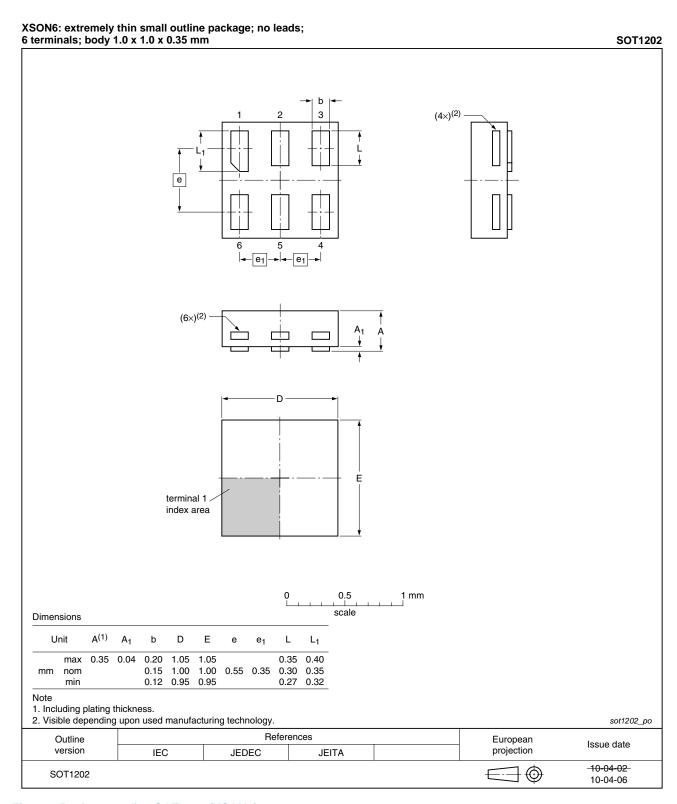


Fig 22. Package outline SOT1202 (XSON6)

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## Low-power configurable multiple function gate

## 16. Abbreviations

#### Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 17. Revision history

#### Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G57 v.4	20100720	Product data sheet	-	74AUP1G57 v.3
Modifications:	• •	number 74AUP1G57GN (SOT number 74AUP1G57GS (SOT	. • ,	
74AUP1G57 v.3	20090622	Product data sheet	-	74AUP1G57 v.2
74AUP1G57 v.2	20090323	Product data sheet	-	74AUP1G57 v.1
74AUP1G57 v.1	20061123	Product data sheet	-	-

#### Low-power configurable multiple function gate

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

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