

**HYBRID - HIGH RELIABILITY
RADIATION HARDENED
DC/DC CONVERTERS**

ARH28XXS SERIES
28V Input, Single Output

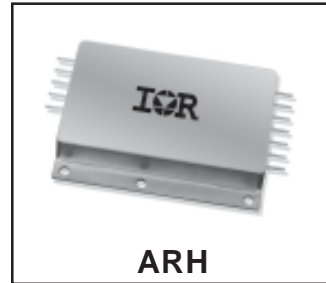
Description

The ARH Series of DC/DC converters has been designed specifically for use in the hostile environments. The high level of radiation tolerance inherent in the ARH design is the result of extensive research, thorough analysis and testing and of careful component specification. Designed to supplement the triple output configuration provided by the ART series, the ARH circuit topology is the follow-on to the successful ART design and incorporates many of the design features characterizing that product line. Capable of uniform high performance over long term exposures in radiation intense environments, this series expands the standard for distributed power systems demanding high performance and reliability in the harsh environments.

The ARH converters are hermetically sealed in a rugged, low profile package by utilizing copper core input and output pins to minimize resistive DC losses. Long-term hermeticity is assured through use of parallel seam welded lid attachment along with rugged ceramic pin-to-package seal. Axial orientation of the leads facilitates preferred bulkhead mounting placing the converter on the principal heat-dissipating surface.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options, refer to device screening table in the data sheet.

Variations in electrical, mechanical and screening specifications can be accommodated. Contact IR Santa Clara for special requirements.



Features

- Total Dose > 100 krad (Si), 2:1 Margin
- SEE Hardened to LET up to 83 MeV.cm²/mg
- Derated per MIL-STD-975 & MIL-STD-1547
- Output Power to 30 Watts
- Regulates to No-Load
- 18 to 50 Volt Input Range
- Input Undervoltage Lockout
- Fully Characterized from -55°C to +125°C
- Continuous Short Circuit Protection
- 12.8 W/in³ Output Power Density
- True Hermetic Package
- External Inhibit Port
- Externally Synchronizable
- Fault Tolerant Design
- Available with Outputs from 2.5V to 15V
- Overload Protection
- Standard Microcircuit Drawings Available

Specifications

Absolute Maximum Ratings		Recommended Operating Conditions	
Input Voltage range	-0.5V to +80VDC	Input Voltage range	+18V to +60VDC +18V to +50V for full derating to MIL-STD-1547
Soldering temperature	300°C for 10 seconds	Output Power	0 to 30W
Storage case temperature	-65°C to +135°C	Operating case temperature	-55°C to +125°C
			-55°C to +85°C for full derating to MIL-STD-975

Electrical Performance $-55^{\circ}\text{C} \leq T_{\text{CASE}} \leq +125^{\circ}\text{C}$, $V_{\text{IN}} = 28\text{V} \pm 5\%$, $C_{\text{L}} = 0$ unless otherwise specified.

Parameter	Symbol	Test Conditions	Limit MIN	Limit MAX	Units
Output voltage accuracy ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{OUT}	$P_{\text{OUT}} = 30\text{ W}$, $T_{\text{C}} = +25^{\circ}\text{C}$	2.487 3.283 4.975 5.174 11.940 14.925	2.513 3.317 5.025 5.226 12.060 15.075	Vdc
Output power	P_{OUT}	18 Vdc < V_{IN} < 50Vdc	0	30	W
Output current ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	I_{OUT}	18 Vdc < V_{IN} < 50Vdc	0 0 0 0 0 0	12000 9090 6000 5770 2500 2000	mAdc
Line regulation Note 3	VR_{LINE}	18 Vdc < V_{IN} < 50Vdc, $0 < I_{\text{OUT}} < I_{\text{MAX}}$	-1.0	+1.0	%
Load regulation Note 4	VR_{LOAD}	18 Vdc < V_{IN} < 50Vdc, $0 < I_{\text{OUT}} < I_{\text{MAX}}$	-2.0	+2.0	%
Total regulation	VR	All conditions of Line, Load, Temperature, Radiation and End of Life	-4.0	+4.0	%
No-load input current	I_{IN}	$I_{\text{OUT}} = 0$ (Pin 3 open)	—	100	mA
		inhibited (Pin 3 shorted to pin 2)	—	8.0	
Output ripple and noise voltage Note 5 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	VR_{RIP}	18 Vdc < V_{IN} < 50Vdc, $I_{\text{OUT}} = I_{\text{MAX}}$		30 30 40 40 50 50	$\text{mV}_{\text{p,p}}$

For Notes to Specifications, refer to page 4

Electrical Performance $-55^{\circ}\text{C} \leq T_{\text{CASE}} \leq +125^{\circ}\text{C}$, $V_{\text{IN}} = 28\text{V} \pm 5\%$, $C_{\text{L}} = 0$ unless otherwise specified. (Continued)

Parameter	Symbol	Test Conditions	Limit MIN	Limit MAX	Units
Input ripple current Note 5	I_{RIP}	$18\text{ Vdc} < V_{\text{IN}} < 50\text{Vdc}$, $I_{\text{OUT}} = I_{\text{MAX}}$		100	$\text{mA}_{\text{p.p}}$
Switching frequency	F_{S}	Synchronization input open. (pin 6)	225	275	KHz
Efficiency ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	Eff	$I_{\text{OUT}} = I_{\text{MAX}}$, $T_{\text{C}} = +25^{\circ}\text{C}$	72 75 76 76 80 80		%
Enable Input open circuit voltage drive current (sink) voltage range			3.0 -0.5	5.0 100 50	V μA V
Synchronization Input frequency range pulse high level pulse low level pulse rise time pulse duty cycle		External clock signal on Sync. input (pin 4)	225 3.5 -0.5 40 20	310 10 0.25 80	KHz V V $\text{V}/\mu\text{s}$ %
Synchronization Output pulse high level		Signal compatible with Synchronization Input	3.7	4.3	V
Power dissipation, Short circuit ARH2802R5S ARH2803R3S & ARH2805S All Others	P_{D}	Short circuit on output		10 12 9.5	W
Output response to step load changes Note 8 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{TLD}	50% Load \Leftrightarrow 100% load	-200 -200 -200 -200 -300 -350	200 200 200 200 300 350	mV_{PK}
Recovery time from step load changes Notes 8, 9 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	T_{TLD}	50% Load \Leftrightarrow 100% load		200 200 200 200 200 200	μs
Output response to step line changes Notes 7, 10 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{TLN}	$I_{\text{OUT}} = I_{\text{MAX}}$, $V_{\text{IN}} = 18\text{ V}$ to/from 50 V	-180 -180 -250 -250 -450 -900	180 180 250 250 450 900	mV_{PK}

For Notes to Specifications, refer to page 4

Electrical Performance $-55^{\circ}\text{C} \leq T_{\text{CASE}} \leq +125^{\circ}\text{C}$, $V_{\text{IN}} = 28\text{V} \pm 5\%$, $C_L = 0$ unless otherwise specified. (Continued)

Parameter	Symbol	Test Conditions	Limit MIN	Limit MAX	Units
Recovery time from step line changes Notes 7, 9, 10 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	T_{TLN}	$I_{\text{OUT}} = I_{\text{MAX}}$, $V_{\text{IN}} = 18\text{ V}$ to/from 50 V		600 600 700 700 320 400	μs
Turn on overshoot	V_{OS}	$I_{\text{OUT}} = 10\%$ or 100% of I_{MAX}		5.0	% V_{out}
Turn on delay Note 11	T_{DLY}	$I_{\text{OUT}} = 10\%$ or 100% of I_{MAX}	2.0	20	ms
Capacitive load Notes 6, 7 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	CL	No effect on DC performance		1200 1200 1000 1000 180 120	μF
Isolation	ISO	500VDC Input to Output or any pin to case	100		$\text{M}\Omega$
Recovery from a short circuit	V_r	Output shorted, then open into max rated load current. $V_{\text{in}} = 28\text{ V}$		10	% of Rated Output Voltage
Overload Trip Current	Ovld	Maximum current at specified output voltage	105	135	% of Max Output Current

Notes to Specifications Tables

1. Operation outside absolute maximum/minimum limits may cause permanent damage to the device. Extended operation at the limits may permanently degrade performance and affect reliability.
2. Device performance specified in Electrical Performance table is guaranteed when operated within recommended limits. Operation outside recommended limits is not specified.
3. Parameter measured from 28 V to 18 V or to 50 V while load remains fixed at 10%, 50% and 100% of I_{MAX} .
4. Parameter measured from 50% to 10% or 100% of maximum load conditions while line remains fixed at 18, 28 or 50 volts.
5. Guaranteed for a bandwidth of DC to 20 Mhz. Tested using a 20 Khz to 2.0 Mhz bandwidth.
6. A capacitive load of any value from 0 to the specified maximum is permitted without compromise to DC performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's short circuit protection, causing erratic behavior during turn on.
7. Parameter is tested as part of design characterization or after design or process changes. Thereafter, parameters shall be guaranteed to the limits specified in the table.
8. Load transient rate of change, $di/dt \leq 2.0\text{ A}/\mu\text{s}$.
9. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within $\pm 1\%$ of its steady state value.
10. Line transient rate of change, $dv/dt \leq 50\text{ V}/\mu\text{s}$.
11. Turn on delay time is for either a step application of input power or a logical low to high transition on the enable pin (pin 3) while power is present at the input.

Group A Tests $V_{IN} = 28V$, $C_L = 0$ unless otherwise specified.

Test	Symbol	Test Conditions	Group A Subgroups	Limit MIN	Limit MAX	Units
Output voltage accuracy ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{OUT}	$I_{OUT} = I_{MAX}$, $T_C = 25^\circ C$	1	2.487 3.283 4.975 5.174 11.940 14.925	2.513 3.317 5.025 5.226 12.060 15.075	V
Output power Note 1	P_{OUT}	$V_{IN} = 18 V, 28V, 50 V$	1, 2, 3	0	30	W
Output current Note 1 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	I_{OUT}	$V_{IN} = 18 V, 28V, 50 V$	1, 2, 3	0 0 0 0 0 0	12000 9090 6000 5770 2500 2000	mA
Output regulation Note 4 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	VR	$I_{OUT} = 10\%, 50\%, 100\%$ of I_{MAX} $V_{IN} = 18 V, 28V, 50 V$	1, 2, 3	2.425 3.201 4.850 5.044 11.640 14.550	2.575 3.399 5.150 5.356 12.360 15.450	V
No Load Input Current	I_{IN}	$I_{OUT} = 0$, Pin 3 open Pin 3 shorted to pin 2 (disabled)	1, 2, 3 1, 2, 3		100 8.0	mA
Output ripple Note 2 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{RIP}	$V_{IN} = 18 V, 28V, 50 V$ $I_{OUT} = I_{MAX}$	1, 2, 3		30 30 40 40 50 50	mV _{p,p}
Switching frequency	F_S	Synchronization pin (pin 6) open	4, 5, 6	225	275	KHz
Input ripple Note 2	I_{RIP}	$V_{IN} = 18 V, 28V, 50 V$ $I_{OUT} = I_{MAX}$	1, 2, 3		100	mA _{p,p}
Recovery from a short circuit	Vr	Output shorted, then open into max rated load current. $V_{in} = 28 V$			5.0	% of Rated Output Voltage
Overload Trip Current	Ovld	Maximum current at specified output voltage	1, 2, 3	105	135	% of Max Output Current

For Notes to Group A Tests, refer to page 6

ARH28XXS Series

International
IRF Rectifier

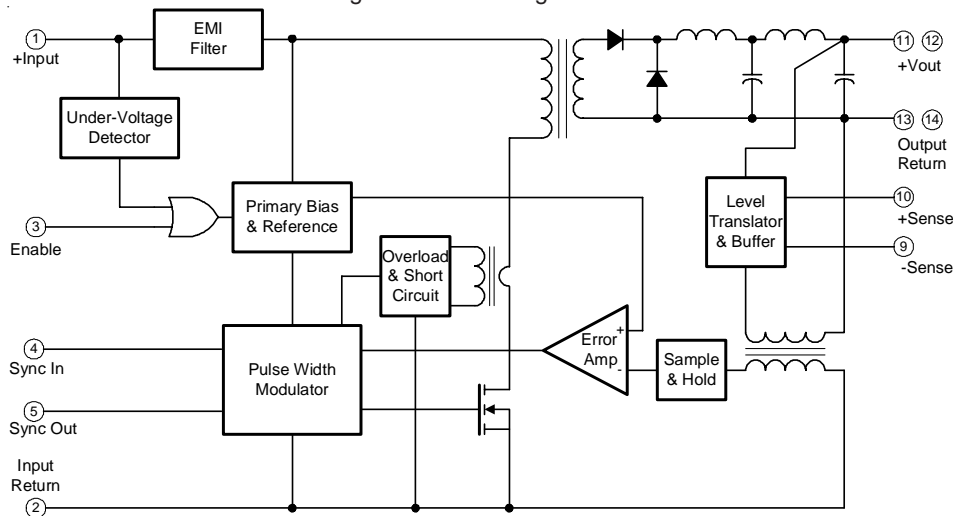
Group A Tests $V_{IN} = 28V$, $C_L = 0$ unless otherwise specified. (continued)

Test	Symbol	Test Conditions	Group A Subgroups	Limit MIN	Limit MAX	Units
Efficiency ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	Eff	$I_{OUT} = I_{MAX}$	1 2, 3	72 75 76 76 80 80 68 68 72 72 78 78		%
Power dissipation, Short circuit ARH2802R5S ARH2803R3S & ARH2805 All Others	P_D	Short circuit across output	1, 2, 3		10 12 9.5	W
Output response to step load changes Note 5 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	V_{TL}	50% Load to/from 100% load	4, 5, 6	-200 -200 -200 -200 -300 -350	200 200 200 200 300 350	mV _{PK}
Recovery from step load changes Notes 5, 6 ARH2802R5S ARH2803R3S ARH2805S ARH2805R2S ARH2812S ARH2815S	T_{TL}	50% Load to/from 100% load	4, 5, 6		200 200 200 200 200 200	μ s
Turn on overshoot	V_{OS}	$I_{OUT} = 10\%$ and 100%	4, 5, 6		5.0	% V_{OUT}
Turn on delay Note 7	T_{DLY}	$I_{OUT} =$ minimum and full rated	4, 5, 6	2.0	20	ms
Isolation	ISO	500VDC Input to output or any pin to case (except pin 12)	1	100		M Ω

Notes to Group A Test Table

- Parameter verified during dynamic load regulation tests.
- Guaranteed for DC to 20 MHz bandwidth. Test conducted using a 20KHz to 2.0MHz bandwidth.
- Deleted
- Output is measured for all combinations of line and load. Only the minimum and maximum readings for the output are recorded.
- Load step transition time $\geq 10\mu$ s.
- Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within $\pm 1\%$ of its steady state value.
- Turn on delay time is tested by application of a logical low to high transition on the enable pin (pin 3) with power present at the input.
- Subgroups 1 and 4 are performed at +25°C, subgroups 2 and 5 at +125°C and subgroups 3 and 6 at -55°C.

Figure I. Block Diagram



Circuit Operation and Application Information

The ARH28XXS series of converters have been designed using a single ended forward switched mode converter topology. (Refer to Figure I.) Single ended topologies enjoy certain advantages in radiation hardened designs in that they eliminate the possibility of simultaneous turn on of both switching elements during a radiation induced upset. In addition, single ended topologies are not subject to transformer saturation problems often associated with double ended implementations.

The design incorporates a two-stage LC input filter to attenuate input ripple current. A low overhead linear bias regulator provides both a bias voltage for the converter primary control logic and a stable, well-regulated reference for the error amplifier. Output control is realized using a wide band discrete pulse width modulator control circuit incorporating a unique non-linear ramp generator circuit. This circuit helps stabilize loop gain over variations in line voltage for superior output transient response. Nominal conversion frequency has been selected as 250 KHz to maximize efficiency and minimize magnetic element size.

Output voltages are sensed and fed back to the controller using a patented magnetic feedback circuit. This circuit is designed to be relatively insensitive to variations in temperature, aging, radiation and manufacturing tolerances making it particularly well suited to radiation hardened designs. The control logic has been designed to use only radiation tolerant components, and current paths include series resistances to limit photocurrents.

Other key circuit design features include output short circuit and overload protection, input undervoltage lockout and an external synchronization input port, permitting operation at an externally set clock rate. Alternately, a synchronization output is provided to lock frequencies with another converter when using more than one converter in a system.

Thermal Considerations

The ARH series of converters is capable of providing relatively high output power from a package of modest volume. The power density exhibited by these devices is obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. Good design practices have effectively addressed this requirement inside the device. However when operating at maximum loads, heat generated at the die junctions depends upon minimally restricted thermal conduction from the base plate for that heat to be carried away. To maintain case temperature at or below the specified maximum of 125°C, this heat can be transferred by attachment of the ARH28XXS to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Effectiveness of this heat transfer is dependent on the intimacy of the baseplate to heatsink interface. It is therefore suggested that a heat-transferring medium possessing good thermal conductivity be inserted between the baseplate and heatsink. A material utilized at the factory during testing and burn-in processes is sold under the

When an external frequency source is not available, an internal clock signal is provided through appropriate buffering at the sync out port. This port can drive a minimum of 3 ARH sync in ports thereby allowing all to operate at the same clock frequency.

Output Short Circuit Protection

Protection against accidental short circuits on the output is provided in the ARH28XXS converter. This protection is implemented by sensing primary switching current and reducing the switching pulse widths when a short occurs. The output current is therefore limited to a maximum value, which protects the converter. Under this condition the internal power dissipation is nearly the same as for maximum loading.

Input Undervoltage Protection

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to a nominal value of 16.8 volts. To preclude the possibility of noise or other voltage variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 1.0 volts is incorporated into this circuit. The converter is guaranteed to operate at 18 Volts input under all specified conditions.

Input Filter

To attenuate input ripple current, the ARH28XXS series converters incorporate a two-stage LC input filter illustrated in Figure III following. The elements of this filter comprise the dominant input load impedance characteristic, and therefore determine the nature of the current inrush at turn-on.

EMI Filtering

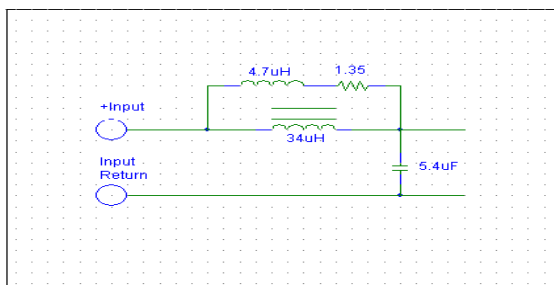
Although the internal filtering provided at both input and output terminals of the ARH series converters is sufficient for most applications, some critical applications may require additional filtering in order to accommodate particular system requirements.

While the internal input filter maintains input ripple current below $50 \text{ mA}_{\text{p-p}}$, an external filter can be applied to further attenuate this ripple to a level below the CE03 limits imposed by MIL-STD-461. International Rectifier currently supplies such a filter housed in a complementary package. The catalog number of this part is ARF461.

Output Noise

When attempting noise measurement at the output of switching converters, measurement techniques employed can have a significant influence on results during these tests. Any noise measurements should be undertaken only with test leads dressed as close to the device output pins as is physically possible. Probe ground leads should be kept to a minimum ($\ll 1''$) length to minimize the influence of parasitic impedances on results.

Figure III. Input Filter



Radiation Performance

The radiation tolerance characteristics inherent in the ARH28XXS converters are a result of a carefully planned ground-up design program with specific radiation design goals. Identification of the general circuit topology, a fundamental task in the design effort, was followed by selection of appropriate elements from a list of devices for which extensive radiation effects data was available. By imposing sufficiently large margins on those electrical parameters showing the worst case degrading effects of radiation, designers were able to select appropriate elements for incorporation into the circuit. Existing radiation data was utilized for input to PSPICE and RadSPICE in the generation of circuit performance verification analyses. Thus, electrical performance capability under all environmental conditions including radiation was well understood before first application of power to the inputs.

A principal design goal was achieving a converter topology that, because of large design margins, had radiation performance essentially independent of radiation induced element-lot performance variations. Where such margins cannot be assured, element lots are either selected following RLAT characterization as radiation hard devices or, purchased as radiation hard devices so that realization of the design goals are maintained.

The following table specifies guaranteed minimum radiation exposure levels tolerated while maintaining specification limits.

Radiation Specification $T_{case} = 25^{\circ}C$

Test	Conditions	Min	Typ	Max	Unit
Total Ionizing Dose (2:1 Margin)	MIL-STD-883, Method 1019.4 Operating bias applied during exposure	100	500		Krads (Si)
Dose Rate Temporary Saturation Survival	MIL-STD-883, Method 1021	1E8 1E11			Rads (Si)/sec
Heavy Ions (Single event effects)	BNL Dual Van de Graf Generator	83			MeV• cm ² /mg

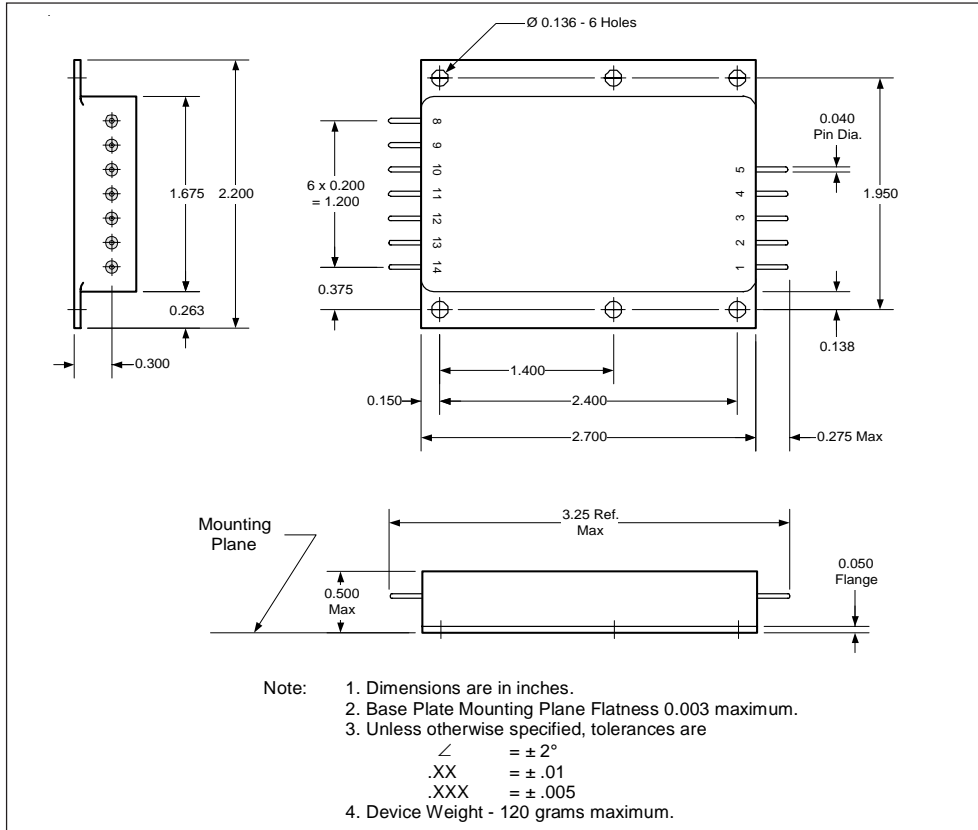
International Rectifier currently does not have a DSCC certified Radiation Hardness Assurance Program.

Standard Quality Conformance Inspections on ARH28XXS Series (Flight Screened)

Inspection	Application	Samples
Group A	Part of Screening on Each Unit	100%
Group B	Each Inspection Lot	* 5 units
Group C	First Inspection Lot or Following Class 1 Change	10 units
Group D	In Line (Part of Element Evaluation)	3 units

* Group B quantity for option 2 End of Line QCI. No Group B samples required for Option 1, In-line.

Mechanical Outline



Pin Designation

Pin #	Designation
1	+ Input
2	Input Return
3	Enable
4	Sync In
5	Sync Out
8	Chassis
9	-Sense
10	+Sense
11	+V Output
12	+V Output
13	Output Return
14	Output Return

Device Screening

Requirement	MIL-STD-883 Method	No Suffix ②	CK ②	EM
Temperature Range	—	-55°C to +85°C	-55°C to +85°C	-55°C to +85°C
Element Evaluation	MIL-PRF-38534	Class K	Class K	N/A
Non-Destructive Bond Pull	2023	Yes	Yes	N/A
Internal Visual	2017	Yes	Yes	①
Temperature Cycle	1010	Cond C	Cond C	Cond C
Constant Acceleration	2001, Y1 Axis	3000 Gs	3000 Gs	3000 Gs
PIND	2020	Cond A	Cond A	N/A
Burn-In	1015	320 hrs @ 125°C (2 x 160 hrs)	320 hrs @ 125°C (2 x 160 hrs)	48 hrs @ 125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	-55°C, +25°C, +85°C	-55°C, +25°C, +85°C	-55°C, +25°C, +85°C
PDA	MIL-PRF-38534	2%	2%	N/A
Seal, Fine and Gross	1014	Cond A, C	Cond A, C	Cond A
Radiographic	2012	Yes	Yes	N/A
External Visual	2009	Yes	Yes	①

Notes:

① Best commercial practice.

② CK is DSCC class K compliant without radiation performance. No Suffix is a radiation rated device but not available as a DSCC qualified SMD per MIL-PRF-38534.

International Rectifier currently does not have a DSCC certified Radiation Hardness Assurance Program.

Standard Microcircuit Drawing Equivalence Table

Standard Microcircuit Drawing Number	IR Standard Part Number
5962-04232	ARH2805S
5962-04233	ARH2803R3S

