



PRELIMINARY

CY62127DV18

MoBL2[®]

1 Mb (64K x 16) Static RAM

Features

- **Very high speed: 55 ns**
- **Voltage range: 1.65V to 2.2V**
- **Ultra-low active power**
 - Typical active current: 0.5 mA @ f = 1 MHz
 - Typical active current: 3.75 mA @ f = f_{MAX}
- **Ultra-low standby power**
- **Easy memory expansion with CE and OE features**
- **Automatic power-down when deselected**
- **Packages offered in a 48-ball FBGA and a 44-lead TSOP Type II**

Functional Description^[1]

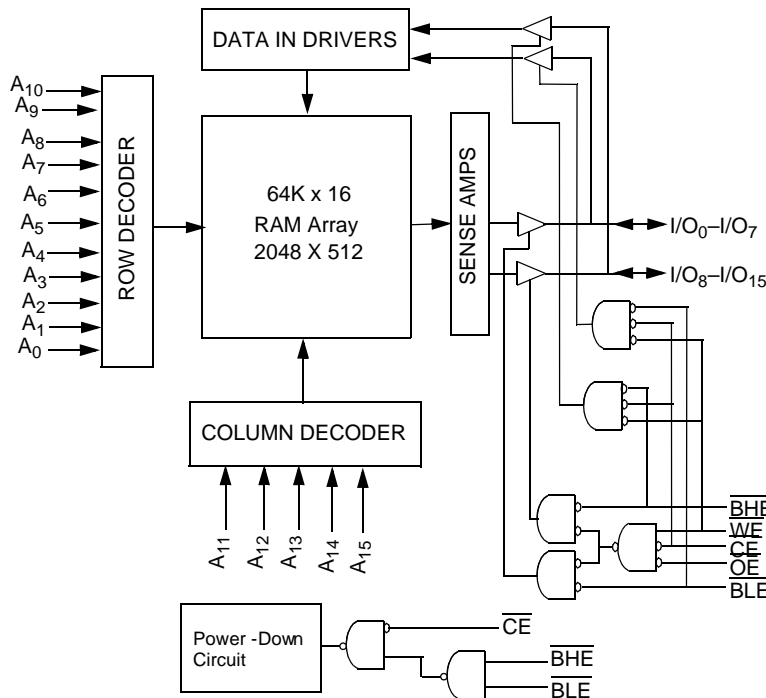
The CY62127DV18 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces

power consumption by 99% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable (CE) HIGH or both BHE and BLE are HIGH. The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected Chip Enable (CE) HIGH, outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH) or during a write operation (Chip Enable (CE) LOW and Write Enable (WE) LOW).

Writing to the device is accomplished by taking Chip Enable (CE) LOW and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇) pins (A₀ through A₁₅). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address.

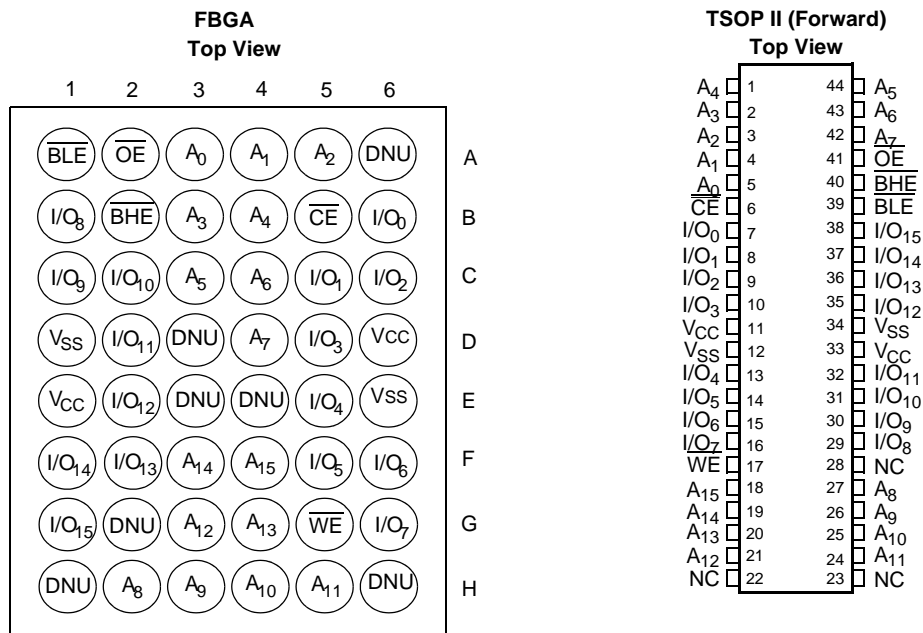
Reading from the device is accomplished by taking Chip Enable (CE) LOW and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write operations.

Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2]

Note:

2. E3 (DNU) can be left as NC or V_{SS} to ensure proper operation. or left open(Expansion Pins E4 - 2M, D3 - 4M, H1 - 8M, G2 - 16M, H6 - 32M)., NC Pins are not connected to the die.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied..... -55°C to +125°C
 Supply Voltage to Ground Potential. -0.2V to V_{CCMAX} + 0.2V
 DC Voltage Applied to Outputs in High-Z State^[3] -0.2V to V_{CC} + 0.2V

DC Input Voltage^[3] -0.2V to V_{CC} + 0.2V
 Output Current into Outputs (LOW)..... 20 mA
 Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
 Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Industrial	-40°C to +85°C	1.65V to 2.2V

Product Portfolio

Product	V _{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
					f = 1 MHz		f = f _{MAX}			
					Min.	Typ.	Max.	Typ. ^[4]	Max.	Typ. ^[4]
CY62127DV18L	1.65	1.8	2.2	55	0.5	1.5	3.75	7.5	0.5	5
CY62127DV18LL				55	0.5	1.5	3.75	7.5	0.5	4

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62127DV18-55			Unit
			Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA			0.2	V
V _{IH}	Input HIGH Voltage		1.4		V _{CC} + 0.2	V
V _{IL}	Input LOW Voltage		-0.2		0.4	V
I _{Ix}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} f = 1 MHz		3.75 0.5	7.5 1.5	mA
I _{SB1}	Automatic CE Power-down Current – CMOS Inputs	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE)	L	0.5	5	μA
			LL	0.5	4	
I _{SB2}	Automatic CE Power-down Current – CMOS Inputs	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} =2.2V	L	0.5	5	μA
			LL	0.5	4	

Capacitance^[5]

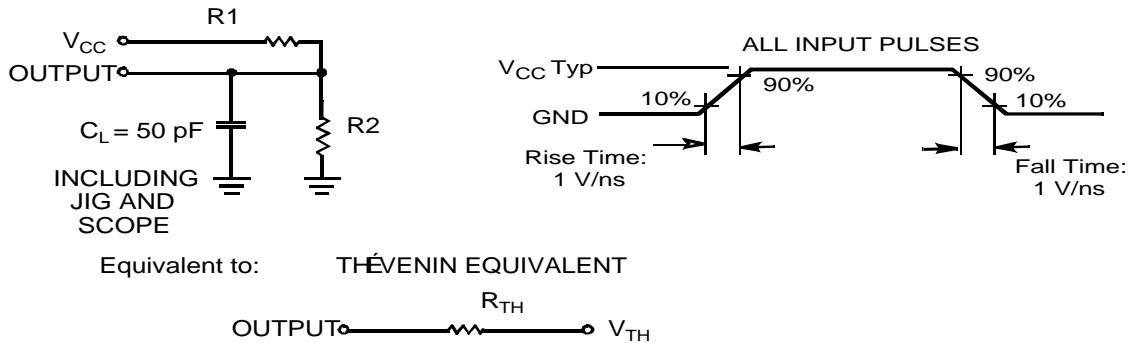
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	TA = 25°C, f = 1 MHz	8	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

Thermal Resistance

Parameter	Description	Test Conditions	FBGA	TSOP II	Unit
θ _{JA}	Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	76	°C/W
θ _{JC}	Thermal Resistance (Junction to Case) ^[5]		12	11	°C/W

Notes:

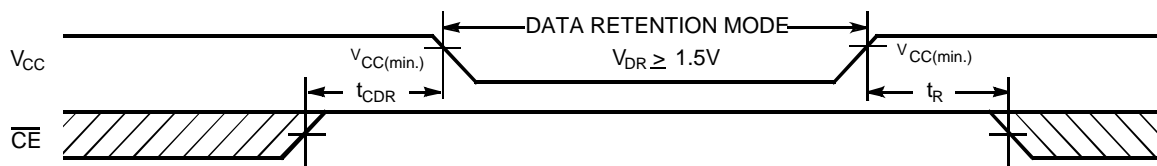
- V_{IL(min.)} = -1.0V for pulse durations less than 20 ns., V_{IH(max.)} = V_{CC}+0.5V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Parameters	1.8V	UNIT
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Data Retention Characteristics

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1		2.2	V
I_{CCDR}	Data Retention Current	$V_{CC}=1.5V, CE \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L		4	μA
			LL		3	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		100			μs

Data Retention Waveform^[7]

Notes: </>

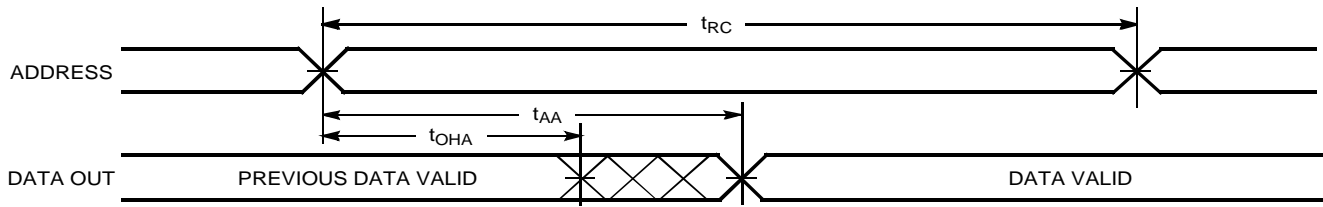
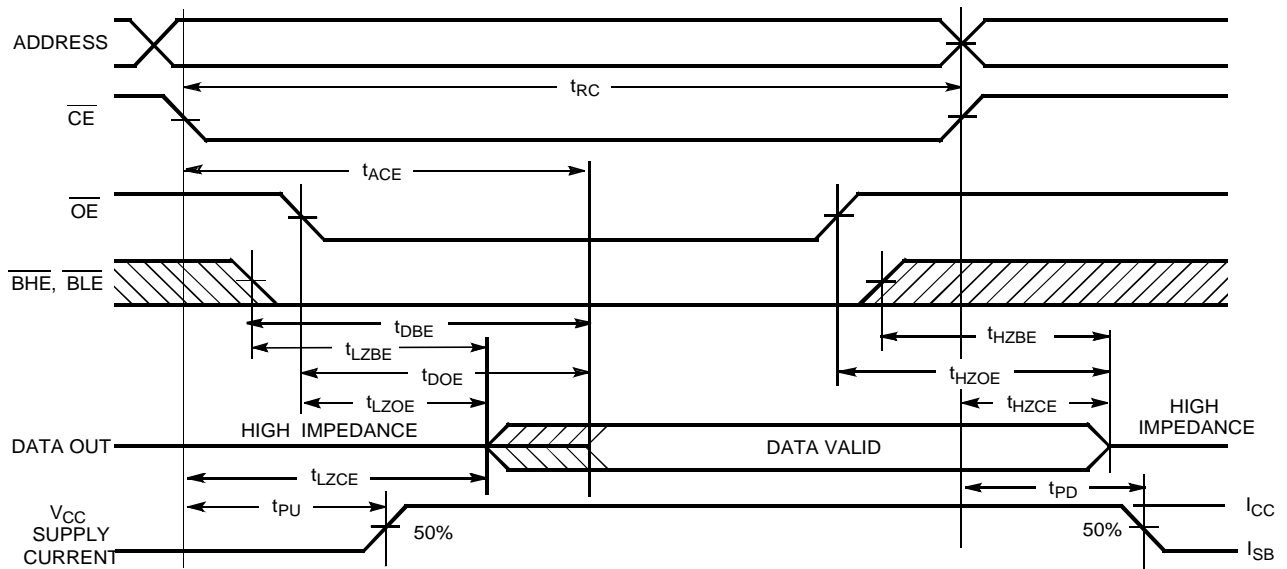
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100 \mu s$.
- $\overline{BHE} \cdot \overline{BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Chip can be deselected by either disabling the Chip Enable signals or by disabling both

Switching Characteristics (Over the Operating Range)^[8]

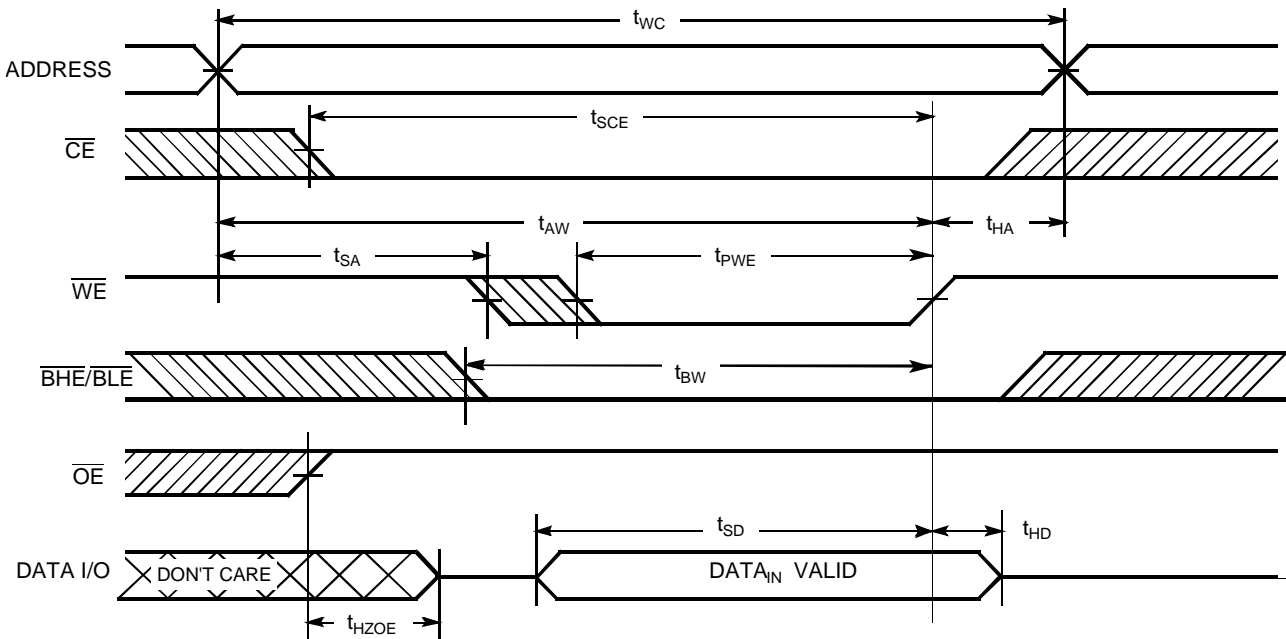
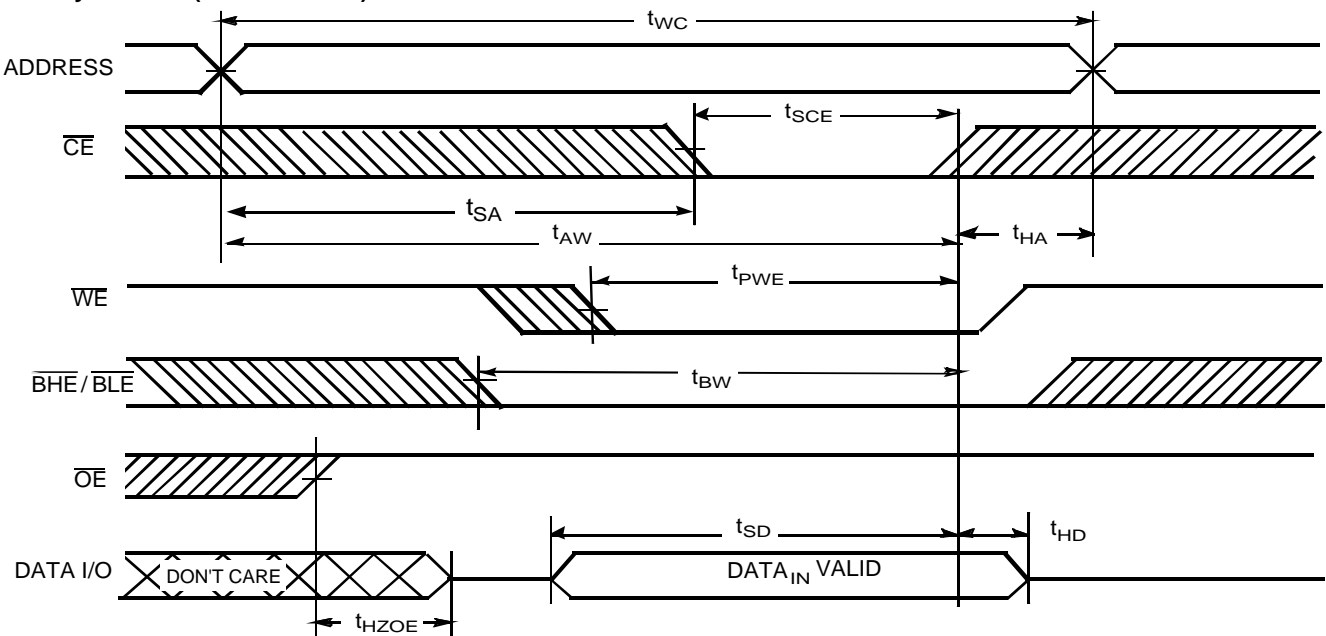
Parameter	Description	CY62127DV18-55		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	CE LOW to Data Valid		55	ns
t_{DOE}	OE LOW to Data Valid		25	ns
t_{LZOE}	OE LOW to Low Z ^[9]	5		ns
t_{HZOE}	OE HIGH to High Z ^[9,11]		20	ns
t_{LZCE}	CE LOW to Low Z ^[9]	10		ns
t_{HZCE}	CE HIGH to High Z ^[9,11]		20	ns
t_{PU}	CE LOW to Power-up	0		ns
t_{PD}	CE HIGH to Power-down		55	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55	ns
t_{LZBE} ^[10]	BLE/BHE LOW to Low Z ^[9]	5		ns
t_{HZBE}	BLE/BHE HIGH to High-Z ^[9,11]		20	ns
Write Cycle^[12]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	CE LOW to Write End	40		ns
t_{AW}	Address Set-up to Write End	40		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	WE Pulse Width	40		ns
t_{BW}	BLE/BHE LOW to Write End	40		ns
t_{SD}	Data Set-up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	WE LOW to High Z ^[9,11]		20	ns
t_{LZWE}	WE HIGH to Low Z ^[9]	10		ns

Notes:

8. Test conditions assume signal transition time of 1V/ns or less, timing reference levels of VCC(typ.)/2, input pulse levels of 0 to VCC(typ.), and output loading of the specified IOL/IOH and 50 pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} .
10. If both byte enables are toggled together, this value is 10 ns.
11. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. The internal Write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE and/or BLE = V_{IL}. All signal

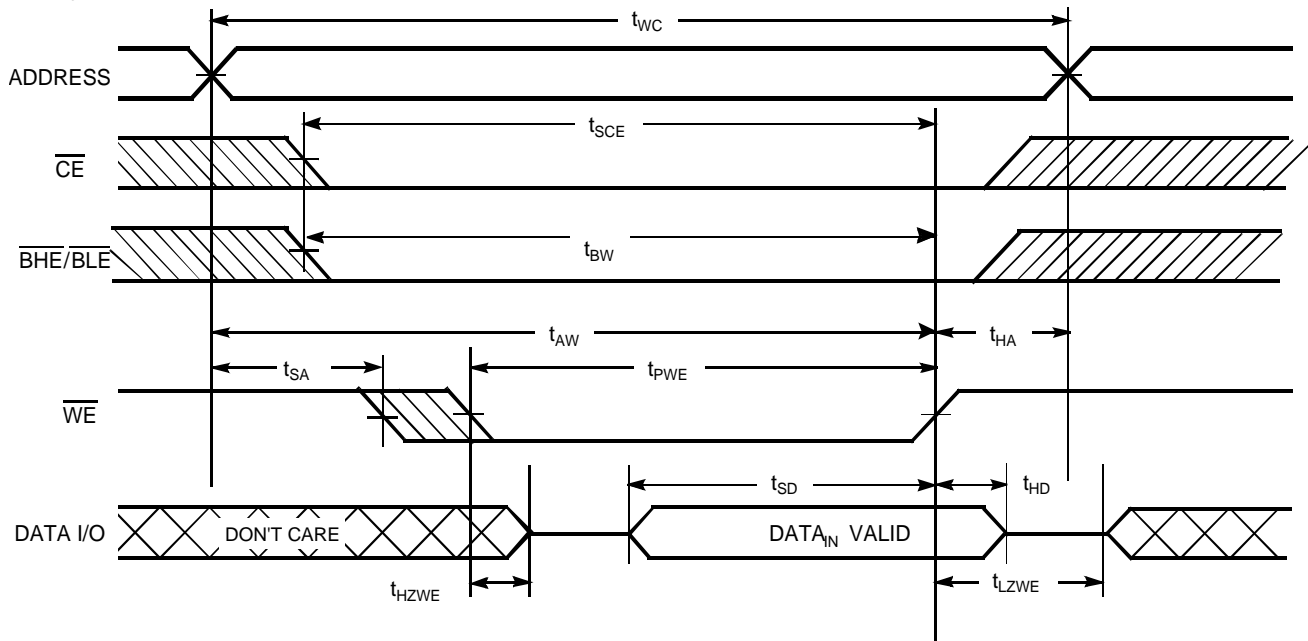
Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[13,14]

Read Cycle No. 2 (\overline{OE} Controlled)^[14,15]

Notes:

13. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} , \overline{BHE} , \overline{BLE} = V_{IL} .
14. \overline{WE} is HIGH for Read cycle.
15. Address valid prior to or coincident with \overline{CE} , \overline{BHE} , \overline{BLE} transition LOW.

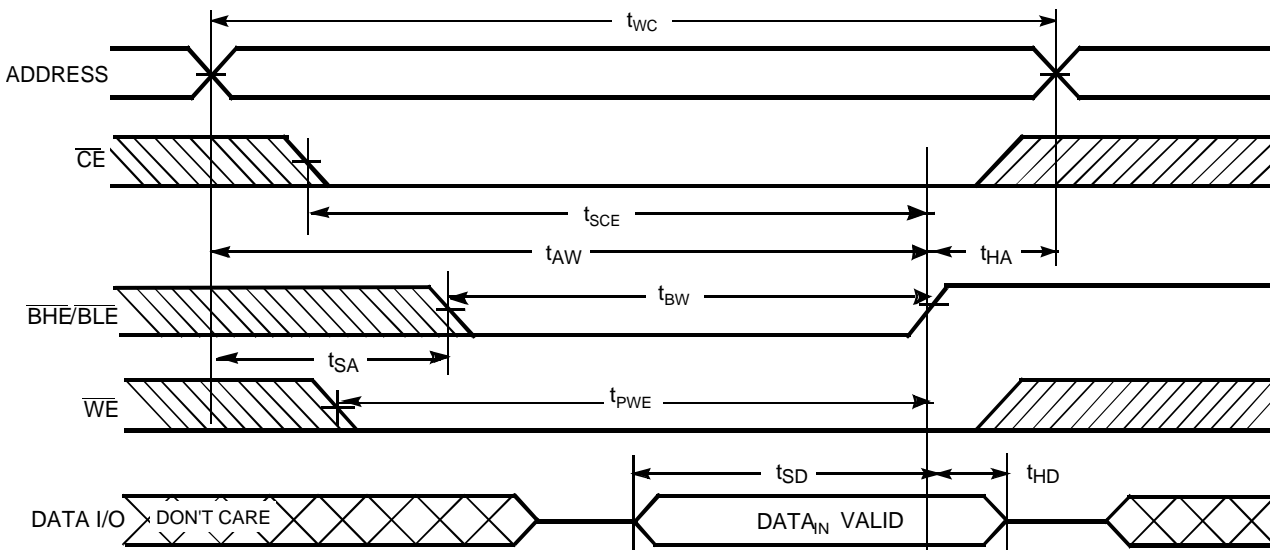
Write Cycle No. 1 (\overline{WE} Controlled) [11,12, 16, 17, 18]

Write Cycle No. 2 (\overline{CE} Controlled) [11,12, 16, 17, 18]

Notes:

16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[17, 18]



Write Cycle No. 4 ($\overline{BHE/}$ BLE $\overline{}$ Controlled, \overline{OE} $\overline{}$ LOW) $\overline{}$ ^[17, 18]

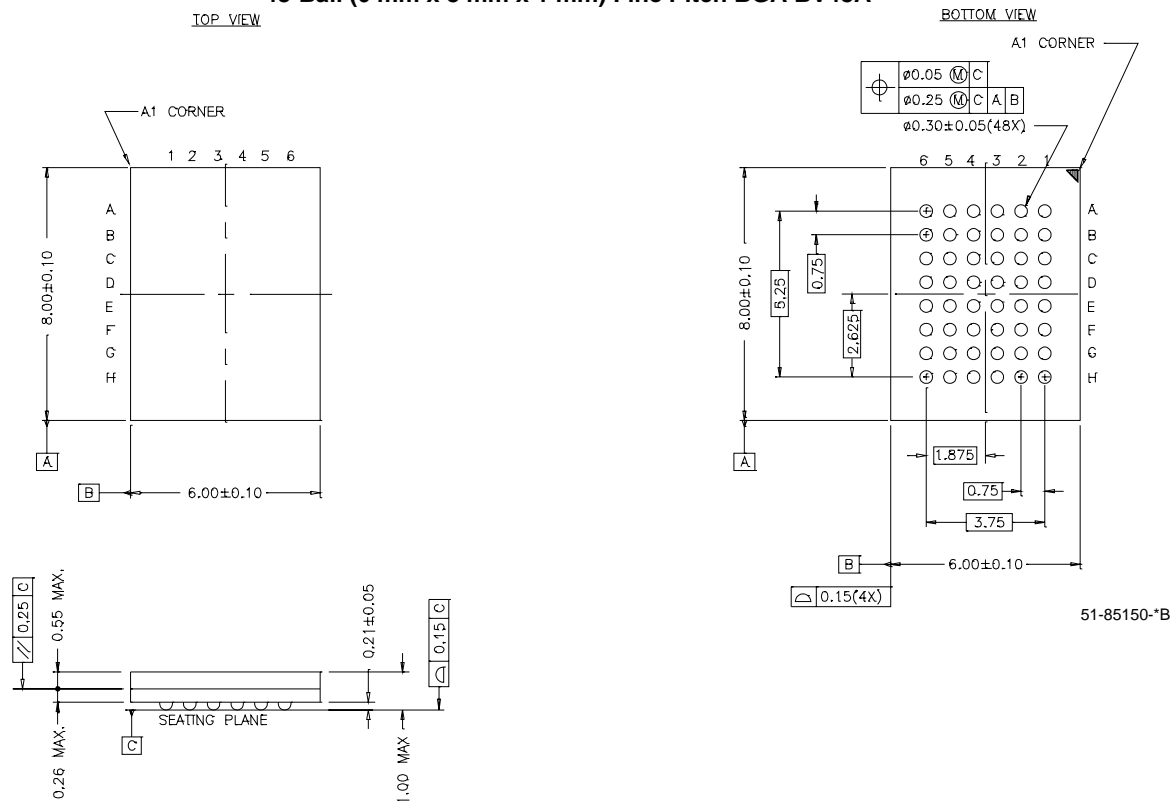


Truth Table

X	X	X	H	H	High Z	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out	Data Out	Read All bits	Active (I_{CC})
L	H	L	H	L	Data Out	High Z	Read Lower Byte Only	Active (I_{CC})
L	H	L	L	H	High Z	Data Out	Read Upper Byte Only	Active (I_{CC})
L	H	H	L	L	High Z	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In	Data In	Write	Active (I_{CC})
L	L	X	H	L	Data In	High Z	Write Lower Byte Only	Active (I_{CC})
L	L	X	L	H	High Z	Data In	Write Upper Byte Only	Active (I_{CC})

Ordering Information

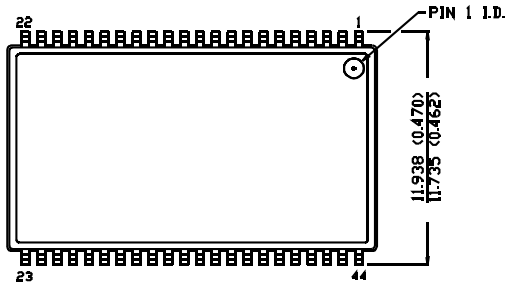
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62127DV18L-55BVI	BV48A	48-ball Fine Pitch BGA (6mm x 8mm x 1mm)	Industrial
	CY62127DV18LL-55BVI	BV48A	48-ball Fine Pitch BGA (6mm x 8mm x 1mm)	
	CY62127DV18L-55ZI	Z44	44-Lead TSOP Type II	
	CY62127DV18LL-55ZI	Z44	44-Lead TSOP Type II	

Package Diagrams
48-Ball (6 mm x 8 mm x 1 mm) Fine Pitch BGA BV48A


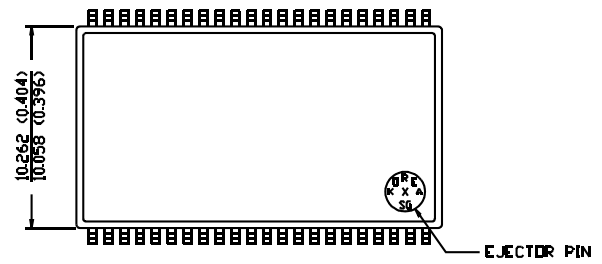
Package Diagrams (continued)

44-Pin TSOP II Z44

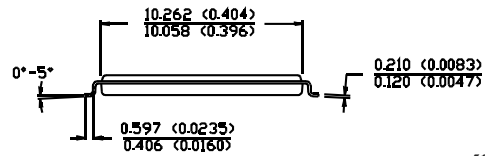
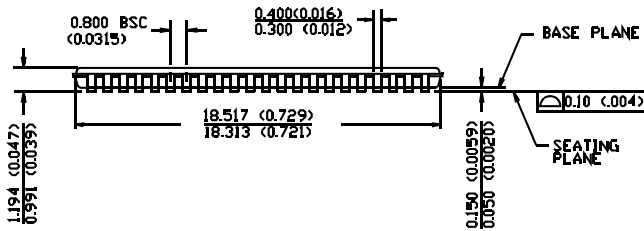
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY62127DV18 MoBL2[®] 1 Mb (64K x 16) Static RAM				
Document Number: 38-05226				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	118006	10/01/02	CDY	New Data Sheet
*A	127312	06/17/03	MPR	Changed status from Advance Information to Preliminary Changed Isb2 to 5 uA(L), 4 uA(LL) Changed lccdr to 4 uA(L), 3 uA(LL) Changed Cin from 6 pF to 8 pF