KAD5610P Preliminary KENET

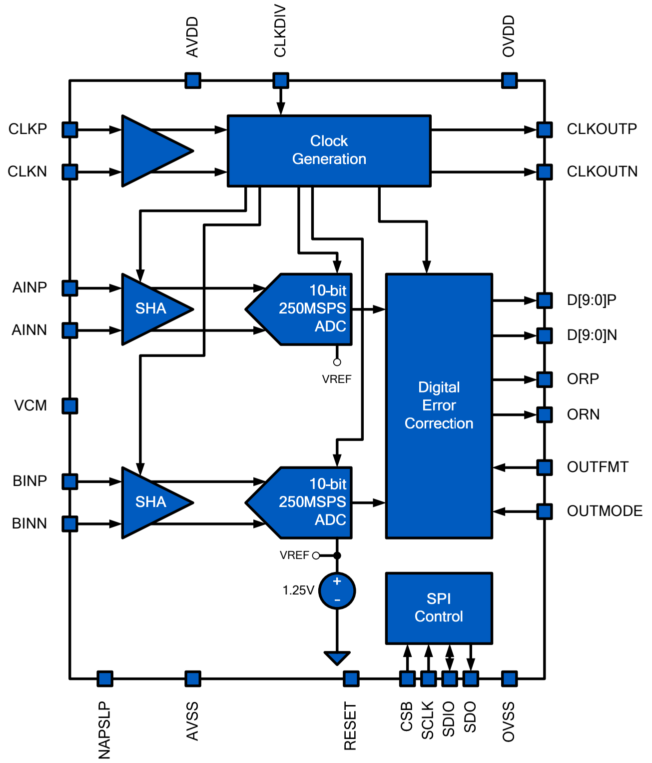
Dual 10-Bit, 250/210/170/125MSPS A/D Converter

General Description

The KAD5610P is a family of low-power, high-performance, dual-channel 10-bit, analog-to-digital converters. Designed with Kenet's proprietary *FemtoCharge®* technology on a standard CMOS process, the family supports sampling rates of up to 250MSPS. The KAD5610P-25 is the fastest member of this pin-compatible family, which also features sample rates of 210MSPS (KAD5610P-21), 170MSPS (KAD5610P-17) and 125MSPS (KAD5610P-12).

A serial peripheral interface (SPI) port allows for extensive configurability, as well as fine control of gain, skew and offset matching between the two converter cores.

Digital output data is presented in selectable LVDS or CMOS formats. The KAD5610P is available in a 72-contact QFN package with an exposed paddle. Performance is specified over the full industrial temperature range (-40 to +85°C).



Features

- **Programmable gain, offset and skew control**
- **1.3 GHz analog input bandwidth**
- **52fs Clock Jitter**
- **Over-range indicator**
- **Selectable Clock Divider: ÷1, ÷2 or ÷4**
- **Clock Phase Selection**
- **Nap and Sleep modes**
- **Two's complement, Gray code or Binary data format**
- **DDR LVDS-compatible or LVCMOS outputs**
- **Programmable Built-in Test Patterns**
- **1.8V Analog and Digital Supplies**

Applications

- **Power Amplifier Linearization**
- **Radar and Satellite Antenna Array Processing**
- **Broadband Communications**
- **High-Performance Data Acquisition**
- **Communications Test Equipment**
- **WiMAX and Microwave Receivers**

Key Specifications

- **SNR = 60.3dBFS for f_{IN} = 124MHz (-1dBFS)**
- **SFDR = 80dBc for f_{IN} = 124MHz (-1dBFS)**
- **Power consumption**
  - **400mW @ 250MSPS**
  - **312mW @ 125MSPS**

Pin-Compatible Family

Model	**Resolution**	**Speed (MSPS)**
KAD5612P-25	12	250
KAD5612P-21	12	210
KAD5612P-17	12	170
KAD5612P-12	12	125
KAD5610P-25	10	250
KAD5610P-21	10	210
KAD5610P-17	10	170
KAD5610P-12	10	125

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Electrical Specifications

All specifications apply under the following conditions unless otherwise noted: AVDD = 1.8V, OVDD = 1.8V, T_A = -40°C to +85°C, A_{IN} = -1dBFS, f_{SAMPLE} = Maximum Conversion Rate (per speed grade).

DC Specifications

			KAD5610P-25			**KAD5610P-21**			**KAD5610P-17**			**KAD5610P-12**			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Analog Input															
Full-Scale Analog Input Range	V_{FS}	Differential	1.38	1.45	1.59	1.38	1.45	1.59	1.38	1.45	1.59	1.38	1.45	1.59	V_{PP}
Input Resistance	R_{IN}	Differential		1000			1000			1000			1000		Ω
Input Capacitance	C_{IN}	Differential		4			4			4			4		pF
Full Scale Range Temp. Drift	A_{VTC}	Full Temp		90			90			90			90		ppm/°C
Input Offset Voltage	V_{OS}			±1.5			±1.5			±1.5			±1.5		mV
Gain Error	E_G			±0.6			±0.6			±0.6			±0.6		%
Common-Mode Output Voltage	V_{CM}			0.535			0.535			0.535			0.535		V
Power Requirements															
1.8V Analog Supply Voltage	AVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
1.8V Digital Supply Voltage	OVDD		1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
1.8V Analog Supply Current	I_{AVDD}			157	TBD		142	TBD		130	TBD		116	TBD	mA
1.8V Digital Supply Current	I_{OVDD}			65.0	TBD		63.6	TBD		60.7	TBD		57.2	TBD	mA
Power Supply Rejection Ratio	PSRR			-53			-53			-53			-53		dBFS
Power Dissipation															
Normal Mode	P_D			400	TBD		371	TBD		345	TBD		312	TBD	mW
Nap Mode	P_D			40	TBD		40	TBD		40	TBD		40	TBD	mW
Sleep Mode	P_D			10	TBD		10	TBD		10	TBD		10	TBD	mW

AC Specifications

			KAD5610P-25			KAD5610P-21			KAD5610P-17			KAD5610P-12			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Differential Nonlinearity	DNL	f_{IN} = 10MHz	TBD		TBD	TBD		TBD	TBD		TBD	TBD		TBD	LSB
Integral Nonlinearity	INL	f_{IN} = 10MHz	TBD		TBD	TBD		TBD	TBD		TBD	TBD		TBD	LSB
Minimum Conversion Rate	f_S MIN				TBD			TBD			TBD			TBD	MSPS
Maximum Conversion Rate	f_S MAX		250			210			170			125			MSPS
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz		60.4											dBFS
		f_{IN} = 70MHz		60.3											dBFS
		f_{IN} = 140MHz	TBD	60.3		TBD			TBD			TBD			dBFS
		f_{IN} = 230MHz		60.2											dBFS
		f_{IN} = 400MHz		60.0			TBD			TBD			TBD		dBFS
		f_{IN} = 1000MHz		58.6			TBD			TBD			TBD		dBFS
Signal-to-Noise and Distortion	SINAD	f_{IN} = 10MHz		59.3											dBFS
		f_{IN} = 70MHz		59.2											dBFS
		f_{IN} = 140MHz	TBD	59.2		TBD			TBD			TBD			dBFS
		f_{IN} = 230MHz		59.1											dBFS
		f_{IN} = 400MHz		58.4			TBD			TBD			TBD		dBFS
		f_{IN} = 1000MHz		52.2			TBD			TBD			TBD		dBFS
Effective Number of Bits	ENOB	f_{IN} = 10MHz		9.6											Bits
		f_{IN} = 70MHz		9.5											Bits
		f_{IN} = 140MHz	TBD	9.5		TBD			TBD			TBD			Bits
		f_{IN} = 230MHz		9.5											Bits
		f_{IN} = 400MHz		9.4			TBD			TBD			TBD		Bits
		f_{IN} = 1000MHz		8.4			TBD			TBD			TBD		Bits
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz		84			84			85			85		dBc
		f_{IN} = 70MHz		84			83			82			83		dBc
		f_{IN} = 140MHz	TBD	80		TBD	80		TBD	80		TBD	79		dBc
		f_{IN} = 230MHz		79			77			77			79		dBc
		f_{IN} = 400MHz		71			TBD			TBD			TBD		dBc
		f_{IN} = 1000MHz		55			TBD			TBD			TBD		dBc
Intermodulation Distortion	IMD	f_{IN} = 10MHz		TBD			TBD			TBD			TBD		dBc
		f_{IN} = 70MHz		-83	TBD		TBD	TBD		TBD	TBD		TBD	TBD	dBc
		f_{IN} = 170MHz		-84			TBD			TBD			TBD		dBc
Two-Tone SFDR	2TSFDR	f_{IN} = 10MHz		TBD			TBD			TBD			TBD		dBc
		f_{IN} = 70MHz		TBD	TBD		TBD	TBD		TBD	TBD		TBD	TBD	dBc
		f_{IN} = 170MHz		TBD			TBD			TBD			TBD		dBc
Channel to Channel Isolation		f_{IN} = 10MHz		90			90			90			90		dB
		f_{IN} = 124MHz		90			90			90			90		dB
		f_{IN} = 170MHz		TBD			TBD			TBD			TBD		dB
Word Error Rate				10^{-12}			10^{-12}			10^{-12}			10^{-12}		
Full Power Bandwidth	FPBW			1.3			1.3			1.3			1.3		GHz

Digital Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Inputs						
Input Current High (RESETN)	I_{IH}	VIN = 1.8V	0	1	10	µA
Input Current Low (RESETN)	I_{IL}	VIN = 0V	25	50	75	µA
Input Current High (OUTMODE, NAP/SLP, CLKDIV, OUTFMT)	I_{IH}		TBD	25	TBD	µA
Input Current Low (OUTMODE, NAP/SLP, CLKDIV, OUTFMT)	I_{IL}		TBD	25	TBD	µA
Input Capacitance	C_{DI}			3		pF
LVDS Outputs						
Differential Output Voltage	V_T			210		mV
Output Offset Voltage	V_{OS}			TBD		mV
Output Rise Time	t_R			500		ps
Output Fall Time	t_F			500		ps
CMOS Outputs						
Voltage Output High	V_{OH}			OVDD-0.1		V
Voltage Output Low	V_{OL}			0.1		V
Output Rise Time	t_R			TBD		ns
Output Fall Time	t_F			TBD		ns

Timing Diagrams

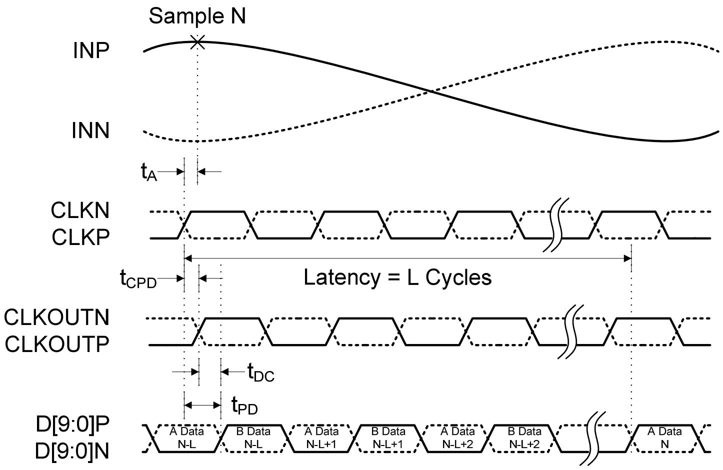


Figure 1. LVDS Timing Diagram—DDR

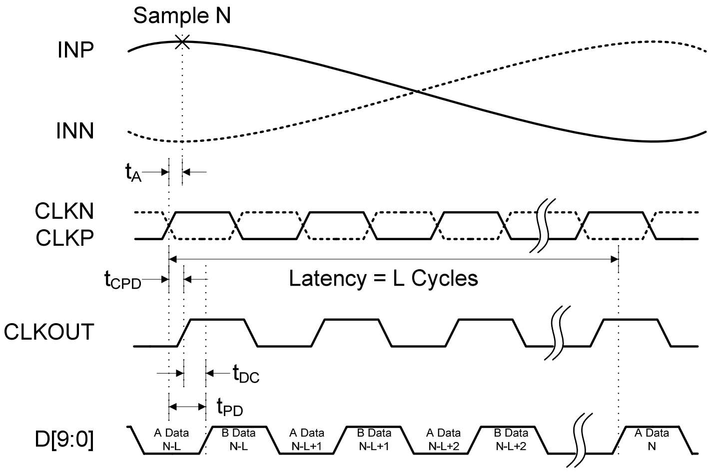


Figure 2. CMOS Timing Diagram—DDR

Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
ADC					
Aperture Delay	t_A		375		ps
RMS Aperture Jitter	j_A		52		fs
Input Clock to Output Clock Propagation Delay	t_{CPD}	TBD	TBD	TBD	ps
Input Clock to Data Propagation Delay	t_{PD}	TBD	TBD	TBD	ps
Output Clock to Data Propagation Delay	t_{DC}	TBD	TBD	TBD	ps
Latency (Pipeline Delay)	L		7.5		cycles
Over Voltage Recovery	t_{OVR}		1		cycles

Absolute Maximum Ratings[1]

Parameter	**Min**	**Max**	**Units**
AVDD to AVSS	-0.4	2.1	V
OVDD to OVSS	-0.4	2.1	V
AVSS to OVSS	-0.3	0.3	V
Analog Inputs to AVSS	-0.4	AVDD + 0.3	V
Clock Inputs to AVSS	-0.4	AVDD + 0.3	V
Logic Input to AVSS	-0.4	OVDD + 0.3	V
Logic Inputs to OVSS	-0.4	OVDD + 0.3	V
Operating Temperature	-40	85	°C
Storage Temperature	-65	150	°C
Junction Temperature		150	°C

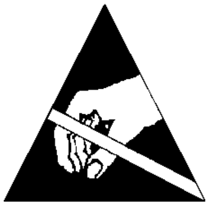
1. Exposing the device to levels in excess of the maximum ratings may cause permanent damage. Exposure to maximum conditions for extended periods may affect device reliability.

Thermal Impedance

Parameter	Symbol	Typ	Unit
Junction to Paddle[2]	Φ_{JP}	30	°C/W
Junction to Case[2]	Φ_{JC}	TBD	°C/W
Junction to Ambient[2]	Φ_{JA}	TBD	°C/W

2. Paddle soldered to ground plane.

ESD



Electrostatic charge accumulates on humans, tools and equipment and may discharge through any metallic package contacts (pins, balls, exposed paddle, etc.) of an integrated circuit. Industry-standard protection techniques have been utilized in the design of this product. However, reasonable care must be taken in the storage and handling of ESD sensitive products. Contact Kenet for the specific ESD sensitivity rating of this product.

Pin Descriptions

Pin #	LVDS [LVCMOS] Name	LVDS [LVCMOS] Function
1, 6, 19, 24, 71	AVDD	1.8V Analog Supply
2-5, 17, 18, 28-35	DNC	Do Not Connect
7, 10-12, 72	AVSS	Analog Ground
8, 9	BINP, BINN	B-Channel Analog Input Positive, Negative
13, 14	AINN, AINP	A-Channel Analog Input Negative, Positive
15	VCM	Common Mode Output
16	CLKDIV	Clock Divider Control
20, 21	CLKP, CLKN	Clock Input True, Complement
22	OUTMODE	Output Mode (LVDS, LVCMOS)
23	NAPSLP	Power Control (Nap, Sleep modes)
25	RESETN	Power On Reset (Active Low)
26, 45, 55, 65	OVSS	Output Ground
27, 36, 56	OVDD	1.8V Output Supply
37, 38	D0N, D0P [NC, D0]	LVDS Bit 0 (LSB) Output Complement, True [NC, LVCMOS Bit 0]
39, 40	D1N, D1P [NC, D1]	LVDS Bit 1 Output Complement, True [NC, LVCMOS Bit 1]
41, 42	D2N, D2P [NC, D2]	LVDS Bit 2 Output Complement, True [NC, LVCMOS Bit 2]
43, 44	D3N, D3P [NC, D3]	LVDS Bit 3 Output Complement, True [NC, LVCMOS Bit 3]
46	RLVDS	LVDS Bias Resistor (connect to OVSS with a 10kΩ, 1% resistor)
47, 48	CLKOUTN, CLKOUTP [NC, CLKOUT]	LVDS Clock Output Complement, True [NC, LVCMOS CLKOUT]
49, 50	D4N, D4P [NC, D4]	LVDS Bit 4 Output Complement, True [NC, LVCMOS Bit 4]
51, 52	D5N, D5P [NC, D5]	LVDS Bit 5 Output Complement, True [NC, LVCMOS Bit 5]
53, 54	D6N, D6P [NC, D6]	LVDS Bit 6 Output Complement, True [NC, LVCMOS Bit 6]
57, 58	D7N, D7P [NC, D7]	LVDS Bit 7 Output Complement, True [NC, LVCMOS Bit 7]
59, 60	D8N, D8P [NC, D8]	LVDS Bit 8 Output Complement, True [NC, LVCMOS Bit 8]
61, 62	D9N, D9P [NC, D9]	LVDS Bit 9 (MSB) Output Complement, True [NC, LVCMOS Bit 9]
63, 64	ORN, ORP [NC, OR]	LVDS Over Range Complement, True [NC, LVCMOS Over Range]
66	SDO	SPI Serial Data Output **(4.7kΩ pull-up to OVDD is required)**
67	CSB	SPI Chip Select (active low)
68	SCLK	SPI Clock
69	SDIO	SPI Serial Data Input/Output
70	OUTFMT	Output Data Format (Two's Comp., Gray Code, Offset Binary)
Exposed Paddle	AVSS	Analog Ground

LVCMOS Output Mode Functionality is shown in brackets (NC = No Connection)

Pin Configuration

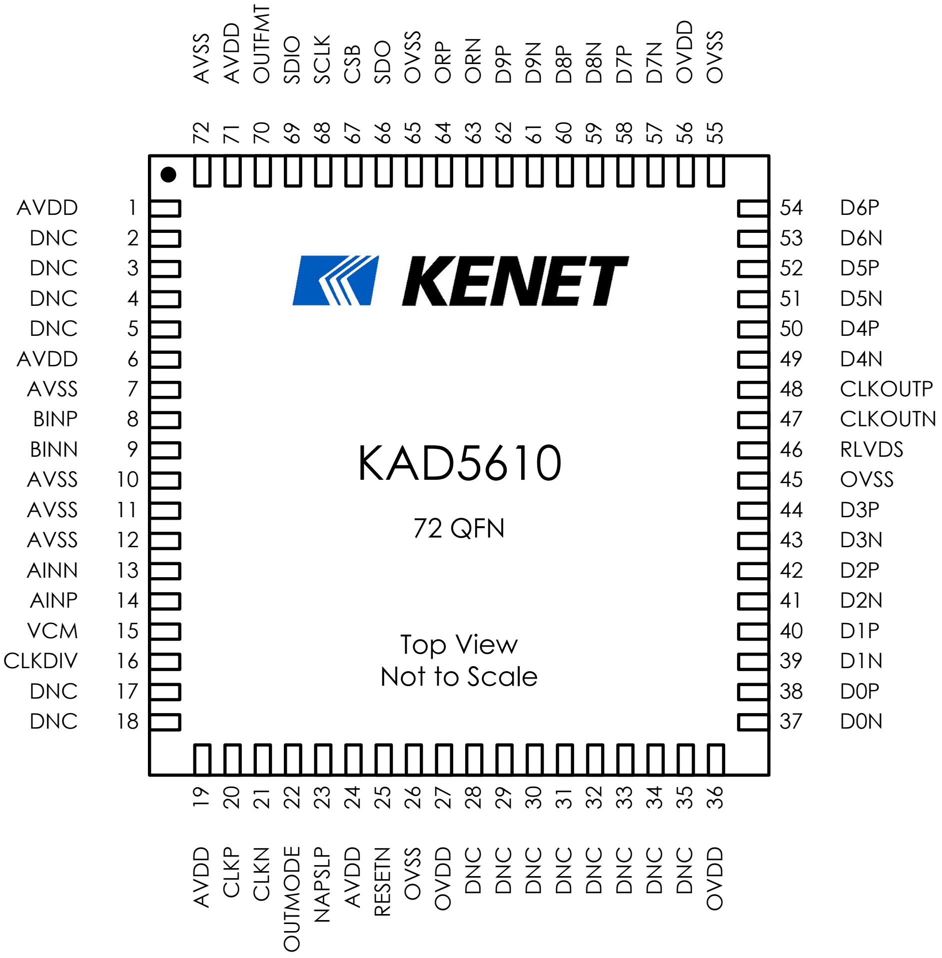


Figure 3. Pin Configuration

Typical Performance Curves

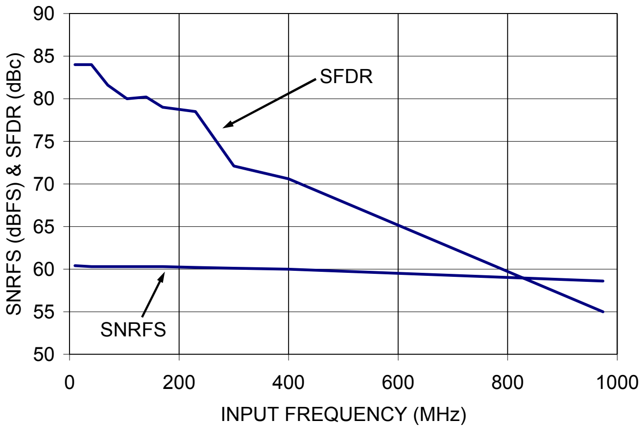


Figure 4. SNR & SFDR vs. f_{IN}

TBD

Figure 5. HD2 & HD3 vs. f_{IN}

TBD

Figure 6. SNR & SFDR vs. A_{IN}

TBD

Figure 7. HD2 & HD3 vs. A_{IN}

TBD

Figure 8. SNR & SFDR vs. f_{SAMPLE}

TBD

Figure 9. HD2 & HD3 vs. f_{SAMPLE}

Typical Performance Curves

TBD

Figure 10. Power vs. f_{SAMPLE}

TBD

Figure 11. Differential Nonlinearity

TBD

Figure 12. Integral Nonlinearity

TBD

Figure 13. SNR & SFDR vs. VCM

TBD

Figure 14. Noise Histogram

TBD

Figure 15. Single Tone Spectrum @ 10 MHz

Typical Performance Curves

TBD

Figure 16. Single Tone Spectrum @ 70 MHz

TBD

Figure 17. Single Tone Spectrum @ 140 MHz

TBD

Figure 18. Single Tone Spectrum @ 240 MHz

TBD

Figure 19. Single Tone Spectrum @ 500 MHz

TBD

Figure 20. Two-Tone Spectrum @ 10 MHz

TBD

Figure 21. Two-Tone Spectrum @ 70 MHz

Typical Performance Curves

TBD

Figure 22. Two-Tone Spectrum @ 140 MHz

TBD

Figure 23. Two-Tone Spectrum @ 240 MHz

TBD

Figure 24. Two-Tone Spectrum @ 500 MHz

TBD

Figure 25. SNR & SFDR vs. Temperature

TBD

Figure 26. SNR & SFDR vs. Power Supply Voltage

Functional Description

The KAD5610P is based upon a 10-bit, 250MSPS A/D converter core that utilizes a pipelined successive approximation architecture (Figure 27). The input voltage is captured by a Sample-Hold Amplifier (SHA) and converted to a unit of charge. Proprietary charge domain techniques are used to successively compare the input to a series of reference charges. Decisions made during the successive approximation operations determine the digital code for each input value. The converter pipeline requires six samples to produce a result. Digital error correction is also applied, resulting in a total latency of seven and a half clock cycles. This is evident to the user as a latency between the start of a conversion and the data being available on the digital outputs.

The device contains two A/D converter cores with carefully matched transfer characteristics. At start-up, each core performs a self-calibration to minimize gain and offset errors. The reset pin (RESETN) is initially set high at power-up and will remain in that state until the calibration is complete. The clock frequency should remain fixed during this time, and no SPI communications should be attempted. Recalibration can be initiated via the SPI port at any time after the initial self-calibration.

Power-On Calibration

At start-up, the core performs a self-calibration to minimize gain and offset errors. An internal power-on-reset (POR) circuit detects the supply voltage ramps and initiates the calibration when the analog and digital supply voltages are above a threshold. The following conditions must be adhered to for the power-on calibration to execute successfully:

- A frequency-stable conversion clock must be applied to the CLKP/CLKN pins
- DNC pins (especially 3, 4 and 18) must not be pulled up or down
- SDO (pin 66) must be high
- RESETN (pin 25) must begin low
- SPI communications must not be attempted

A user-initiated reset can subsequently be invoked in the event that the above conditions cannot be met at power-up.

The SDO pin requires an external 4.7kΩ pull-up to OVDD. If the SDO pin is pulled low externally during power-up, calibration will not be executed properly.

After the power supply has stabilized the internal POR releases RESETN and an internal pull-up pulls it high, which starts the calibration sequence. The RESETN pin should be connected to an open-drain driver with a drive strength of less than 0.5mA.

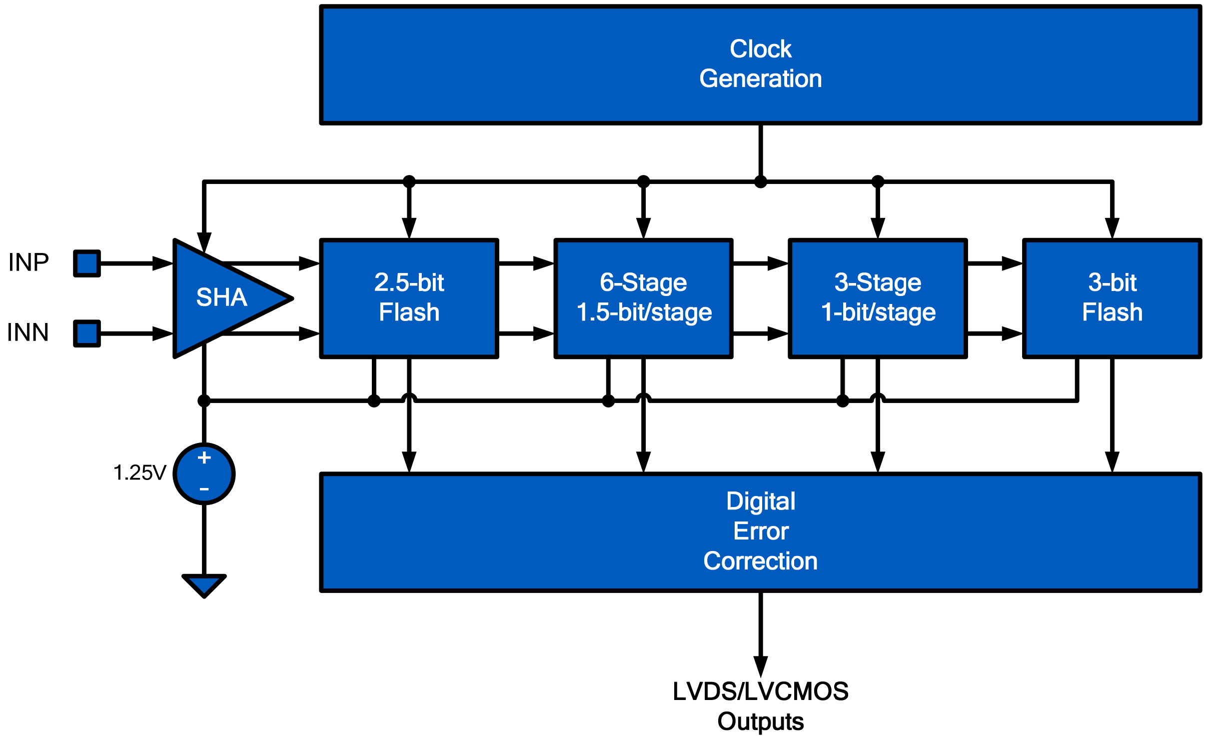


Figure 27. ADC Core Block Diagram

The calibration sequence is initiated on the rising edge of RESETN, as shown in Figure 28. The over-range output (OR) is set high once RESETN is pulled low, and remains in that state until calibration is complete. The OR output returns to normal operation at that time, so it's important that the analog input be within the converter's full-scale range in order to observe the transition. If the input is in an over-range condition the OR pin will stay high and it will not be possible to detect the end of the calibration cycle.

While RESETN is low, the output clock (CLKOUTP/CLKOUTN) stops toggling and is set low. Normal operation of the output clock resumes at the next input clock edge (CLKP/CLKN) after RESETN is deasserted. At 250MSPS the nominal calibration time is 300ms.

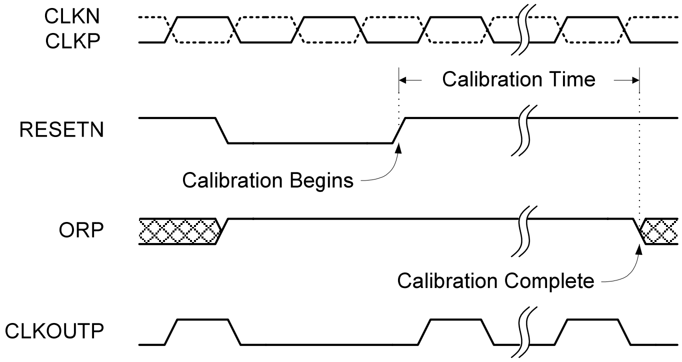


Figure 28. Calibration Timing

User-Initiated Reset

Recalibration of the ADC can be initiated at any time by driving the RESETN pin low for a minimum of one clock cycle. An open-drain driver with a drive strength of less than 0.5mA is recommended. As is the case during power-on reset, the SDO, RESETN and DNC pins must be in the proper state for the calibration to successfully execute.

Analog Input

Each ADC core contains a fully differential input (AINP/AINN, BINP/BINN) to the sample and hold amplifier (SHA). The ideal full-scale input voltage is 1.45V, centered at the VCM voltage of 0.535V as shown in Figure 29.

Best performance is obtained when the analog inputs are driven differentially. The common mode output voltage, VCM, should be used to properly bias the inputs as shown in Figures 30 through 32.

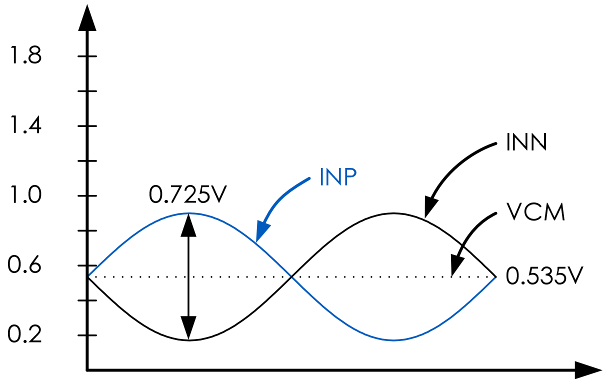


Figure 29. Analog Input Range

An RF transformer will give the best noise and distortion performance for wideband and/or high intermediate frequency (IF) inputs. Two different transformer input schemes are shown in Figures 30 and 31.

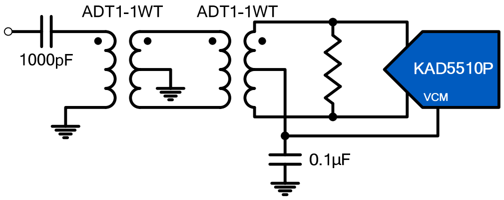


Figure 30. Transformer Input for General Purpose Applications

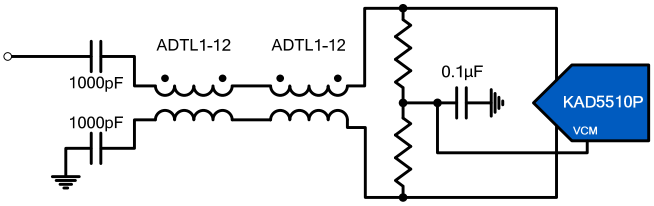


Figure 31. Transmission-line Transformer Input for High IF Applications

A back-to-back transformer scheme is used to improve common mode rejection, which keeps the common mode level of the input matched to VCM. The value of the shunt resistor should be determined based on the desired load impedance. The differential input resistance of the KAD5610P is 1000Ω.

The SHA design uses a switched capacitor input stage, which creates charge kick-back when the sampling capacitance is reconnected to the input voltage. This kick-back creates a disturbance at the input which must settle before the next sampling point. Lower source impedance will result in faster settling and improved performance. Therefore a 1:1 transformer and low shunt resistance are recommended for optimal performance.

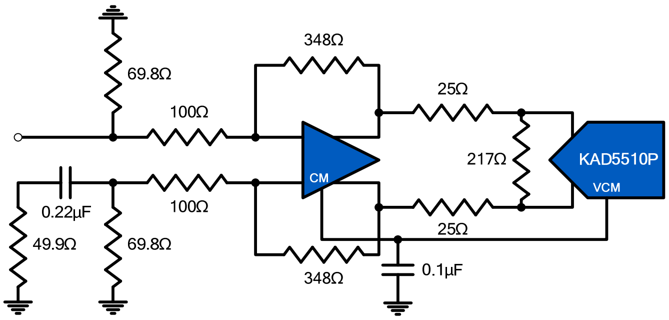


Figure 32. Differential Amplifier Input

A differential amplifier, as shown in Figure 32, can be used in applications that require dc-coupling. In this configuration the amplifier will typically dominate the achievable SNR and distortion performance.

Clock Input

The clock input circuit is a differential pair (see Figure 47). Driving these inputs with a high level (up to 1.8V_{PP} on each input) sine or square wave will provide the lowest jitter performance. A transformer with 4:1 impedance ratio will provide increased drive levels.

The recommended drive circuit is shown in Figure 33. The clock can be driven single-ended, but this will reduce the edge rate and may impact SNR performance. The clock inputs are internally self-biased to AVDD/2 to facilitate ac coupling.

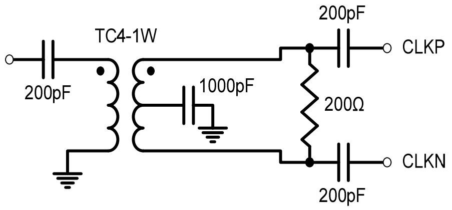


Figure 33. Recommended Clock drive

A selectable 2X/4X divider is provided in series with the clock input. The divider can be used in the 2X mode with a sample clock equal to twice the desired sample rate. This will result in a clock input with 50% duty cycle and will maximize the converter's performance.

CLKDIV Pin	Divide Ratio
AVSS	2
Float	1
AVDD	4

Table 1. CLKDIV Pin Settings

The clock divider can also be controlled through the SPI port, which overrides the CLKDIV pin setting. Details on this are contained in the **Serial Peripheral Interface** section.

A delay-locked loop (DLL) generates internal clock signals for various stages within the charge pipeline. If the frequency of the input clock changes, the DLL may take up to 52µs to regain lock at 250MSPS. The lock time is inversely proportional to the sample rate.

Jitter

In a sampled data system, clock jitter directly impacts the achievable SNR performance. The theoretical relationship between clock jitter (t_J) and SNR is shown in Equation 1 and is illustrated in Figure 34.

$$SNR = 20\log_{10}\left(\frac{1}{2\pi f_{IN} t_J}\right)$$

Equation 1.

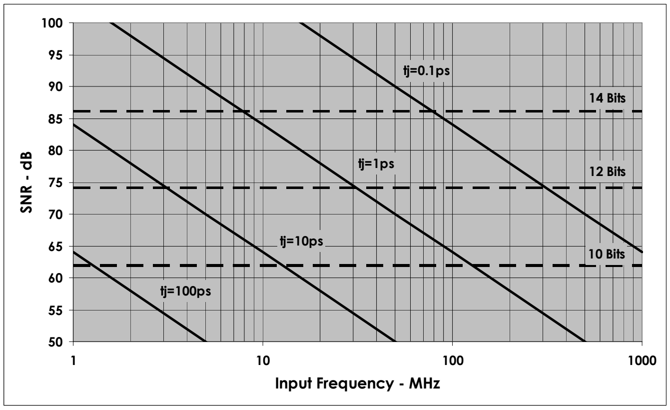


Figure 34. SNR vs. Clock Jitter

This relationship shows the SNR that would be achieved if clock jitter were the only non-ideal factor. In reality, achievable SNR is limited by internal factors such as linearity, aperture jitter and thermal noise. Internal aperture jitter is the uncertainty in the sampling instant shown in Figure 1. The internal aperture jitter combines with the input clock jitter in a root-sum-square fashion, since they are not statistically correlated, and this determines the total jitter in the system. The total jitter, combined with other noise sources, then determines the achievable SNR.

Voltage Reference

A temperature compensated voltage reference provides the reference charges used in the successive approximation operations. The full-scale range of each A/D is proportional to the reference voltage. The nominal value of the voltage reference is 1.25V.

Digital Outputs

Output data is available as a parallel bus in LVDS-compatible or CMOS modes. In either case, the data is presented in double data rate (DDR) format with the A and B channel data available on alternating clock edges. When CLKOUT is low channel A data is output, while on the high phase channel B data is presented. Figures 1 and 2 show the timing relationships for LVDS and CMOS modes, respectively.

Additionally, the drive current for LVDS mode can be set to a nominal 3 mA or a power-saving 2 mA. The lower current setting can be used in designs where the receiver is in close physical proximity to the ADC. The applicability of this setting is dependent upon the PCB layout, therefore the user should experiment to determine if performance degradation is observed.

The output mode and LVDS drive current are selected via the OUTMODE pin as shown in Table 2.

OUTMODE Pin	Mode
AVSS	LVCMOS
Float	LVDS, 3 mA
AVDD	LVDS, 2 mA

Table 2. OUTMODE Pin Settings

The output mode can also be controlled through the SPI port, which overrides the OUTMODE pin setting. Details on this are contained in the **Serial Peripheral Interface** section.

An external resistor creates the bias for the LVDS drivers. A 10kΩ, 1% resistor must be connected from the RLVDS pin to OVSS.

Power Dissipation

The power dissipated by the KAD5610P is primarily dependent on the sample rate, but is also related to the input signal in CMOS output mode. There is a static bias in the analog supply, while the remaining power dissipation is linearly related to the sample rate. The output supply dissipation is approximately constant in LVDS mode, but linearly related to the clock frequency in CMOS mode. Figures 35 and 36 illustrate these relationships.

TBD

Figure 35. Power vs. Sample Rate, LVDS Mode

TBD

Figure 36. Power vs. Sample Rate, CMOS Mode

Nap/Sleep

Portions of the device may be shut down to save power during times when operation of the ADC is not required. Two power saving modes are available: nap, and sleep. Nap mode reduces power dissipation to 40mW and recovers to normal operation in approximately 1µs. Sleep mode reduces power dissipation to 10mW but requires 1ms to recover. The clock should remain running and at a fixed frequency during Nap or Sleep. Recovery time from Nap mode will increase if the clock is stopped, since the internal DLL can take up to 52µs to regain lock at 250MSPS.

By default after the device is powered on, the nap and sleep state is controlled by the NAPSLP pin as shown in Table 3.

NAPSLP Pin	Mode
AVSS	Normal
Float	Sleep
AVDD	Nap

Table 3. NAPSLP Pin Settings

The power down mode can also be controlled through the SPI port, which overrides the NAPSLP pin setting. Details on this are contained in the **Serial Peripheral Interface** section. This is an indexed function when controlled from the SPI, but a global function when driven from the pin.

Data Format

Output data can be presented in three formats: two's complement, Gray code and offset binary. The data format is selected via the OUTFMT pin as shown in Table 4.

OUTFMT Pin	Mode
AVSS	Offset Binary
Float	Two's Complement
AVDD	Gray Code

Table 4. OUTFMT Pin Settings

The data format can also be controlled through the SPI port, which overrides the OUTFMT pin setting. Details on this are contained in the **Serial Peripheral Interface** section.

Offset binary coding maps the most negative input voltage to code 0x000 (all zeros) and the most positive input to 0xFFF (all ones). Two's complement coding simply complements the MSB of the offset binary representation.

When calculating Gray code the MSB is unchanged. The remaining bits are computed as the XOR of the current bit position and the next most significant bit. Figure 37 shows this operation.

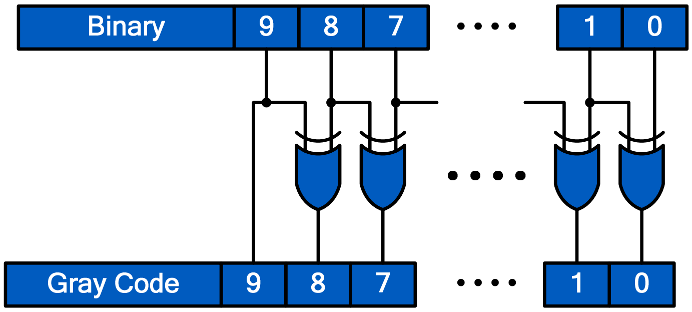


Figure 37. Binary to Gray Code Conversion

Converting back to offset binary from gray code must be done recursively, using the result of each bit for the next lower bit as shown in Figure 38.

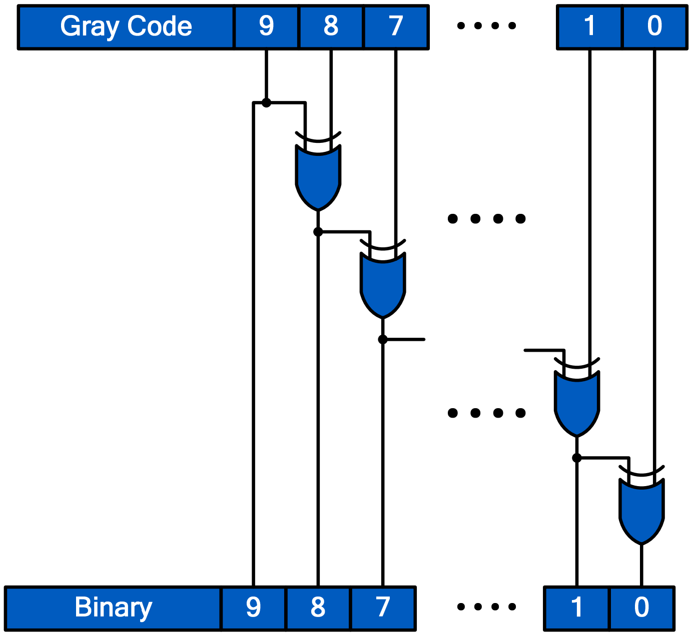


Figure 38. Gray Code to Binary Conversion

Mapping of the input voltage to the various data formats is shown in Table 5.

Input Voltage	Offset Binary	Two's Complement	Gray Code
–Full Scale	0000000000	1000000000	0000000000
–Full Scale + 1LSB	0000000001	1000000001	0000000001
Mid–Scale	1000000000	0000000000	1100000000
+Full Scale – 1LSB	1111111110	0111111110	1000000001
+Full Scale	1111111111	0111111111	1000000000

Table 5. Input Voltage to Output Code Mapping

Serial Peripheral Interface

A serial peripheral interface (SPI) bus is used to facilitate configuration of the device and to optimize performance. The SPI bus consists of chip select (CSB), serial clock (SCLK) and serial data input/output (SDIO). The maximum SCLK rate is equal to the ADC sample rate (f_{SAMPLE}) divided by 16 for write operations and f_{SAMPLE} divided by 66 for reads. At f_{SAMPLE} = 250MHz, maximum SCLK is 15.63MHz for writing and 3.79MHz for write operations. There is no minimum SCLK rate.

The following sections describe various registers that are used to configure the SPI or adjust performance or functional parameters. Many registers in the available address space (0x00 to 0xFF) are not defined in this document. Additionally, within a defined register there may be certain bits or bit combinations that are reserved. Undefined registers and undefined values within defined registers are reserved and should not be selected. Setting any reserved register or value may produce indeterminate results.

SPI Physical Interface

The SPI port operates in a half or full duplex master/slave configuration, with the KAD5610P functioning as a slave. Multiple slave devices can interface to a single master. The chip-select bar (CSB) pin determines when a slave device is being addressed. Multiple slave devices can be written to concurrently, but only one slave device can be read from at a given time. If multiple slave devices are selected for reading at the same time, the results will be indeterminate.

The serial clock pin (SCLK) provides synchronization for the data transfer. By default, all data is presented on the serial data input/output (SDIO) pin. The state of the SDIO pin is set automatically in the communication protocol (described below). A dedicated serial data output pin (SDO) can be activated by setting 0x00[7] high to allow operation in full duplex mode.

The communication protocol begins with an instruction/address phase. The first rising SCLK edge following a high to low transition on CSB determines the beginning of the two-byte instruction/address command. Data can be presented in MSB-first order or LSB-first order. The default is MSB-first, but this can be changed by setting 0x00[6] high. Figures 39 and 40 show the appropriate bit ordering for the MSB-first and LSB-first modes, respectively. In MSB-first mode the address is incremented for multi-byte transfers, while in LSB-first mode it's decremented.

In the default mode the MSB is R/W, which determines if the data is to be read (active high) or written. The next two bits, W1 and W0, determine the number of data bytes to be read or written (see Table 6). The lower 13 bits contain the first address for the data transfer. This relationship is illustrated in Figure 41, and timing values are given in the **Switching Specifications** section.

After the instruction/address bytes have been read, the appropriate number of data bytes are written to or read from the ADC (based on the R/W bit status). The data transfer will continue as long as CSB remains low and SCLK is active. Stalling of the CSB pin is allowed at any byte boundary (instruction/address or data) if the number of bytes being transferred is three or less. For transfers of four bytes or more, CSB is allowed stall in the middle of the instruction/address bytes or before the first data byte. If CSB transitions to a high state after that point the state machine will reset and terminate the data transfer.

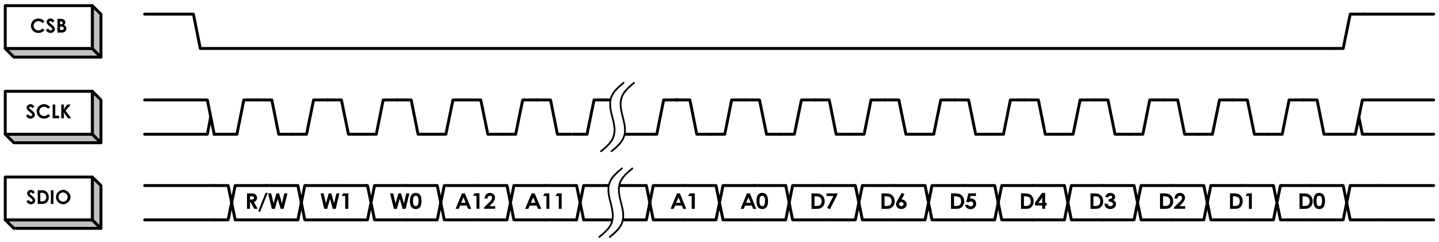


Figure 39. MSB-First Addressing

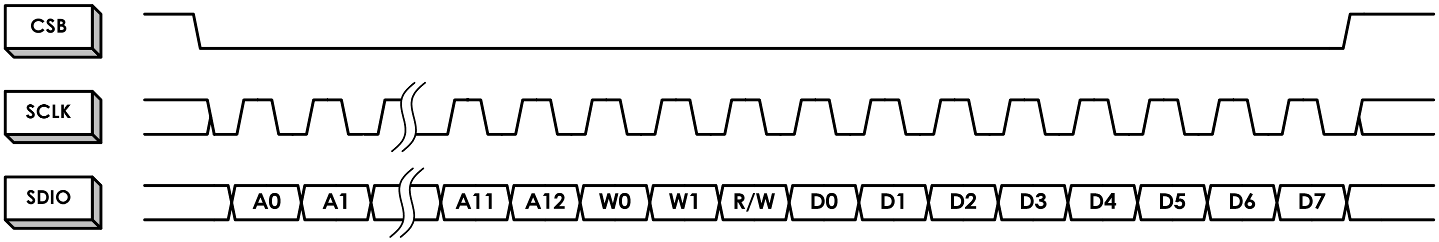


Figure 40. LSB-First Addressing

[W1:W0]	Bytes Transferred
00	1
01	2
10	3
11	4 or more

Table 6. Byte Transfer Selection

Figures 42 and 43 illustrate the timing relationships for 2-byte and N-byte transfers, respectively. The operation for a 3-byte transfer can be inferred from these diagrams.

SPI Configuration

Address 0x00: chip_port_config

Bit ordering and SPI reset are controlled by this register. Bit order can be selected as MSB to LSB (MSB first) or LSB to MSB (LSB first) to accommodate various microcontrollers.

Bit 7 SDO Active

Bit 6 LSB First

Setting this bit high configures the SPI to interpret serial data as arriving in LSB to MSB order.

Bit 5 Soft Reset

Setting this bit high resets all SPI registers to default values.

Bit 4 Reserved

This bit should always be set high.

Bits 3:0 These bits should always mirror bits 4:7 to avoid ambiguity in bit ordering.

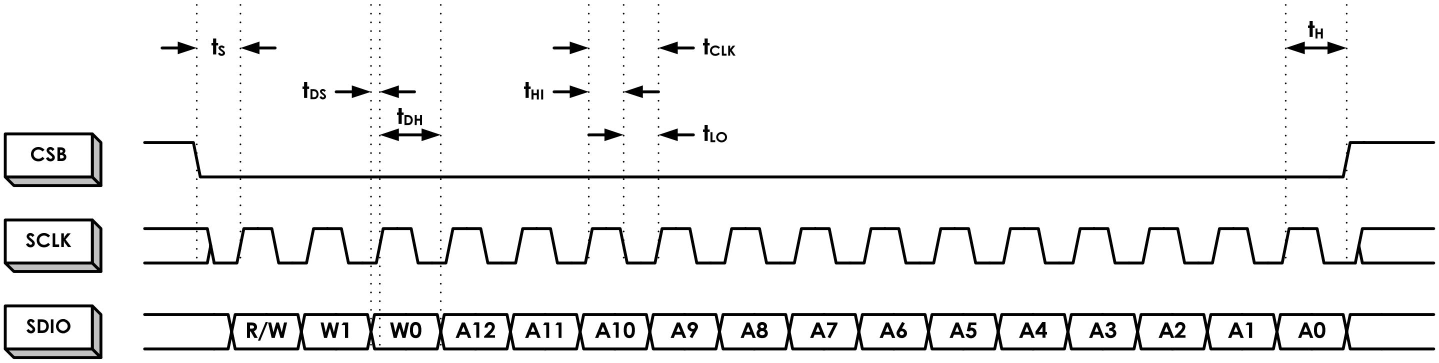


Figure 41. Instruction/Address Phase

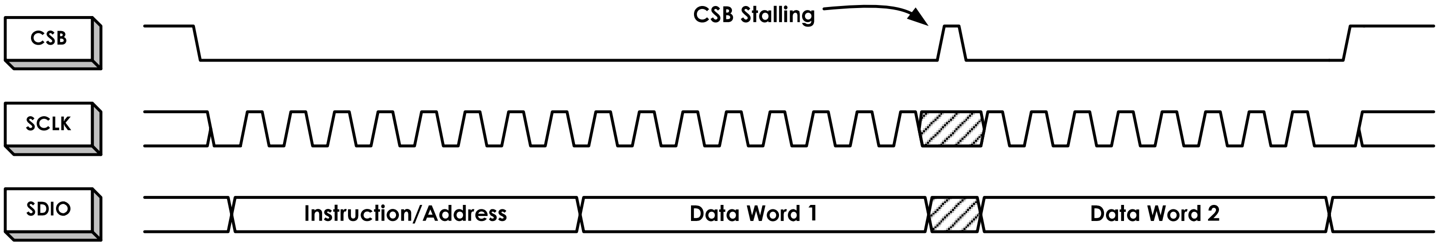


Figure 42. 2-Byte Transfer

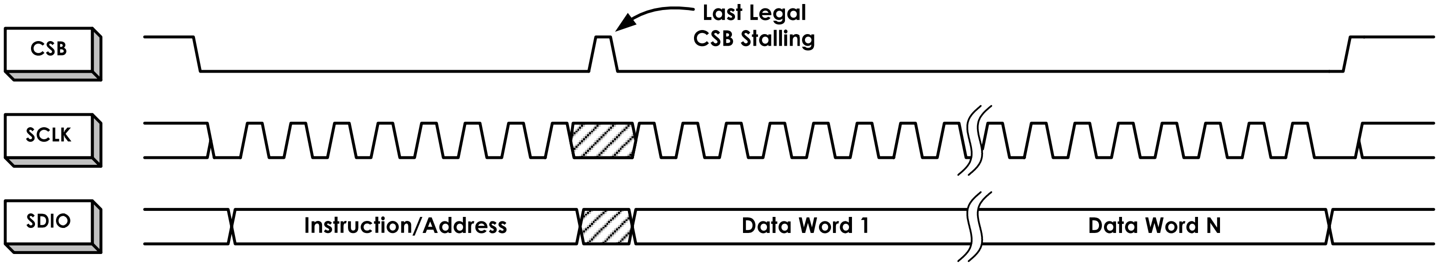


Figure 43. N-Byte Transfer

Address 0x02: burst_end

If a series of sequential registers are to be set, burst mode can improve throughput by eliminating redundant addressing. In 3-wire SPI mode the burst is ended by pulling the CSB pin high. If the device is operated in 2-wire mode the CSB pin is not available. In that case, setting the burst_end address determines the end of the transfer. During a write operation, the user must be cautious to transmit the correct number of bytes based on the starting and ending addresses.

Bits 7:0 Burst End Address

This register value determines the ending address of the burst data.

DUT Information

Address 0x08: chip_id

Address 0x09: chip_version

The generic die identifier and a revision number, respectively, can be read from these two registers.

Indexed DUT Configuration/Control

Address 0x10: device_index_A

A common SPI map, which can accommodate single-channel or multi-channel devices, is used for all Kenet ADC products. Certain configuration commands (identified as Indexed in the SPI map) can be executed on a per-converter basis. This register determines which converter is being addressed for an Indexed command. It is important to note that only a single converter can be addressed at a time.

This register defaults to 00h, indicating that no ADC is addressed.

Address 0x20: offset_coarse

Address 0x21: offset_fine

The input offset of each ADC core can be adjusted in fine and coarse steps. Both adjustments are made via an 8-bit word as detailed in Table 7. The data format is twos complement.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

Parameter	0x20[7:0] Coarse Offset	0x21[7:0] Fine Offset
Steps	256	256
–Full Scale (0x80)	-24.0mV	-1.7mV
Mid–Scale (0x00)	0.0mV	0.0mV
+Full Scale (0x7F)	+23.8mV	+1.7mV
Nominal Step Size	187.5µV	13.3µV

Table 7. Offset Adjustments

Address 0x22: gain_coarse

Address 0x23: gain_medium

Address 0x24: gain_fine

Gain of each ADC core can be adjusted in coarse, medium and fine steps. Coarse gain is a 4-bit adjustment while medium and fine are 8-bit. The data format is twos complement for all three registers.

The default value of each register will be the result of the self-calibration after initial power-up. If a register is to be incremented or decremented, the user should first read the register value then write the incremented or decremented value back to the same register.

Parameter	0x22[3:0] Coarse Gain
Steps	16
–Full Scale (0x08)	-11.2%
Mid–Scale (0x00)	0.0%
+Full Scale (0x07)	+9.8%
Nominal Step Size	1.4%

Table 8. Coarse Gain Adjustment

Parameter	0x23[7:0] Medium Gain	0x24[7:0] Fine Gain
Steps	256	256
–Full Scale (0x80)	-10.56%	-1.06%
Mid–Scale (0x00)	0.0%	0.0%
+Full Scale (0x7F)	+10.48%	+1.05%
Nominal Step Size	0.0825%	0.00825%

Table 9. Medium and Fine Gain Adjustments

Address 0x25: modes

Two distinct reduced power modes can be selected. By default, the tri-level NAPSLP pin can select normal operation, nap or sleep modes (refer to **Nap/Sleep** section). This functionality can be overridden and controlled through the SPI. This is an indexed function when controlled from the SPI, but a global function when driven from the pin. This register is not changed by a Soft Reset.

Value	0x25[2:0] Power Down Mode
000	Pin Control
001	Normal Operation
010	Nap Mode
100	Sleep Mode

Table 10. Power Down Control

Global DUT Configuration/Control

Address 0x70: skew_diff

The value in the skew_diff register adjusts the timing skew between the two ADCs cores. The nominal range and resolution of this adjustment are given in Table 11. The default value of this register after power-up is 00h.

Parameter	0x70[7:0] Differential Skew
Steps	256
–Full Scale (0x08)	-6.5ps
Mid–Scale (0x00)	0.0ps
+Full Scale (0x07)	+6.5ps
Nominal Step Size	51fs

Table 11. Differential Skew Adjustment

Address 0x71: phase_slip

When using a clock divider, it's not possible to determine the synchronization of the incoming and divided clock phases. This is particularly important when multiple ADCs are used in a time-interleaved system. The phase slip feature allows the rising edge of the divided clock to be advanced by one input clock cycle, as shown in Figure 44.

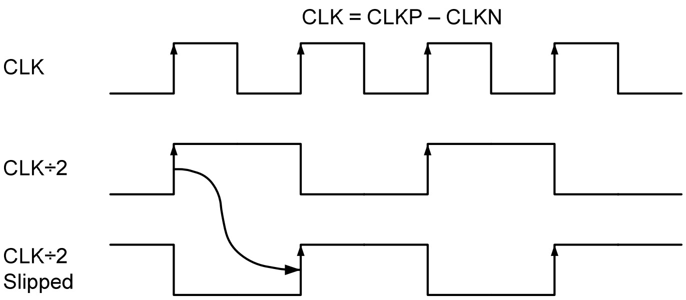


Figure 44. Phase Slip

Address 0x72: clock_divide

The KAD5610P has a selectable clock divider that can be set to divide by four, two or one (no division). By default, the tri-level CLKDIV pin selects the divisor (refer to **Clock Input** section). This functionality can be overridden and controlled through the SPI, as shown in Table 12. This register is not changed by a Soft Reset.

Value	0x72[2:0] Clock Divider
000	Pin Control
001	Divide by 1
010	Divide by 2
100	Divide by 4

Table 12. Clock Divider Selection

Address 0x73: output_mode_A

The output_mode_A register controls the physical output format of the data, as well as the logical coding. The KAD5610P can present output data in two physical formats: LVDS or LVCMOS. Additionally, the drive strength in LVDS mode can be set high (3mA) or low (2mA). By default, the tri-level OUTMODE pin selects the mode and drive level (refer to **Digital Outputs** section). This functionality can be overridden and controlled through the SPI, as shown in Table 13.

Data can be coded in three possible formats: two's complement, Gray code or offset binary. By default, the tri-level OUTFMT pin selects the data format (refer to **Data Format** section). This functionality can be overridden and controlled through the SPI, as shown in Table 14.

This register is not changed by a Soft Reset.

Value	0x93[7:5]
000	Pin Control
001	LVDS 2mA
010	LVDS 3mA
100	LVCMOS

Table 13. Output Mode Control

Value	0x93[2:0] Output Format
000	Pin Control
001	Two's Complement
010	Gray Code
100	Offset Binary

Table 14. Output Format Control

Address 0x74: output_mode_B

Address 0x75: config_status

Bit 6 DLL Range

This bit sets the DLL operating range to fast (TBD2MSPS to 250MSPS) or slow (40 to TBD1MSPS).

Bit 4 DDR Enable

Setting this bit enables Double Data-Rate mode.

The output_mode_B and config_status registers are used in conjunction to enable DDR mode and select the frequency range of the DLL clock generator. The method of setting these options is different from the other registers.

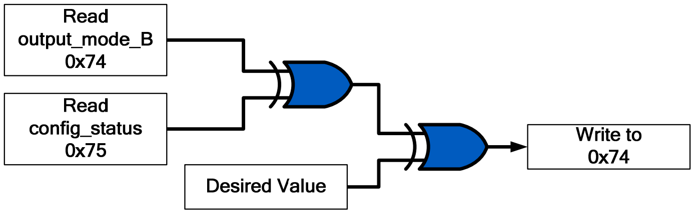


Figure 45. Setting output_mode_B register

The procedure for setting output_mode_B is shown in Figure 45. Read the contents of output_mode_B and config_status and XOR them. Then XOR this result with the desired value for output_mode_B and write that XOR result to the register.

DUT Test

The KAD5610 can produce preset or user defined patterns on the digital outputs to facilitate in-situ testing. A static word can be placed on the output bus, or two different words can alternate. In the alternate mode,

Address 0xC0: test_io

Bits 7:6 User Test Mode

These bits set the test mode to static (0x00) or alternate (0x01) mode. Other values are reserved.

The four LSBs in this register (Output Test Mode) determine the test pattern in combination with registers 0xC2 through 0xC5. Refer to Table 15.

Value	0xC0[3:0] Output Test Mode	Word 1	Word 2
0000	Off		
0001	Midscale	0x8000	N/A
0010	Positive Full-Scale	0xFFFF	N/A
0011	Negative Full-Scale	0x0000	N/A
0100	Checkerboard	0xAAAA	0x5555
0101	Reserved	N/A	N/A
0110	Reserved	N/A	N/A
0111	One/Zero	0xFFFF	0x0000
1000	User Pattern	user_patt1	user_patt2

Table 15. Output Test Modes

Address 0xC2: user_patt1_lsb

Address 0xC3: user_patt1_msb

These registers define the lower and upper eight bits, respectively, of the first user-defined test word.

Address 0xC2: user_patt2_lsb

Address 0xC3: user_patt2_msb

These registers define the lower and upper eight bits, respectively, of the second user-defined test word.

SPI Memory Map

	Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Def. Value (Hex)	Indexed/ Global
SPI Config	00	port_config	SDO Active	LSB First	Soft Reset			Mirror (bit5)	Mirror (bit6)	Mirror (bit7)	00h	G
	01	reserved	Reserved									
	02	burst_end	Burst end address [7:0]								00h	G
	03-07	reserved	Reserved									
DUT Info	08	chip_id	Chip ID #								Read only	G
	09	chip_version	Chip Version #								Read only	G
Indexed DUT Config/Control	10	device_index_A	Reserved						ADC01	ADC00	00h	I
	11-1F	reserved	Reserved									
	20	offset_coarse	Coarse Offset								cal. value	I
	21	offset_fine	Fine Offset								cal. value	I
	22	gain_coarse	Reserved				Coarse Gain				cal. value	I
	23	gain_medium	Medium Gain								cal. value	I
	24	gain_fine	Fine Gain								cal. value	I
	25	modes						**Power Down Mode [2:0]** 000=Pin Control 001=Normal Operation 010=Nap 100=Sleep other codes=reserved			00h NOT affected by Soft Reset	I
	26-5F	reserved	Reserved									
	60-6F	reserved	Reserved									
Global DUT Config/Control	70	skew_diff	Differential Skew								7Fh	G
	71	phase_slip	Reserved							Next Clock Edge	00h	G
	72	clock_divide						**Clock Divide [2:0]** 000=Pin Control 001=divide by 1 010=divide by 2 100=divide by 4 other codes=reserved			00h NOT affected by Soft Reset	G
	73	output_mode_A	**Output Mode [2:0]** 000=Pin Control 001=LVDS 2mA 010=LVDS 3mA 100=LVCMOS other codes=reserved					**Output Format [2:0]** 000=Pin Control 001=Twos Complement 010=Gray Code 100=Offset Binary other codes=reserved			00h NOT affected by Soft Reset	G
	74	output_mode_B		**DLL Range** 0=fast 1=slow		DDR Enable					00h NOT affected by Soft Reset	G
	75	config_status		XOR Result		XOR Result					Read Only	G
	76-BF	reserved	Reserved									
DUT Test	C0	test_io	**User Test Mode [2:0]** 00=Single 01=Alternate 10=Single Once 11=Alternate Once		Reset PN Long Gen	Reset PN Short Gen	**Output Test Mode [3:0]** 0=Off 1=Midscale Short 2=+FS Short 3=−FS Short 4=Checker Board 5=reserved 6=reserved		7=One/Zero Word Toggle 8=User Input 9-15=reserved		00h	G
	C1	Reserved	Reserved								00h	G
	C2	user_patt1_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	G
	C3	user_patt1_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	G
	C4	user_patt2_lsb	B7	B6	B5	B4	B3	B2	B1	B0	00h	G
	C5	user_patt2_msb	B15	B14	B13	B12	B11	B10	B9	B8	00h	G
	C6-FF	reserved	Reserved									

Table 16. SPI Memory Map

Equivalent Circuits

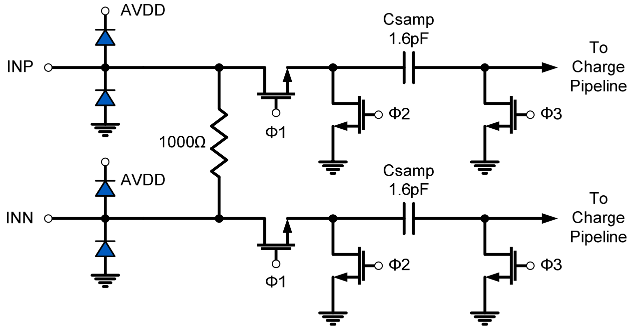


Figure 46. Analog Inputs

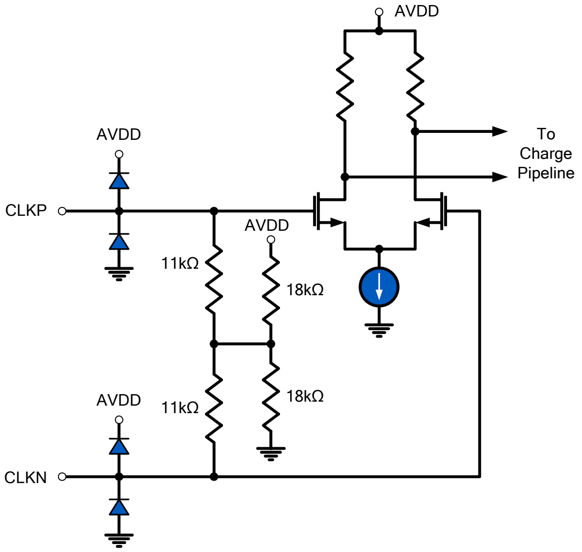


Figure 47. Clock Inputs

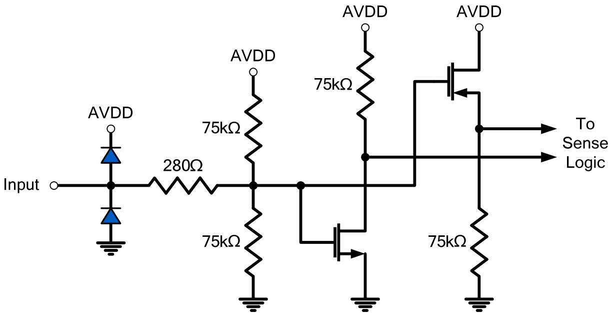


Figure 48. Tri-Level Digital Inputs

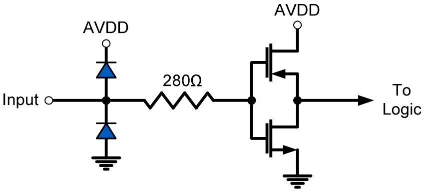


Figure 49. Digital Inputs

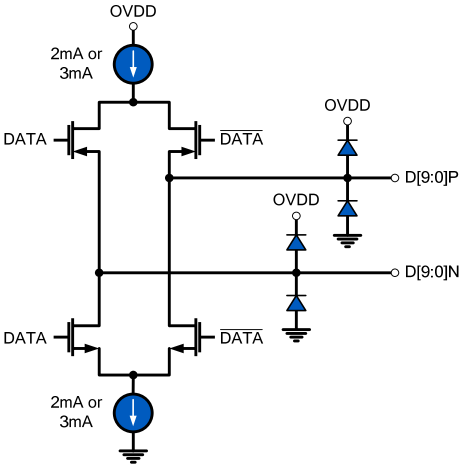


Figure 50. LVDS Outputs

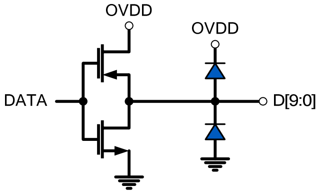


Figure 51. CMOS Outputs

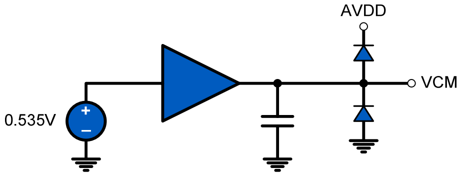


Figure 52. VCM_OUT Output

Layout Considerations

Split Ground and Power Planes

Data converters operating at high sampling frequencies require extra care in PC board layout. Many complex board designs benefit from isolating the analog and digital sections. Analog supply and ground planes should be laid out under signal and clock inputs. Locate the digital planes under outputs and logic pins. Grounds should be joined under the chip.

Clock Input Considerations

Use matched transmission lines to the transformer inputs for the analog input and clock signals. Locate transformers and terminations as close to the chip as possible.

Exposed Paddle

The exposed paddle must be electrically connected to analog ground (AVSS) and should be connected to a large copper plane using numerous vias for optimal thermal performance.

Bypass and Filtering

Bulk capacitors should have low equivalent series resistance. Tantalum is a good choice. For best performance, keep ceramic bypass capacitors very close to device pins. Longer traces will increase inductance, resulting in diminished dynamic performance and accuracy. Make sure that connections to ground are direct and low impedance. Avoid forming ground loops.

LVDS Outputs

Output traces and connections must be designed for 50Ω (100Ω differential) characteristic impedance. Keep traces direct and minimize bends where possible. Avoid crossing ground and power plane breaks with signal traces.

LVCMOS Outputs

Output traces and connections must be designed for 50Ω characteristic impedance.

Unused Inputs

Standard logic inputs (RESETN, CSB, SCLK, SDIO, SDO) which will not be operated do not require connection to ensure optimal ADC performance. These inputs can be left floating if they are not used. Tri-level inputs (NAPSLP, OUTMODE, OUTFMT, CLKDIV) accept a floating input as a valid state, and therefore should be biased according to the desired functionality.

Definitions

Analog Input Bandwidth is the analog input frequency at which the spectral output power at the fundamental frequency (as determined by FFT analysis) is reduced by 3dB from its full-scale low-frequency value. This is also referred to as Full Power Bandwidth.

Aperture Delay or Sampling Delay is the time required after the rise of the clock input for the sampling switch to open, at which time the signal is held for conversion.

Aperture Jitter is the RMS variation in aperture delay for a set of samples.

Clock Duty Cycle is the ratio of the time the clock wave is at logic high to the total time of one clock period.

Differential Non-Linearity (DNL) is the deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB) is an alternate method of specifying Signal to Noise-and-Distortion Ratio (SINAD). In dB, it is calculated as: ENOB = (SINAD-1.76) / 6.02

Gain Error is the ratio of the difference between the voltages that cause the lowest and highest code transitions to the full-scale voltage (less 2 LSB). It is typically expressed in percent.

Integral Non-Linearity (INL) is the deviation of each individual code from a line drawn from negative full-scale (1/2 LSB below the first code transition) through positive full-scale (1/2 LSB above the last code transition). The deviation of any given code from this line is measured from the center of that code.

Least Significant Bit (LSB) is the bit that has the smallest value or weight in a digital word. Its value in terms of input voltage is $V_{FS}/(2^N-1)$ where N is the resolution in bits.

Missing Codes are output codes that are skipped and will never appear at the ADC output. These codes cannot be reached with any input value.

Most Significant Bit (MSB) is the bit that has the largest value or weight.

Pipeline Delay is the number of clock cycles between the initiation of a conversion and the appearance at the output pins of the data.

Power Supply Rejection Ratio (PSRR) is the ratio of a change in input voltage necessary to correct a change in output code that results from a change in power supply voltage.

Signal to Noise-and-Distortion (SINAD) is the ratio of the RMS signal amplitude to the RMS value of the sum of all other spectral components below one half the clock frequency, including harmonics but excluding DC.

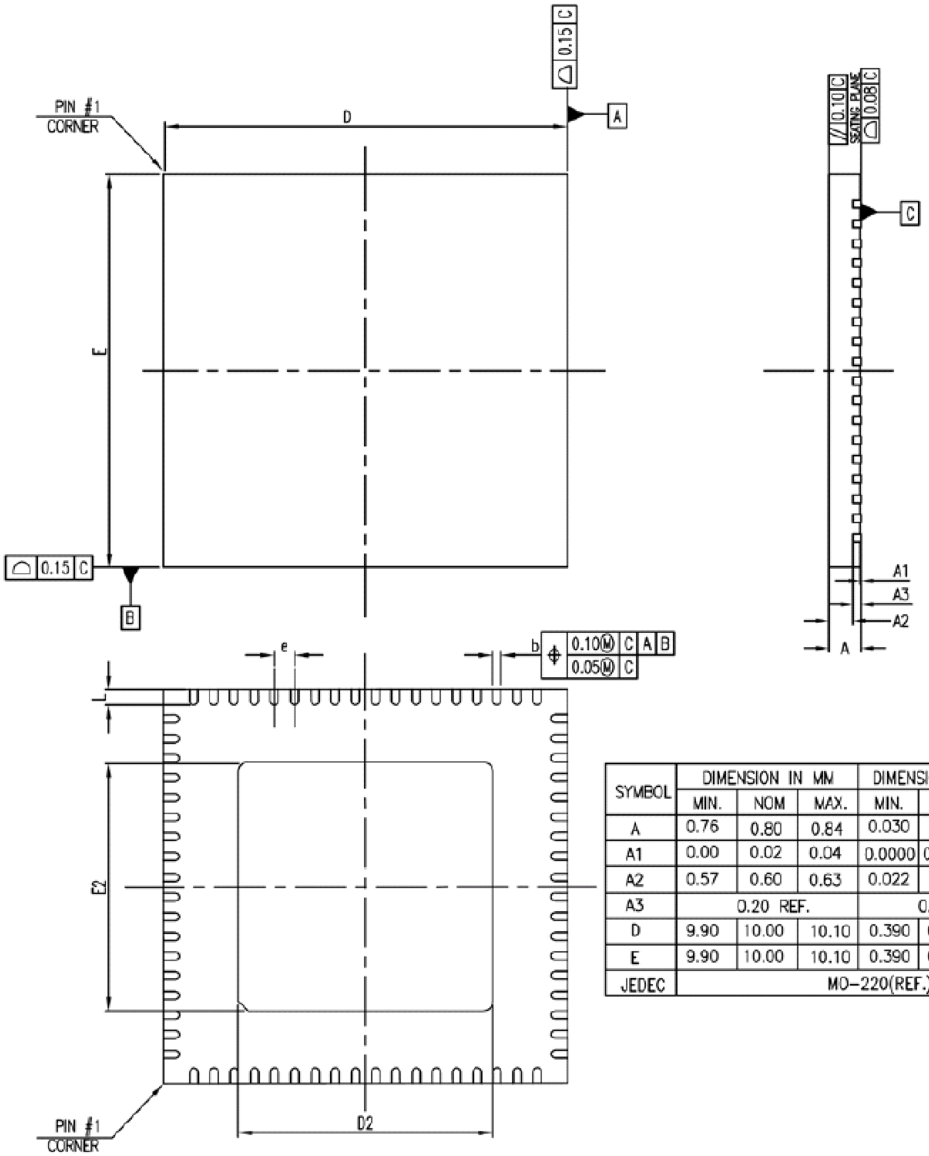
Signal-to-Noise Ratio (without Harmonics) is the ratio of the RMS signal amplitude to the sum of all other spectral components below one-half the sampling frequency, excluding harmonics and DC.

SNR and SINAD are either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the converter's full-scale input power is used as the reference.

Spurious-Free-Dynamic Range (SFDR) is the ratio of the RMS signal amplitude to the RMS value of the peak spurious spectral component. The peak spurious spectral component may or may not be a harmonic.

Two-Tone SFDR is the ratio of the RMS value of the lowest power input tone to the RMS value of the peak spurious component, which may or may not be an IMD product.

Outline Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.76	0.80	0.84	0.030	0.031	0.033
A1	0.00	0.02	0.04	0.0000	0.0008	0.0015
A2	0.57	0.60	0.63	0.022	0.024	0.025
A3	0.20 REF.			0.008 REF.		
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
JEDEC	MO-220(REF.)					

N	b			D2			E2			e	L			JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
72L	0.15	0.20	0.25	6.25	6.30	6.35	6.25	6.30	6.35	0.500 BSC	0.30	0.40	0.50	

Figure 53. 72QFN Dimensions

Ordering Guide

The KAD5610P is compliant with EU directive 2002/95/EC regarding the Restriction of Hazardous Substances (RoHS). Contact Kenet for a materials declaration for this product.

Model	**Speed**	**Package**	**Temp. Range**
KAD5610P-25Q72	250MSPS	72-QFN	-40°C to +85°C
KAD5610P-21Q72	210MSPS	72-QFN	-40°C to +85°C
KAD5610P-17Q72	170MSPS	72-QFN	-40°C to +85°C
KAD5610P-12Q72	125MSPS	72-QFN	-40°C to +85°C

Revision History

14-May-07:	Rev 0.1	Updated to new format
21-Jun-07:	Rev 0.2	Errata Updated
13-Aug-07:	Rev 0.3	Content/specification updates
07-Dec-07:	Rev 0.4	Content/specification updates
21-Feb-08:	Rev 0.5	New Pinout, Updated specifications, added functional descriptions
25-Feb-08:	Rev 0.5.1	Added skew_diff SPI register description (p. 22)

Preliminary Datasheet

This datasheet contains preliminary technical data, which is subject to change without notice. Contact Kenet prior to initiating design activity using this product.