ACT8325

Rev0, 13-May-08

Dual PWM Step-Down DC/DCs in TDFN33

FEATURES

- **Multiple Patents Pending**
- **Two Integrated Step-Down DC/DC Converters**
  - **REG1: 350mA**
  - **REG2: 550mA**
- **180° Out-of-Phase Operation**
  - **Reduces Input Capacitor Requirements**
- **Fixed or Adjustable Output Voltage Options**
- **Independent Enable/Disable Control**
- **Minimal External Components**
- **3x3mm, Thin-DFN (TDFN33-10) Package**
  - **Only 0.75mm Height**
  - **RoHS-Compliant**

APPLICATIONS

- **Portable Devices and PDAs**
- **MP3/MP4 Players**
- **Wireless Handhelds**
- **GPS Receivers**

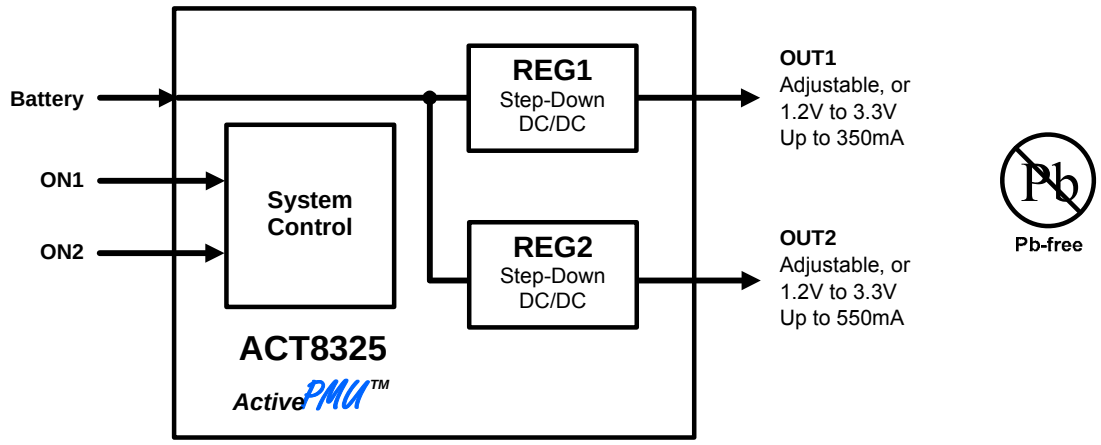
GENERAL DESCRIPTION

The patent-pending ACT8325 integrates two step-down DC/DCs into a single, thin, space-saving package to provide a cost-effective, highly-efficient *ActivePMU*™ power management solution. This device is ideal for a wide range of portable hand-held equipment that can benefit from the advantages of *ActivePMU* technology but do not require a high level of integration.

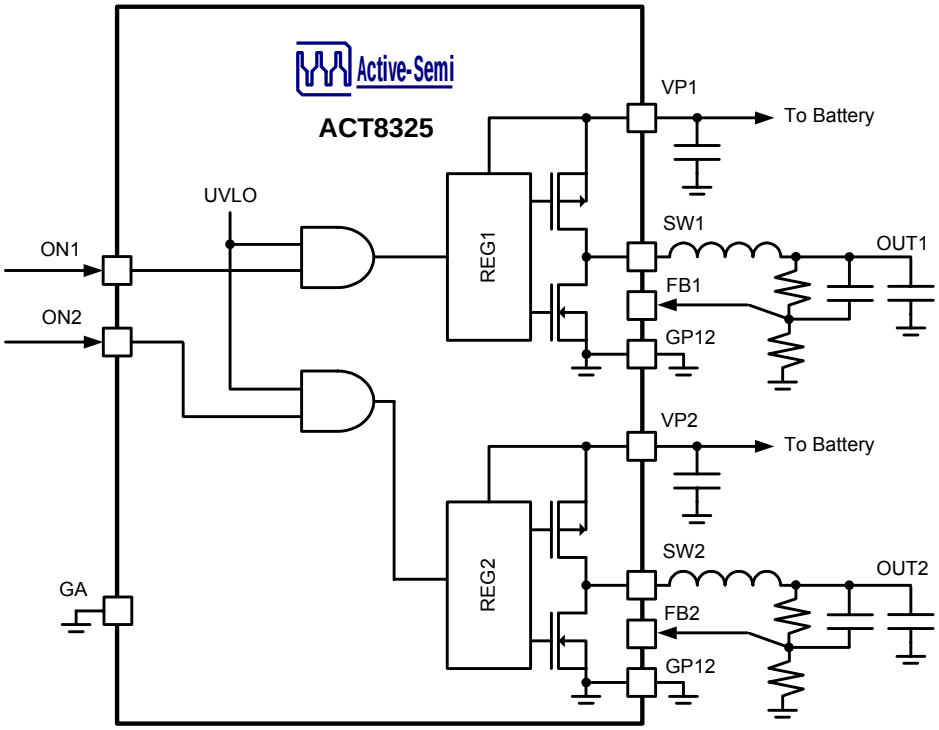
REG1 and REG2 are fixed-frequency, current-mode PWM step-down DC/DC converters that are optimized for high efficiency and are capable of supplying up to 350mA and 550mA, respectively. Both outputs are available in a wide range of factory-preset output voltage options, and an adjustable output voltage mode is also available.

The ACT8325 is available in a tiny 3mm x 3mm 10-pin Thin-DFN package that is just 0.75mm thin.

SYSTEM BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION①②

PART NUMBER	V_{OUT1}	V_{OUT2}	PACKAGE	PINS	TEMPERATURE RANGE
ACT8325NDAAA-T	Adjustable	Adjustable	TDFN33-10	10	-40°C to +85°C

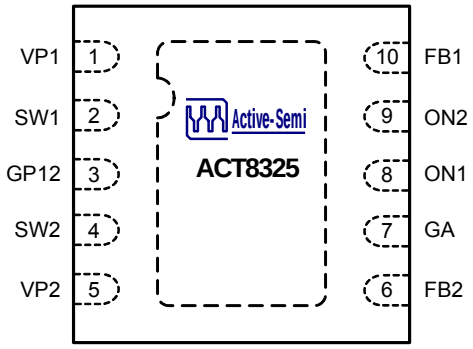
OUTPUT VOLTAGE CODES										
A	C	P	J	D	E	F	I	Q	G	H
Adjustable	1.2V	1.3V	1.4V	1.5V	1.8V	2.5V	2.8V	2.85V	3.0V	3.3V

①: Output voltage options detailed in this table represent standard voltage options, and are available for samples or production orders. Additional output voltage options, as detailed in the *Output Voltage Codes* table, are available for production subject to minimum order quantities. Contact Active-Semi for more information regarding semi-custom output voltage combinations.

②: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

PIN CONFIGURATION

TOP VIEW



Thin - DFN (TDFN 33-10)

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	VP1	Power Input for REG1. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
2	SW1	Switching Node Output for REG1. Connect this pin to the switching end of the inductor.
3	GP12	Power Ground for REG1, REG2. Connect GA and GP12 together at single point as close to the IC as possible.
4	SW2	Switching Node Output for REG2. Connect this pin to the switching end of the inductor.
5	VP2	Power Input for REG2. Bypass to GP12 with a high quality ceramic capacitor placed as close as possible to the IC.
6	FB2	Feedback Node for REG2. For fixed output voltage options, connect this pin directly to the output. For the adjustable output voltage options the voltage at this pin is regulated to 0.625V, connect this pin to the center of the output feedback resistor divider for voltage setting.
7	GA	Analog Ground. Connect GA directly to a quiet ground node. Connect GA and GP12 together at a single point as close to the IC as possible.
8	ON1	Enable Control Input for REG1. Drive ON1 to VP1 or to a logic high for normal operation, drive to GA or to a logic low to disable REG1.
9	ON2	Enable Control Input for REG2. Drive ON2 to VP1or to a logic high for normal operation, drive to GA or to a logic low to disable REG2.
10	FB1	Feedback Node for REG1. For fixed output voltage options, connect this pin directly to the output. For the adjustable output voltage options the voltage at this pin is regulated to 0.625V, connect this pin to the center of the output feedback resistor divider for voltage setting.
EP	EP	Exposed Pad. Must be soldered to ground on PCB.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
VP1, SW1, VP2, SW2 to GP12, FB1, FB2, ON1, ON2 to GA	-0.3 to +6	V
SW1 to VP1, SW2 to VP2	-6 to +0.3	V
GP12 to GA	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	33	°C/W
Operating Temperature Range	-40 to 85	°C
Junction Temperature	125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (REG1)

(V_{VP1} = 3.6V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP1 Operating Voltage Range		3.1		5.5	V
VP1 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP1 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON1 = GA, V_{VP1} = 4.2V		0.1	1	µA
Adjustable Output Option Regulation Voltage			0.625		V
Output Voltage Regulation Accuracy	V_{NOM1} < 1.3V, I_{OUT1} = 10mA	-2.4%	V_{NOM1}	+1.8%	V
	V_{NOM1} ≥ 1.3V, I_{OUT1} = 10mA	-1.2%	V_{NOM1}①	+1.8%	
Line Regulation	V_{VP1} = Max(V_{NOM1} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT1} = 10mA to 350mA		0.0017		%/mA
Current Limit		0.45	0.6		A
Oscillator Frequency	V_{OUT1} ≥ 20% of V_{NOM1}	1.35	1.6	1.85	MHz
	V_{OUT1} = 0V		530		kHz
PMOS On-Resistance	I_{SW1} = -100mA		0.52	0.88	Ω
NMOS On-Resistance	I_{SW1} = 100mA		0.27	0.46	Ω
SW1 Leakage Current	V_{VP1} = 5.5V, V_{SW1} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM1}
Minimum On-Time			70		ns
Logic High Input Voltage	ON1	1.4			V
Logic Low Input Voltage	ON1			0.4	V
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Falling		20		°C

①: V_{NOM1} refers to the nominal output voltage level for V_{OUT1} as defined by the *Ordering Information* section.

ELECTRICAL CHARACTERISTICS (REG2)

(V_{VP2} = 3.6V, T_A = 25°C, unless otherwise specified.)

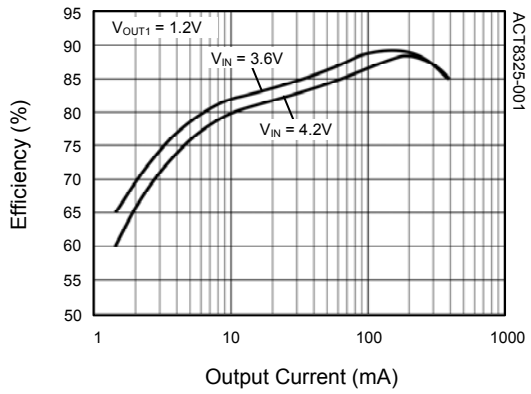
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP2 Operating Voltage Range		3.1		5.5	V
VP2 UVLO Threshold	Input Voltage Rising	2.9	3	3.1	V
VP2 UVLO Hysteresis	Input Voltage Falling		80		mV
Standby Supply Current			130	200	µA
Shutdown Supply Current	ON2 = GA, V_{VP2} = 4.2V		0.1	1	µA
Adjustable Output Option Regulation Voltage			0.625		V
Output Voltage Regulation Accuracy	V_{NOM2} < 1.3V, I_{OUT2} = 10mA	-2.4%	V_{NOM2}①	+1.8%	V
	V_{NOM2} ≥ 1.3V, I_{OUT2} = 10mA	-1.2%	V_{NOM2}	+1.8%	
Line Regulation	V_{VP2} = Max(V_{NOM2} + 1V, 3.2V) to 5.5V		0.15		%/V
Load Regulation	I_{OUT2} = 10mA to 550mA		0.0017		%/mA
Current Limit		0.65	0.85		A
Oscillator Frequency	V_{OUT2} ≥ 20% of V_{NOM2}	1.35	1.6	1.85	MHz
	V_{OUT2} = 0V		530		kHz
PMOS On-Resistance	I_{SW2} = -100mA		0.40	0.68	Ω
NMOS On-Resistance	I_{SW2} = 100mA		0.27	0.46	Ω
SW2 Leakage Current	V_{VP2} = 5.5V, V_{SW2} = 5.5V or 0V			1	µA
Power Good Threshold			94		%V_{NOM2}
Minimum On-Time			70		ns
Logic High Input Voltage	ON2	1.4			V
Logic Low Input Voltage	ON2			0.4	V
Thermal Shutdown Temperature	Temperature Rising		160		°C
Thermal Shutdown Hysteresis	Temperature Falling		20		°C

①: V_{NOM2} refers to the nominal output voltage level for V_{OUT2} as defined by the *Ordering Information* section.

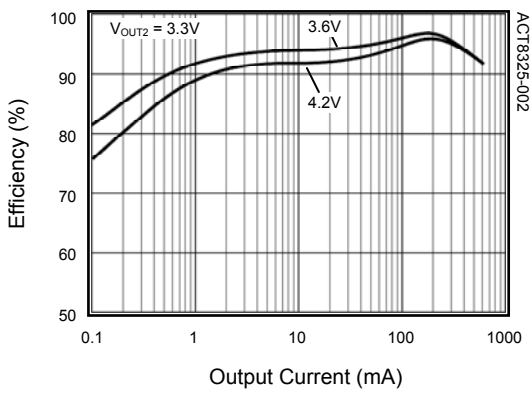
TYPICAL PERFORMANCE CHARACTERISTICS

(ACT8325NDAAA, V_{VP1} = V_{VP2} = 3.6V, L = 3.3μH, C_{VP1} = C_{VP2} = 2.2μF, C_{OUT1} = C_{OUT2} = 10μF, T_A = 25°C, unless otherwise specified.)

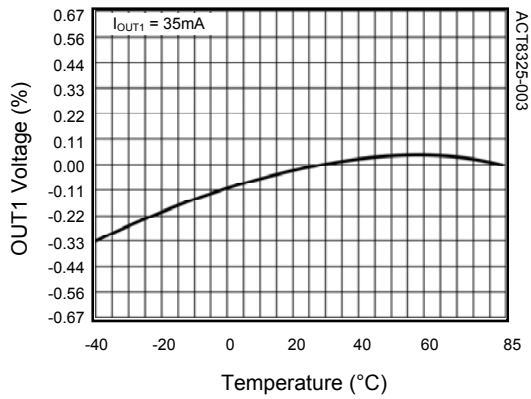
REG1 Efficiency vs. Load Current



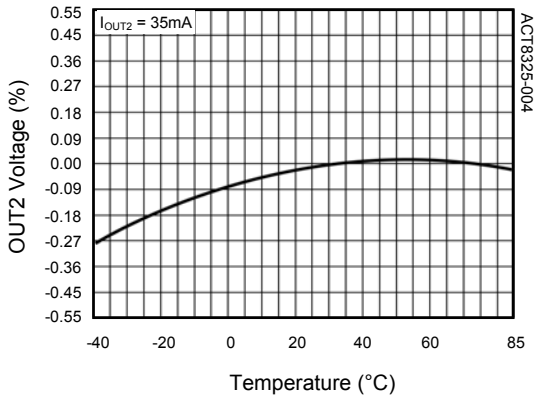
REG2 Efficiency vs. Load Current



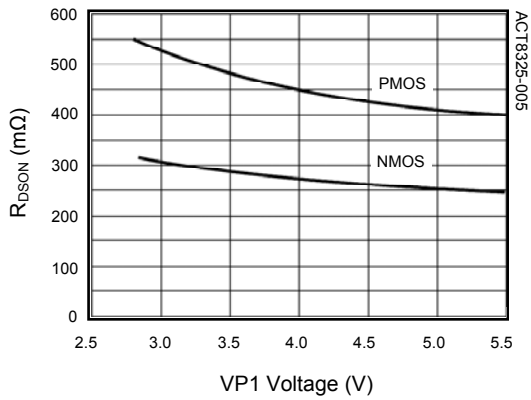
OUT1 Regulation Voltage



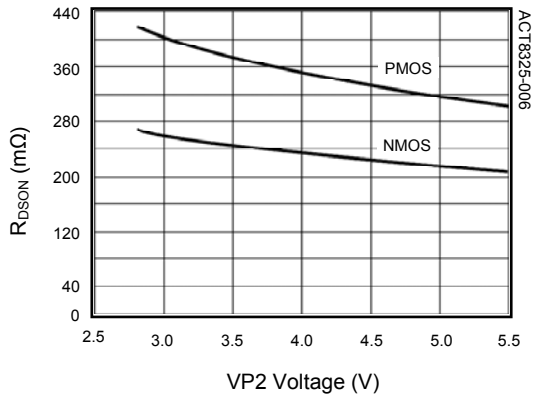
OUT2 Regulation Voltage



REG1 MOSFET Resistance



REG2 MOSFET Resistance



FUNCTIONAL DESCRIPTION

General Description

REG1 and REG2 are fixed-frequency, current-mode, synchronous PWM step-down converters that achieve peak efficiencies of up to 97%. REG1 is capable of supplying up to 350mA of output current, while REG2 supports up to 550mA. These regulators operate with a fixed frequency of 1.6MHz, minimizing noise in sensitive applications and allowing the use of small external components. REG1 and REG2 are available with a variety of standard and custom output voltages, as described in the Ordering Information section of this datasheet.

100% Duty Cycle Operation

Both REG1 and REG2 are capable of operating at up to 100% duty cycle. During 100% duty-cycle operation, the high-side power MOSFET is held on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery-powered applications.

Synchronous Rectification

REG1 and REG2 both feature integrated n-channel synchronous rectifiers, maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Enabling and Disabling REG1 and REG2

Each of the ACT8325's regulators features independent pin-controlled enable control. Drive ON1 to a logic-high to enable REG1, drive ON1 to a logic-low to disable REG1. Similarly, drive ON2 to a logic-high to enable REG2, drive ON2 to a logic-low to disable REG2. When disabled, each regulator's supply current drops to less than 1µA.

Soft-Start

REG1 and REG2 each include matched soft-start circuitry. When enabled, the output voltages track the internal 80µs soft-start ramp and both power up in a monotonic manner that is independent of loading on either output. This circuitry ensures that both outputs power up in a controlled manner, greatly simplifying power sequencing design considerations.

Compensation

REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Thermal Shutdown

The ACT8325 integrates thermal shutdown protection circuitry to prevent damage resulting from excessive thermal stress, as may be encountered under fault conditions. This circuitry disables all regulators if the ACT8325 die temperature exceeds 160°C, and prevents the regulators from being enabled until the IC temperature drops by 20°C (typ).

Input Capacitor Selection

The input capacitor reduces peak currents and noise induced upon the voltage source. A 2.2µF ceramic capacitor for each of REG1 and REG2 is recommended for most applications.

Output Capacitor Selection

For most applications, 10µF ceramic output capacitors are recommended for both REG1 and REG2. Although the these regulators were designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR, low-ESR tantalum capacitors can provide acceptable results as well.

Output Voltage Programming

Figure 4:

Output Voltage Programming

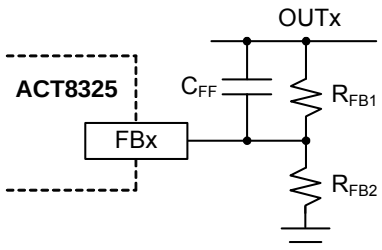


Figure 4 shows the feedback network necessary to set the output voltage when using the adjustable

output voltage option. output voltage option. Select components as follows: Set R_{FB2} = 51kΩ, then calculate R_{FB1} using the following equation:

$$R_{FB1} = R_{FB2}\left(\frac{V_{OUTX}}{V_{FBX}} - 1\right) \quad (1)$$

where V_{FBX} is 0.625V. Finally choose C_{FF} using the following equation:

$$C_{FF} = \frac{2.2 \times 10^{-6}}{R_{FB1}} \quad (2)$$

Where R_{FB1} = 47kΩ, use 47pF.

Inductor Selection

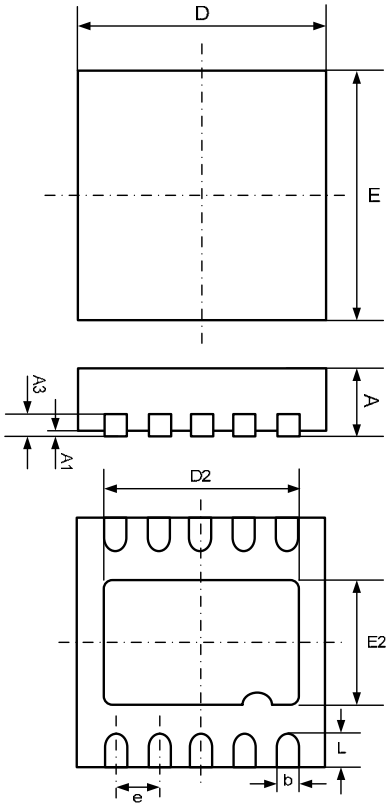
REG1 and REG2 utilize current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These devices were optimized for operation with 3.3µH inductors, although inductors in the 2.2µH to 4.7µH range can be used. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current of the application by at least 30%.

PCB Layout Considerations

High switching frequencies and large peak current make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Step-down DC/DCs exhibit discontinuous input current, so the input capacitors should be placed as close as possible to the IC, and avoiding the use of vias if possible. The inductor, input filter capacitor, and output filter capacitor should be connected as close together as possible, with short, direct, and wide traces. The ground nodes for each regulator's power loop should be connected at a single point in a star-ground configuration, and this point should be connected to the backside ground plane with multiple vias. For fixed output voltage options, connect the output node directly to the FBx pin. For adjustable output voltage options, connect the feedback resistors and feed-forward capacitor to the FBx pin through the shortest possible route. In both cases, the feedback path should be routed to maintain sufficient distance from switching nodes to prevent noise injection.

PACKAGE OUTLINE

TDFN33-10 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.0000	0.002
A3	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D2	2.350	2.450	0.093	0.096
E2	1.650	1.750	0.065	0.069
b	0.200	0.320	0.008	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

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