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Fax: 886-2-29174598
URL: http://www.princeton.com.tw

2.5W × 2 Class AB Audio Power Amplifier **PT2305**

EDESCRIPTION

The PT2305 is an audio power amplifier utilizing CMOS Technology specially designed for audio purpose. It can deliver 2.5W × 2 power output to the 4Ω load. The power consumption is very low in stand-by. Total harmonic distortion is lower than 0.03%. The output structure is BTL (Bridge-Tied Load) mode for driving speaker load mode. Built-in over-temperature protection, package size is not occupies PCB space. It is suitable for small or portable products.

FEATURES

- CMOS technology
- Operating voltage: 2.7V ~ 6V
- Output power 2.5W × 2 (4Ω/10%THD)
- Built-in 31 steps volume controller
- Suppress the pop and click noise when mode changed
- Extreme low current consumption in Shutdown mode (Icc<0.7μA)
- Built-in over temperature protection

APPLICATIONS

- LCD monitor or TV
- Portable audio
- Multimedia speakers
- Other audio applications

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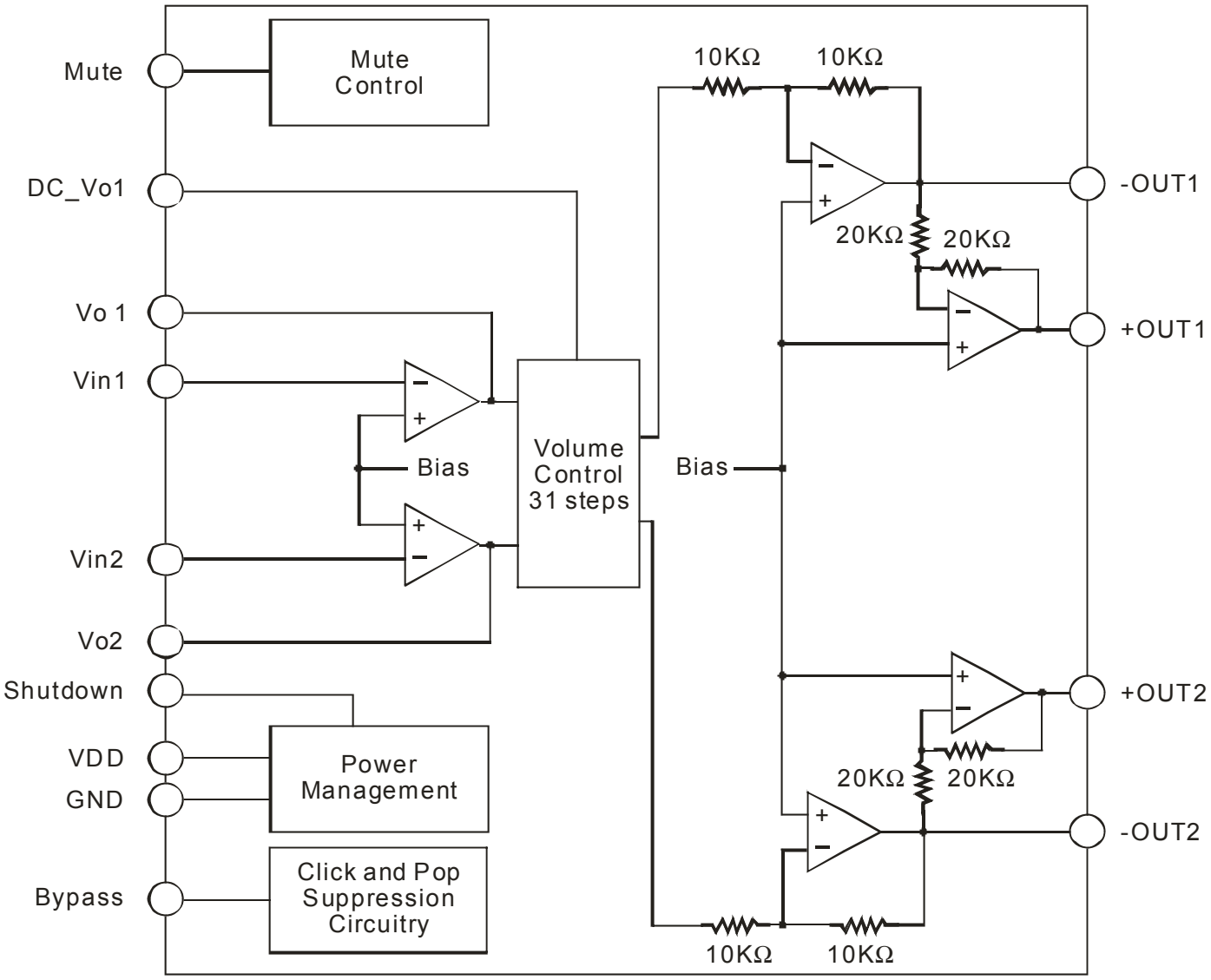
BLOCK DIAGRAM



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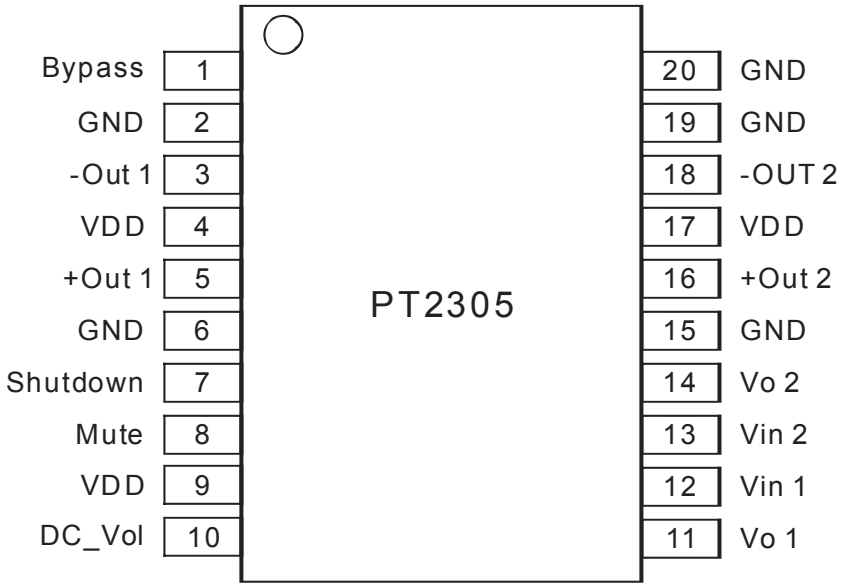
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
Bypass	O	Internal bias reference bypassing	1
GND		Ground	2, 6, 15, 19, 20
-OUT1	O	Channel 1 Output (-)	3
VDD		Power Supply Input	4, 9, 17
+OUT1	O	Channel 1 Output (+)	5
Shutdown	I	Shutdown pin。Entire IC into the shutdown mode when this pin connected to the VDD	7
Mute	I	Mute Pin, Output muted when it connected to VDD	8
DC_Vol	I	DC Volume control input pin	10
Vo1	I	Channel 1 output for external feedback circuit	11
Vin1	I	Channel 1 audio input	12
Vin2	I	Channel audio input	13
Vo2	I	Channel 2 output for external feedback circuit	14
+OUT2	O	Channel 2 Output (+)	16
-OUT2	O	Channel 2 Output (-)	18

FUNCTION DESCRIPTION

POWER SUPPLY

The operating voltage of PT2305 is from 2.7V to 6V, In general operation 5V is recommended. When the supply voltage less then 3V the IC can work properly, but the distortion reading will rise. After the supply voltage over 6.5V, the higher stand-by current consumption will rising the temperature on chip surface。

SHUTDOWN

When the DC supply still powered the chip Vcc, pull-up the shutdown pin to the Vcc level will take the chip into the shutdown mode. After the shutdown mode is active the total current consumption is less than 0.7μA. and the all of input or output pins no voltage output。When shutdown pin set to GND, the IC is back to the normal operation.

Shutdown Pin	Output State
VDD	Shutdown ON
GND	Normal

MUTE

When the mute pin is connected to the VDD all of outputs signal will be muted immediately, otherwise connected to the GND the IC is back to the normal operation.

Mute Pin	Output State
VDD	Mute ON
GND	Normal

INPUT GAIN ADJUST

The input gain of the PT2305 can be adjust by the external resistor, in normal operation 0dB gain setting is recommended, please refer to the application circuit. If the source output level is not so high (ex: < 2Vpp), increase the input gain can get the higher volume. The minimum value of the input series resistance is 10KΩ for the modest input impedance.
To make sure the input stage will not be distortion by overload, please confirm the input signal level, for the gain set please refer to the following table:

Operating Voltage	Input Gain=-6dB	Input Gain=0dB	Input Gain=+6dB
VDD=3V	Vin <5Vpp	Vin <2.5Vpp	Vin <1.25Vpp
VDD=5V	Vin <8Vpp	Vin<4Vpp	Vin<2Vpp

OVER TEMPERATURE PROTECTION

The PT2305 has a built-in over temperature protection circuit, it will turn off all power output when the chip temperature over 150℃, ,the chip will return to normal operation automatically after the temperature cool down to 105℃.

POP AND CLICK SURPPRESS

A power amplifier uses single supply voltage may almost have noise on output in the power-on period. It is because of the output DC potential needs time to stable on 1/2Vcc, the period relative with the capacitance on the Bypass pin. Higher CB value will extend the stable time, and also can suppress the noise when power-on. In supply voltage=5V and CB=1μF, stable time is about 200mS。The value of CB also relative with the value of the DC blocking capacitor connected in input terminal. In general condition the time constant of DC blocking capacitor should be less than CB stable time. Recommend parts values please refer to application circuit.

CB and delay time, please refer to following table:

CB	T_{ON}
0.01uF	2ms
0.1uF	20ms
0.22uF	44ms
0.47uF	94ms
1.0uF	200ms

VOLUME CONTROLLER

The PT2305 has a built-in 31 steps volume controller, output volume is determinate by voltage applied at the DC Vol pin. Range is from 0dB ~ -75dB. The lower DC voltage is means more volume attenuation. The attenuation levels are -1dB/step from 0dB ~ -6dB, -2dB/step from -6dB ~ -36dB, -3dB/step from -36dB ~ -47dB, -4dB/step from -47dB ~ -51dB, -5dB/step from -51dB ~ -66dB and -12dB/step to the last step at -78dB.

About relation between the volume setup and DC Vol, please refer to the following table.

VOLUME CONTROL TABLE

Step	Gain (dB)	Voltage Range (%VDD)			Voltage Range (VDD=5V)			Voltage Range (VDD=3V)		
		Low	High	Recommended	Low	High	Recommended	Low	High	Recommended
1	0	77.5 %	100.00 %	100.000%	3.875	5.000	5.000	2.325	3.000	3.000
2	-1	75.0 %	78.5 %	76.875 %	3.750	3.938	3.844	2.250	2.363	2.306
3	-2	72.5 %	76.25 %	74.375 %	3.625	3.813	3.719	2.175	2.288	2.231
4	-3	70.0 %	73.75 %	71.875 %	3.500	3.688	3.594	2.100	2.213	2.156
5	-4	67.5 %	71.25 %	69.375 %	3.375	3.563	3.469	2.025	2.138	2.081
6	-5	65.0 %	68.75 %	66.875 %	3.250	3.438	3.344	1.950	2.063	2.006
7	-6	62.5 %	66.25 %	64.375 %	3.125	3.313	3.219	1.875	1.988	1.931
8	-8	60.5 %	63.75 %	61.875 %	3.000	3.188	3.094	1.800	1.913	1.856
9	-10	57.5 %	61.25 %	59.375 %	2.875	3.063	2.969	1.725	1.838	1.781
10	-12	55.0 %	58.75 %	56.875 %	2.750	2.938	2.844	1.650	1.763	1.706
11	-14	52.5 %	56.25 %	54.375 %	2.625	2.813	2.719	1.575	1.688	1.631
12	-16	50.0 %	53.75 %	51.875 %	2.500	2.688	2.594	1.500	1.613	1.556
13	-18	47.5 %	51.25 %	49.375 %	2.375	2.563	2.469	1.425	1.538	1.481
14	-20	45.0 %	48.75 %	46.875 %	2.250	2.438	2.344	1.350	1.463	1.406
15	-22	42.5 %	46.25 %	44.375 %	2.125	2.313	2.219	1.275	1.388	1.331
16	-24	40.0 %	43.75 %	41.875 %	2.000	2.188	2.094	1.200	1.313	1.256
17	-26	37.5 %	41.25 %	39.375 %	1.875	2.063	1.969	1.125	1.238	1.181
18	-28	35.0 %	38.75 %	36.875 %	1.750	1.938	1.844	1.050	1.163	1.106
19	-30	32.5 %	36.25 %	34.375 %	1.625	1.813	1.719	0.975	1.088	1.031
20	-32	30.0 %	33.75 %	31.875 %	1.500	1.688	1.594	0.900	1.013	0.956
21	-34	27.5 %	31.25 %	29.375 %	1.375	1.563	1.469	0.825	0.937	0.881
22	-36	25.0 %	28.75 %	26.875 %	1.250	1.438	1.344	0.750	0.862	0.806
23	-39	22.5 %	26.25 %	24.375 %	1.125	1.313	1.219	0.675	0.787	0.731
24	-42	20.0 %	23.75 %	21.875 %	1.000	1.188	1.094	0.600	0.712	0.656
25	-45	17.5 %	21.25 %	19.375 %	0.875	1.063	0.969	0.525	0.637	0.581
26	-47	15.0 %	18.75 %	16.875 %	0.750	0.937	0.844	0.450	0.562	0.506
27	-51	12.5 %	16.25 %	14.375 %	0.625	0.812	0.719	0.375	0.487	0.431
28	-56	10.0 %	13.75 %	11.875 %	0.500	0.687	0.594	0.300	0.412	0.356
29	-61	7.5 %	11.25 %	9.375 %	0.375	0.562	0.469	0.225	0.337	0.281
30	-66	5.0 %	8.75 %	6.875 %	0.250	0.437	0.344	0.150	0.262	0.206
31	-78	0.0 %	6.25 %	0.000 %	0.000	0.312	0.000	0.000	0.187	0.000

HEAT DISSIPATION

During normal operation, the chip only consumes very little stand-by current. In high output power conditions, the package temperature will rise. For proper operating temperature, a modest heat sink mounted on the top side of the chip is required. The thermal resistance requirement of the heat sink demand may be obtained by the formula below:

$\theta_{JA} = (T_{J(max)} - T_A) \div P_{DISS}$
P_{DISS} = IC dissipation power
$T_{J\,(max)}$ = Maximum chip conjunction temperature
T_A = external environment temperature
θ_{JA} = thermal resistance from chip conjunction to ambience environment

With 60% estimated efficiency (eff), PT2305 in 2W + 2W output power dissipation is probably

$P_{DISS} = (Po \div eff) - Po = 2.6W$

The maximum chip conjunction temperature is 150°C. Exceeding this temperature will damage the chip, assuming the outside environment air temperature is 50°C. From the chip conjunction dissipation to external environment thermal resistance θJA should be:

$\theta_{JA} = (150 - 50) \div 2.6 = 38.4℃/W$

The PT2305 chip conjunction to case thermal resistance θJC is 26℃ /W. Therefore the heat sink thermal resistance should be:

$\theta_{JA} - \theta_{JC} = 12.4℃/W$

In normal operating, no need extra heat sink, only utilize the ground (copper foil) of PCB to heat dissipation.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	VDD	-	7	V
Operating temperature	Topr	-40	+85	℃
Storage temperature	Tstg	-65	+150	℃
Maximum input voltage	Vimax	-0.3	VDD +0.3	V
Maximum input current	Iimax	-10	+10	mA

* Input pins surge current can reach 100mA does not induce the CMOS latched up.

ELECTRICAL CHARACTERISTICS

(Unless otherwise, Vcc=5V, bandwidth=22 ~ 22KHz)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}			2.7	5	6	V
Operating current	Is	Vin=0V		-	15	30	mA
		$V_{shutdown}=V_{DD}$		-	0.7	2.0	μA
Two channels gain error	Gerr	RIN=RF=20KΩ		-	0	±1	dB
THD+N	THD	Po=1W, RL=8Ω		-	0.3	-	%
		Po=340mW, RL=32Ω		-	1	-	
Power output	Po	THD=1%, RL=3Ω		-	2.2	-	W
		THD=1%, RL=4Ω		-	2	-	
		THD=10%, RL=4Ω		-	2.5	-	
		THD=1%, RL=8Ω		1.0	1.1	-	
		THD=10%, RL=8Ω		-	1.5	-	
Signal-to-noise ratio	SNR	Pout=1.1W, RL=8Ω, A-Weighted		-	93	-	dB
Residual noise	Vno	A-Weighted		25	40	50	μV
Output offset	Voff	Vin=0V, +OUT ~ -OUT		-	10	±50	mV
Channel separation	CS	F=1KHz		-	70	-	dB
Power supply rejection ratio	PSRR	C_B=1.0μF, f=120Hz V_{RIPPLE}=200mVrms: R_L= 8Ω		-	74	-	dB
Volume control range	Vatt	DC Vol=5V	F=1KHz	-0.75	0	+0.75	dB
		DC Vol=0V		-75	-78	-	
Volume setup step	Gstep	Vatt=0 ~ -51dB		-	0	1	dB
Mute	mute	DC Vol=0V		-78	-	-	dB
Temperature protect	TH	TSSOP	Overheat close	-	150	-	℃
			Back to work	-	105	-	
		SOP	Overheat close	-	135	-	
			Back to work	-	105	-	
Shutdown voltage	V_{SD}	Shutdown on		0.5	0.6	-	V_{DD}
		Shutdown off		-	0.2	0.3	
Mute voltage	V_{MT}	Mute on		0.5	0.6	-	V_{DD}
		Mute off		-	0.2	0.3	

PACKAGE THERMAL CHARACTERISTIC

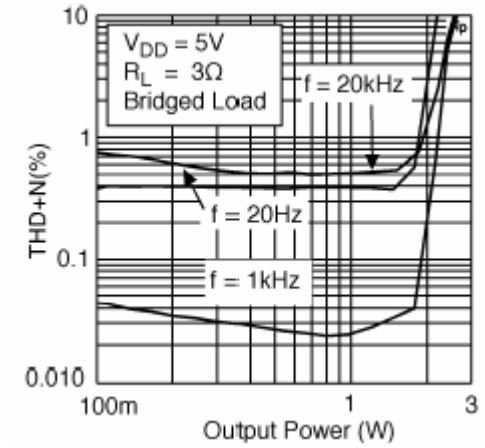
PACKAGE TYPE: TSSOP, 20PINS, 173MIL

Parameter	Symbol	Condition	Value	Unit
From chip conjunction dissipation to external environment	θ_{JA}	Ta=45℃	68.66	℃/W
From chip conjunction dissipation to package surface	θ_{JC}		22.94	℃/W

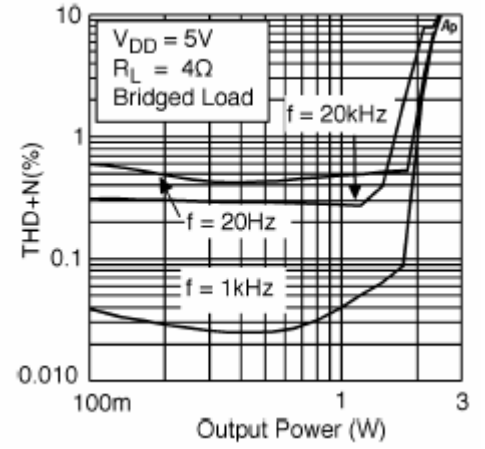
PACKAGE TYPE: SOP, 20PINS, 300MIL

Parameter	Symbol	Condition	Value	Unit
From chip conjunction dissipation to external environment	θ_{JA}	Ta=45℃	45.44	℃/W
From chip conjunction dissipation to package surface	θ_{JC}		27.00	℃/W

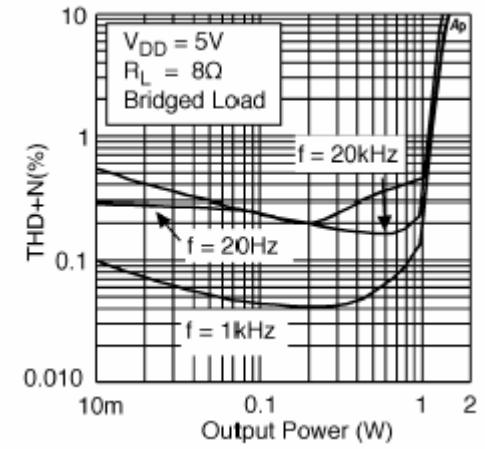
TYPICAL PERFORMANCE CHARACTERISTICS



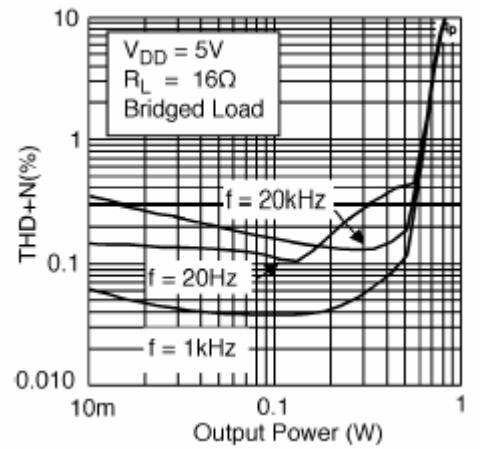
THD+N vs Output Power



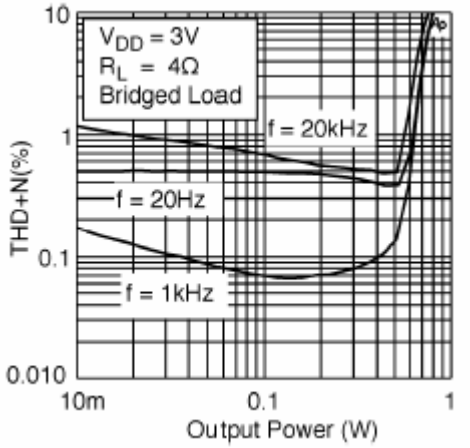
THD+N vs Output Power



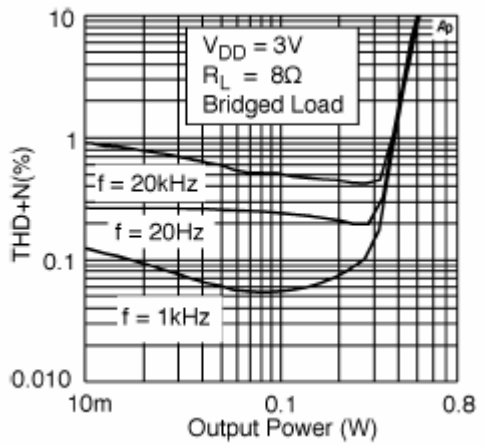
THD+N vs Output Power



THD+N vs Output Power



THD+N vs Output Power



THD+N vs Output Power

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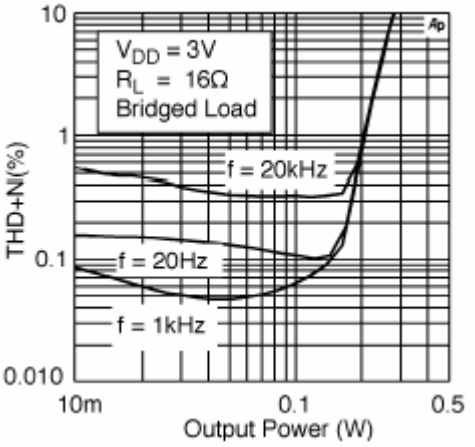
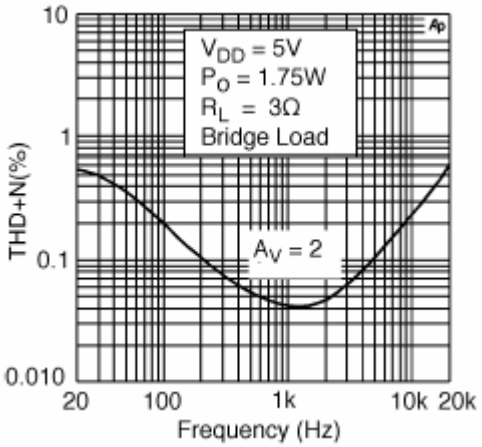
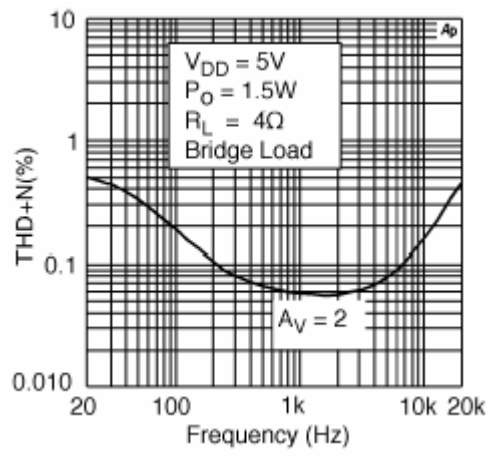


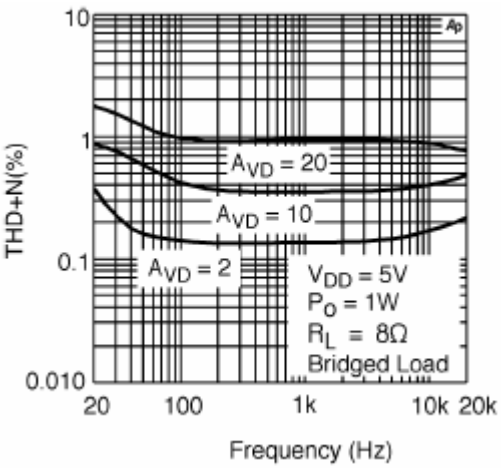
THD+N vs Output Power



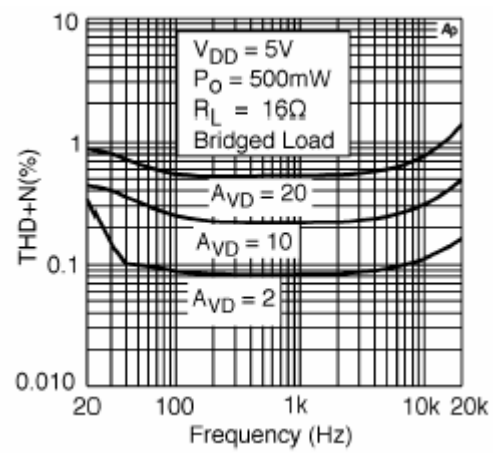
THD+N vs Frequency



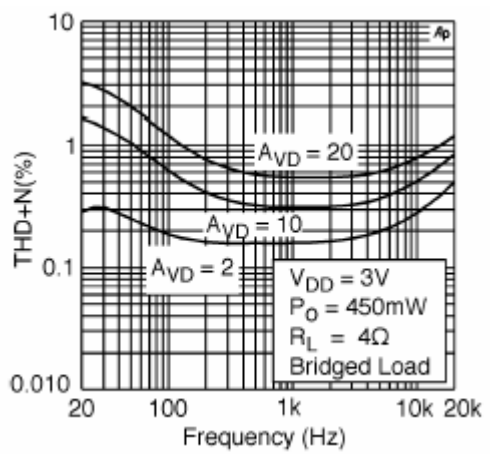
THD+N vs Frequency



THD+N vs Frequency

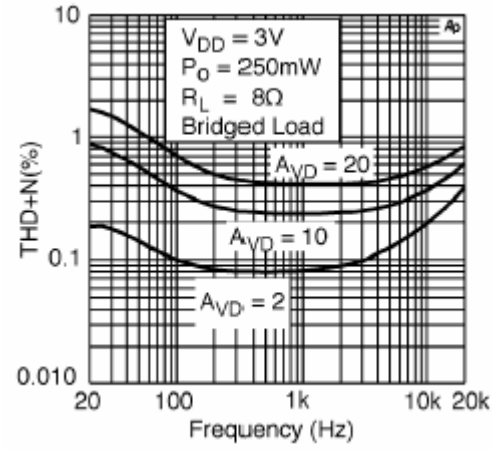


THD+N vs Frequency

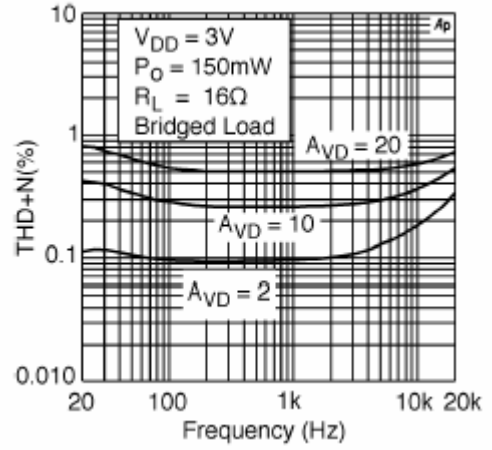


THD+N vs Frequency

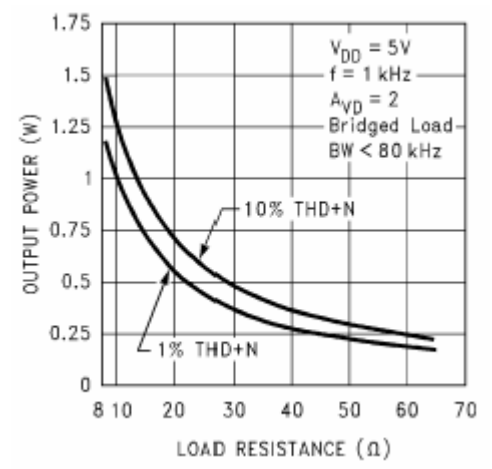
2.5W × 2 Class AB Audio Power Amplifier PT2305



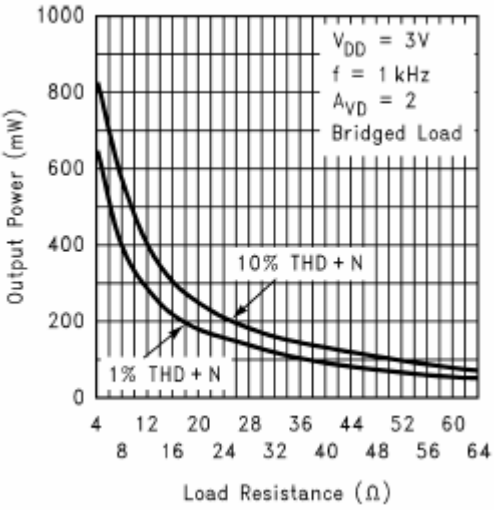
THD+N vs Output Power



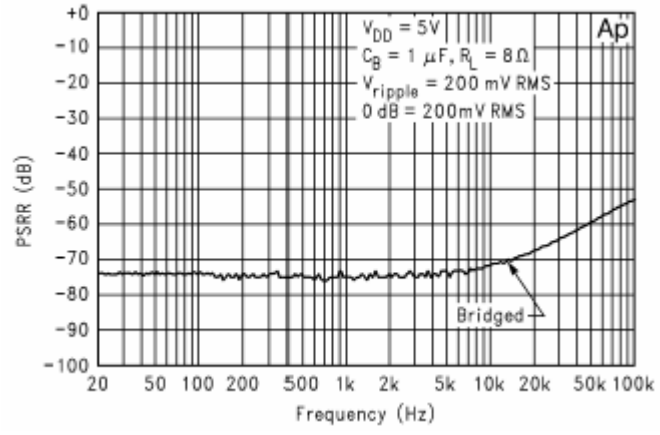
THD+N vs Frequency



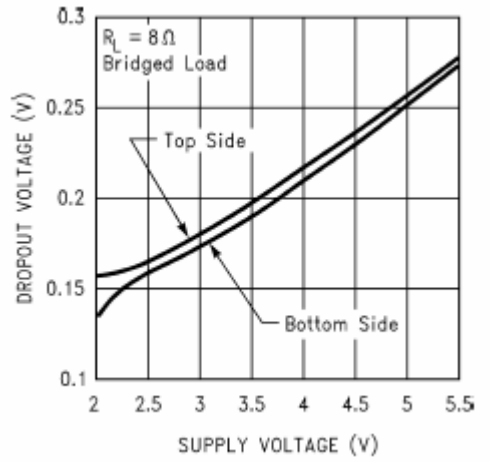
Output Power vs Load Resistance



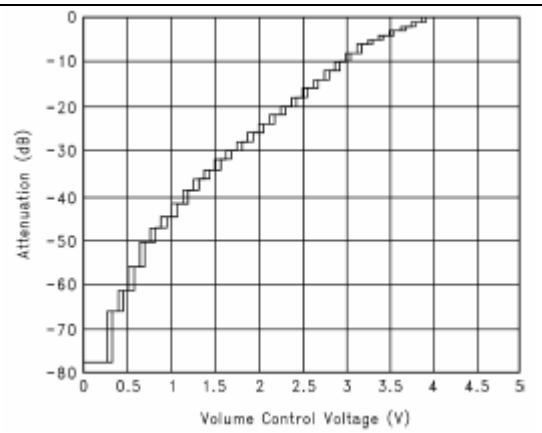
Output Power vs Load Resistance



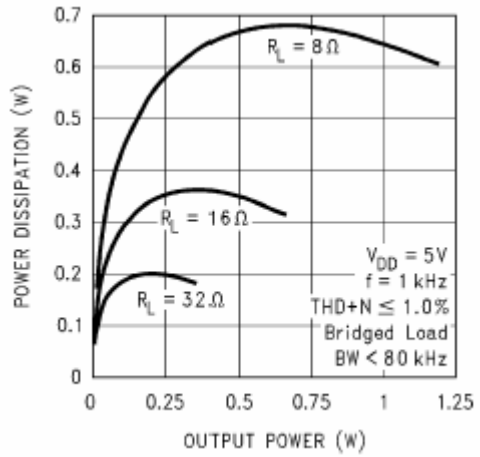
Power Supply Rejection Ratio



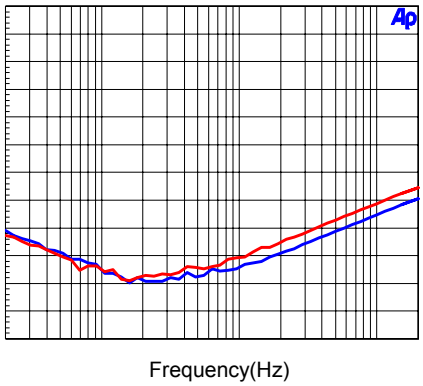
Dropout Voltage



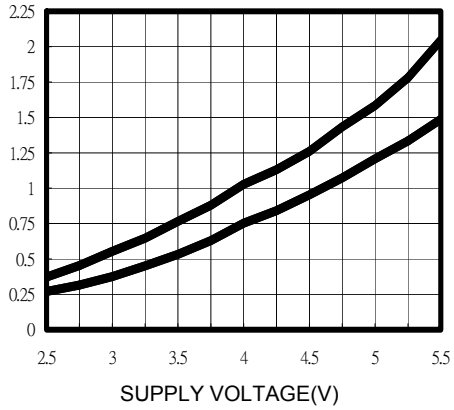
Volume Control Characteristics



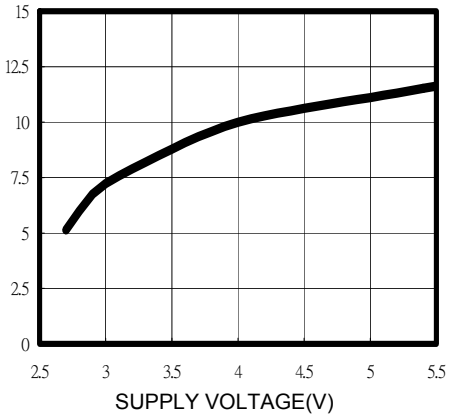
Power Dissipation vs Output Power



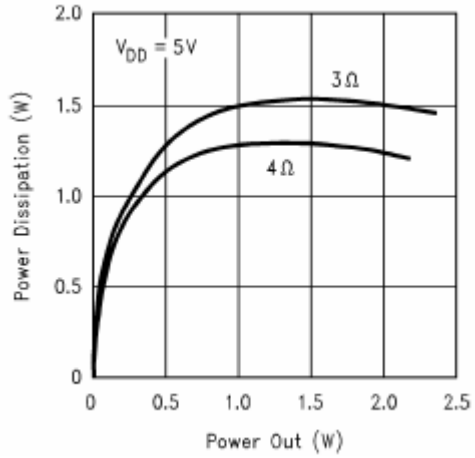
Crosstalk



Output Power vs Supply Voltage



Supply Current vs Supply Voltage



Power Dissipation vs Output Power

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Fax: 886-2-29174598
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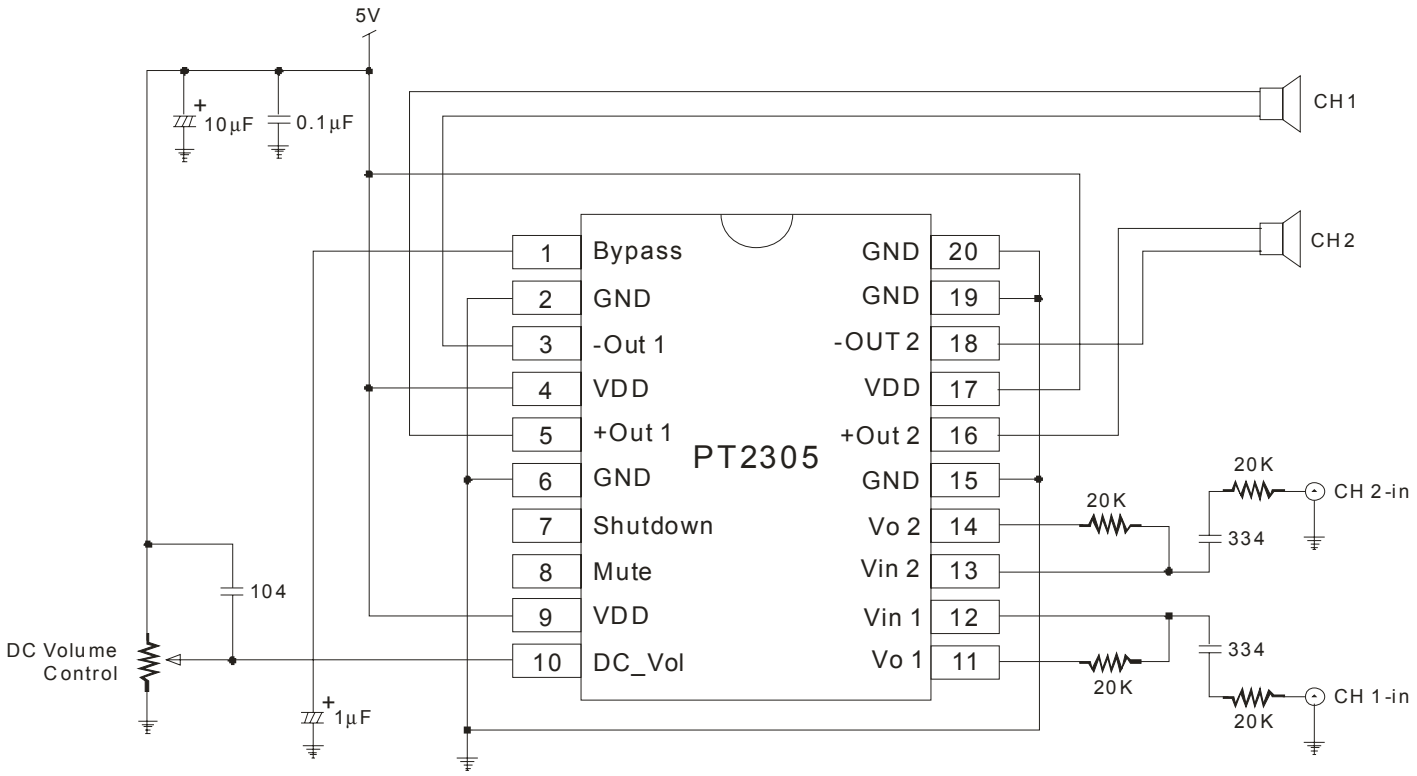
APPLICATION CIRCUIT



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2305	20 Pins, TSSOP, 173mil	PT2305
PT2305-HT	20 Pins, HTSSOP, 173mil	PT2305-HT
PT2305-S	20 Pins, SOP, 300mil	PT2305-S
PT2305-D	20 Pins, DIP, 300mil	PT2305-D

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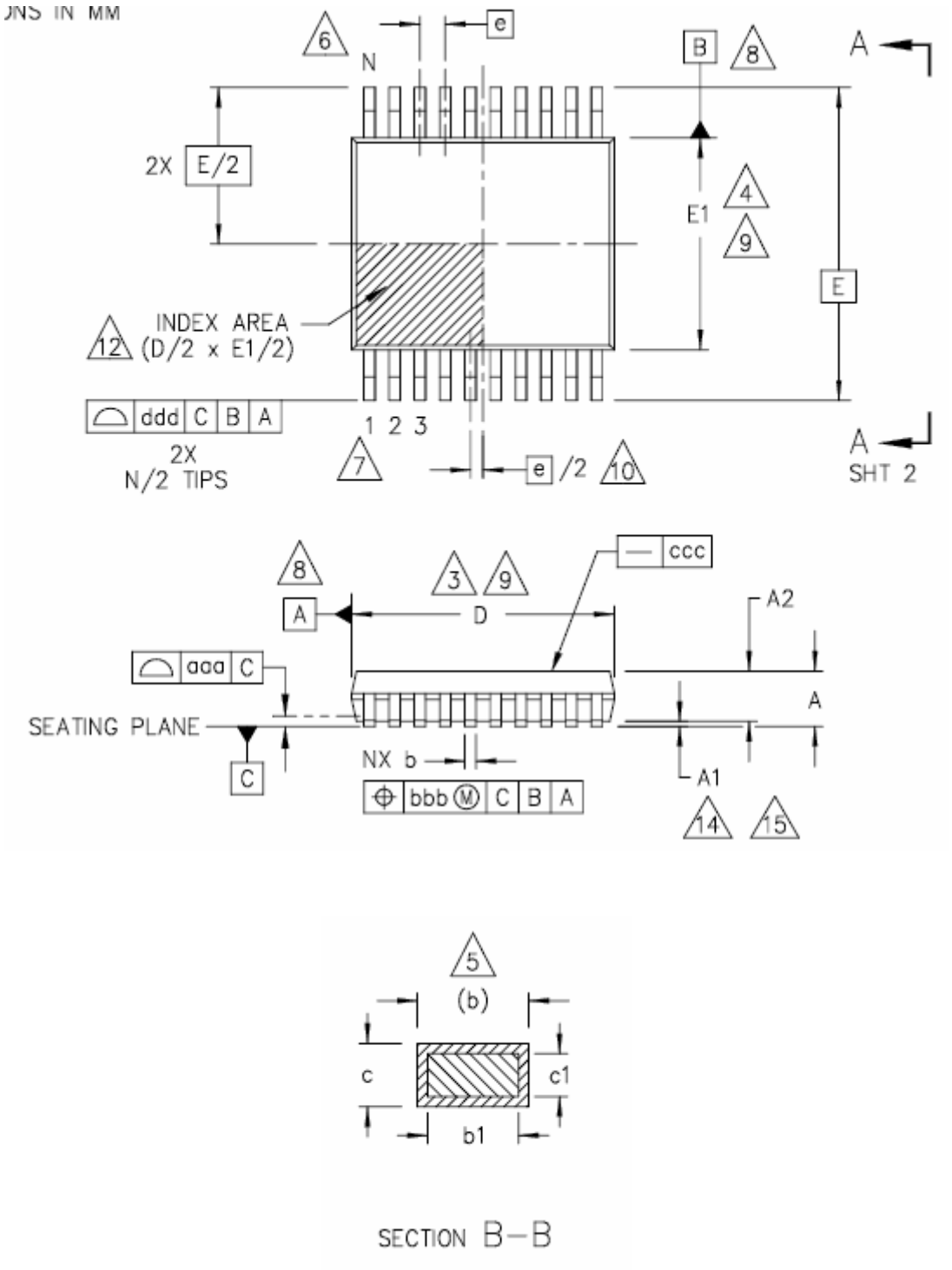
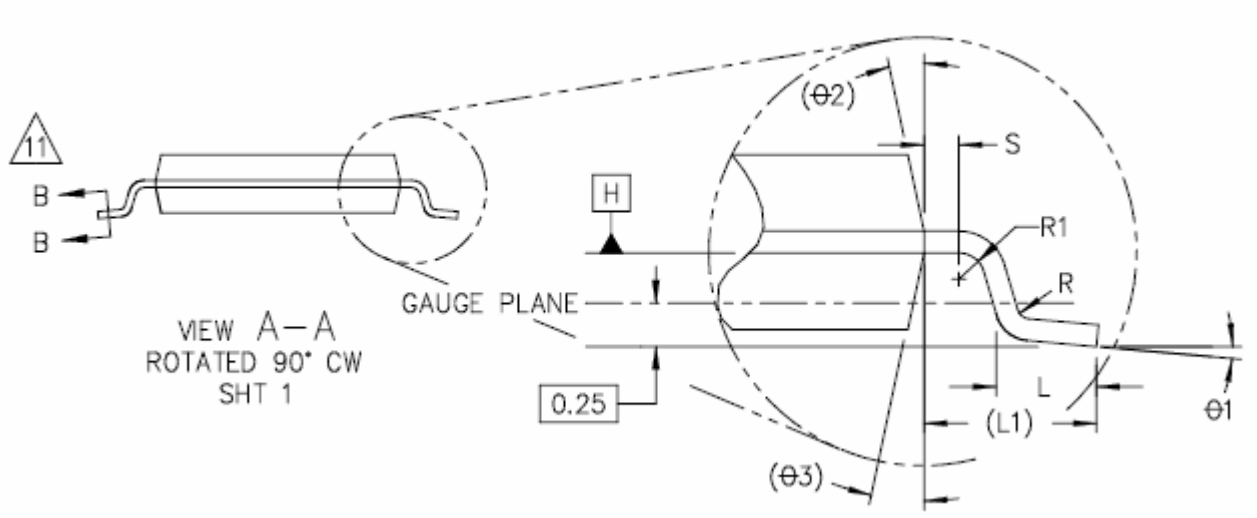
PACKAGE INFORAMTION

20PINS, TSSOP, 173MIL





Symbols	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
D	6.40	6.50	6.60
E		6.40 BSC.	
E1	4.30	4.40	4.50
e		0.65 BSC.	
L	0.45	0.60	0.75
L1		1.00 REF.	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2		12 REF.	
θ3		12 REF.	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Controlling Dimension: Millimeters
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per end.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
6. N is the maximum number of terminal positions for the specified package length. Depopulation is allowed, but only under the following conditions:
   - Depopulation may reduce N by increments of four leads only.
   - Only end leads may be removed.
   - Leads must be symmetrically arranged with respect to datum A (Note 10) to avoid any array shifting.
7. Terminal numbers are shown for reference only.
8. Datum A and B to be determined at datum plane H.
9. Dimensions D and E1 to be determined at datum plane H.
10. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per side, the center lead must be coincident with the package centerline, datum A.
11. Cross section B-B to be determined at 0.10 to 0.25 mm from the lead tip.
12. Details of the pin 1 identifier are optional, but must be located within the zone indicated.
13. D1 and E2 minimum dimensions of thermally enhanced types are variables depending on device function (die paddle size). D1 and E2 maximum dimensions can be equal to D/E1 maximum dimensions. End user should verify actual size of exposed thermal pad for specific device application.
14. A1 is defined as the vertical distance from the seating plane to the lowest point on the package body excluding the lid and or thermal enhancement on cavity down package configurations.
15. Caution should be taken during design, assembly and processing to prevent deposited board solder from holding the leads up off the board. This is applicable to thermal enhanced variations where A1 dimension is allowed to be zero.
16. Refer to JEDEC MO-153 Variation AC

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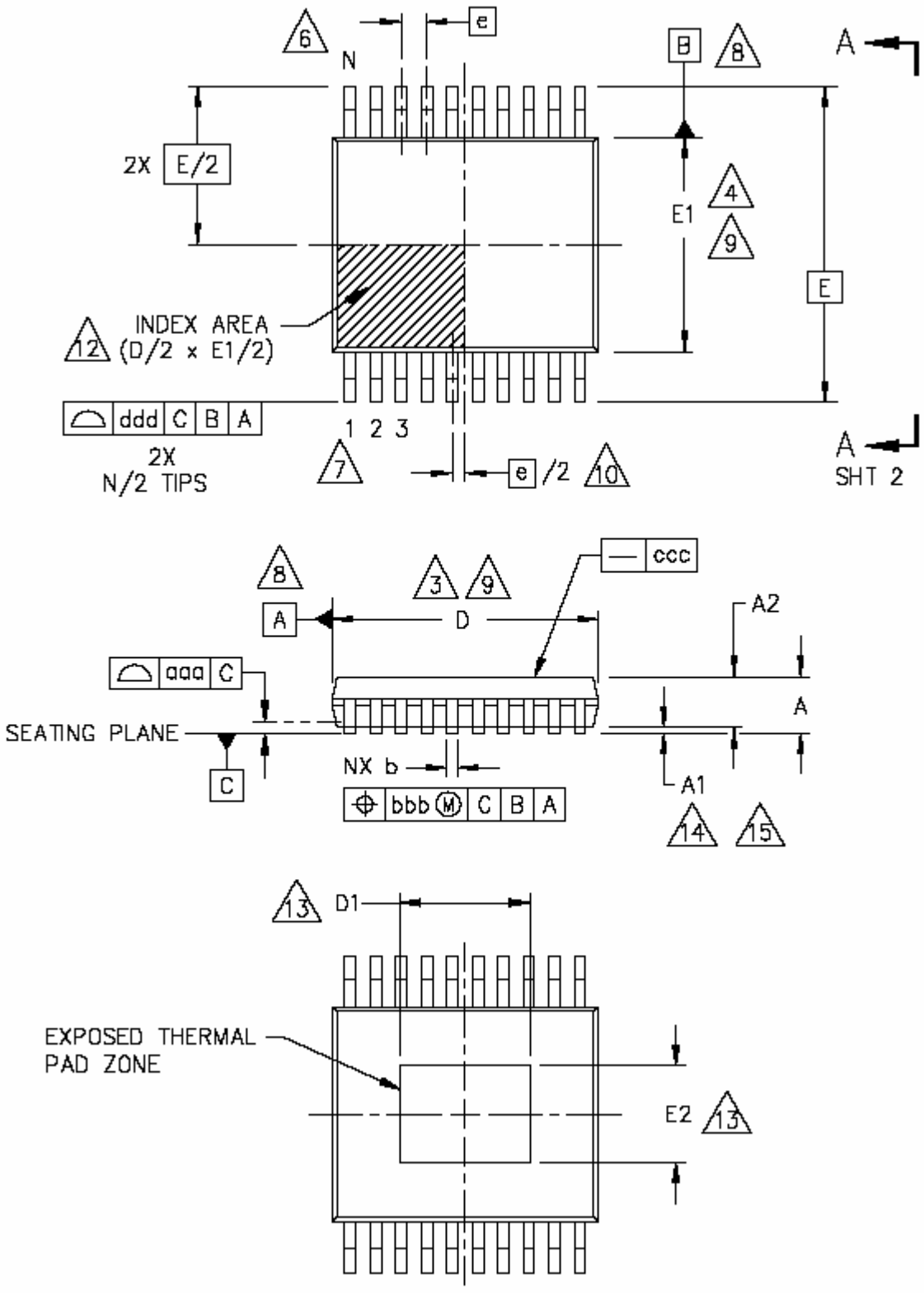
20 PINS, HTSSOP, 173MIL



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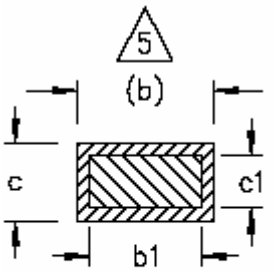
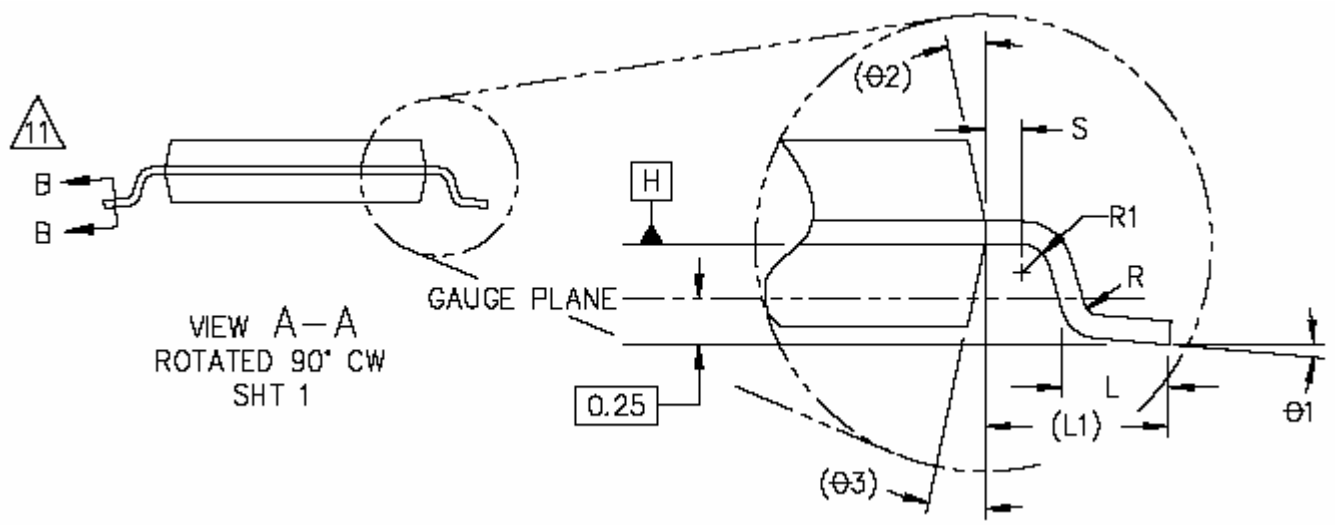


SECTION B–B



Symbols	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
D	6.40	6.50	6.60
D1	2.20	-	-
E	6.40 BSC.		
E1	4.30	4.40	4.50
E2	1.50	-	-
e	0.65 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	12 REF.		
θ3	12 REF.		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Controlling Dimension: Millimeters
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per end.
4. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
5. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
6. N is the maximum number of terminal positions for the specified package length. Depopulation is allowed, but only under the following conditions:
   - Depopulation may reduce N by increments of four leads only.
   - Only end leads may be removed.
   - Leads must be symmetrically arranged with respect to datum A (Note 10) to avoid any array shifting.
7. Terminal numbers are shown for reference only.
8. Datum A and B to be determined at datum plane H.
9. Dimensions D and E1 to be determined at datum plane H.
10. This dimension applies only to variations with an even number of leads per side. For variations with an odd number of leads per side, the center lead must be coincident with the package centerline, datum A.
11. Cross section B-B to be determined at 0.10 to 0.25 mm from the lead tip.
12. Details of the pin 1 identifier are optional, but must be located within the zone indicated.
13. D1 and E2 minimum dimensions of thermally enhanced types are variables depending on device function (die paddle size). D1 and E2 maximum dimensions can be equal to D/E1 maximum dimensions. End user should verify actual size of exposed thermal pad for specific device application.
14. A1 is defined as the vertical distance from the seating plane to the lowest point on the package body excluding the lid and or thermal enhancement on cavity down package configurations.
15. Caution should be taken during design, assembly and processing to prevent deposited board solder from holding the leads up off the board. This is applicable to thermal enhanced variations where A1 dimension is allowed to be zero.
16. Refer to JEDEC MO-153 Variation ACT

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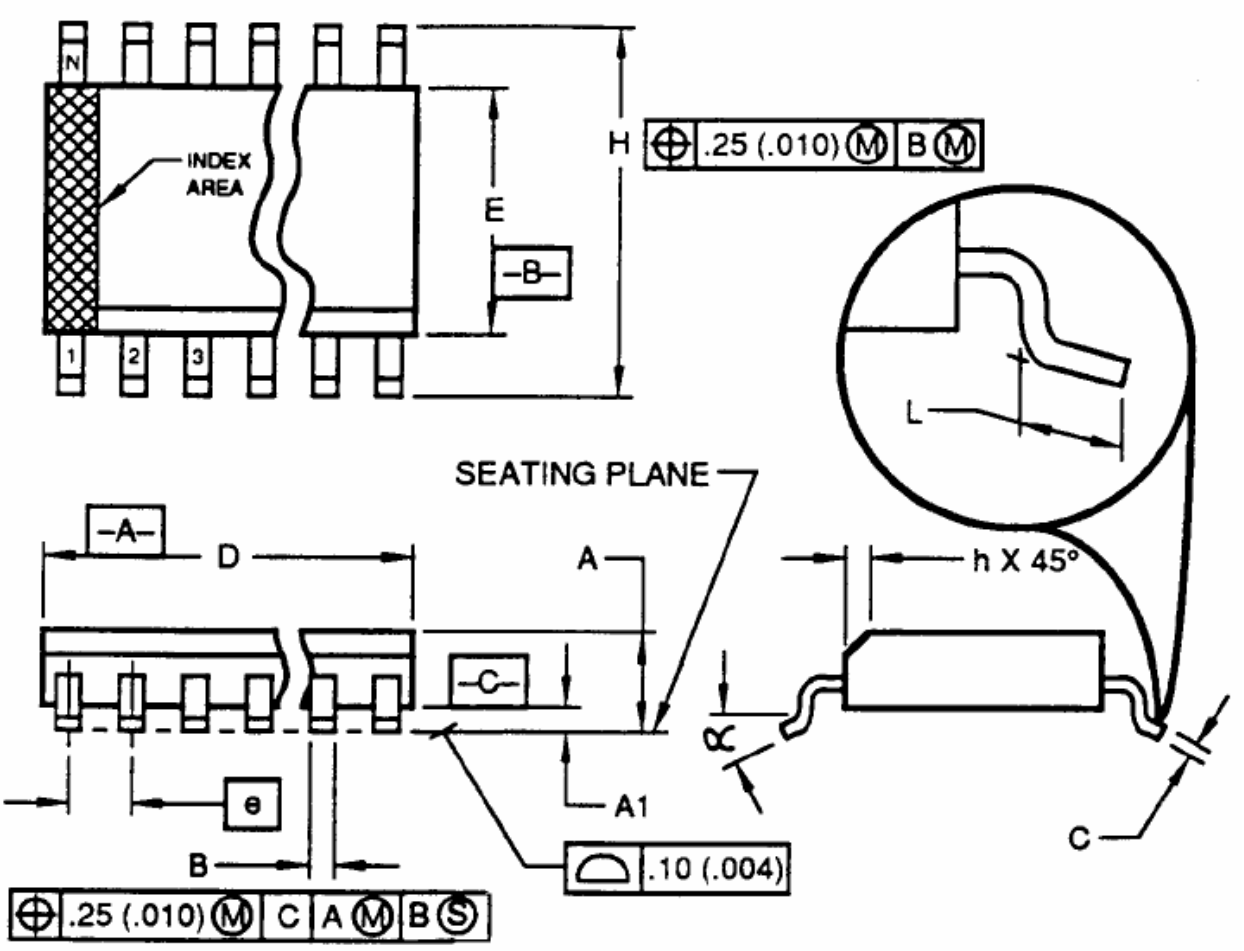
20 PINS, SOP, 300MIL



Symbol	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	12.60		13.00
E	7.40		7.60
e		1.27 bsc.	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
α	0°		8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=20)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013, Variation AC.

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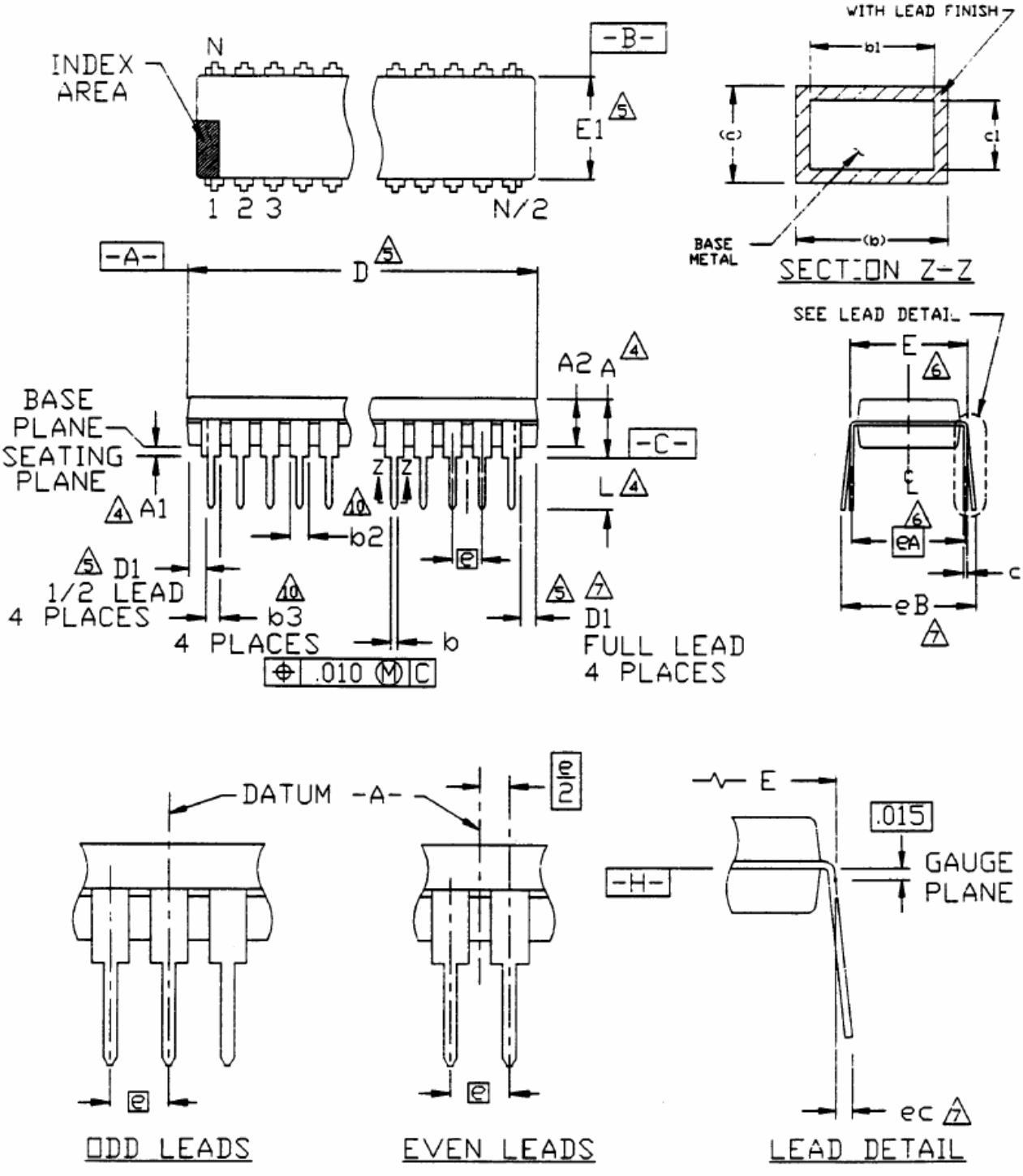
20PINS, DIP, 300 MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.980	1.030	1.060
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	-	0.100 bsc.	-
eA	-	0.300 bsc.	-
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension ”A”，”A1” and ”L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3
4. “D”，”D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c- .
6. “eB” and “eC” are measured at the lead tips with the leads unconstrained.
7. N is the number of the terminal positions (N=20)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
10. Distance between leads including dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
12. Refer to JEDEC MS-001, Variation AD.

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