

1. Overview

1.1 Features

The R8C/33A Group of single-chip MCUs incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

The R8C/33A Group has data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/33A Group.

Table 1.1 Specifications for R8C/33A Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 1.8$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/33A Group .
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	<ul style="list-style-type: none"> • Input-only: 1 pin • CMOS I/O ports: 27, selectable pull-up resistor • High current drive ports: 27
Clock	Clock generation circuits	<ul style="list-style-type: none"> • 3 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, low-speed on-chip oscillator), wait mode, stop mode Real-time clock (timer RE)
Interrupts		<ul style="list-style-type: none"> • Number of interrupt vectors: 69 • External Interrupt: 7 ($\overline{INT} \times 3$, Key input $\times 4$) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits \times 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		<ul style="list-style-type: none"> • 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits \times 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.2 Specifications for R8C/33A Group (2)

Item	Function	Specification
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART x 2 channel
	UART2	Clock synchronous serial I/O/UART, I ² C mode (I ² C-bus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C-bus)
I ² C bus		1 (shared with SSU)
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution x 12 channels, includes sample and hold function, with sweep mode
D/A Converter		8-bit resolution x 2 circuits
Comparator A		<ul style="list-style-type: none"> • 2 circuits (shared with voltage monitor 1 and voltage monitor 2) • External reference voltage input available
Comparator B		2 circuits
Flash Memory		<ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 to 5.5 V)
Current Consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 3.5 μA (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) Typ. 2.0 μA (VCC = 3.0 V, stop mode)
Operating Ambient Temperature		-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾
Package		32-pin LQFP Package code: PLQP0032GB-A (previous code: 32P6U-A)

Note:

1. Specify the D version if D version functions are to be used.

1.2 Product List

Table 1.3 lists Product List for R8C/33A Group, and Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/33A Group.

Table 1.3 Product List for R8C/33A Group **Current of Sep. 2009**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21331ANFP	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	N version
R5F21332ANFP	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334ANFP	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335ANFP	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336ANFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	
R5F21331ADFP (P)	4 Kbytes	1 Kbyte × 4	512 bytes	PLQP0032GB-A	D version
R5F21332ADFP (P)	8 Kbytes	1 Kbyte × 4	1 Kbyte	PLQP0032GB-A	
R5F21334ADFP (P)	16 Kbytes	1 Kbyte × 4	1.5 Kbytes	PLQP0032GB-A	
R5F21335ADFP (P)	24 Kbytes	1 Kbyte × 4	2 Kbytes	PLQP0032GB-A	
R5F21336ADFP (P)	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0032GB-A	

(P): Under planning

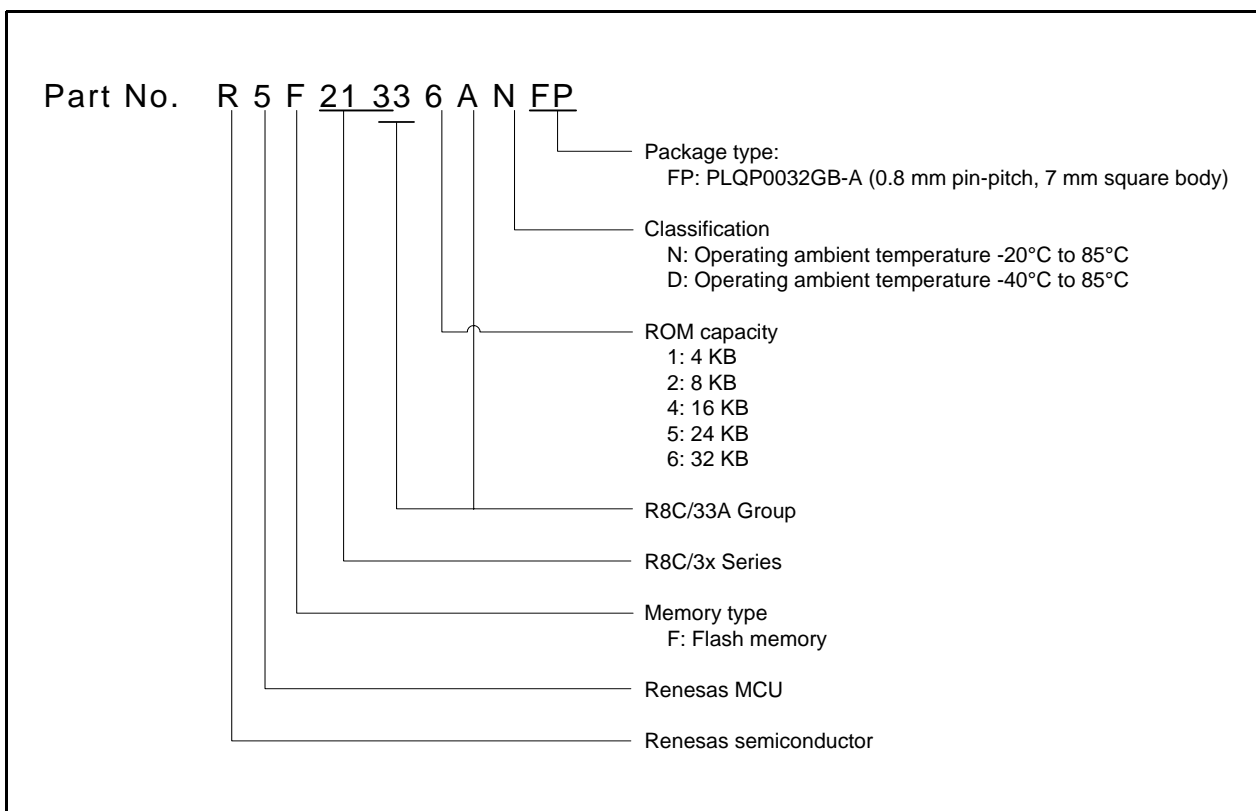


Figure 1.1 Part Number, Memory Size, and Package of R8C/33A Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

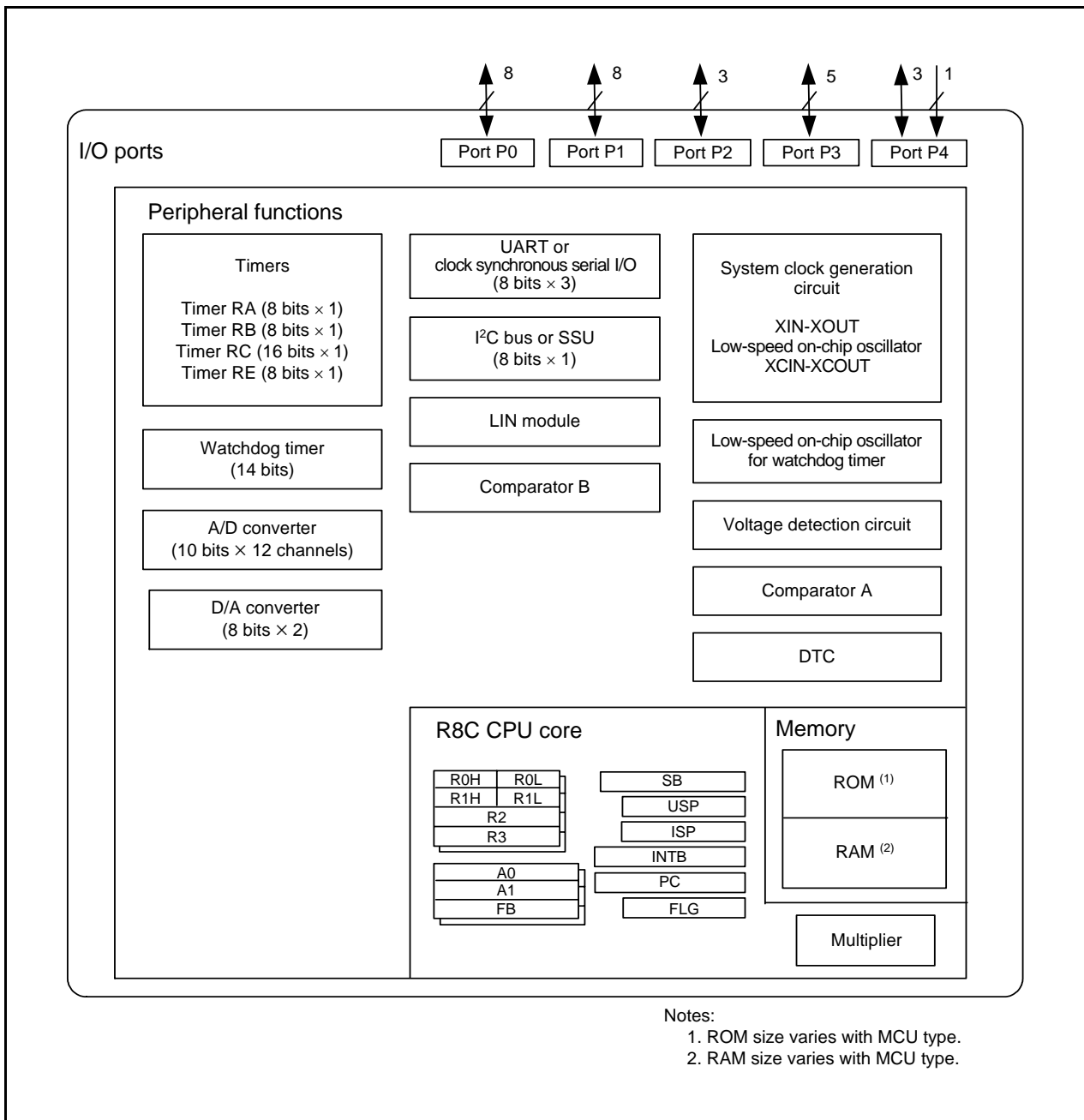


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines the Pin Name Information by Pin Number.

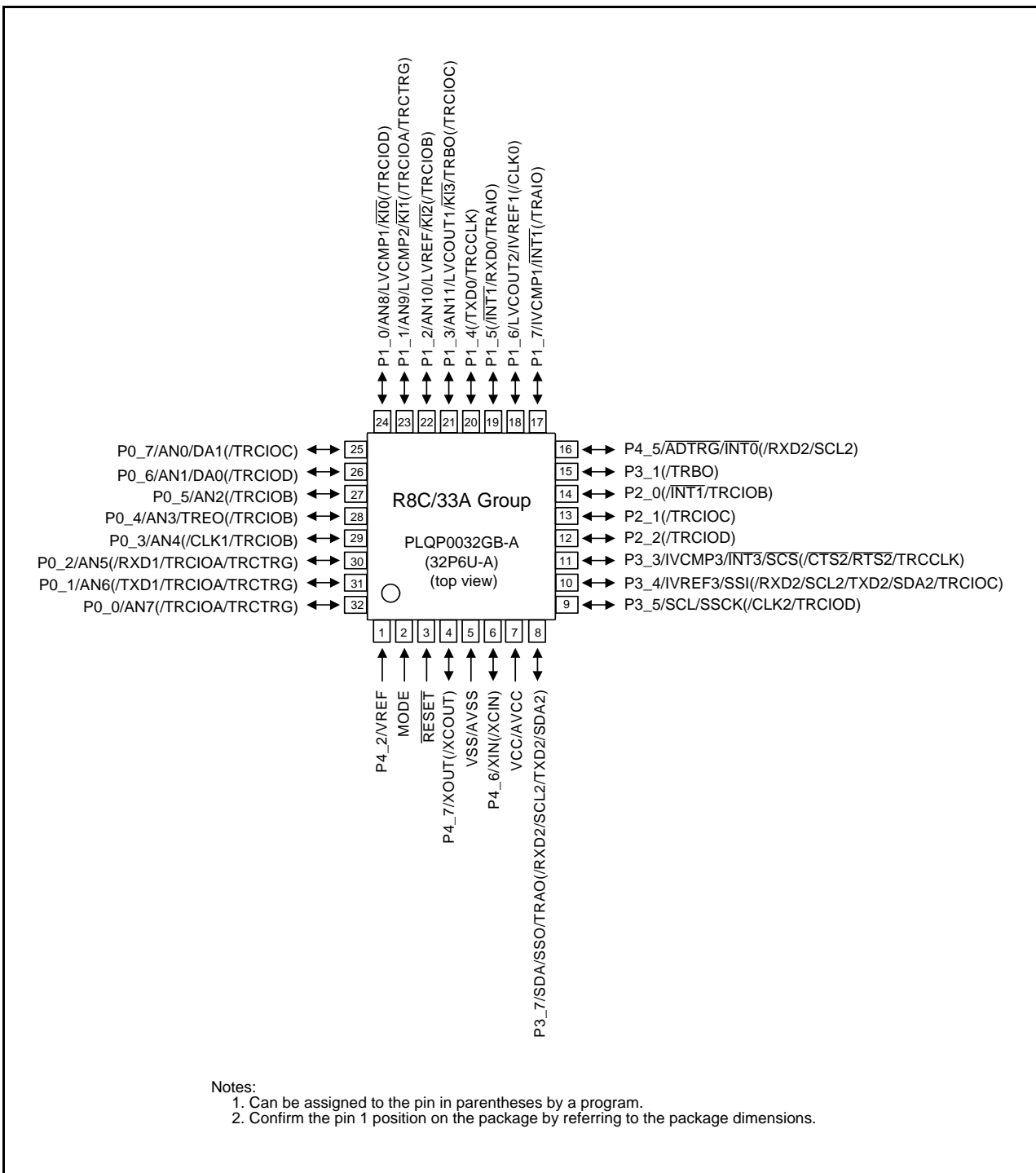


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator A, Comparator B, Voltage Detection Circuit
1		P4_2						VREF
2	MODE							
3	RESET							
4	XOUT(/XCOUT)	P4_7						
5	VSS/AVSS							
6	XIN(/XCIN)	P4_6						
7	VCC/AVCC							
8		P3_7		TRAO	(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	
9		P3_5		(TRCIOD)	(CLK2)	SSCK	SCL	
10		P3_4		(TRCIOA)	(RXD2/SCL2/ TXD2/SDA2)	SSI		IVREF3
11		P3_3	INT3	(TRCCLK)	(CTS2/RTS2)	SCS		IVCMP3
12		P2_2		(TRCIOD)				
13		P2_1		(TRCIOA)				
14		P2_0	(INT1)	(TRCIOB)				
15		P3_1		(TRBO)				
16		P4_5	INT0		(RXD2/SCL2)			ADTRG
17		P1_7	INT1	(TRAIO)				IVCMP1
18		P1_6			(CLK0)			LVCOUT2/IVREF1
19		P1_5	(INT1)	(TRAIO)	(RXD0)			
20		P1_4		(TRCCLK)	(TXD0)			
21		P1_3	KI3	TRBO (/TRCIOA)				AN11/LVCOUT1
22		P1_2	KI2	(TRCIOB)				AN10/LVREF
23		P1_1	KI1	(TRCIOA/ TRCTRG)				AN9/LVCMP2
24		P1_0	KI0	(TRCIOD)				AN8/LVCMP1
25		P0_7		(TRCIOA)				AN0/DA1
26		P0_6		(TRCIOD)				AN1/DA0
27		P0_5		(TRCIOB)				AN2
28		P0_4		TREO (/TRCIOB)				AN3
29		P0_3		(TRCIOB)	(CLK1)			AN4
30		P0_2		(TRCIOA/ TRCTRG)	(RXD1)			AN5
31		P0_1		(TRCIOA/ TRCTRG)	(TXD1)			AN6
32		P0_0		(TRCIOA/ TRCTRG)				AN7

Note:

1. Can be assigned to the pin in parentheses by a program.

1.5 Pin Functions

Tables 1.5 and 1.6 list Pin Functions.

Table 1.5 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	–	Apply 1.8 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	–	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open.
XCIN clock output	XCOU	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. INT0 is timer RB, and RC input pin.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA	TRAIO	I/O	Timer RA I/O pin
	TRAO	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RE	TREO	O	Divided clock output pin
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I ² C mode clock I/O pin
	SDA2	I/O	I ² C mode data I/O pin
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.6 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	AD external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator A	LVCMP1, LVCMP2	I	Comparator A analog voltage input pins
	LVREF	I	Comparator A reference voltage input pin
	LVCOUT1, LVCOUT2	O	Comparator A output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
Voltage detection circuit	LVCMP2	I	Detection voltage input pin for voltage detection 2
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_2, P3_1, P3_3 to P3_5, P3_7, P4_5 to P4_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

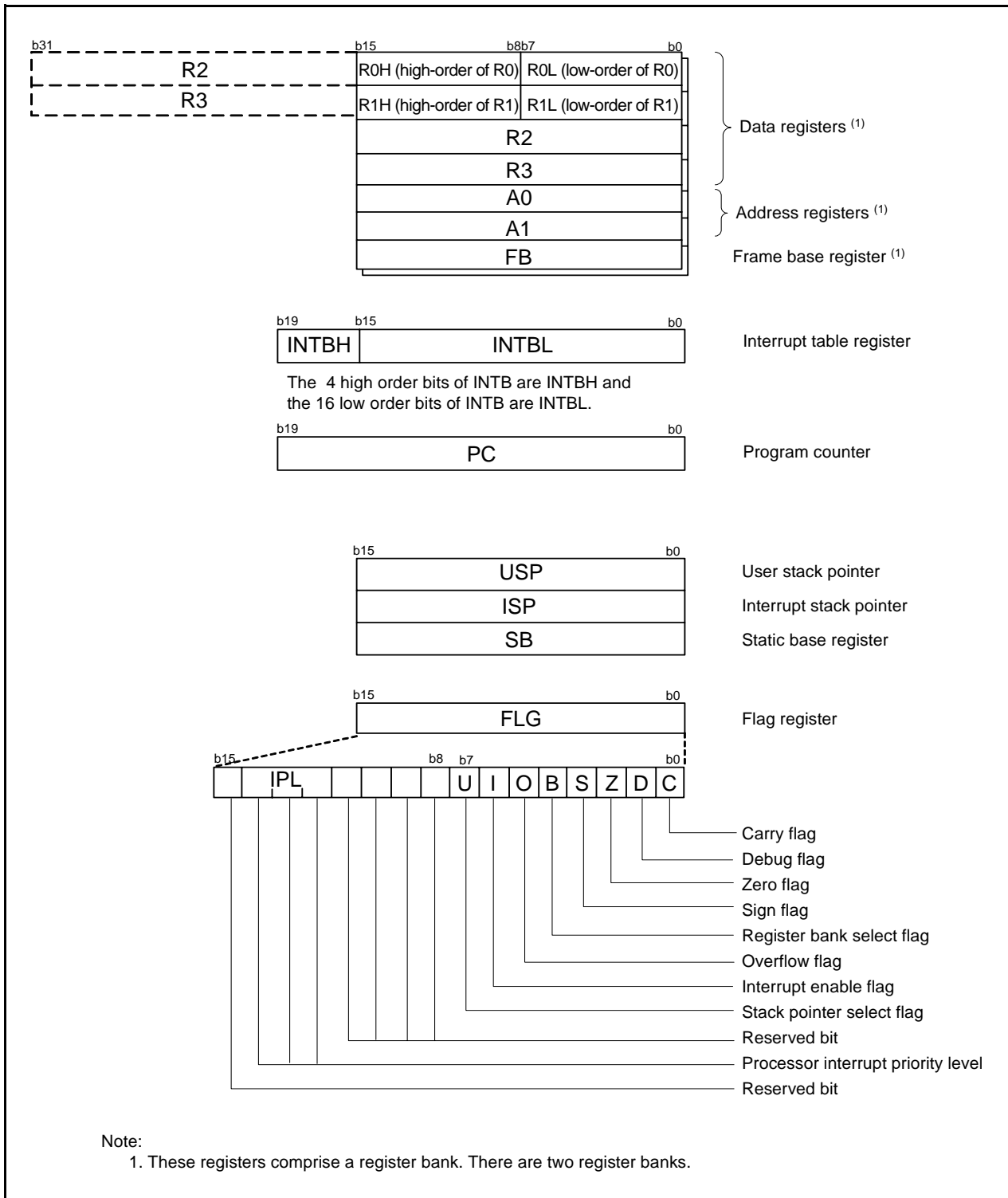


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/33A Group

Figure 3.1 is a Memory Map of R8C/33A Group. The R8C/33A Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 00000h. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

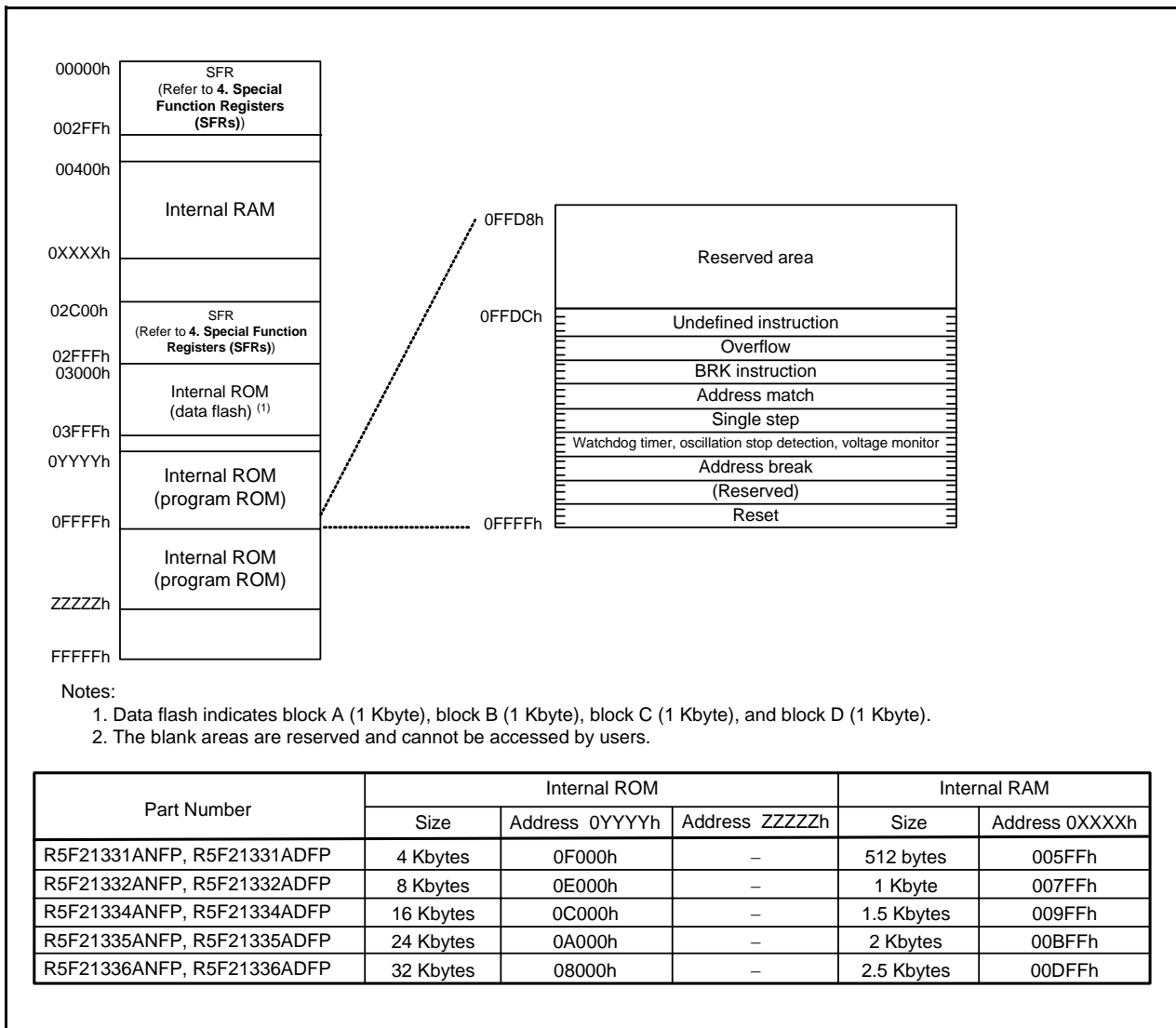


Figure 3.1 Memory Map of R8C/33A Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h	Voltage Monitor Circuit/Comparator A Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	1000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1/Compare A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2/Compare A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After Reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After Reset
0140h			
0141h			
0142h			
0143h			
0144h			
0145h			
0146h			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			XXh
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h	UART1 Transmit/Receive Mode Register	U1MR	00h
0161h	UART1 Bit Rate Register	U1BRG	XXh
0162h	UART1 Transmit Buffer Register	U1TB	XXh
0163h			XXh
0164h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
0165h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
0166h	UART1 Receive Buffer Register	U1RB	XXh
0167h			XXh
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111010b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	1000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01EC			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h	Port P2 Drive Capacity Control Register	P2DRR	00h
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset		
2C70h	DTC Control Data 6	DTCD6	XXh		
2C71h			XXh		
2C72h			XXh		
2C73h			XXh		
2C74h			XXh		
2C75h			XXh		
2C76h			XXh		
2C77h			XXh		
2C78h			DTC Control Data 7	DTCD7	XXh
2C79h					XXh
2C7Ah	XXh				
2C7Bh	XXh				
2C7Ch	XXh				
2C7Dh	XXh				
2C7Eh	XXh				
2C7Fh	XXh				
2C80h	DTC Control Data 8	DTCD8			XXh
2C81h					XXh
2C82h			XXh		
2C83h			XXh		
2C84h			XXh		
2C85h			XXh		
2C86h			XXh		
2C87h			XXh		
2C88h			DTC Control Data 9	DTCD9	XXh
2C89h					XXh
2C8Ah	XXh				
2C8Bh	XXh				
2C8Ch	XXh				
2C8Dh	XXh				
2C8Eh	XXh				
2C8Fh	XXh				
2C90h	DTC Control Data 10	DTCD10			XXh
2C91h					XXh
2C92h			XXh		
2C93h			XXh		
2C94h			XXh		
2C95h			XXh		
2C96h			XXh		
2C97h			XXh		
2C98h			DTC Control Data 11	DTCD11	XXh
2C99h					XXh
2C9Ah	XXh				
2C9Bh	XXh				
2C9Ch	XXh				
2C9Dh	XXh				
2C9Eh	XXh				
2C9Fh	XXh				
2CA0h	DTC Control Data 12	DTCD12			XXh
2CA1h					XXh
2CA2h			XXh		
2CA3h			XXh		
2CA4h			XXh		
2CA5h			XXh		
2CA6h			XXh		
2CA7h			XXh		
2CA8h			DTC Control Data 13	DTCD13	XXh
2CA9h					XXh
2CAAh	XXh				
2CABh	XXh				
2CACH	XXh				
2CADh	XXh				
2CAEh	XXh				
2CAFh	XXh				

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFh			

X: Undefined

Note:

- The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Register	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
- The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /AV _{CC}	Supply voltage		-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} + 0.3	V
V _O	Output voltage		-0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	-40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit		
				Min.	Typ.	Max.			
V _{CC} /AV _{CC}	Supply voltage			1.8	–	5.5	V		
V _{SS} /AV _{SS}	Supply voltage			–	0	–	V		
V _{IH}	Input “H” voltage	Other than CMOS input			0.8 V _{CC}	–	V _{CC}	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5 V _{CC}	–	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.55 V _{CC}	–	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.65 V _{CC}	–	V _{CC}	V
			Input level selection : 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65 V _{CC}	–	V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0.7 V _{CC}	–	V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0.8 V _{CC}	–	V _{CC}	V	
		Input level selection : 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.85 V _{CC}	–	V _{CC}	V		
			2.7 V ≤ V _{CC} < 4.0 V	0.85 V _{CC}	–	V _{CC}	V		
1.8 V ≤ V _{CC} < 2.7 V	0.85 V _{CC}		–	V _{CC}	V				
V _{IL}	Input “L” voltage	Other than CMOS input			0	–	0.2 V _{CC}	V	
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	–	0.2 V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	–	0.2 V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	–	0.2 V _{CC}	V
			Input level selection : 0.5 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	–	0.4 V _{CC}	V	
				2.7 V ≤ V _{CC} < 4.0 V	0	–	0.3 V _{CC}	V	
				1.8 V ≤ V _{CC} < 2.7 V	0	–	0.2 V _{CC}	V	
		Input level selection : 0.7 V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	–	0.55 V _{CC}	V		
			2.7 V ≤ V _{CC} < 4.0 V	0	–	0.45 V _{CC}	V		
1.8 V ≤ V _{CC} < 2.7 V	0		–	0.35 V _{CC}	V				
I _{OH(sum)}	Peak sum output “H” current	Sum of all pins I _{OH(peak)}			–	–	–160	mA	
I _{OH(sum)}	Average sum output “H” current	Sum of all pins I _{OH(avg)}			–	–	–80	mA	
I _{OH(peak)}	Peak output “H” current	Drive capacity Low			–	–	–10	mA	
		Drive capacity High			–	–	–40	mA	
I _{OH(avg)}	Average output “H” current	Drive capacity Low			–	–	–5	mA	
		Drive capacity High			–	–	–20	mA	
I _{OL(sum)}	Peak sum output “L” current	Sum of all pins I _{OL(peak)}			–	–	160	mA	
I _{OL(sum)}	Average sum output “L” current	Sum of all pins I _{OL(avg)}			–	–	80	mA	
I _{OL(peak)}	Peak output “L” current	Drive capacity Low			–	–	10	mA	
		Drive capacity High			–	–	40	mA	
I _{OL(avg)}	Average output “L” current	Drive capacity Low			–	–	5	mA	
		Drive capacity High			–	–	20	mA	
f _(XIN)	XIN clock input oscillation frequency	2.7 V ≤ V _{CC} ≤ 5.5 V			–	–	20	MHz	
		1.8 V ≤ V _{CC} < 2.7 V			–	–	5	MHz	
f _(XCIN)	XCIN clock input oscillation frequency	1.8 V ≤ V _{CC} ≤ 5.5 V			–	32.768	50	kHz	
–	System clock frequency	2.7 V ≤ V _{CC} ≤ 5.5 V			–	–	20	MHz	
		1.8 V ≤ V _{CC} < 2.7 V			–	–	5	MHz	
f _(BCLK)	CPU clock frequency	2.7 V ≤ V _{CC} ≤ 5.5 V			–	–	20	MHz	
		1.8 V ≤ V _{CC} < 2.7 V			–	–	5	MHz	

Notes:

1. V_{CC} = 1.8 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

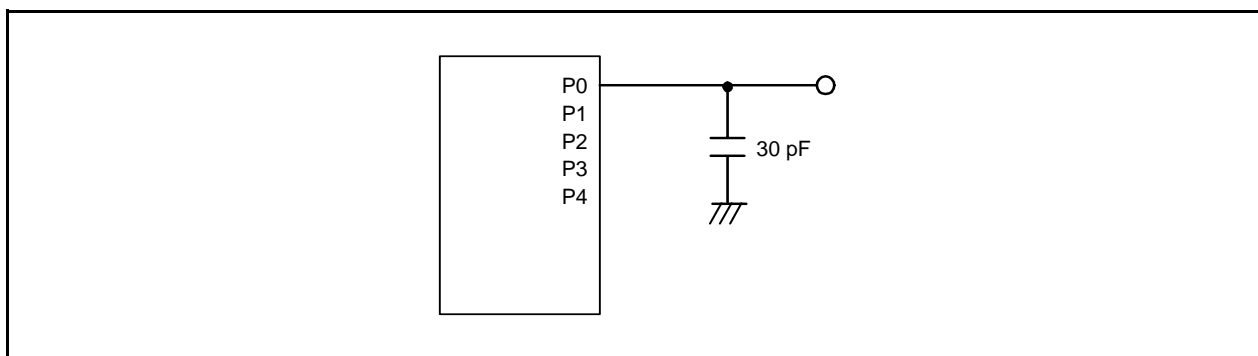


Figure 5.1 Ports P0 to P4 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		$V_{ref} = AV_{CC}$	–	–	10	Bit
–	Absolute accuracy	10-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 3	LSB
			$V_{ref} = AV_{CC} = 3.3\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 5	LSB
			$V_{ref} = AV_{CC} = 3.0\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 5	LSB
			$V_{ref} = AV_{CC} = 2.2\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 5	LSB
		8-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 2	LSB
			$V_{ref} = AV_{CC} = 3.3\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 2	LSB
			$V_{ref} = AV_{CC} = 3.0\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 2	LSB
			$V_{ref} = AV_{CC} = 2.2\text{ V}$ AN0 to AN7 input, AN8 to AN11 input	–	–	± 2	LSB
ϕ_{AD}	A/D conversion clock		$4.0\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$	2	–	20	MHz
			$3.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$	2	–	16	MHz
			$2.7\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$	2	–	10	MHz
			$2.2\text{ V} \leq V_{ref} = AV_{CC} \leq 5.5\text{ V}^{(2)}$	2	–	5	MHz
–	Tolerance level impedance			–	3	–	$k\Omega$
DNL	Differential non-linearity error			–	–	± 1	LSB
t_{CONV}	Conversion time	10-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$, $\phi_{AD} = 20\text{ MHz}$	2.15	–	–	μs
		8-bit mode	$V_{ref} = AV_{CC} = 5.0\text{ V}$, $\phi_{AD} = 20\text{ MHz}$	2.15	–	–	μs
t_{SAMP}	Sampling time		$\phi_{AD} = 20\text{ MHz}$	0.75	–	–	μs
I_{Vref}	V_{ref} current		$V_{CC} = 5\text{ V}$, $XIN = f_1 = \phi_{AD} = 20\text{ MHz}$	–	45	–	μA
V_{ref}	Reference voltage			2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage ⁽³⁾			0	–	V_{ref}	V

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2$ to 5.5 V , $V_{SS} = 0\text{ V}$ at $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- When the CPU and flash memory stop, the A/D conversion result will be undefined.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution		–	–	8	Bit
–	Absolute accuracy		–	–	2.5	LSB
t_{su}	Setup time		–	–	3	μs
R_o	Output resistor		–	6	–	$k\Omega$
I_{Vref}	Reference power input current	(Note 2)	–	–	1.5	mA

Notes:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V at $T_{opr} = -20$ to $85^\circ C$ (N version) / -40 to $85^\circ C$ (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DA_i register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator A Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
LVREF	External reference voltage input range		1.4	–	V_{CC}	V
LVCMP1, LVCMP2	External comparison voltage input range		–0.3	–	$V_{CC} + 0.3$	V
–	Offset		–	50	200	mV
–	Comparator output delay time (2)	At falling, $V_i = V_{ref} - 100$ mV	–	3	–	μs
–		At falling, $V_i = V_{ref} - 1$ V or below	–	1.5	–	μs
–		At rising, $V_i = V_{ref} + 100$ mV	–	2	–	μs
–		At rising, $V_i = V_{ref} + 1$ V or above	–	0.5	–	μs
–	Comparator operating current	$V_{CC} = 5.0$ V	–	0.5	–	μA

Notes:

- $V_{CC} = 2.7$ to 5.5 V, $T_{opr} = -20$ to $85^\circ C$ (N version) / -40 to $85^\circ C$ (D version), unless otherwise specified.
- When the digital filter is disabled.

Table 5.6 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	$IVREF1$, $IVREF3$ input reference voltage		0	–	$V_{CC} - 1.4$	V
V_i	$IVCMP1$, $IVCMP3$ input voltage		–0.3	–	$V_{CC} + 0.3$	V
–	Offset		–	5	100	mV
t_d	Comparator output delay time (2)	$V_i = V_{ref} \pm 100$ mV	–	0.1	–	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	–	17.5	–	μA

Notes:

- $V_{CC} = 2.7$ to 5.5 V, $T_{opr} = -20$ to $85^\circ C$ (N version) / -40 to $85^\circ C$ (D version), unless otherwise specified.
- When the digital filter is disabled.

Table 5.7 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	–	–	times
–	Byte program time		–	80	–	μs
–	Block erase time		–	0.3	–	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		33	–	–	ms
–	Suspend interval necessary for auto-erasure to complete		33	–	–	ms
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	–	–	year

Notes:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	–	μs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	–	μs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	–	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	–	s
t _d (SR-SUS)	Time delay from suspend request until suspend		–	–	5+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		33	–	–	ms
–	Suspend interval necessary for auto-erasure to complete		33	–	–	ms
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		1.8	–	5.5	V
–	Program, erase temperature		–20 ⁽⁷⁾	–	85	°C
–	Data hold time ⁽⁸⁾	Ambient temperature = 55°C	20	–	–	year

Notes:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

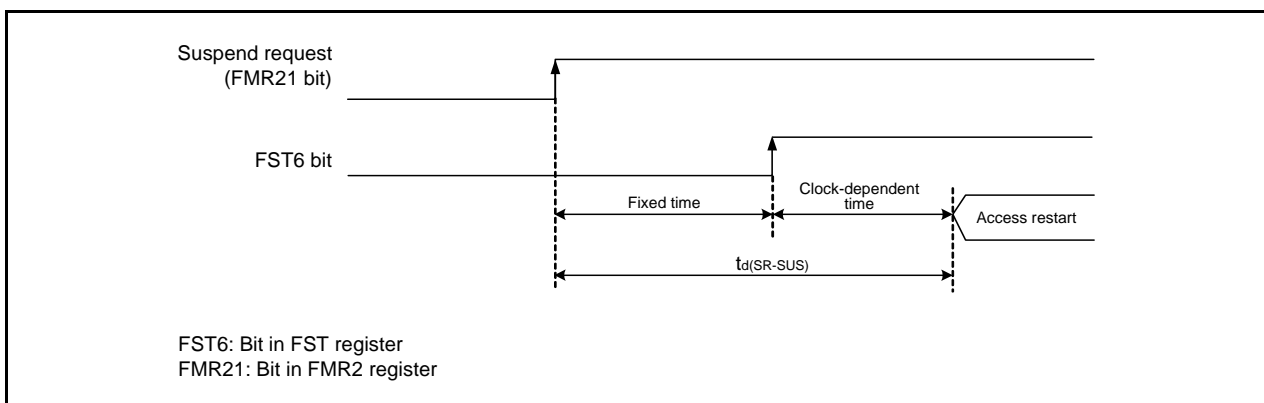
**Figure 5.2 Time delay until Suspend**

Table 5.9 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} (2)		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} (2)		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} (2)		2.65	2.85	3.00	V
	Voltage detection level V _{det0_3} (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of V _{cc} from 5 V to (V _{det0_0} – 0.1) V	–	6	150	μs
–	Voltage detection circuit self power consumption	VCA25 = 1, V _{cc} = 5.0 V	–	1.5	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (3)		–	–	100	μs

Notes:

1. The measurement condition is V_{cc} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} (2)	At the falling of V _{cc}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} (2)	At the falling of V _{cc}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} (2)	At the falling of V _{cc}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} (2)	At the falling of V _{cc}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} (2)	At the falling of V _{cc}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} (2)	At the falling of V _{cc}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} (2)	At the falling of V _{cc}	2.90	3.10	3.30	V
	Voltage detection level V _{det1_7} (2)	At the falling of V _{cc}	3.05	3.25	3.45	V
	Voltage detection level V _{det1_8} (2)	At the falling of V _{cc}	3.20	3.40	3.60	V
	Voltage detection level V _{det1_9} (2)	At the falling of V _{cc}	3.35	3.55	3.75	V
	Voltage detection level V _{det1_A} (2)	At the falling of V _{cc}	3.50	3.70	3.90	V
	Voltage detection level V _{det1_B} (2)	At the falling of V _{cc}	3.65	3.85	4.05	V
	Voltage detection level V _{det1_C} (2)	At the falling of V _{cc}	3.80	4.00	4.20	V
	Voltage detection level V _{det1_D} (2)	At the falling of V _{cc}	3.95	4.15	4.35	V
	Voltage detection level V _{det1_E} (2)	At the falling of V _{cc}	4.10	4.30	4.50	V
	Voltage detection level V _{det1_F} (2)	At the falling of V _{cc}	4.25	4.45	4.65	V
–	Hysteresis width at the rising of V _{cc} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	–	0.07	–	V
		V _{det1_6} to V _{det1_F} selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of V _{cc} from 5 V to (V _{det1_0} – 0.1) V	–	60	150	μs
–	Voltage detection circuit self power consumption	VCA26 = 1, V _{cc} = 5.0 V	–	1.7	–	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts (4)		–	–	100	μs

Notes:

1. The measurement condition is V_{cc} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.11 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2	Voltage detection level Vdet2_0 ⁽²⁾	At the falling of Vcc	3.70	4.00	4.30	V
	Voltage detection level Vdet2_EXT ⁽²⁾	At the falling of LVCMP2	1.20	1.34	1.48	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time ⁽³⁾	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	μs
–	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	–	1.7	–	μA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		–	–	100	μs

Notes:

1. The measurement condition is Vcc = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
3. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
trth	External power Vcc rise gradient		0	–	50000	mV/msec

Notes:

1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

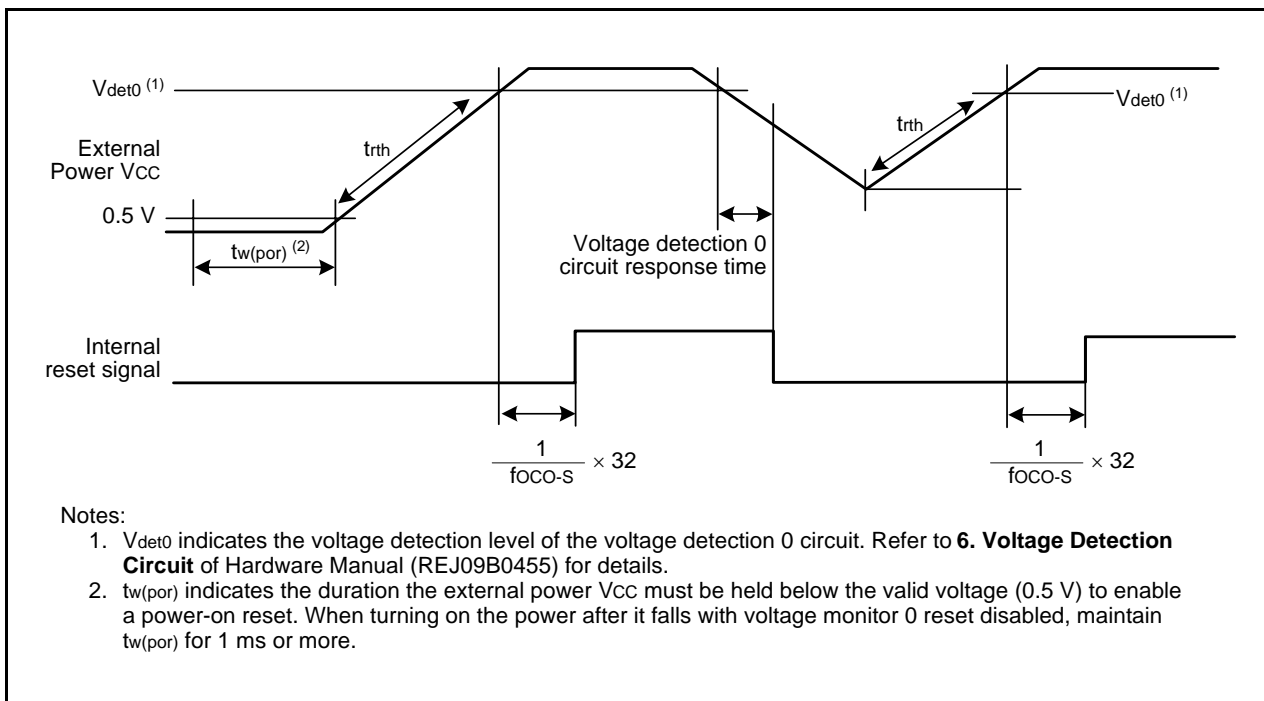
**Figure 5.3 Power-on Reset Circuit Electrical Characteristics**

Table 5.13 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		60	125	250	kHz
–	Oscillation stability time	V _{CC} = 5.0 V, T _{opr} = 25°C	–	30	100	μs
–	Self power consumption at oscillation	V _{CC} = 5.0 V, T _{opr} = 25°C	–	2	–	μA

Note:

1. V_{CC} = 1.8 to 5.5 V, T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Table 5.14 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during power-on ⁽²⁾		–	–	2000	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.15 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tsucyc	SSCK clock cycle time			4	–	–	tcyc (2)
tHI	SSCK clock "H" width			0.4	–	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	–	0.6	tsucyc
tRISE	SSCK clock rising time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tFALL	SSCK clock falling time	Master		–	–	1	tcyc (2)
		Slave		–	–	1	μs
tsu	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tcyc (2)
tLEAD	$\overline{\text{SCS}}$ setup time	Slave		1tcyc + 50	–	–	ns
tLAG	$\overline{\text{SCS}}$ hold time	Slave		1tcyc + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tcyc (2)
tsa	SSI slave access time		$2.7 \text{ V} \leq V_{\text{CC}} \leq 5.5 \text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8 \text{ V} \leq V_{\text{CC}} < 2.7 \text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns
tor	SSI slave out open time		$2.7 \text{ V} \leq V_{\text{CC}} \leq 5.5 \text{ V}$	–	–	$1.5\text{tcyc} + 100$	ns
			$1.8 \text{ V} \leq V_{\text{CC}} < 2.7 \text{ V}$	–	–	$1.5\text{tcyc} + 200$	ns

Notes:

1. $V_{\text{CC}} = 1.8$ to 5.5 V , $V_{\text{SS}} = 0 \text{ V}$ at $T_{\text{opr}} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1\text{tcyc} = 1/f_1(\text{s})$

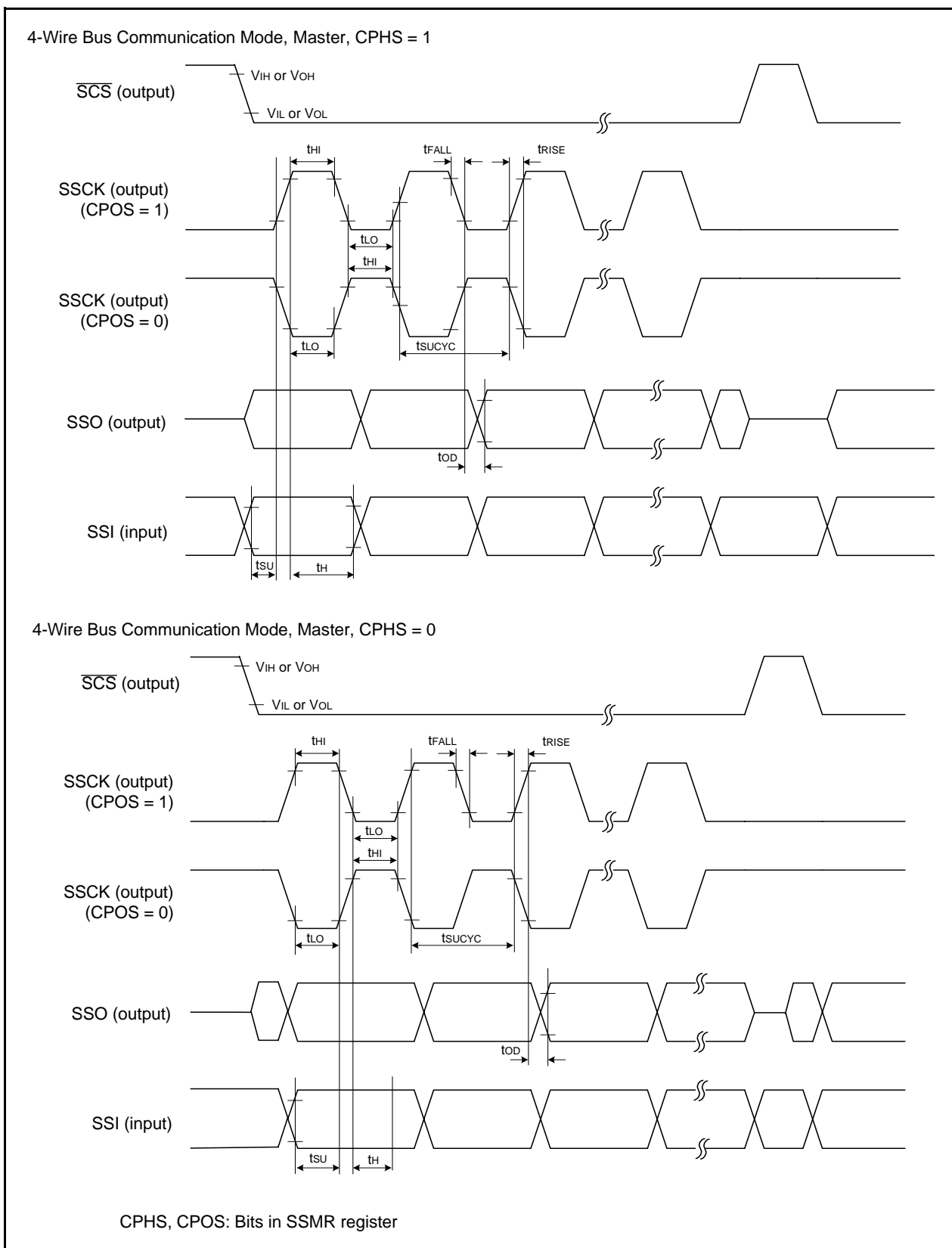


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

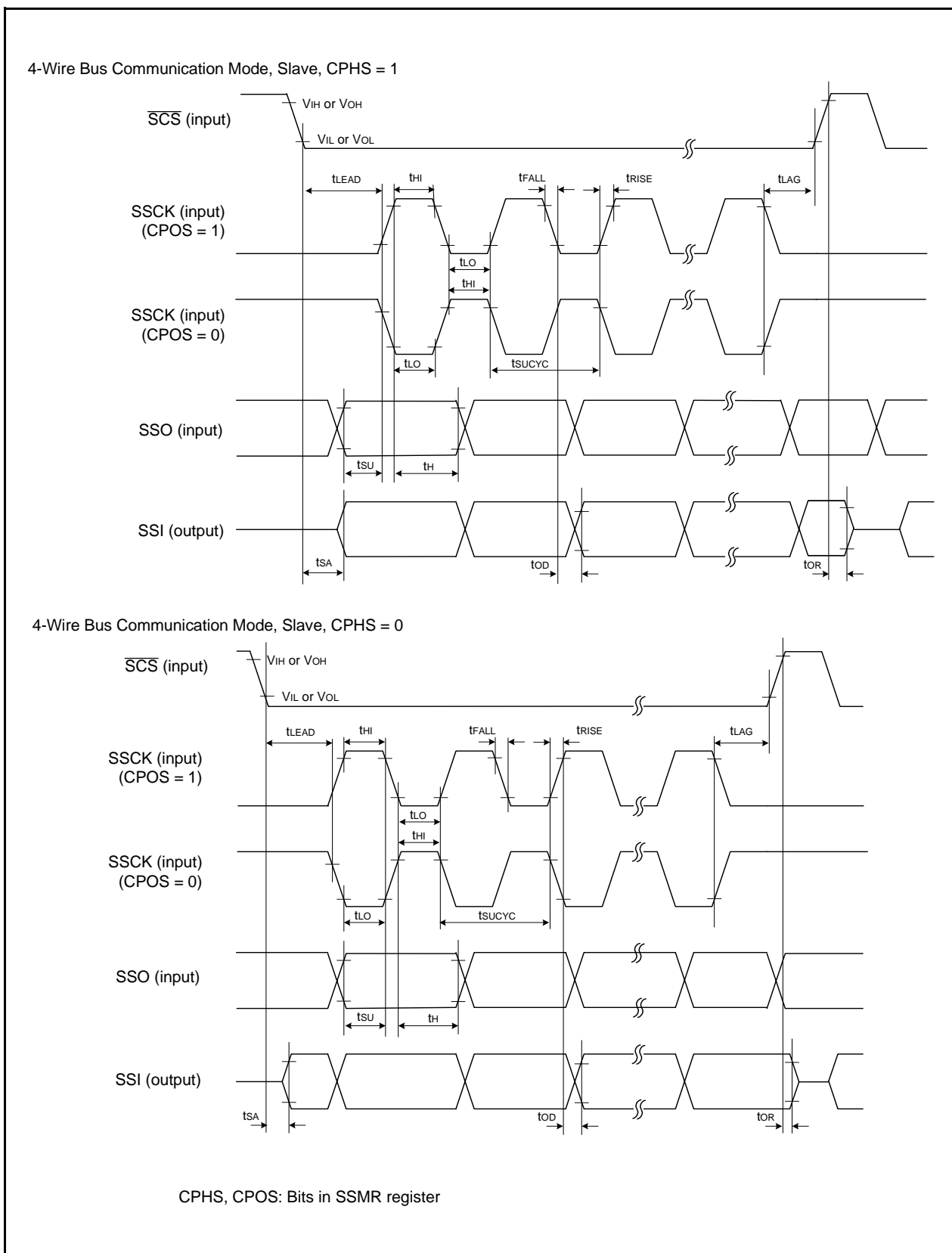


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

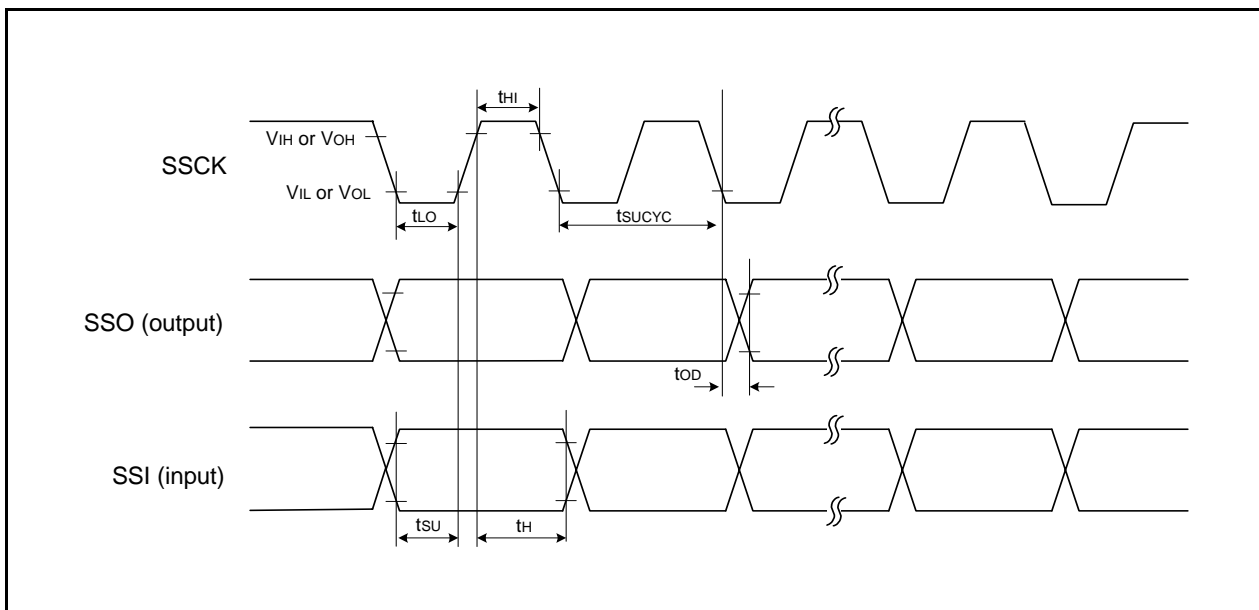


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.16 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tcyc + 600 (2)	–	–	ns
tSCLH	SCL input “H” width		3tcyc + 300 (2)	–	–	ns
tSCLL	SCL input “L” width		5tcyc + 500 (2)	–	–	ns
tsf	SCL, SDA input fall time		–	–	300	ns
tSP	SCL, SDA input spike pulse rejection time		–	–	1tcyc (2)	ns
tBUF	SDA input bus-free time		5tcyc (2)	–	–	ns
tSTAH	Start condition input hold time		3tcyc (2)	–	–	ns
tSTAS	Retransmit start condition input setup time		3tcyc (2)	–	–	ns
tSTOP	Stop condition input setup time		3tcyc (2)	–	–	ns
tSDAS	Data input setup time		1tcyc + 40 (2)	–	–	ns
tSDAH	Data input hold time		10	–	–	ns

Notes:

1. VCC = 1.8 to 5.5 V, VSS = 0 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

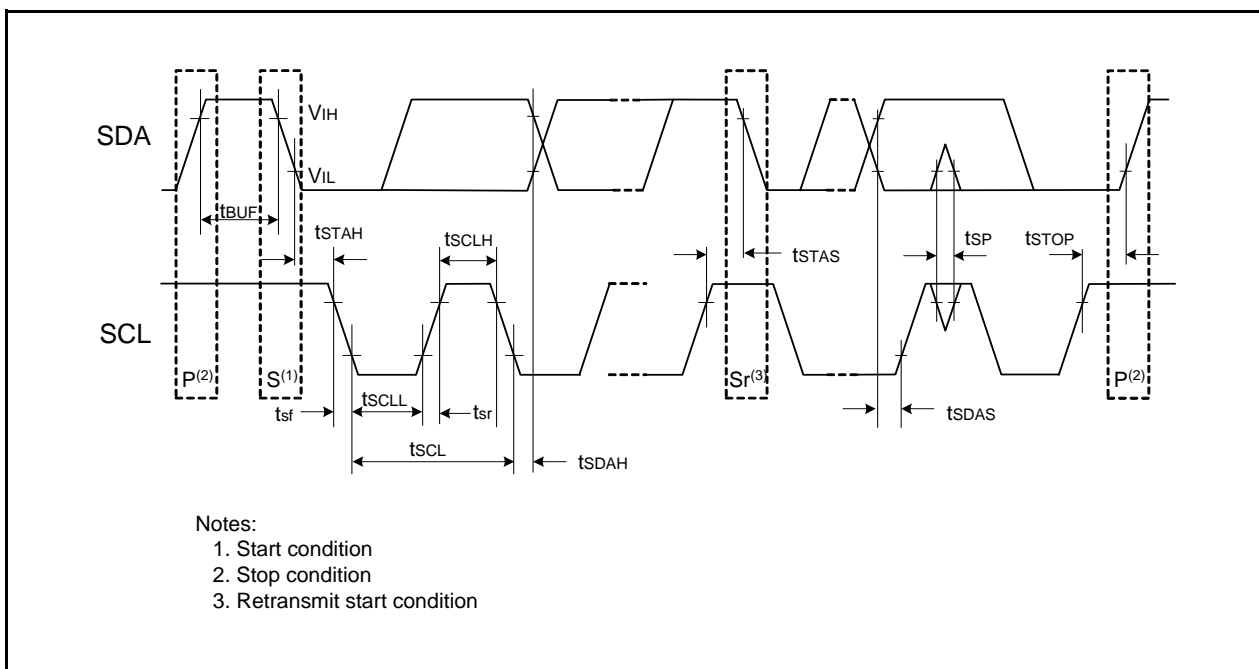


Figure 5.7 I/O Timing of I²C bus Interface

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage		Drive capacity High Vcc = 5.0V	IOH = -20 mA	Vcc - 2.0	-	Vcc	V
			Drive capacity Low Vcc = 5.0V	IOH = -5 mA	Vcc - 2.0	-	Vcc	V
VOL	Output "L" voltage		Drive capacity High Vcc = 5.0V	IOl = 20 mA	-	-	2.0	V
			Drive capacity Low Vcc = 5.0V	IOl = 5 mA	-	-	2.0	V
VT+ - VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOc, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	-	V
		RESET			0.1	1.2	-	V
IiH	Input "H" current		VI = 5 V, Vcc = 5.0 V		-	-	5.0	μA
IiL	Input "L" current		VI = 0 V, Vcc = 5.0 V		-	-	-5.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5.0 V		25	50	100	kΩ
RfXIN	Feedback resistance	XIN			-	0.3	-	MΩ
RfXCIN	Feedback resistance	XCIN			-	8	-	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	-	-	V

Note:

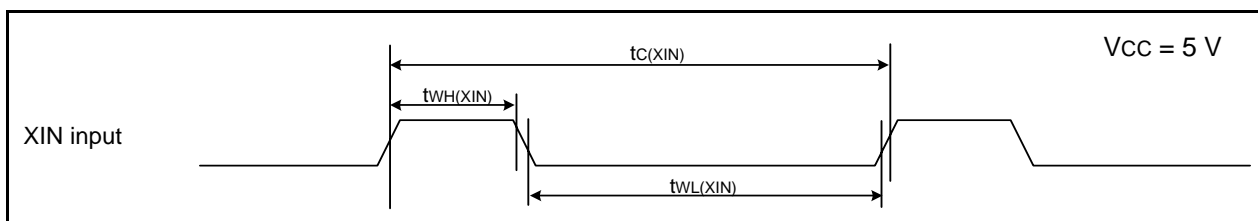
1. 4.2 V ≤ Vcc ≤ 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.18 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz No division	–	6.5	15	mA
			XIN = 16 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz No division	–	5.3	12.5	mA
			XIN = 10 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			Low-speed on-chip oscillator mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400
		Low-speed clock mode	XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	85	400	μA
			XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	47	–	μA
			Wait mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	100
		Wait mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	90	μA
			XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
			Stop mode	XIN clock off, Topr = 25°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0
		Stop mode	XIN clock off, Topr = 85°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^\circ\text{C}$)****Table 5.19 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	24	–	ns
$t_{WL(XIN)}$	XIN input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	μs

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

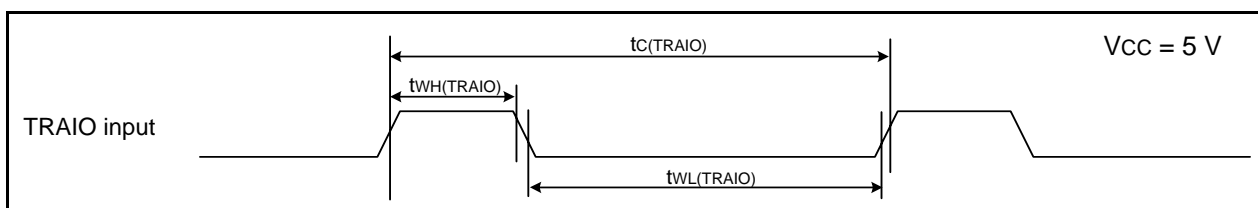
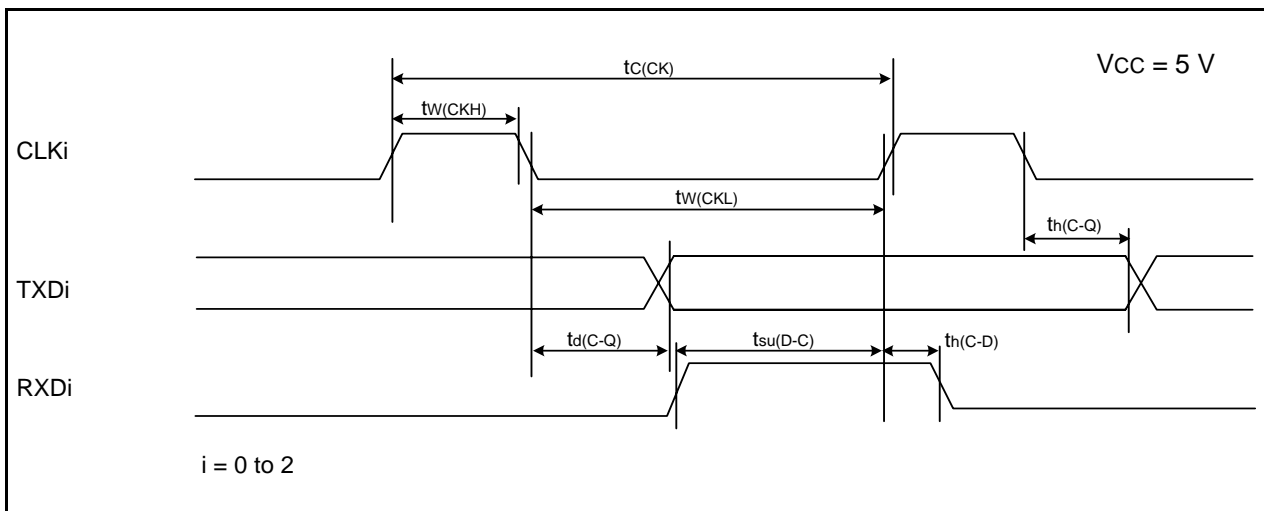
**Figure 5.9 TRAIO Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.21 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{w(CKH)}$	CLKi input “H” width	100	–	ns
$t_{w(CKL)}$	CLKi input “L” width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

**Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V****Table 5.22 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input “H” width, \overline{Kli} input “H” width	250 (1)	–	ns
$t_{w(INL)}$	\overline{INTi} input “L” width, \overline{Kli} input “L” width	250 (2)	–	ns

Notes:

- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

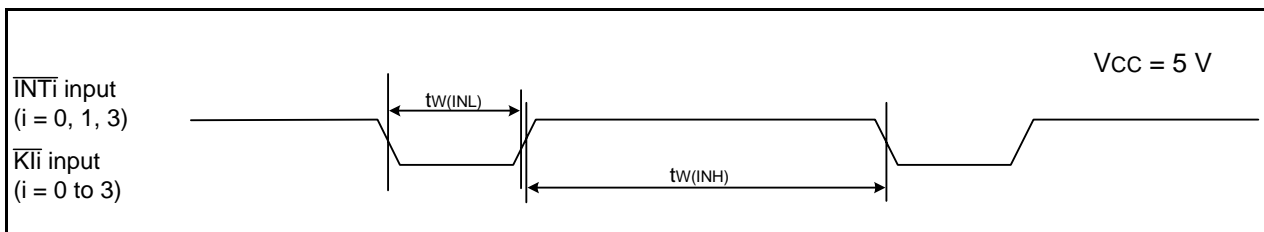
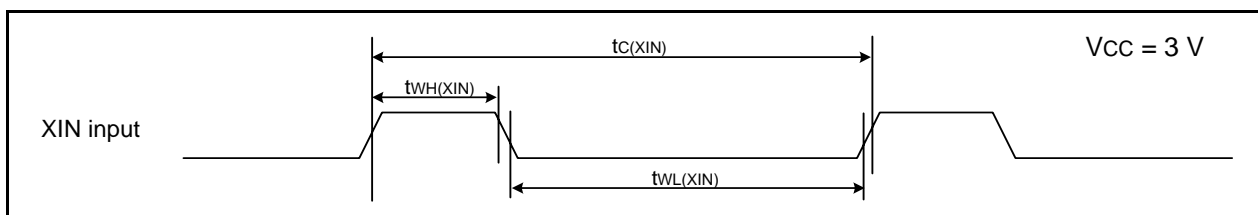
**Figure 5.11 Input Timing for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 5 V**

Table 5.24 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		Low-speed on-chip oscillator mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390	μA
		Low-speed clock mode	XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	400	μA
			XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
			Wait mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90
		XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1		–	4	80	μA
		XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1		–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	μA
			XIN clock off, Topr = 85°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{op} = 25^{\circ}\text{C}$)****Table 5.25 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	24	–	ns
$t_{WL(XIN)}$	XIN input "L" width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs

**Figure 5.12 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.26 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	120	–	ns

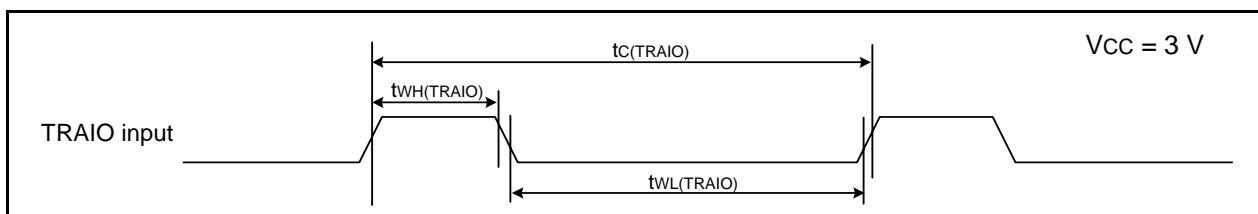
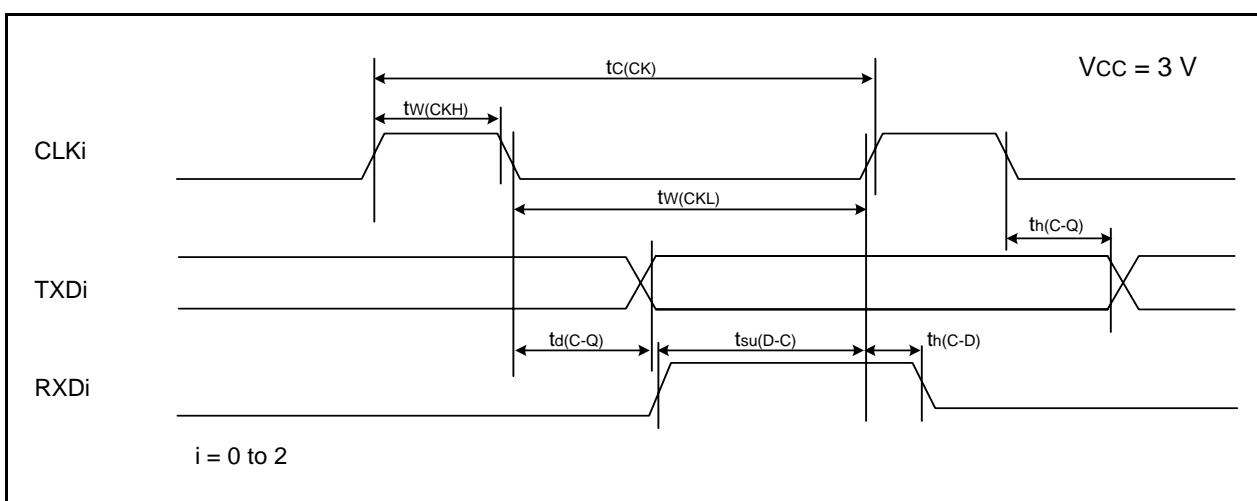
**Figure 5.13 TRAIO Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.27 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{w(CKH)}$	CLKi input “H” width	150	–	ns
$t_{w(CKL)}$	CLKi Input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 to 2

**Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.28 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input “H” width, \overline{Kli} input “H” width	380 (1)	–	ns
$t_{w(INL)}$	\overline{INTi} input “L” width, \overline{Kli} input “L” width	380 (2)	–	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

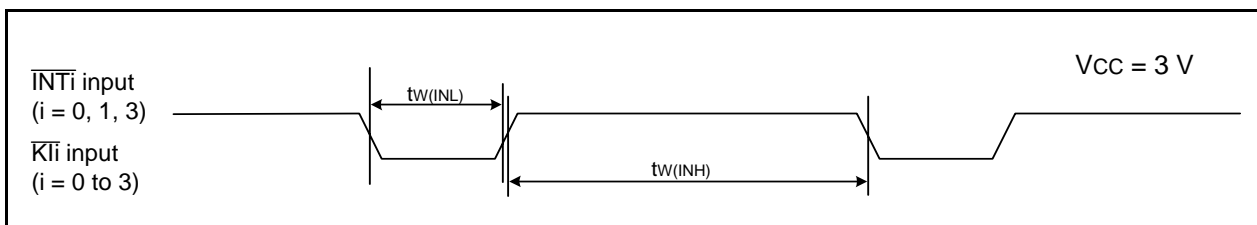
**Figure 5.15 Input Timing for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 3 V**

Table 5.29 Electrical Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" voltage		Drive capacity High	IOH = -2 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity Low	IOH = -1 mA	Vcc - 0.5	-	Vcc	V
VOL	Output "L" voltage		Drive capacity High	IOL = 2 mA	-	-	0.5	V
			Drive capacity Low	IOL = 1 mA	-	-	0.5	V
VT+ - VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, ADTRG, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.20	-	V
		RESET			0.05	0.2	-	V
IiH	Input "H" current		VI = 2.2 V, Vcc = 2.2 V		-	-	4.0	μA
IiL	Input "L" current		VI = 0 V, Vcc = 2.2 V		-	-	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 2.2 V		70	140	300	kΩ
RfXIN	Feedback resistance	XIN			-	0.3	-	MΩ
RfXCIN	Feedback resistance	XCIN			-	8	-	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	-	-	V

Note:

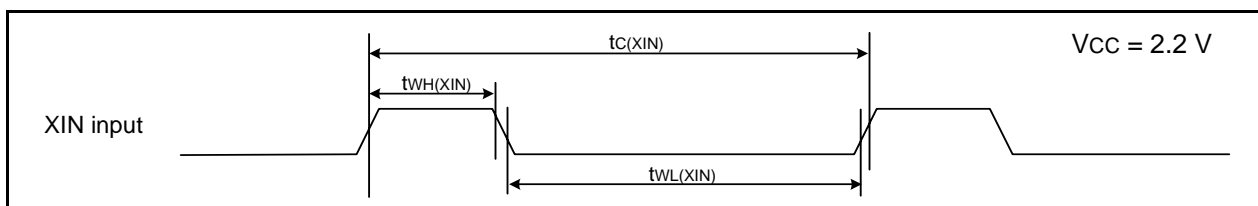
- 1.8 V ≤ Vcc < 2.7 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.30 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Typ.	Max.		
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz No division	–	2.2	–	mA
			XIN = 5 MHz (square wave) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	0.8	–	mA
		Low-speed on-chip oscillator mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	300	μA
		Low-speed clock mode	XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	350	μA
			XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	μA
		Wait mode	XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	μA
			XIN clock off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	μA
			XIN clock off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	μA
		Stop mode	XIN clock off, Topr = 25°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5	μA
			XIN clock off, Topr = 85°C Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$)****Table 5.31 XIN Input, XCIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	–	ns
$t_{WH(XIN)}$	XIN input "H" width	90	–	ns
$t_{WL(XIN)}$	XIN input "L" width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs

**Figure 5.16 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.32 TRAIO Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	–	ns

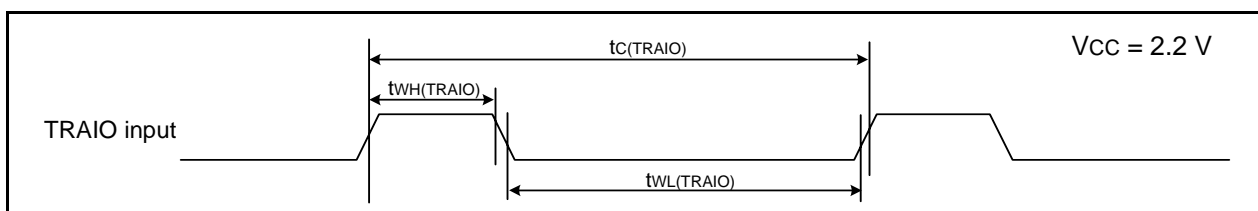
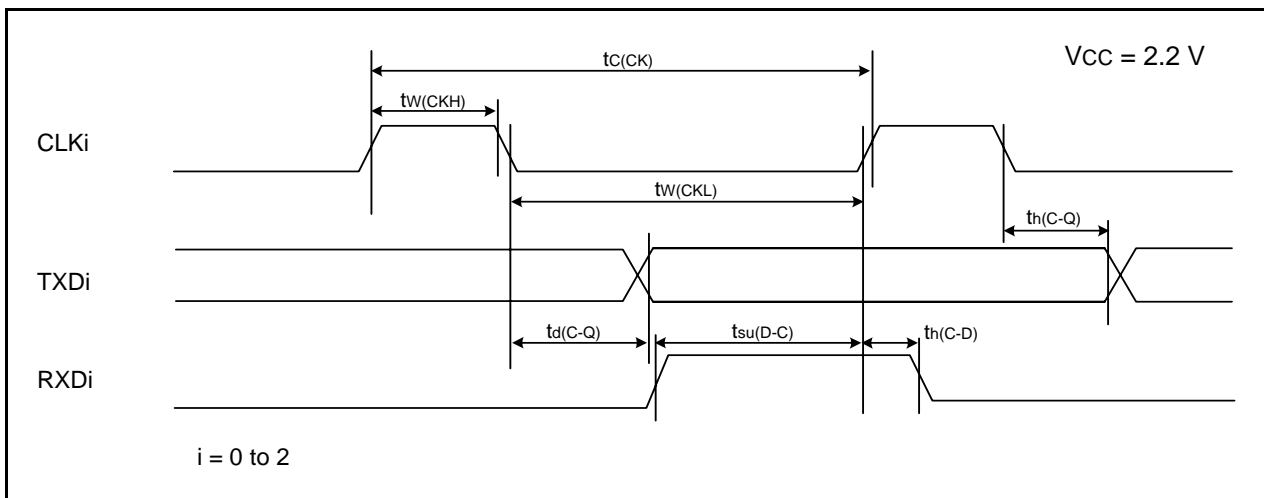
**Figure 5.17 TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.33 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	–	ns
$t_{w(CKH)}$	CLKi input “H” width	400	–	ns
$t_{w(CKL)}$	CLKi input “L” width	400	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	150	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

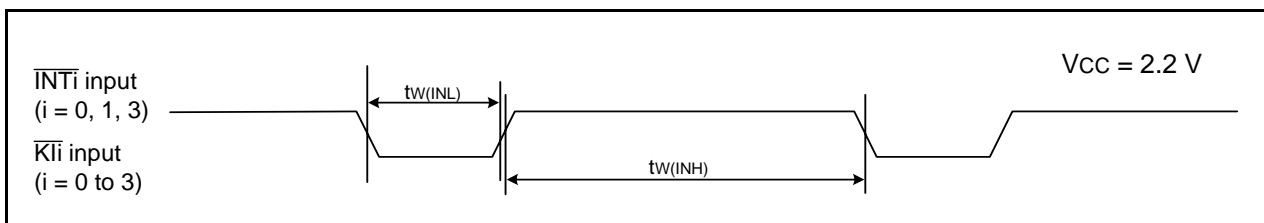
i = 0 to 2

**Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V****Table 5.34 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 3)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	\overline{INTi} input “H” width, \overline{Kli} input “H” width	1000 (1)	–	ns
$t_{w(INL)}$	\overline{INTi} input “L” width, \overline{Kli} input “L” width	1000 (2)	–	ns

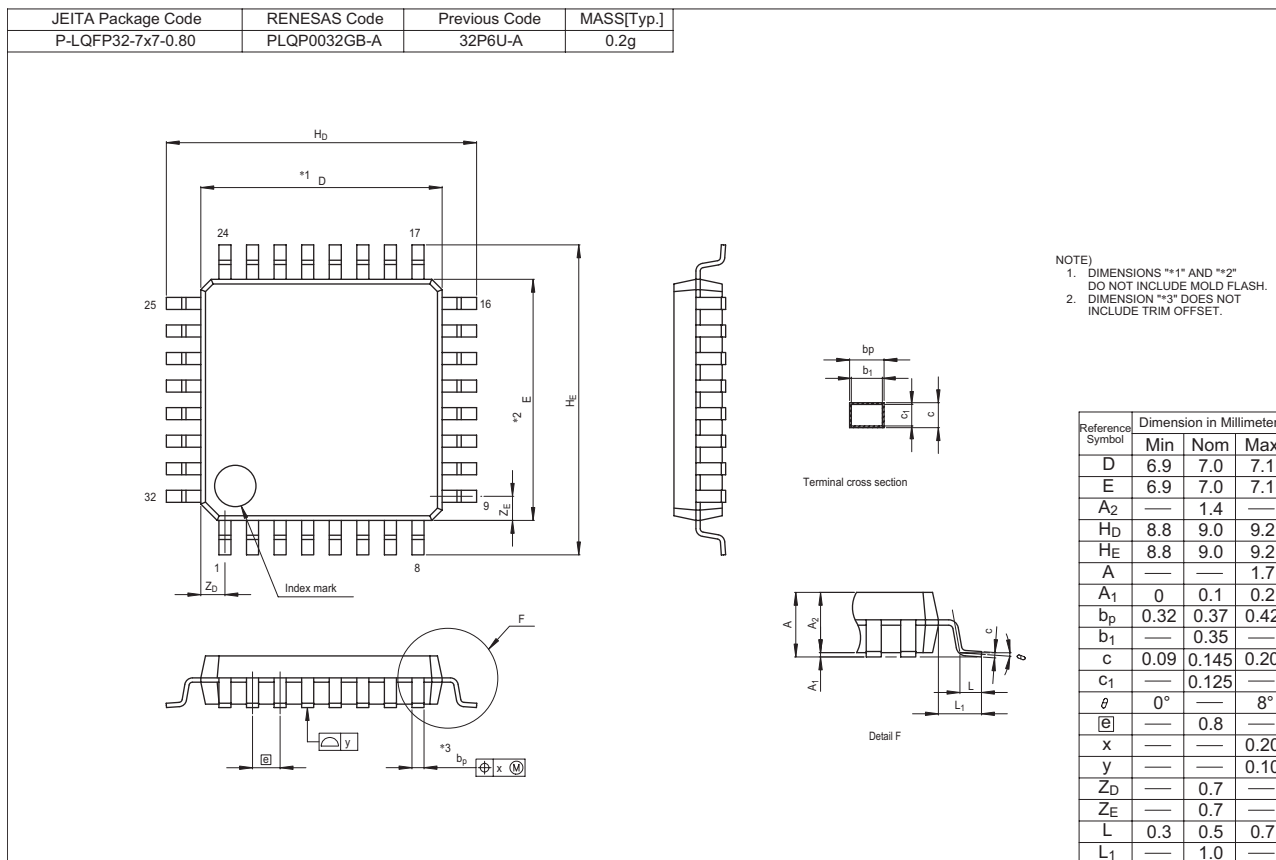
Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

**Figure 5.19 Input Timing for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when Vcc = 2.2 V**

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.



REVISION HISTORY	R8C/33A Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Oct 26, 2007	–	First Edition issued
0.02	Feb 05, 2008	2	Table 1.1 Interrupts: Specification “• Number of interrupt vectors: 44” → “• Number of interrupt vectors: 69”
		3	Table 1.2 Serial Interface: Specification revised, Note1 deleted
		6	Figure 1.3 revised
		7	Table 1.4 revised
		8	Table 1.5 XIN clock input, XIN clock output: revised Note2 added
		13	Figure 3.1 “Expanded area” deleted, Note1 revised
0.10	Mar 17, 2008	7	Table 1.4 I/O Pin Functions for Peripheral Modules: “Voltage Detection Circuit” added
		9	Table 1.6 Voltage Detection Circuit added
		13	Figure 3.1 revised
		15	Table 4.2 revised
		16	Table 4.3 008Ch: deleted
		20	Table 4.7 0186h, 018Fh: deleted
		26	5. Electrical Characteristics added
0.20	Dec 05, 2008	1	1.1 “These MCUs also use an are designed to withstand EMI.” → “These MCUs are designed to maximize EMI/EMS performance.”
		2	Table 1.1 revised
		3	Table 1.2 revised
		4	Figure 1.1 revised
		5	Figure 1.2 revised
		14	Table 4.1 “0XXX00XXb” → “0XXXXXXXXb” Note2 revised
		20	Table 4.7 019Ah “00010000b /” added
		26, 27, 29 to 35, 37 to 42, 45 to 47, 49, 50	Table 5.1 to Table 5.13, Table 5.15, Table 5.17 to Table 5.19, Table 5.24 to Table 5.26, Table 5.30, Table 5.31 revised Figure 5.3 to Figure 5.6 revised
		43, 47, 51	Timing Requirements “[VCC = 5 V]”, “[VCC = 3 V]”, “[VCC = 2.2 V]” deleted
		1.00	Sep 10, 2009
4	Table 1.3 revised		
8	Table 1.5 Note 2 deleted		
17	Table 4.4 AD0 “XXh” → “XXh”		
25	Table 4.12 revised, Table 4.13 added		
27	Table 5.2 revised, Note 3 deleted		

REVISION HISTORY	R8C/33A Group Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 10, 2009	31, 32	Table 5.7, Table 5.8 revised
		33	Table 5.9, Table 5.10 revised
		34	Table 5.11, Table 5.12 revised
		35	Old Table 5.13 deleted
		41, 45, 49	Table 5.17, Table 5.23, Table 5.29 revised
		42, 46, 50	Table 5.18, Table 5.24, Table 5.30 revised
		44, 48, 52	Table 5.22, Table 5.28, Table 5.34 $\overline{INT0} \rightarrow \overline{INTi}$

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510