

# UT54ACS374/UT54ACTS374

## Radiation-Hardened

## Octal D-Type Flip-Flops with Three-State Outputs

### FEATURES

- 8 latches in a single package
- Three-state bus-driving true outputs
- Full parallel access for loading
- 1.2 $\mu$  radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack

### DESCRIPTION

The UT54ACS374 and the UT54ACTS374 are non-inverting octal D type flip-flops with three-state outputs designed for driving highly capacitive or relatively low-impedance loads. The device is suitable for buffer registers, I/O ports, and bidirectional bus drivers.

The eight flip-flops are edge triggered D-type flip-flops. On the positive transition of the clock the Q outputs will follow the data (D) inputs.

An output-control input ( $\overline{OC}$ ) places the eight outputs in either a normal logic state (high or low logic level) or a high-impedance state. The high-impedance third state and increased drive provide the capability to drive the bus line in a bus-organized system without the need for interface or pull-up components.

The output control  $\overline{OC}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

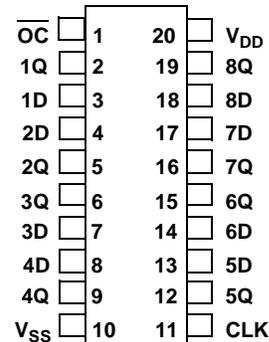
The devices are characterized over full military temperature range of -55°C to +125°C.

### FUNCTION TABLE

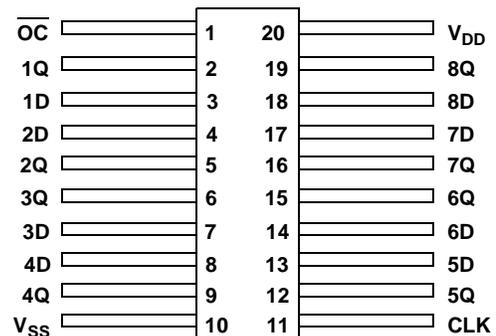
| INPUTS          |            |    | OUTPUT          |
|-----------------|------------|----|-----------------|
| $\overline{OC}$ | CLK        | nD | nQ              |
| L               | $\uparrow$ | H  | H               |
| L               | $\uparrow$ | L  | L               |
| L               | L          | X  | nQ <sub>0</sub> |
| H               | X          | X  | Z               |

### PINOUTS

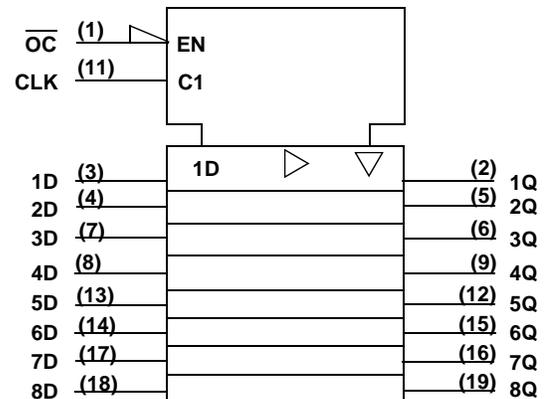
#### 20-Pin DIP Top View



#### 20-Lead Flatpack Top View



### LOGIC SYMBOL



#### Note:

1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



**RECOMMENDED OPERATING CONDITIONS**

| <b>SYMBOL</b> | <b>PARAMETER</b>      | <b>LIMIT</b>  | <b>UNITS</b> |
|---------------|-----------------------|---------------|--------------|
| $V_{DD}$      | Supply voltage        | 4.5 to 5.5    | V            |
| $V_{IN}$      | Input voltage any pin | 0 to $V_{DD}$ | V            |
| $T_C$         | Temperature range     | -55 to + 125  | °C           |

**DC ELECTRICAL CHARACTERISTICS <sup>7</sup>**(V<sub>DD</sub> = 5.0V ±10%; V<sub>SS</sub> = 0V <sup>6</sup>, -55 °C < T<sub>C</sub> < +125°C)

| SYMBOL             | PARAMETER                                               | CONDITION                                                                                                                                                                  | MIN                                         | MAX                      | UNIT       |
|--------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|--------------------------|------------|
| V <sub>IL</sub>    | Low-level input voltage <sup>1</sup><br>ACTS<br>ACS     |                                                                                                                                                                            |                                             | 0.8<br>.3V <sub>DD</sub> | V          |
| V <sub>IH</sub>    | High-level input voltage <sup>1</sup><br>ACTS<br>ACS    |                                                                                                                                                                            | .5V <sub>DD</sub><br>.7V <sub>DD</sub>      |                          | V          |
| I <sub>IN</sub>    | Input leakage current<br>ACTS/ACS                       | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>                                                                                                                       | -1                                          | 1                        | μA         |
| V <sub>OL</sub>    | Low-level output voltage <sup>3</sup><br>ACTS<br>ACS    | I <sub>OL</sub> = 8.0mA<br>I <sub>OL</sub> = 100μA                                                                                                                         |                                             | 0.40<br>0.25             | V          |
| V <sub>OH</sub>    | High-level output voltage <sup>3</sup><br>ACTS<br>ACS   | I <sub>OH</sub> = -8.0mA<br>I <sub>OH</sub> = -100μA                                                                                                                       | .7V <sub>DD</sub><br>V <sub>DD</sub> - 0.25 |                          | V          |
| I <sub>OZ</sub>    | Three-state output leakage current                      | V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>                                                                                                                       | -20                                         | 20                       | μA         |
| I <sub>OS</sub>    | Short-circuit output current <sup>2,4</sup><br>ACTS/ACS | V <sub>O</sub> = V <sub>DD</sub> and V <sub>SS</sub>                                                                                                                       | -200                                        | 200                      | mA         |
| I <sub>OL</sub>    | Output current <sup>10</sup><br>(Sink)                  | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub><br>V <sub>OL</sub> = 0.4V                                                                                             | 8                                           |                          | mA         |
| I <sub>OH</sub>    | Output current <sup>10</sup><br>(Source)                | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub><br>V <sub>OH</sub> = V <sub>DD</sub> - 0.4V                                                                           | -8                                          |                          | mA         |
| P <sub>total</sub> | Power dissipation <sup>2, 8, 9</sup>                    | C <sub>L</sub> = 50pF                                                                                                                                                      |                                             | 1.9                      | mW/<br>MHz |
| I <sub>DDQ</sub>   | Quiescent Supply Current                                | V <sub>DD</sub> = 5.5V                                                                                                                                                     |                                             | 10                       | μA         |
| ΔI <sub>DDQ</sub>  | Quiescent Supply Current Delta<br>ACTS                  | For input under test<br>V <sub>IN</sub> = V <sub>DD</sub> - 2.1V<br>For all other inputs<br>V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub><br>V <sub>DD</sub> = 5.5V |                                             | 1.6                      | mA         |
| C <sub>IN</sub>    | Input capacitance <sup>5</sup>                          | f = 1MHz @ 0V                                                                                                                                                              |                                             | 15                       | pF         |
| C <sub>OUT</sub>   | Output capacitance <sup>5</sup>                         | f = 1MHz @ 0V                                                                                                                                                              |                                             | 15                       | pF         |

## UT54ACS374/UT54ACTS374

### Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.