Synchronous DRAM Module 256Mbyte (32Mx72bit), DIMM with ECC based on 16Mx8, 4Banks, 4K Ref., 3.3V Part No. HSD32M72D18R

GENERAL DESCRIPTION

The HSD32M72D18R is a 32M x 72 bit Synchronous Dynamic RAM high-density memory module. The module consists of eighteen CMOS 16M x 8 bit with 4banks Synchronous DRAMs in TSOP-II 400mil packages and 2K EEPROM in 8-pin TSSOP package on a 168-pin glass-epoxy. One 0.22uF and two 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The HSD32M72D18AR is a DIMM (Dual in line Memory Module) and is intended for mounting into 168-pin edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications All module components may be powered from a single 3.3V DC power supply and all inputs and outputs are LVTTL-compatible.

FEATURES

• Part Identification
  HSD32M72D18R : 100MHz (CL=2, CL=3)
  HSD32M72D18R : 133MHz (CL=3)
• Burst mode operation
• Auto & self refresh capability (4096 Cycles/64ms)
• LVTTL compatible inputs and outputs
• Single 3.3V ±0.3V power supply

• MRS cycle with address key programs
  - Latency (Access from column address)
  - Burst length (1, 2, 4, 8 & Full page)
  - Data scramble (Sequential & Interleave)

• All inputs are sampled at the positive going edge of the system clock
• The used device is 4M x 8bit x 4Banks SDRAM

PIN ASSIGNMENT

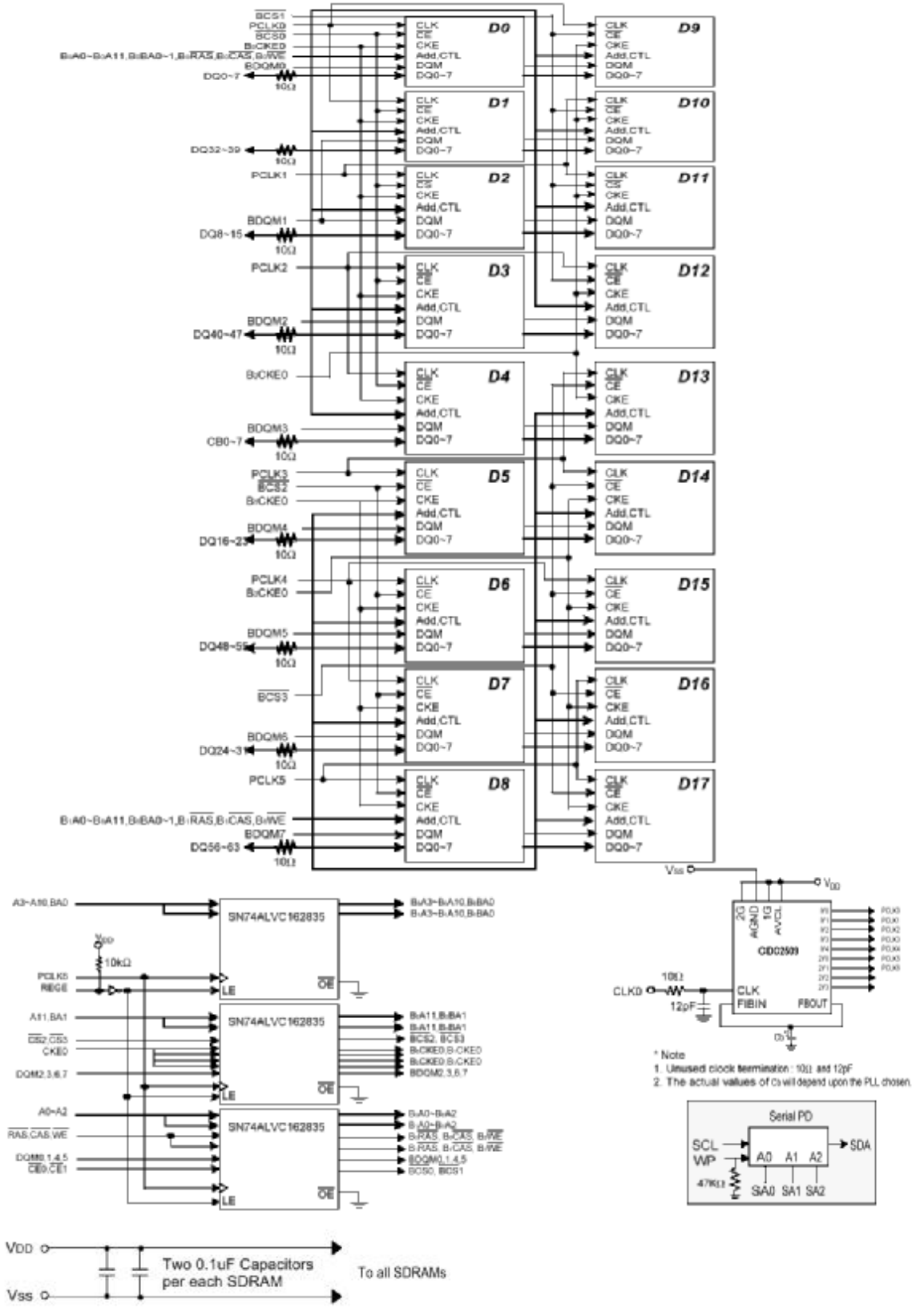
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	/CE0	58	DQ19	86	DQ32	114	/CE1	142	DQ51
3	DQ1	31	NC	59	Vcc	87	DQ33	115	/RAS	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	NC	90	Vcc	118	A3	146	NC
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	NC	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	/CE2	73	Vcc	101	DQ45	129	/CE3	157	Vcc
18	Vcc	46	DQM2	74	DQ28	102	Vcc	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	NC	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CLK2	107	Vss	135	NC	163	CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	/WE	55	DQ16	83	SCL	111	/CAS	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	Vcc	112	DQM4	140	DQ49	168	Vcc

* These pins are not used in this module ** These pins should be NC in the system which does not support SPD

*Pin Names

A0~A11: Address input (Multiplexed)
BA0~BA1: Select bank
DQ0~DQ63: Data input/output
CB0~7: Check bit (Data-in/data-out)
CLK0: Clock input
CKE0: Clock enable input
/CE0~/CE3: Chip select input
/RAS: Row address strobe
/CAS: Coulmn address strobe
/WE: Write enable
DQM0~7: DQM
V_{CC}: Power supply(3.3V)
V_{SS}: Ground
*V_{REF}:Power supply for reference
REGE: Register enable
SDA: Serial data I/O
SCL: Serial clock
SA0~2: Address in EEPROM
NC: No connection

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	System clock	Active on the positive going edge to sample all inputs.
/CE	Chip enable	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	Clock enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	Address	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	Bank select address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
/RAS	Row address strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column address strobe	Latches column addresses on the positive going edge of the CLK with /CAS low. Enables column access.
/WE	Write enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQM0 ~ 7	Data input/output mask	Makes data output Hi-Z, tsHZ after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. The inputs are strobed in the latch/flip-flop on the riging edge of CLK. REGE is tied to V_{DD} through 10K ohm register on PCB. So if REGE of module is floating, this module will be operated as registerd mode.
DQ0 ~ 63	Data input/output	Data inputs/outputs are multiplexed on the same pins.
CB0~7	Check bit	Check bits for ECC.
WP	Write Protection	WP pin is connected to Vcc. When WP is “high”, EEPROM Programming will be inhibited and the entire memory will be write-protected.
VDD/VSS	Power supply/ground	Power and ground for the input buffers and the core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	V_{IN} ,$_{OUT}$	-1V to 4.6V
Voltage on Vcc Supply Relative to Vss	Vcc	-1V to 4.6V
Power Dissipation	P_D	18W
Storage Temperature	T_{STG}	-55^{o}C to 150^{o}C
Short Circuit Output Current	I_{OS}	50mA

Notes:
Permanent device damage may occur if " Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

(Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C))

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT	NOTE
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Input High Voltage	V_{IH}	2.0	3.0	Vcc+0.3	V	1
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	2
Output High Voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes :
1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE

(Vcc = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input capacitance(A0~A11)	C_{IN1}		19	pF
Input capacitance(/RAS, /CAS,/WE)	C_{IN2}		19	pF
Input capacitance(CKE0)	C_{IN3}		33	pF
Input capacitance(CLK0)	C_{IN4}		12	pF
Input capacitance(/CE0~/CE3)	C_{IN5}		12	pF
Input capacitance(DQM0~DQM7)	C_{IN3}		12	pF
Input capacitance(BA0~BA1)	C_{IN3}		12	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}		19	pF
Data input/output capacitance (CB0 ~ CB7)	C_{OUT1}		19	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	VERSION			UNIT	NOTE
			-1H	-1L	-13		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0mA	1980		2160	mA	1
Precharge standby current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max) t_{CC}=10ns	18			mA	3
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max) t_{CC}=∞	18			mA	3
Precharge standby current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min) /CE ≥ V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	360			mA	3
	$I_{CC2}NS$	CKE ≥ V_{IH}(min) CLK ≤ V_{IL}(max), tcc=∞ Input signals are stable	126				
Active standby current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), tcc=10ns	90			mA	3
	$I_{CC3}PS$	CKE&CLK ≤ V_{IL}(max) tcc=∞	90				
Active standby current in non power-down mode (One bank active)	$I_{CC3}N$	CKE≥V_{IH}(min), /CE≥V_{IH}(min), tcc=10ns Input signals are changed one time during 20ns	540			mA	3
	$I_{CC3}NS$	CKE≥VIH(min) CLK ≤VIL(max), tcc=∞ Input signals are stable	360				
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	2250		2700	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	3780		3960	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	27			mA	3

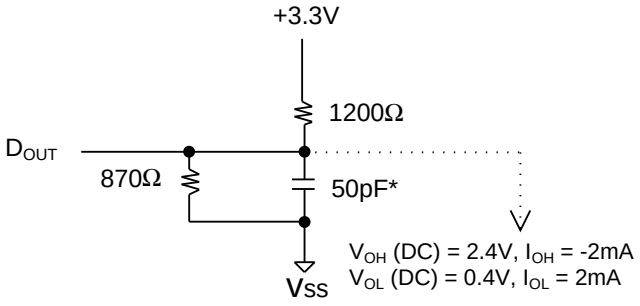
Notes:

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1PLL & 3 Drive Ics.
4. Unless otherwise noticed, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}).

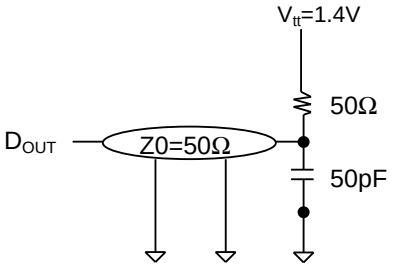
AC OPERATING TEST CONDITIONS

(vcc = 3.3V ± 0.3V, T_A = 0 to 70°C)

PARAMETER	Value	UNIT
AC Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VERSION			UNIT	NOTE
			-1H	-1L	-13		
Row active to row active delay		t_{RRD}(min)	20	20	15	ns	1
/RAS to /CAS delay		t_{RCD}(min)	20	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	20	ns	1
Row active time		t_{RAS}(min)	50	50	45	ns	1
		t_{RAS}(max)	100			ns	
Row cycle time		t_{RC}(min)	70	70	65	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2,5
Last data in to Active delay		t_{DAL}(min)	2 CLK + 20 ns			-	5
Last data in to new col. address delay		t_{CDL}(min)	1			CLK	2
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		1		-		

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
.5. For -1H/1L, tRDL=1CLK and tDAL=1CLK+20ns is also supported .
(recommend : tRDL=2CLK and tDAL=2CLK + 20ns.)

AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	-1H		-1L		-13		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency=3	t_{CC}	10	1000	10	1000	7.5	1000	ns	1
	CAS latency=2		10		12		-			
CLK to valid output delay	CAS latency=3	t_{SAC}	6	6				5.4	ns	1,2
	CAS latency=2		6	7				-		
``Output data hold time	CAS latency=3	t_{OH}	3		3		2.7		ns	1,2
	CAS latency=2		3		3		-			
CLK high pulse width		t_{CH}	3			3	2.5		ns	3
CLK low pulse width		t_{CL}	3			3	2.5		ns	3
Input setup time		t_{SS}	2			2	1.5		ns	3
Input hold time		t_{SH}	1			1	0.8		ns	3
CLK to output in Low-Z		t_{SLZ}	1			1	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		6		6		5.4	ns	1
	CAS latency=2			6		7		-	ns	1

Notes :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

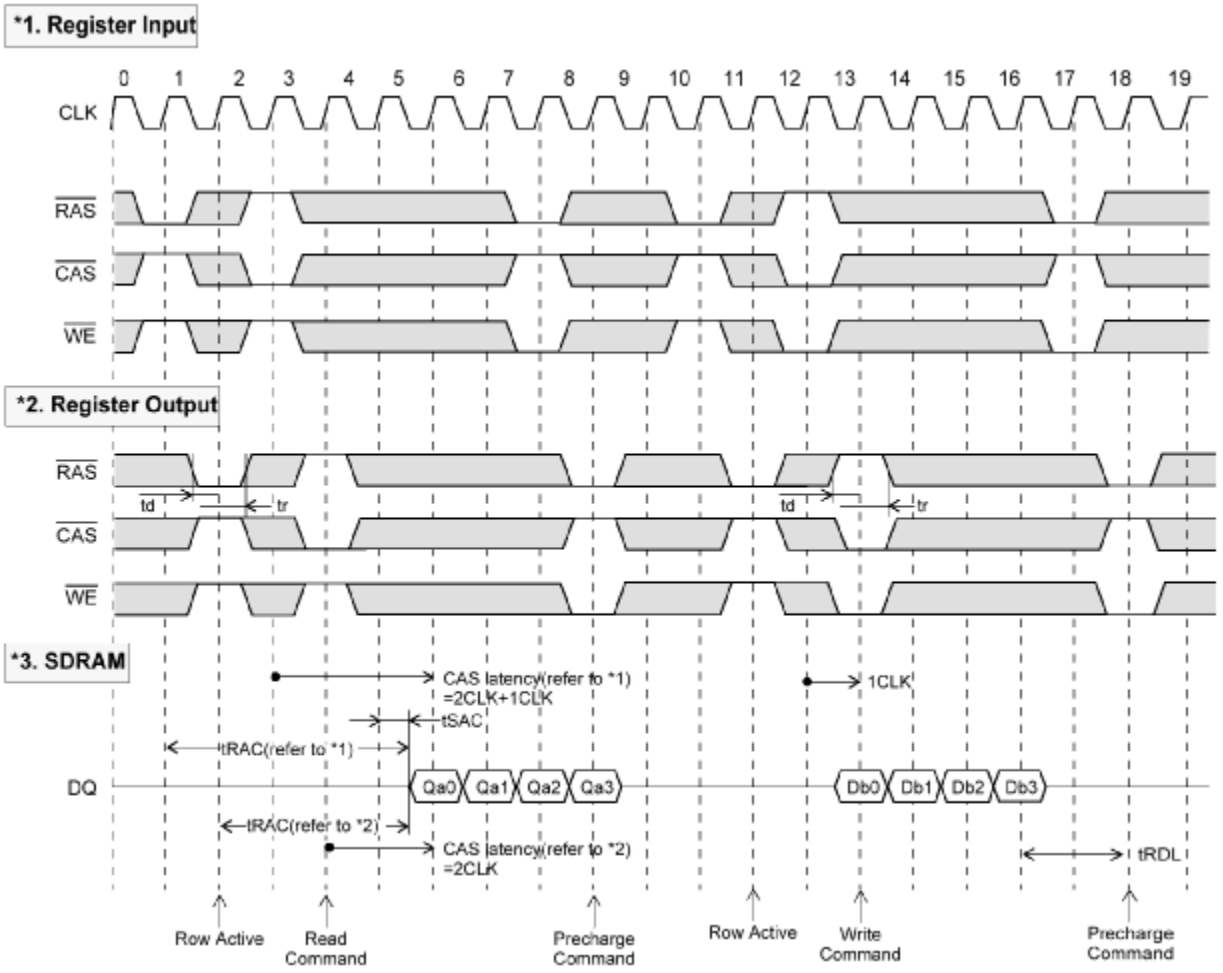
COMMAND			CKE n-1	CKE n	/CE	/RAS	/CAS	/WE	DQM	BA 0,1	A10/AP	A11 A9~A0	NOTE
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge eable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address (A0 ~ A9)	4
	Auto precharge enable							L			H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :

1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank B is selected.
   If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

TIMING DIAGRAMS



td, tr = Delay of register (74LVC162835)

Notes : 1.In case of module timing, command cycles 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74LVC162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

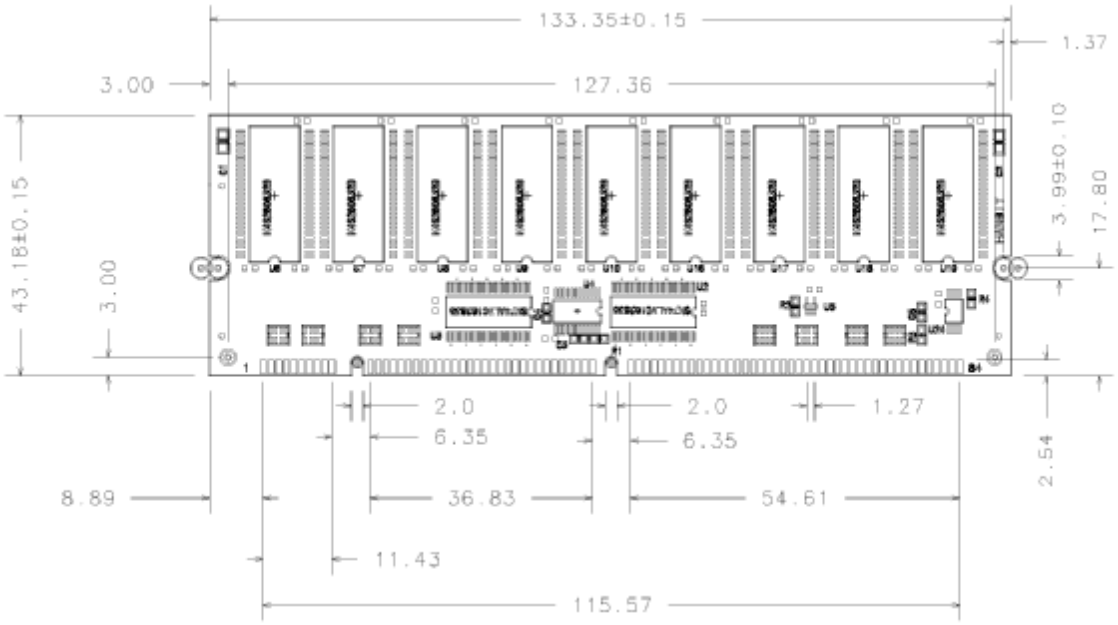
2. D_{IN} is to be issued 1 clock after write command in external timing because D_{IN} is issued directly to module.

PACKAGING INFORMATION

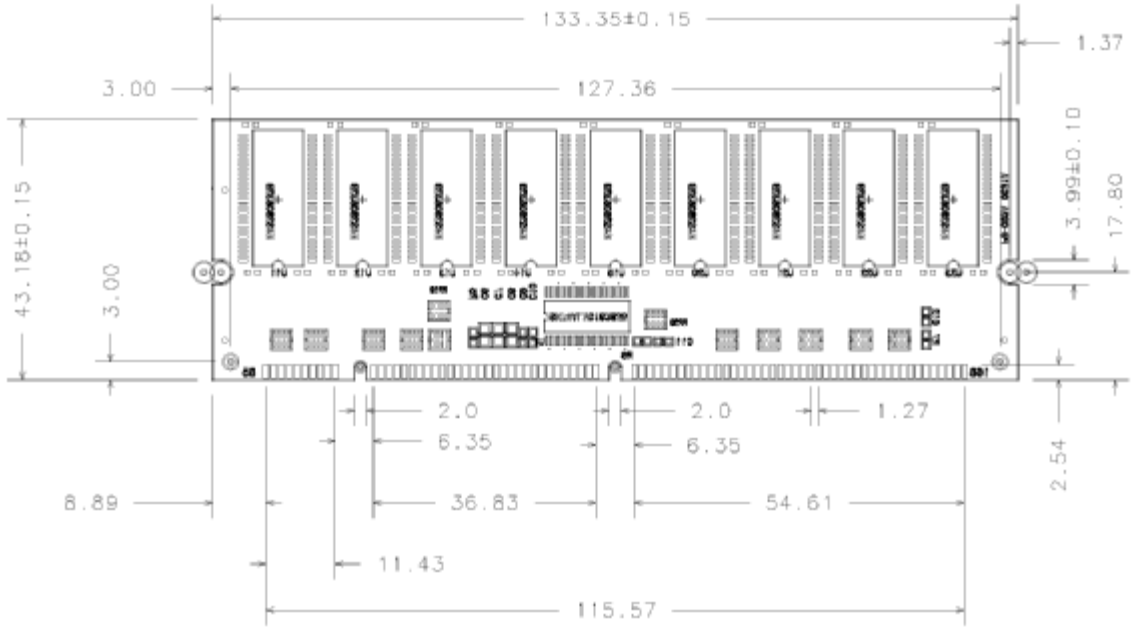
Unit : inch [mm]

Front –Side

TOLERANCE : ±0.008 [±0.20]



Rear-Side



ORDERING INFORMATION

Part Number	Density	Org.	Package	Ref.	Vcc	MODE	MAX.frq
HSD32M72D18R-10L	256MByte	32M x 72	168 Pin-DIMM	4K	3.3V	SDRAM ECC	CL3 100MHz
HSD32M72D18R –10	256MByte	32M x 72	168 Pin-DIMM	4K	3.3V	SDRAM ECC	CL2 100MHz
HSD32M72D18R –12N	256MByte	32M x 72	168 Pin-DIMM	4K	3.3V	SDRAM ECC	CL3 125MHz
HSD32M72D18R –13N	256MByte	32M x 72	168 Pin-DIMM	4K	3.3V	SDRAM ECC	CL3 133MHz