INTEGRATED TECHNOLOGY EXPRESS, INC.

IT7001M/IT7001N

Programmable 8-Bit Binary Counter with Synchronous Preset Enable

Preliminary Specification V0.2

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Revision History

Section	Revision	Page No.
-	• To avoid the custom misunderstanding of CLR and PR signal in the IT7001 specification, CLR and PR signals were replaced by CLR_N and PR_N respectively.	-
-	• Sections 6, 7, 8 in the previous version were removed.	-
-	• The section arrangement was adjusted as follows: Section 9 was changed to section 6. Section 10 was changed to section 7. Section 11 was changed to section 9. Section 12 was changed to section 10.	-
1	• Section 1 Features was revised.	1
7	• Figure 7-1. Timing Diagram When Jn is fixed was revised.	13
8	• Section 8 Electrical Characteristics was revised.	15

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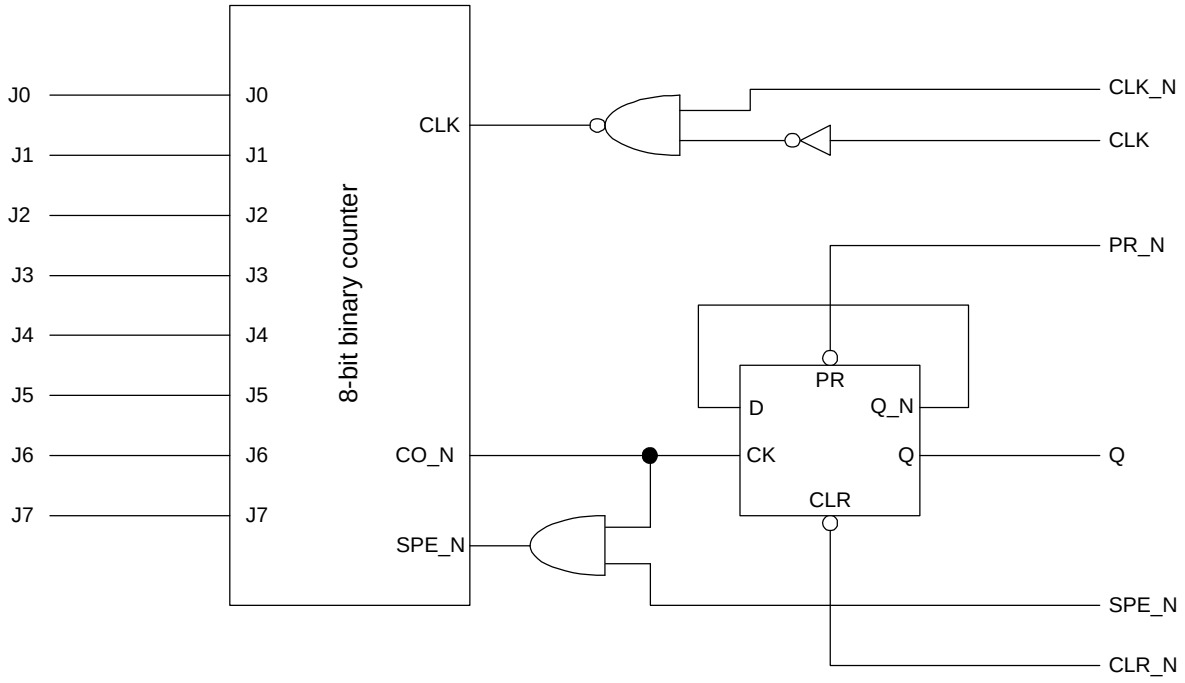
1. Features

- **Wide Operation Voltage**
  - Vcc = 2.5 to 5.5 V
- **Low Static Current (Ta = 25°C)**
  - Icc (Static) = 10 μA (max)
- **Package:**
  - IT7001M: 16-SOP
  - IT7001N: 16-TSSOP

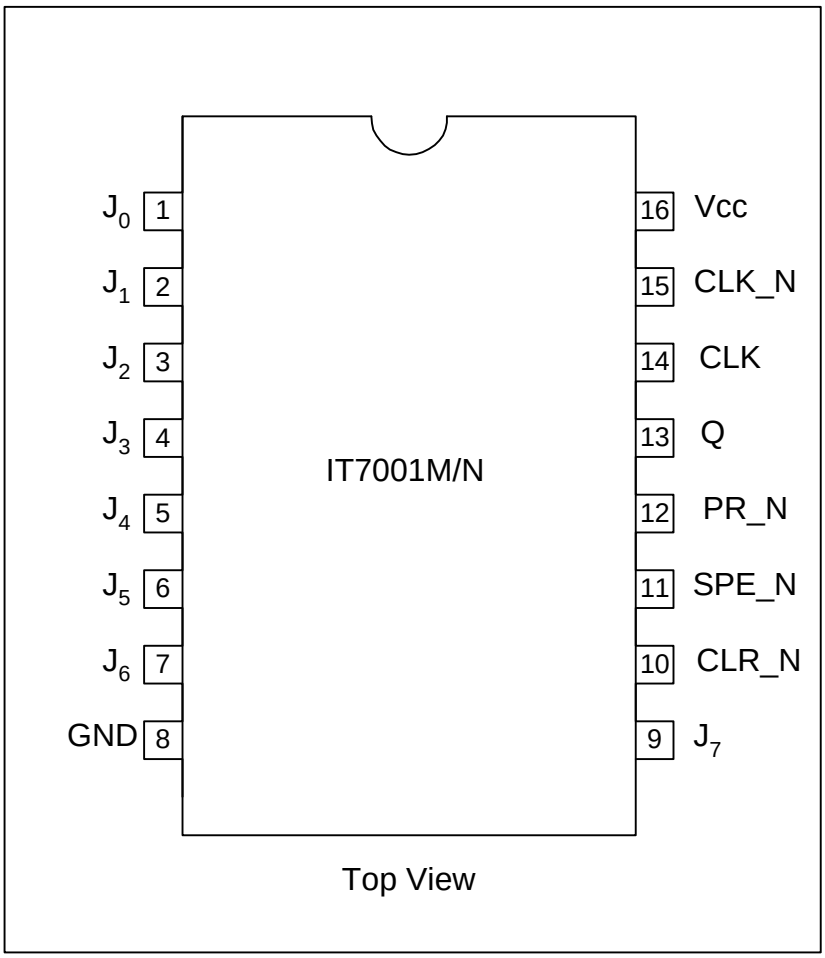
2. General Description

The IT7001M/IT7001N consists of 8-bit binary down counter and D-type Flip Flop. The counter can set up to max 256 counts and synchronous preset (SPE_N) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rising edge. It is applied to generate AC signal for STN-type liquid crystal and divider for general usage.

3. Block Diagram



4. Pin Configuration



5. IT7001M/IT7001N Pin Description

Signal	Pin(s) No.	Attribute	Description
VCC	16	—	Power
GND	8	—	Ground
J0 to J7	1-7,9	I	Count data input for option
CLK, CLK_N	14,15	I	Clock inputs CLK: Rising edge trigger CLK_N: Falling edge trigger
SPE_N	11	I	Preset input for Jn data Please refer to the table below
PR_N	12	I	Preset input for D-type Flip Flop (Initialize "L" at Q output) Please refer to the table below
CLR_N	10	I	Clear input for D-type Flip Flop (Initialize "H" at Q output) Please refer to the table below
Q	13	O	Output for D-type Flip Flop

Table 5-1. Function Table of CLR_N, PR_N and SPE_N Pins

Control Inputs			Mode	Operation Description
CLR_N	PR_N	SPE_N		
H	H	H	Generally count	Down count at the rising edge of clock (CLK) Down count at the falling edge of clock (CLK_N)
X	X	L	Synchronous preset	Jn data is preset at the rise of clock (CLK) , the fall of clock (CLK_N)
L	H	—	Initialize of Q output	Initialize of Q = "L"
H	L	—	Initialize of Q output	Initialize of Q = "H"

H: High level X: Immaterial

L: Low level —: Irrespective of condition

1) Synchronous preset (SPE_N) input can set max 256 down counts.
2) When the count value is 0, the next clock pulse presets the data to invert the output.
3) CLR_N and PR_N inputs initialize the output data.

6. Example of Application Circuit

- **AC Signal Generator for STN-Type Liquid Crystal Panel**

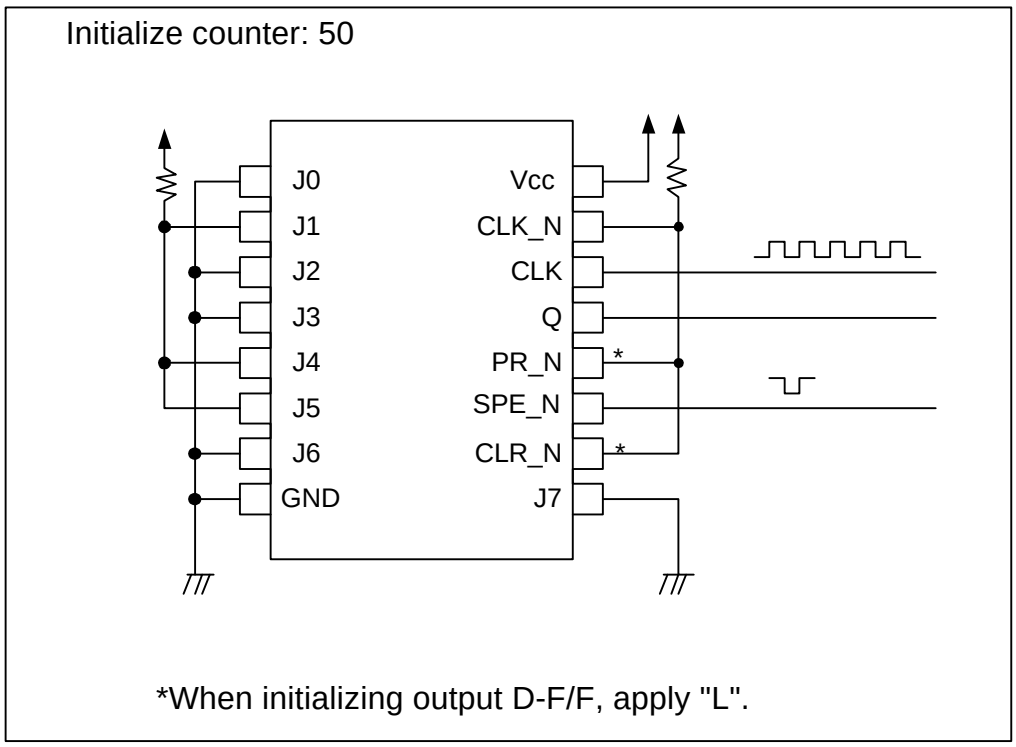


Figure 6-1. Example of Application Circuit

7. Timing Chart: Example of AC Signal Generator

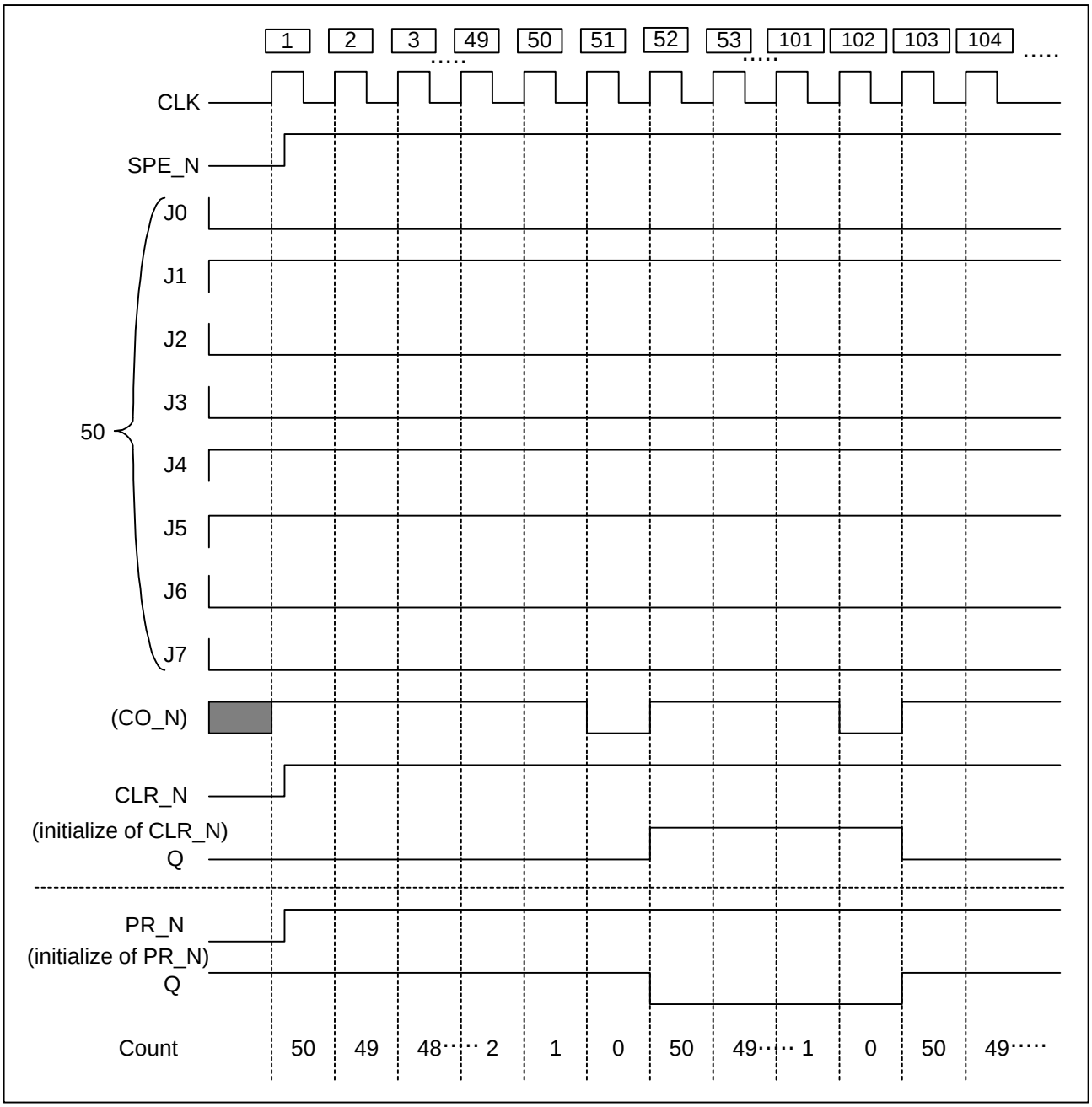


Figure 7-1. Timing Diagram When Jn is fixed

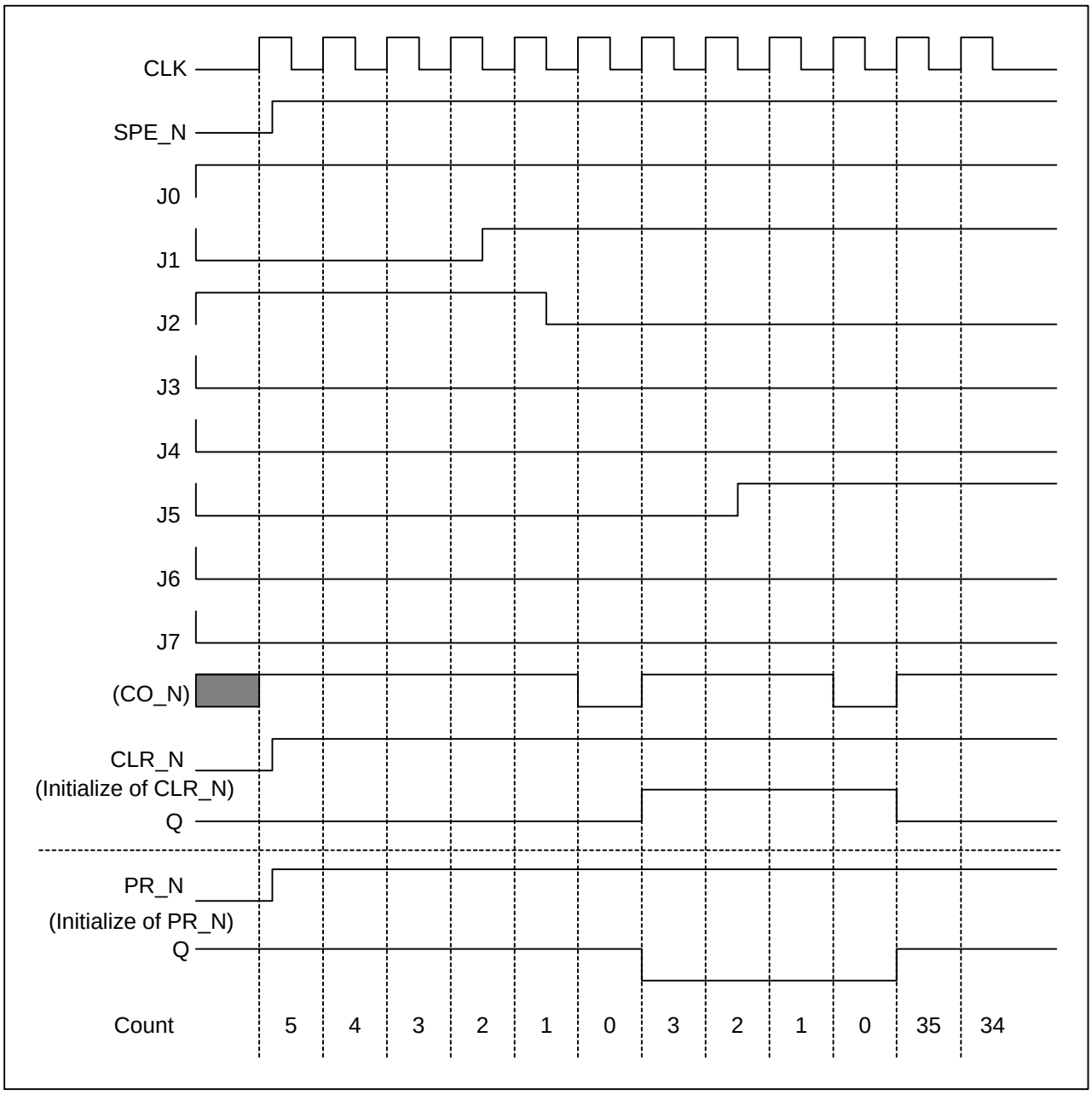


Figure 7-2. Timing Diagram When Jn is changed

8. DC Characteristics

Absolute Maximum Ratings

Power Supply (V_{CC}) ..... -0.3V to 6.0V

input Voltage (V_{IN}) ..... -0.3V to VCC + 0.3V

Output Voltage (V_{OUT}) ..... -0.3V to VCC + 0.3V

Output current / pin (I_{OUT}) 24mA

Storage Temperature (T_{STG}) ..... -40°C to 125°C

***Comments**

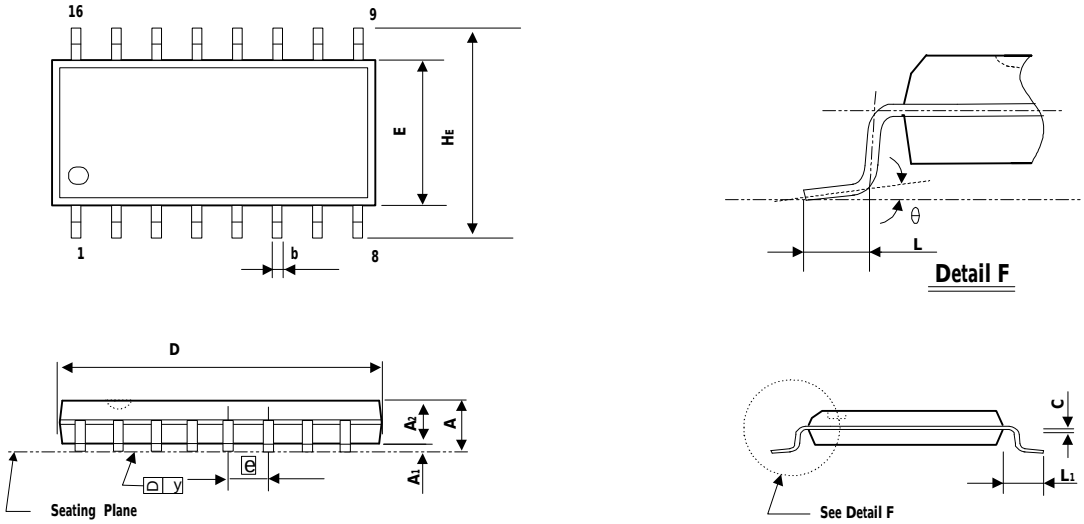
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Operation Condition Vcc=2.5V~5.5V, V_{IN} / V_{OUT}=0~Vcc, Tj=-30°C~85°C) (Note : This item guarantees maximum limit when one input switches.)

Item	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	CMOS	0.7*Vcc	—	—	V
Low Level Input Voltage	V_{IL}	CMOS	—	—	0.3*Vcc	V
High Level Output Voltage	V_{OH}	I_{OH} =-2mA	0.7*Vcc	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} =2mA	—	—	0.3*Vcc	V
Input Leakage Current	I_{IL}	V_{IN} = Vcc or GND	—	—	±1.0	µA
Static Current	I_{CC}	V_{IN} = Vcc or GND	—	—	10	µA
Maximum clock frequency	f_{max}	Vcc = 3.3V	—	20	—	MHz

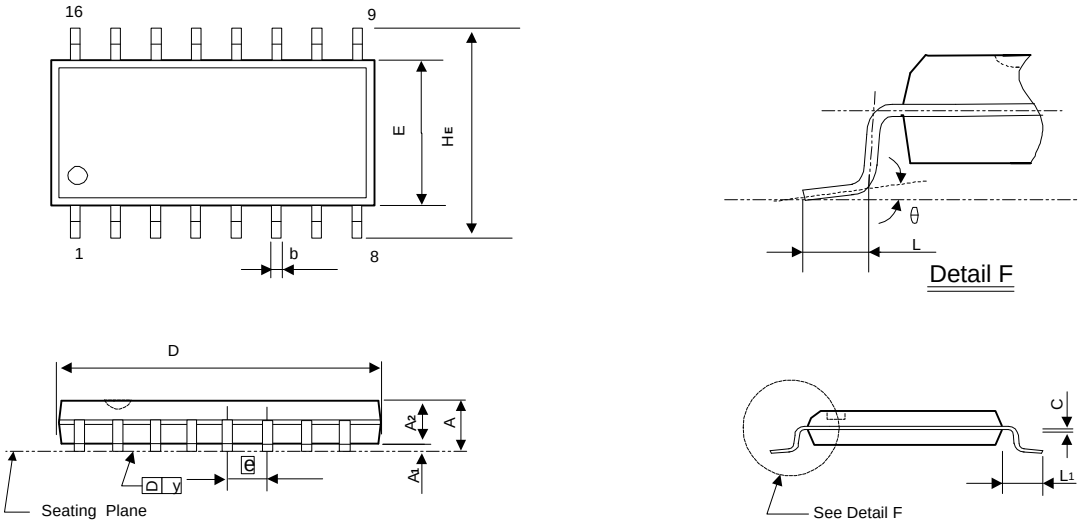
9. Package Information

SOP 16L Outline Dimensions **Unit: inches/mm**



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.053	0.064	0.069	1.35	1.63	1.75
A_1	0.004	0.006	0.010	0.10	0.15	0.25
A_2	0.051	0.055	0.059	1.30	1.40	1.50
b	0.013	0.016	0.020	0.33	0.41	0.51
C	0.007	—	0.010	0.19	—	0.25
D	0.386	0.390	0.394	9.80	9.91	10.01
E	0.150	0.154	0.157	3.80	3.90	4.00
e		0.050			1.27	
H_E	0.228	0.236	0.244	5.80	6.00	6.20
L	0.016	0.025	0.050	0.40	0.64	1.27
L_1		0.042			1.07	
y	—	—	0.004	—	—	0.10
θ	0°	—	8°	0°	—	8°

TSSOP 16L Outline Dimensions **Unit: inches/mm**



Symbol	Dimension in inches			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.031	0.035	0.041	0.80	0.90	1.05
b	0.007	—	0.012	0.19	—	0.30
C	0.004	—	0.008	0.09	—	0.20
D	0.193	0.197	0.201	4.90	5.00	5.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026BSC.			0.65BSC.		
H_E	0.252BSC.			6.40BSC.		
L	0.020	0.024	0.030	0.50	0.60	0.75
L_1	0.039REF.			1.0REF.		
y	—	—	0.004	—	—	0.10
θ	0°	—	8°	0°	—	8°

10. Ordering Information

Part No.	Package
IT7001M	16-SOP
IT7001N	16-TSSOP