Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Datasheet Describes Mode 0 Operation
- 33 MHz Clock Rate
- Byte Mode and 256-byte Page Mode for Program Operations
- Sector Architecture:
  - Four Sectors with 32K Bytes Each (1M)
  - 128 Pages per Sector
- Product Identification Mode
- Low-voltage Operation
  - 2.7 (V_{CC} = 2.7V to 3.6V)
- Sector Write Protection
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for both Hardware and Software Data Protection
- Self-timed Program Cycle (20 µs/Byte Typical)
- Self-timed Sector Erase Cycle (1 second/Sector Typical)
- Single Cycle Reprogramming (Erase and Program) for Status Register
- High Reliability
  - Endurance: 10,000 Write Cycles Typical
  - Data Retention: 20 Years
- Lead-free/Halogen-free Devices
- 8-lead JEDEC SOIC and 8-lead SAP Packages

Description

The AT25F1024A provides 1,048,576 bits of serial reprogrammable Flash memory organized as 131,072 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25F1024A is available in a space-saving 8-lead JEDEC SOIC and 8-lead SAP packages.

The AT25F1024A is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All write cycles are completely self-timed.

Block Write protection for top 1/4, top 1/2 or the entire memory array is enabled by programming the status register. Separate write enable and write disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

1Mbit High Speed SPI Serial Flash Memory

1M (131,072 x 8)

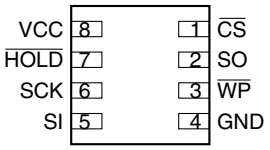
AT25F1024A

Rev. 3346G–SFLSH–7/07

Table 0-1. Pin Configurations

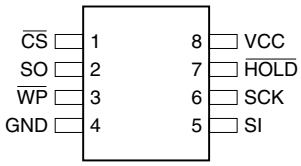
Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

8-lead SAP



Bottom View

8-lead SOIC



Absolute Maximum Ratings*

Operating Temperature	–40°C to +85°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +5.0V
Maximum Operating Voltage	4.2V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram

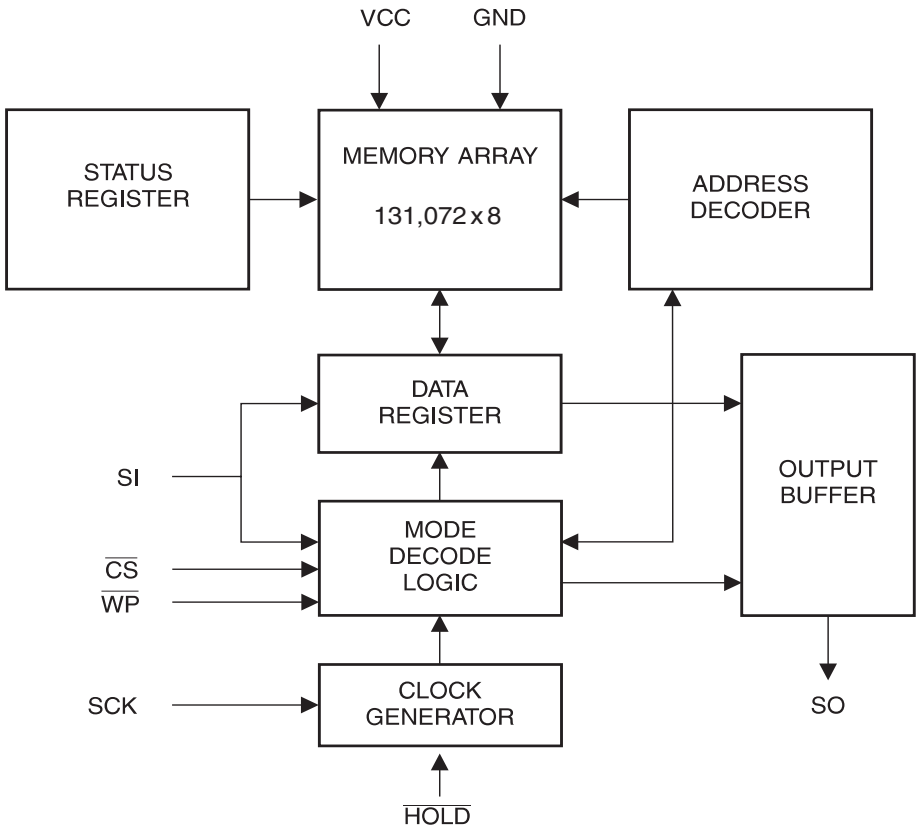


Table 0-2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 20.0 MHz, V_{CC} = +3.6V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 0-3. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40 to +85°C, V_{CC} = +2.7 to +3.6V, T_{AC} = 0 to +70°C, V_{CC} = +2.7 to +3.6V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC}	Supply Voltage			2.7		3.6	V
I_{CC1}	Supply Current	V_{CC} = 3.6V at 33 MHz, SO = Open Read			10.0	17.0	mA
I_{CC2}	Supply Current	V_{CC} = 3.6V at 33 MHz, SO = Open Write			25.0	45.0	mA
I_{SB}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			2.0	10.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL}[1]	Input Low Voltage			–0.6		V_{CC} x 0.3	V
V_{IH}[1]	Input High Voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH}	Output High Voltage		I_{OH} = –100 µA	V_{CC} – 0.2			V

Note: 1. V_{IL} and V_{IH} max are reference only and are not tested.

Table 0-4. AC Characteristics

Applicable over recommended operating range from T_A = –40 to +85°C, V_{CC} = +2.7 to +3.6V
C_L = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency	0		33	MHz
t_{RI}	Input Rise Time			20	ns
t_{FI}	Input Fall Time			20	ns
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			ns
t_{CS}	$\overline{CS}$ High Time	25			ns
t_{CSS}	$\overline{CS}$ Setup Time	25			ns
t_{CSH}	$\overline{CS}$ Hold Time	10			ns
t_{SU}	Data In Setup Time	5			ns
t_H	Data In Hold Time	5			ns
t_{HD}	$\overline{Hold}$ Setup Time	15			ns
t_{CD}	$\overline{Hold}$ Time	15			ns
t_V	Output Valid			9	ns
t_{HO}	Output Hold Time	0			ns
t_{LZ}	$\overline{Hold}$ to Output Low Z			200	ns
t_{HZ}	$\overline{Hold}$ to Output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{EC}	Erase Cycle Time per Sector			1.1	s
t_{SR}	Status Register Write Cycle Time			60	ms
t_{BPC}	Byte Program Cycle Time(1)		30	50	µs
Endurance(2)			10K		Write Cycles(3)

Notes:
1. The programming time for n bytes will be equal to n x t_{BPC}.
2. This parameter is ensured by characterization at 3.0V, 25°C only.
3. One write cycle consists of erasing a sector, followed by programming the same sector.

1. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25F1024A always operates as a slave.

TRANSMITTER/RECEIVER: The AT25F1024A has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{CS}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

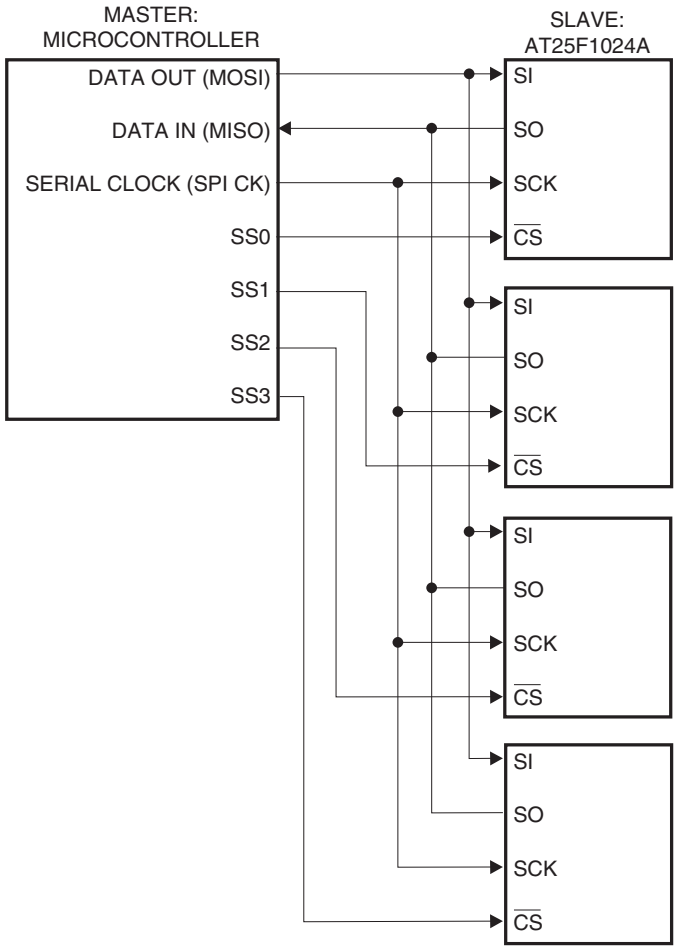
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25F1024A, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{CS}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25F1024A is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the AT25F1024A. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The AT25F1024A has a write lockout feature that can be activated by asserting the write protect pin ($\overline{WP}$). When the lockout feature is activated, locked-out sectors will be READ only. The write protect pin will allow normal read/write operations when held high. When the $\overline{WP}$ is brought low and WPEN bit is “1”, all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal status register write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is “0”. This will allow the user to install the AT25F1024A in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to “1”.

Figure 1-1. SPI Serial Interface



2. Functional Description

The AT25F1024A is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25F1024A utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 2-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low transition.

Write is defined as program and/or erase in this specification. The following commands, Program, Sector Erase, Chip Erase, and WRSR are write instructions for AT25F1024A.

Table 2-1. Instruction Set for the AT25F1024A

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
PROGRAM	0000 X010	Program Data into Memory Array
SECTOR ERASE	0101 X010	Erase One Sector in Memory Array
CHIP ERASE	0110 X010	Erase All Sectors in Memory Array
RDID	0001 X101	Read Manufacturer and Product ID

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All write instructions must therefore be preceded by the WREN instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the WRDI instruction disables all write commands. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

READ STATUS REGISTER (RDSR): The RDSR instruction provides access to the status register. The Ready/Busy and write enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction. During internal write cycles, all other commands will be ignored except the RDSR instruction.

Table 2-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Table 2-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = “0” ($\overline{RDY}$) indicates the device is ready. Bit 0 = “1” indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = “0” indicates the device *is not* write enabled. Bit 1 = “1” indicates the device is write enabled.
Bit 2 (BP0)	See Table 2-4.
Bit 3 (BP1)	See Table 2-4.
Bits 4-6 are 0s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 2-5 on page 10.
Bits 0-7 are 1s during an internal write cycle.	

READ PRODUCT ID (RDID): The RDID instruction allows the user to read the manufacturer and product ID of the device. The first byte after the instruction will be the manufacturer code (1FH = ATMEL), followed by the device code, 60H.

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection for the AT25F1024A. The AT25F1024A is divided into four sectors where the top quarter (1/4), top half (1/2), or all of the memory sectors can be protected (locked out) from write. Any of the locked-out sectors will therefore be Read only. The locked-out sector and the corresponding status register control bits are shown in Table 2-4.

The three bits, BP0, BP1, and WPEN, are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 2-4. Block Write Protect Bits

	Status Register Bits		AT25F1024A	
Level	BP1	BP0	Array Addresses Locked Out	Locked-out Sector(s)
0	0	0	None	None
1(1/4)	0	1	018000 – 01FFFF	Sector 4
2(1/2)	1	0	010000 – 01FFFF	Sector 3, 4
3(All)	1	1	000000 – 01FFFF	All sectors (1 – 4)

The WRSR instruction also allows the user to enable or disable the Write Protect ($\overline{WP}$) pin through the use of the write protect enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is “1”. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is “0.” When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the locked-out sectors in the memory array are disabled. Write is only allowed to sectors of the memory which are not locked out. The WRSR instruction is self-timed to automatically erase and program BP0, BP1, and WPEN bits. In order to write the status register, the device must first be write enabled via the WREN instruction. Then, the instruction and data for the three bits are entered. During the internal write cycle, all instructions will be ignored except RDSR instructions. The AT25F1024A will automatically return to write disable state at the completion of the WRSR cycle.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to “0”, as long as the $\overline{WP}$ pin is held low.

Table 2-5. WPEN Operation

WPEN	WP	WEN	ProtectedBlocks	UnprotectedBlocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ (READ): Reading the AT25F1024A via the SO pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the Read instruction is transmitted via the SI line followed by the byte address to be read (see Table 3-6 on page 13). Upon completion, any data on the SI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The Read instruction can be continued since the byte address is automatically incremented and data will continue to be shifted out. For the AT25F1024A, when the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous Read instruction.

PROGRAM (PROGRAM): In order to program the AT25F1024A, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the Program instruction can be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal self-timed programming cycle, all commands will be ignored except the RDSR instruction.

The Program instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Program instruction is transmitted via the SI line followed by the byte address and the data (D7-D0) to be programmed (see Table 3-7 on page 14). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a RDSR instruction. If Bit 0 = 1, the program cycle is still in progress. If Bit 0 = 0, the program cycle has ended. Only the RDSR instruction is enabled during the program cycle.

A single Program instruction programs 1 to 256 consecutive bytes within a page if it is not write protected. The starting byte could be anywhere within the page. When the end of the page is reached, the address will wrap around to the beginning of the same page. If the data to be programmed are less than a full page, the data of all other bytes on the same page will remain unchanged. If more than 256 bytes of data are provided, the address counter will roll over on the same page and the previous data provided will be replaced. The same byte cannot be reprogrammed without erasing the whole sector first. The AT25F1024A will automatically return to the write disable state at the completion of the Program cycle.

Note: If the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re-initiate the serial communication.

Table 2-6. Address Key

Address	AT25F1024A
A_N	$A_{16} – A_0$
Don't Care Bits	$A_{23} – A_{17}$

SECTOR ERASE (SECTOR ERASE): Before a byte can be reprogrammed, the sector which contains the byte must be erased. In order to erase the AT25F1024A, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then the Sector Erase instruction can be executed.

Table 1. Sector Addresses

Sector Address	AT25F1024A Sector
000000 to 007FFF	Sector 1
008000 to 00FFFF	Sector 2
010000 to 017FFF	Sector 3
018000 to 01FFFF	Sector 4

The Sector Erase instruction erases every byte in the selected sector if the sector is not locked out. Sector address is automatically determined if any address within the sector is selected. The Sector Erase instruction is internally controlled; it will automatically be timed to completion. During this time, all commands will be ignored, except RDSR instruction. The AT25F1024A will automatically return to the write disable state at the completion of the Sector Erase cycle.

CHIP ERASE (CHIP ERASE): As an alternative to the Sector Erase, the Chip Erase instruction will erase every byte in all sectors that are not locked out. First, the device must be write enabled via the WREN instruction. Then the Chip Erase instruction can be executed. The Chip Erase instruction is internally controlled; it will automatically be timed to completion. The Chip Erase cycle time typically is 3.5 seconds. During the internal erase cycle, all instructions will be ignored except RDSR. The AT25F1024A will automatically return to the write disable state at the completion of the Chip Erase cycle.

3. Timing Diagrams (for SPI Mode 0 (0, 0))

Figure 3-1. Synchronous Data Timing

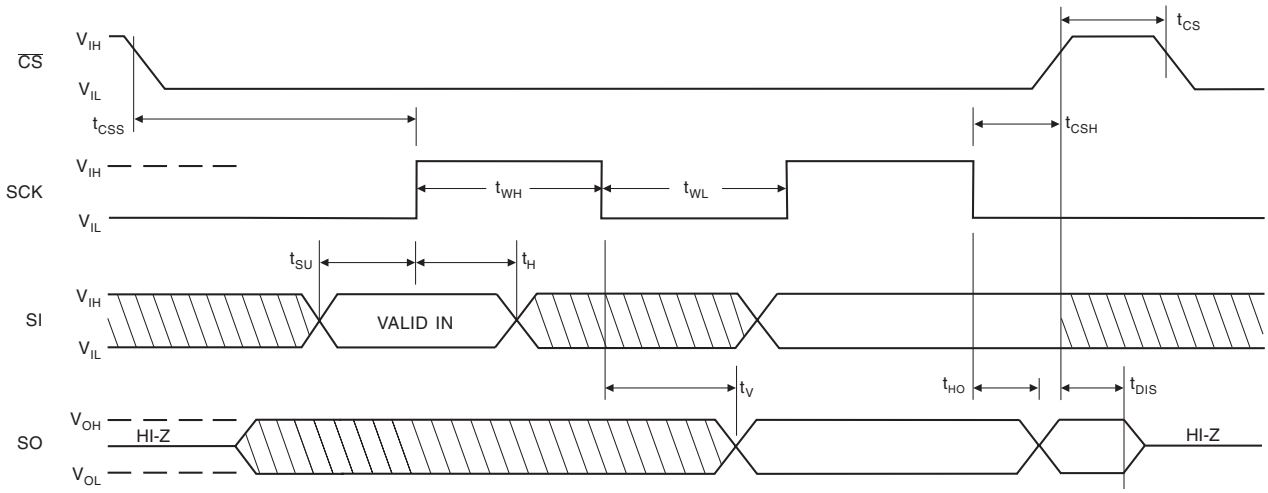


Figure 3-2. WREN Timing

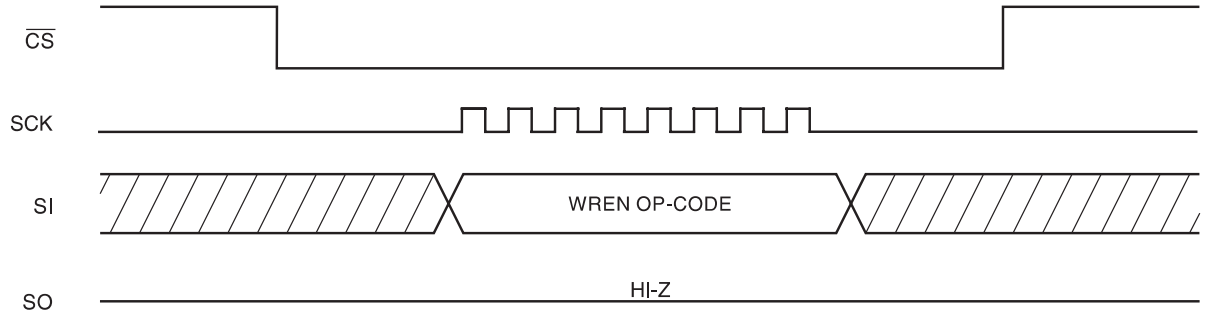


Figure 3-3. WRDI Timing

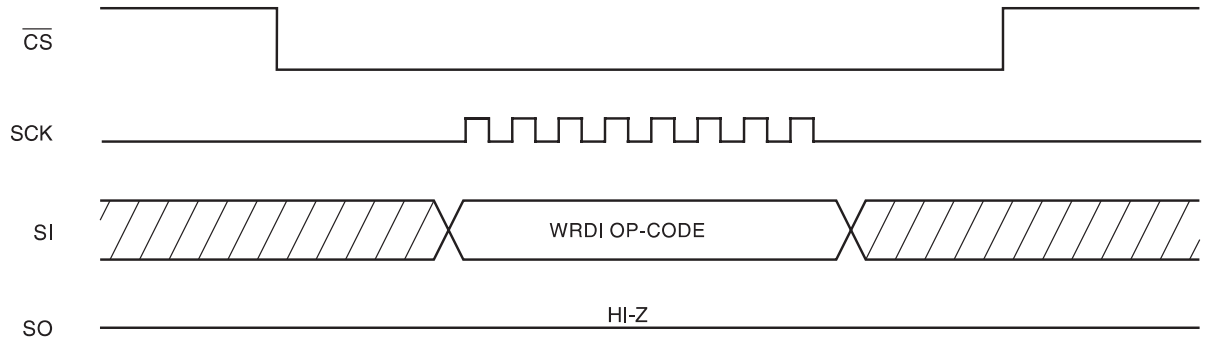


Figure 3-4. RDSR Timing

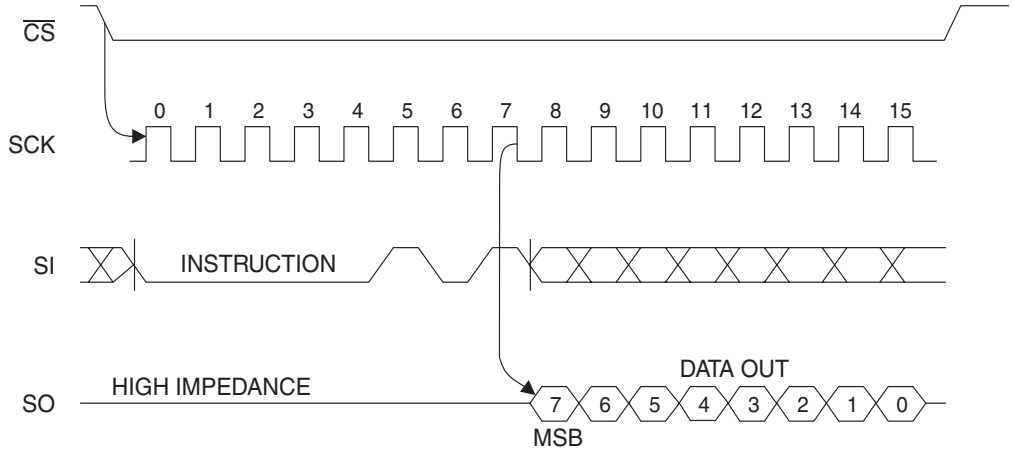


Figure 3-5. WRSR Timing

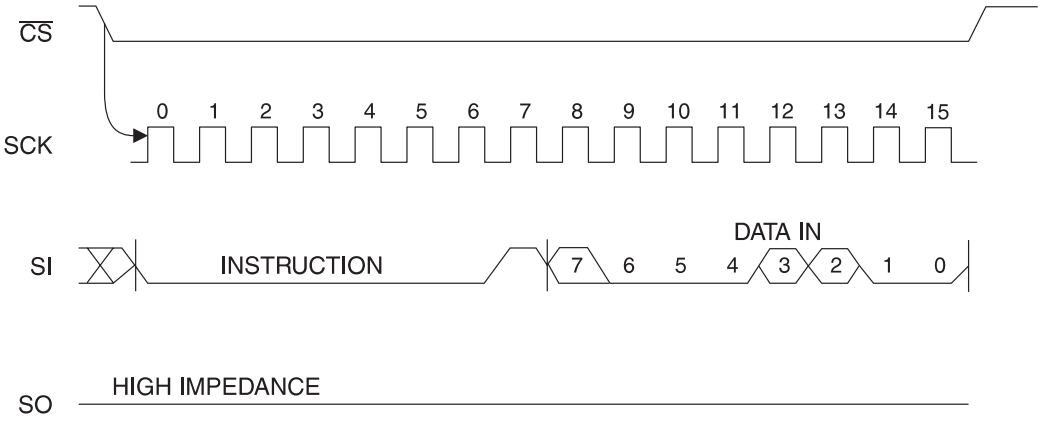


Figure 3-6. READ Timing

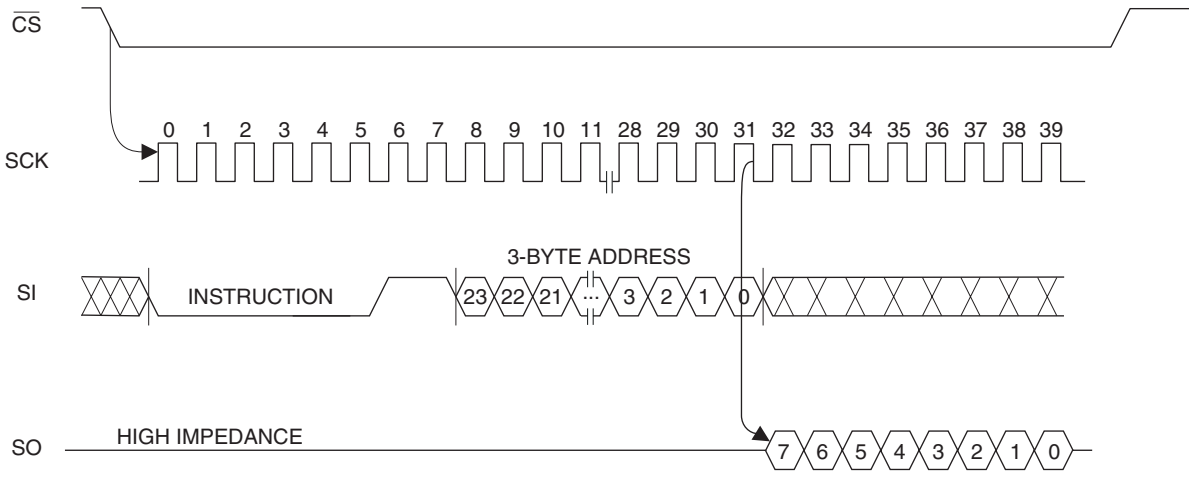


Figure 3-7. PROGRAM Timing

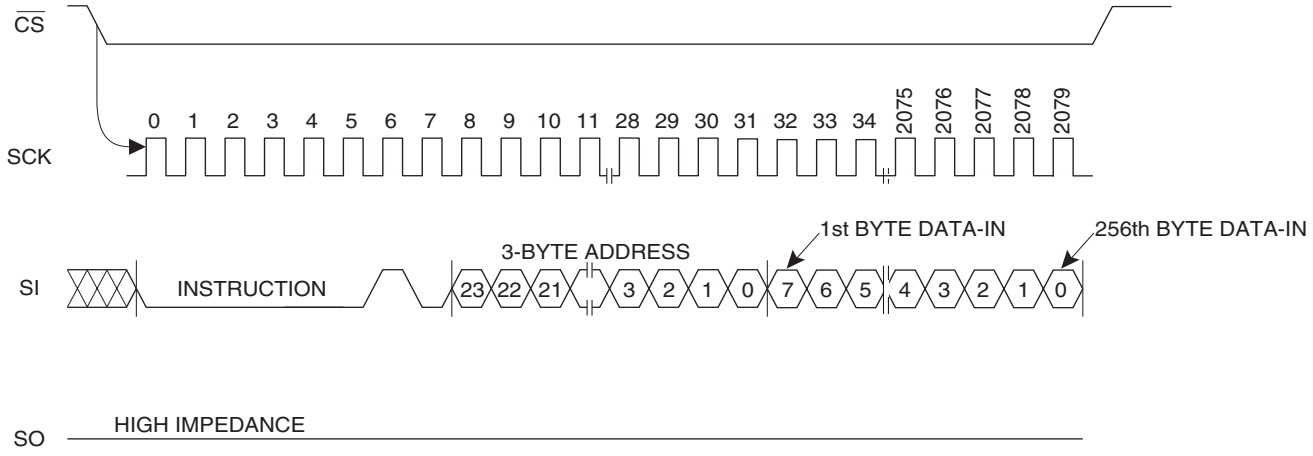


Figure 3-8. HOLD Timing

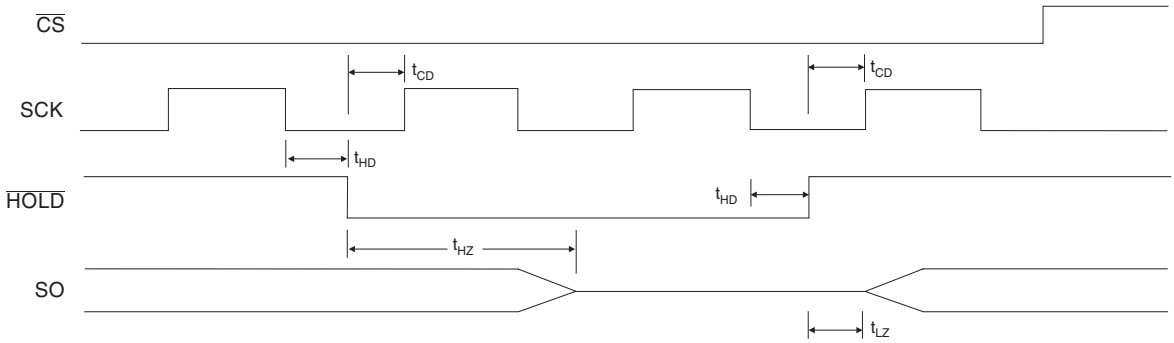
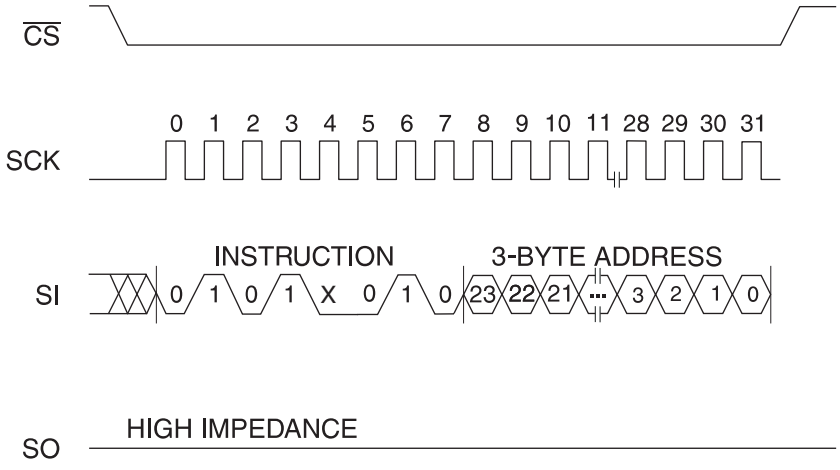
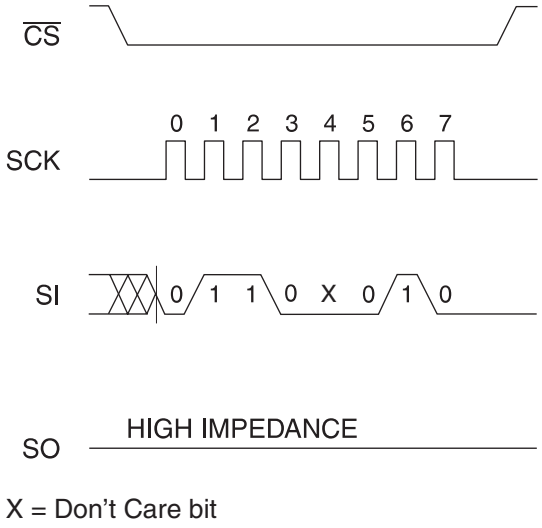


Figure 3-9. SECTOR ERASE Timing



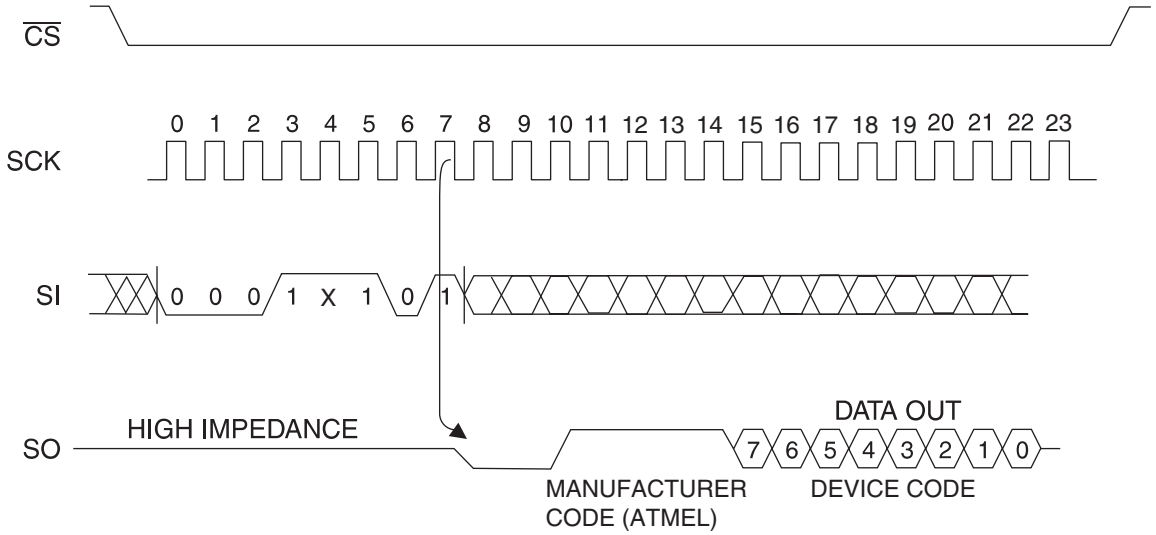
X = Don't Care bit

Figure 3-10. CHIP ERASE Timing



X = Don't Care bit

Figure 3-11. RDID Timing



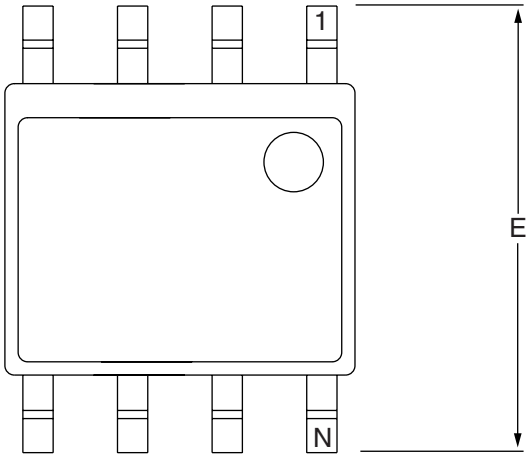
Ordering Information

Ordering Code	Package	Operation Range
AT25F1024AN-10SU-2.7 AT25F1024AY4-10YU-2.7	8S1 8Y4	Lead-free/Halogen-free Industrial Temperature (–40 to 85°C)

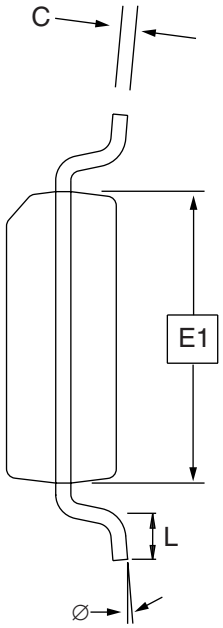
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8Y4	8-lead, 6.00 mm x 4.90 mm Body, Dual Footprint, Non-leaded, Small Array Package (SAP)
Options	
–2.7	Low-voltage (2.7V to 3.6V)

Package Drawing

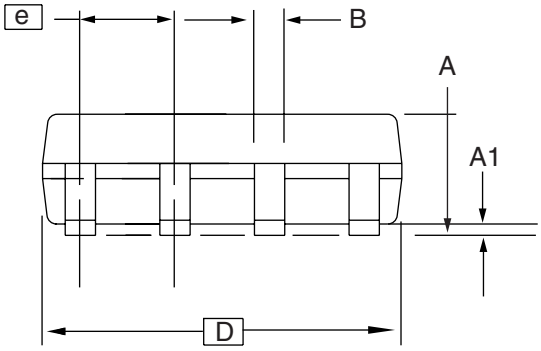
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

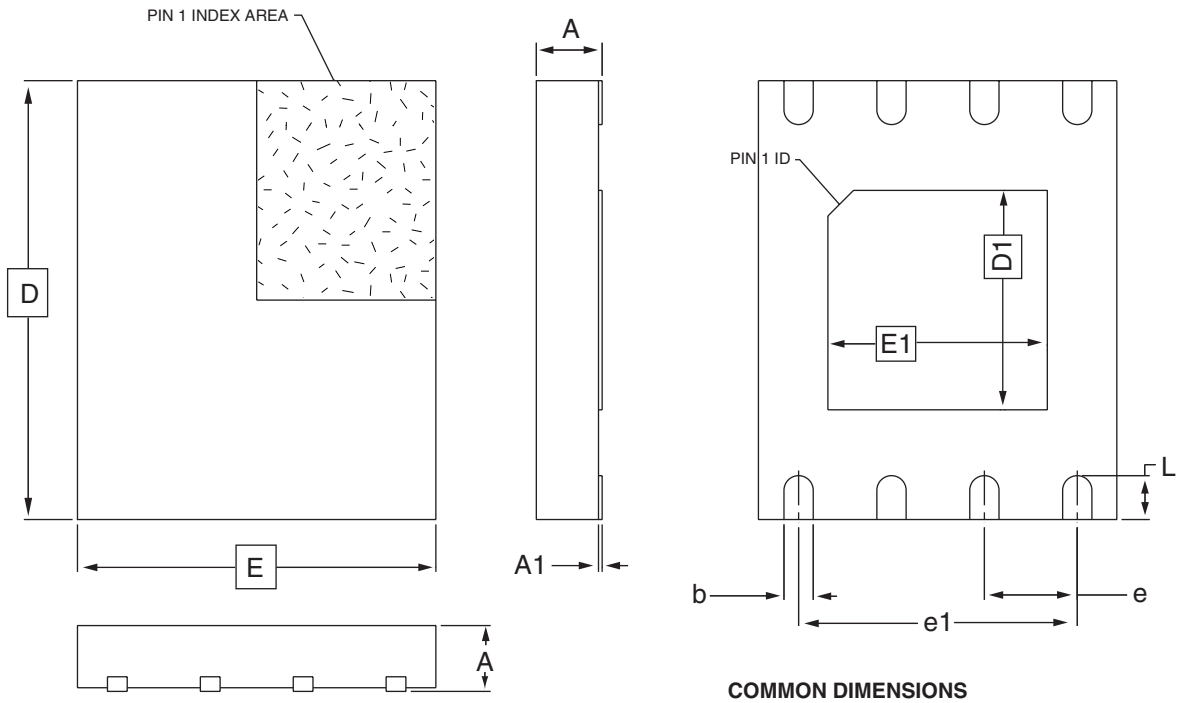
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

8Y4 – SAP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.90	
A1	0.00	–	0.05	
D	5.80	6.00	6.20	
E	4.70	4.90	5.10	
D1	2.85	3.00	3.15	
E1	2.85	3.00	3.15	
b	0.35	0.40	0.45	
e	1.27 TYP			
e1	3.81 REF			
L	0.50	0.60	0.70	

5/24/04

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8Y4**, 8-lead (6.00 x 4.90 mm Body) SOIC Array Package (SAP) Y4	**DRAWING NO.** 8Y4	**REV.** A

Revision History

Doc. Rev.	Date	Comments
3346G	7/2007	Implemented revision history Converted to new template

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