FUJITSU MICROELECTRONICS
DATA SHEET

DS05-11463-1E

MEMORY Consumer FCRAM™

CMOS

512M Bit (4 bank x 2M word x 64 bit)

Consumer Applications Specific Memory for SiP

MB81EDS516545

= 4.6 ns Min / 216 MHz Max (Tj ≤ + 105 °C)
-t_{CK} = 5 ns Min / 200 MHz Max (Tj ≤ + 125 °C)

- Low Voltage Power Supply: $V_{DD} = V_{DDQ}$ + 1.7 V to + 1.9 V
- Junction Temperature: T_J = − 10 °C to + 125 °C
- 1.8 V-CMOS compatible inputs
- Unidirectional READ Data Strobe per 2 byte
- Unidirectional WRITE Data Strobe per 2 byte
- Burst Length: 2, 4, 8, 16
- CAS latency: 2, 3, 4
- Clock Stop capability during idle periods
- Auto Precharge option for each burst access
- Configurable Driver Strength and Pre Driver Strength
- Auto Refresh and Self Refresh Modes
- Deep Power Down Mode
- Low Power Consumption
  -I_{DD4R} =330 mA Max @ 3.46 GByte/s
  -I_{DD4W} =380 mA Max @ 3.46 GByte/s
- 8 K refresh cycles /16.7 ms (Tj ≤ +125 °C)

(Continued)

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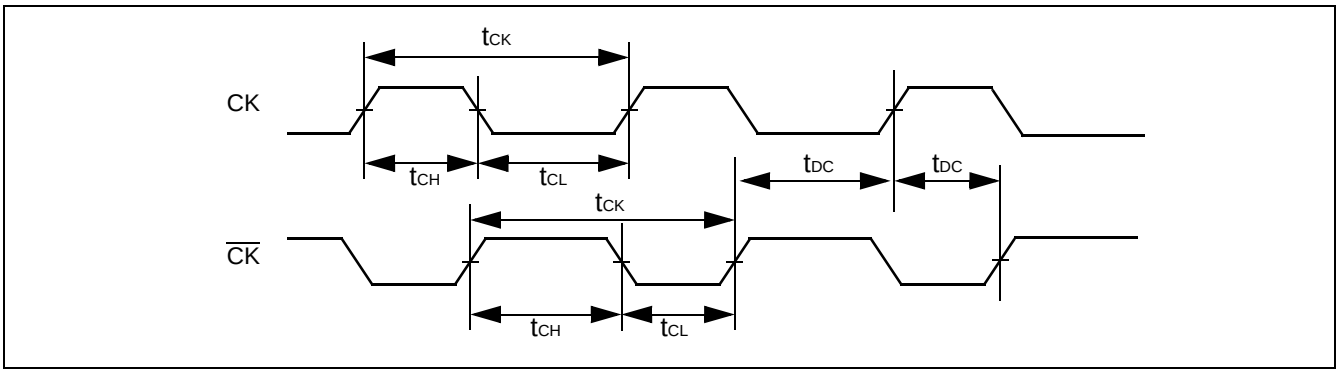
- Optional commands and features
  -Multi Bank Active (MACT)
  -Multi Bank Precharge (MPRE)
  -Background Refresh (BREF)
  -Additional RDQS Toggle (ART)

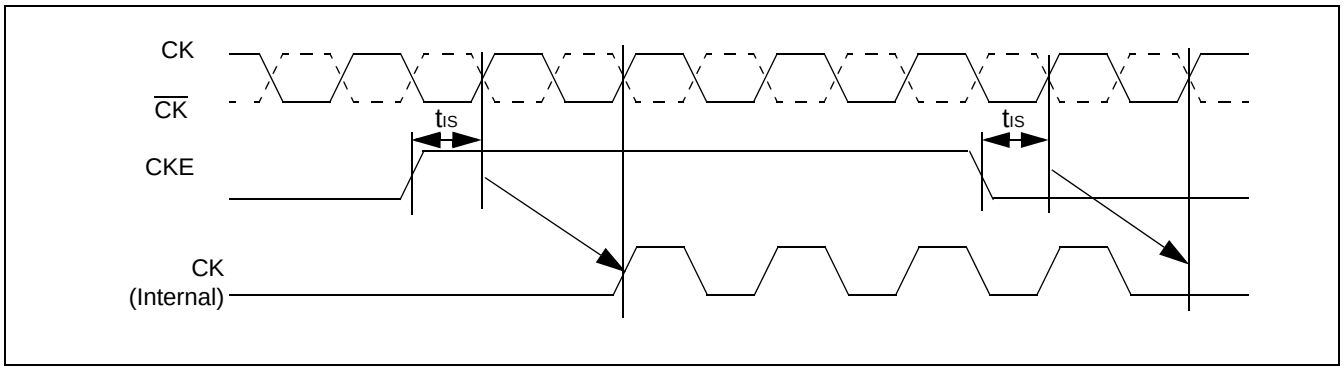
1. Clock Inputs (CK and $\overline{CK}$)

CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the rising edge of CK. And the rising edge of CK and the rising edge of $\overline{CK}$ increment device internal address counter and drive even and odd data input/out respectively.



2. Clock Enable (CKE)

CKE is a high active clock enable signal. When CKE = Low is latched at the rising edge of CK, the next CK rising edge will be invalid. CKE controls power down mode and self refresh mode.



3. Chip Select ($\overline{CS}$)

$\overline{CS}$ enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address inputs. $\overline{CS}$ = High disable command input but internal operation such as burst cycle will not be suspended.

4. Command Inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$)

The combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ at a rising edge of the CK define the command for device operation. Refer to the "■COMMAND TRUTH TABLE".

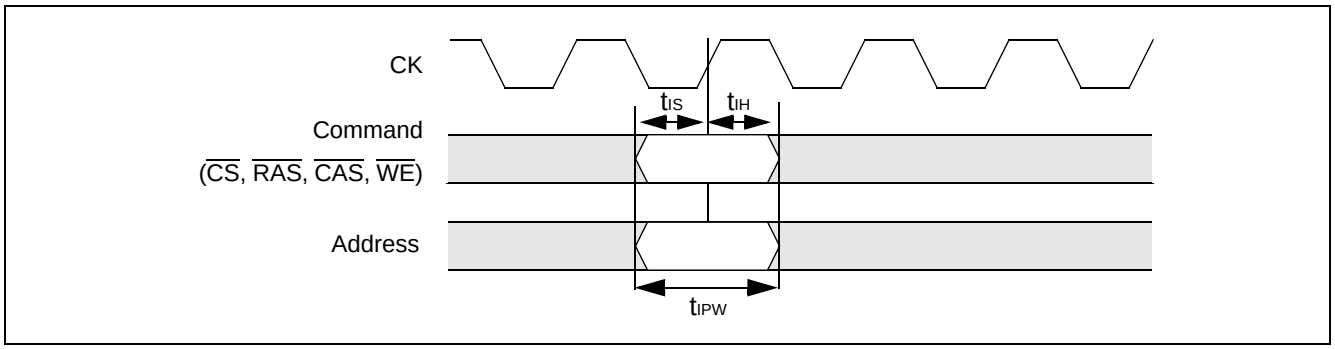
5. Bank Address Inputs (BA0, BA1)

BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.

6. Address Inputs (A0 to A12)

Address input selects an arbitrary location of a total of 2,097,152 words of each memory cell matrix. Total 21 address input signals are required to decode such a matrix. Row Address (RA) is input from A0 to A12 and Column Address (CA) is input from A0 to A7. Row addresses are latched with ACTIVE (ACT or MACT) commands, and Column addresses and Auto Precharge (AP) bit are latched with Read (READ or READA) or Write command (WRIT or WRITA).

• Command and address inputs setup and hold time



7. Input Data Mask (DM0 to DM7)

DM is an input mask signal for write data. Input data is masked when DM is sampled High on the both edges of WDQS along with input data. DM0, DM1, DM2, DM3, DM4, DM5, DM6 and DM7 correspond to DQ[7:0], DQ[15:8], DQ[23:16], DQ[31:24], DQ[39:32], DQ[47:40], DQ[55:48] and DQ[63:56] respectively. Refer to the “DQ/RDQS/WDQS/DM Correspondence Table”.

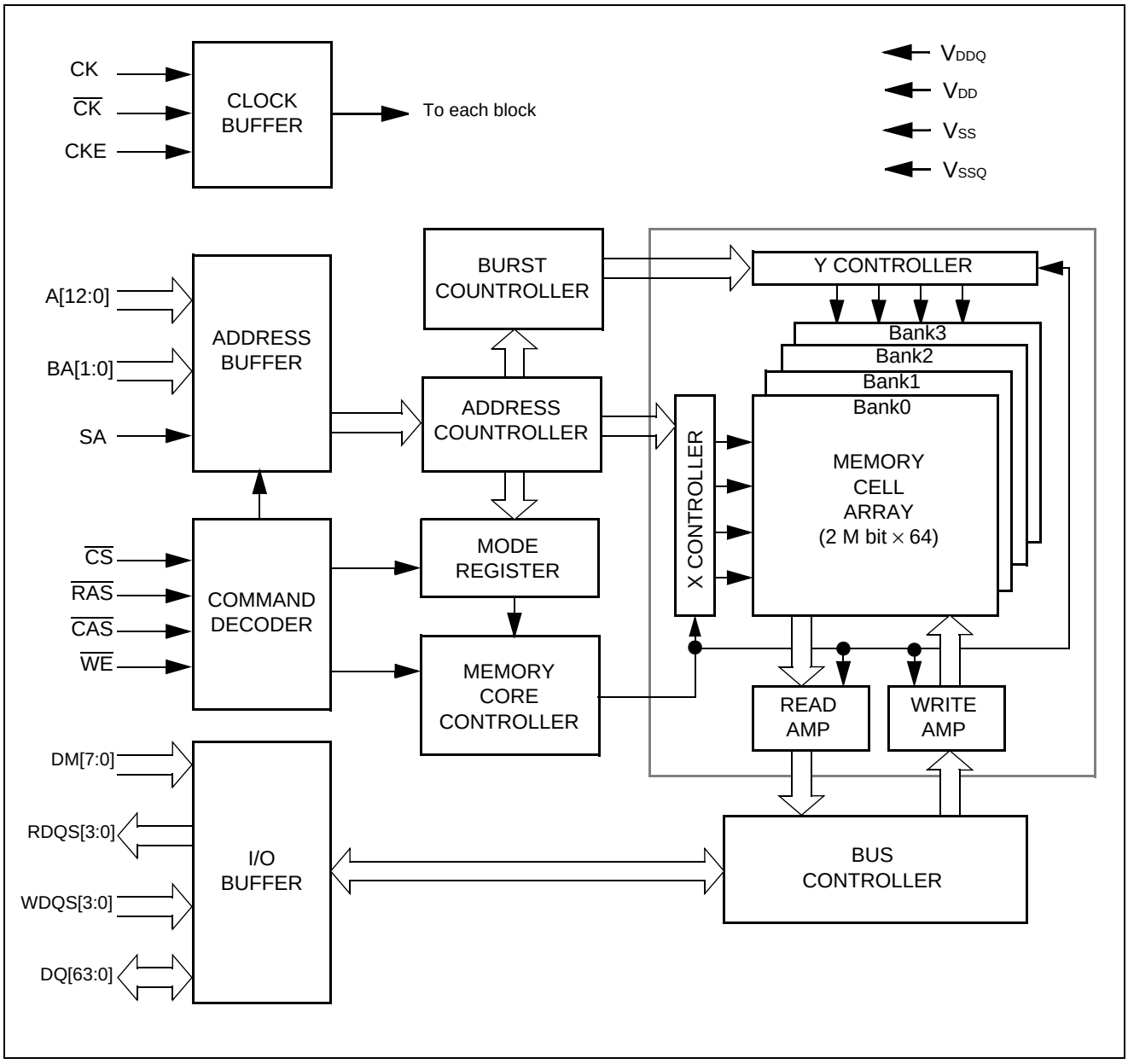
8. Data Bus Input / Output (DQ0 to DQ63)

DQ is data bus input / output signal.

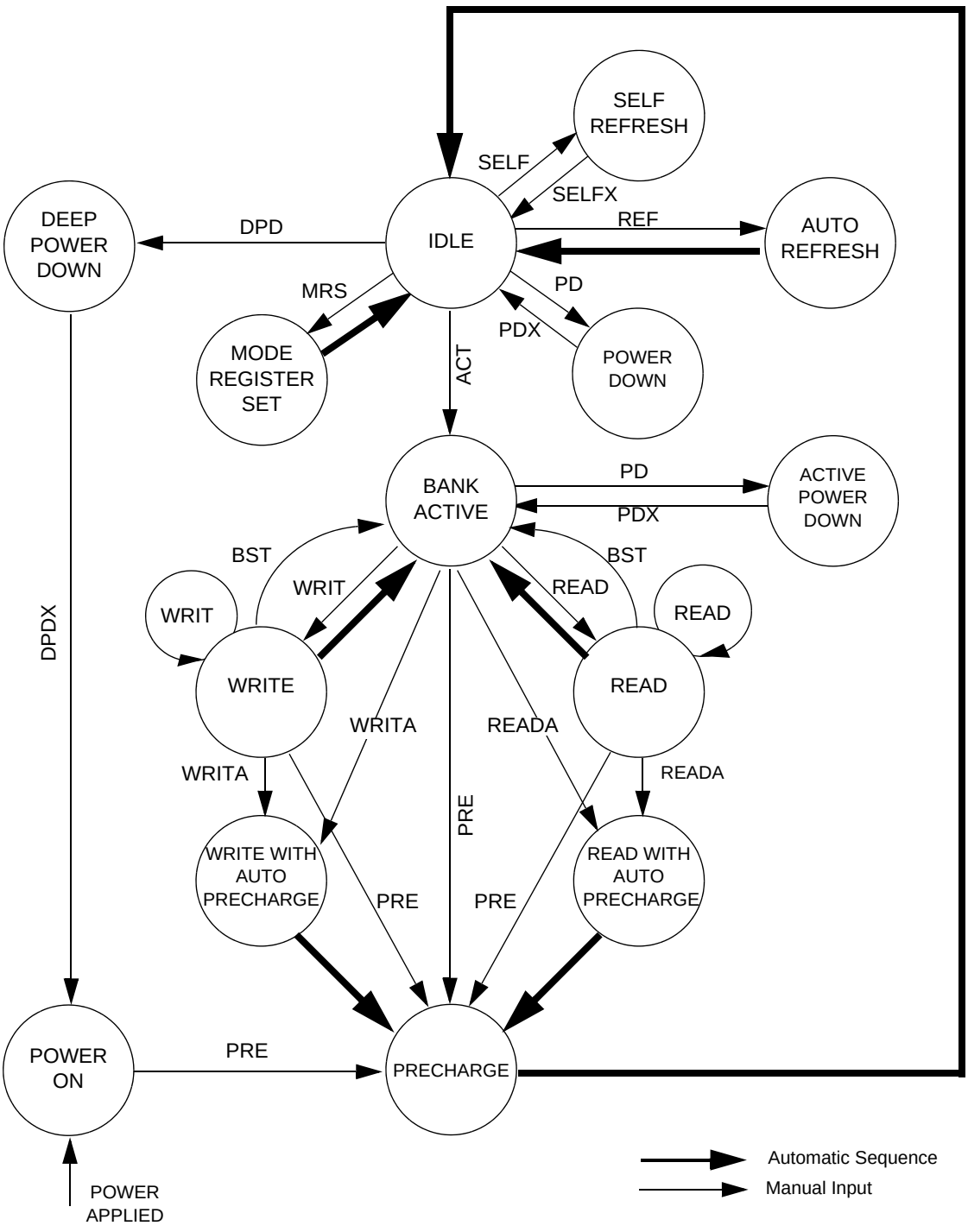
9. Read Data Strobe (RDQS0 to RDQS3)

RDQS is output signal transmitted by memory during read operation. RDQS is edge aligned with output data. RDQS0, RDQS1, RDQS2 and RDQS3 correspond to DQ[15:0], DQ[31:16], DQ[47:32] and DQ[63:48] respectively. Refer to the “DQ/RDQS/WDQS/DM Correspondence Table”.
After stable power supply, RDQS outputs Low.

■ BLOCK DIAGRAM



■ SIMPLIFIED STATE DIAGRAM



Note: "■SIMPLIFIED STATE DIAGRAM" is based on the single bank operation.
State transition of multi bank operation are not described in all detail.

3. Burst Length (BL)

Burst Length (BL) is the number of word to be read or write as the result of a single READ or WRITE command. It can be set on 2, 4, 8, 16 words boundary through Mode Register. The burst type is sequential that is incremental decoding scheme within a boundary address to be determined by burst length. Device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0).

Burst Length	Starting Column Address				Burst Address Sequence (Hexadecimal)
	A_3	A_2	A_1	A_0	
2	X	X	X	0	0 - 1
	X	X	X	1	1 - 0
4	X	X	0	0	0 - 1 - 2 - 3
	X	X	0	1	1 - 2 - 3 - 0
	X	X	1	0	2 - 3 - 0 - 1
	X	X	1	1	3 - 0 - 1 - 2
8	X	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	X	0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0
	X	0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1
	X	0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2
	X	1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	X	1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4
	X	1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5
	X	1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E

4. CAS Latency (CL)

CAS Latency (CL) is the delay between READ command being registered and first read data becoming available during read operation. First read data will be valid after (CL-1) × t_{CK} + t_{AC} from the CK rising edge where Read command being latched.

5. Driver Strength (DS)

Driver Strength (DS) is to adjust the driver strength of data output.

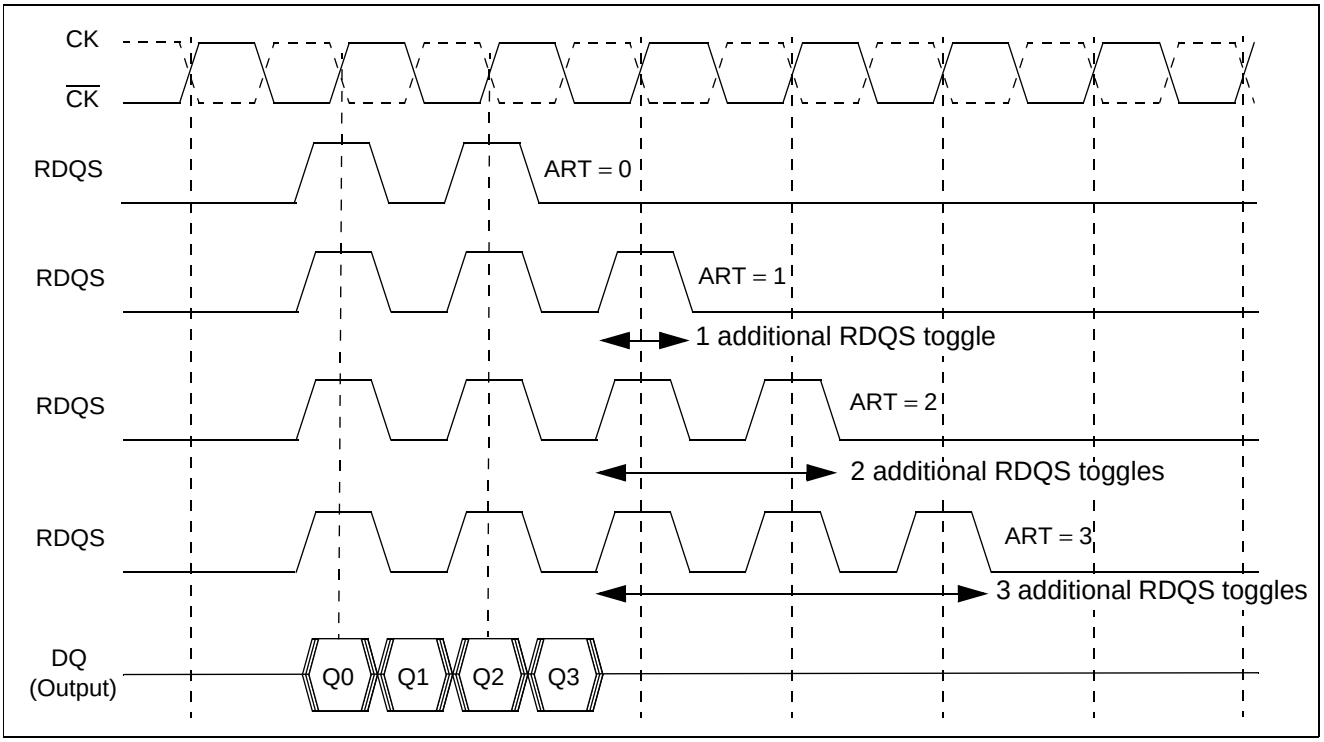
6. Pre Driver Strength (PDS)

Pre Driver Strength (PDS) is to adjust the transition time of the data output without changing the output driver impedance.

7. Additional RDQS Toggle (ART)

Additional RDQS Toggle (ART) is to set RDQS toggle count after the last pair of data output. Total RDQS toggle count is BL/2 + ART.

RDQS Timing with Additional RDQS Toggle (ART) function @BL=4



3) Single Bank Operation

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
IDLE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT/MACT	Bank Active
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	NOP *2
	L	L	L	H	X	REF/BREF	Auto Refresh or Background Refresh *3
	L	L	L	L	MODE	MRS	Mode Register Set *3, *4
BANK ACTIVE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Start Read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Start Write; Determine AP
	L	L	H	H	BA, RA	ACT/MACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	Precharge; Determine Precharge Type
	L	L	L	H	X	REF/BREF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
READ	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst Terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst read by new burst read; Determine AP
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Illegal
	L	L	H	H	BA, RA	ACT/MACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	Terminate burst read by precharge → IDLE
	L	L	L	H	X	REF/BREF	Illegal
	L	L	L	L	MODE	MRS	
WRITE	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Burst terminate → BANK ACTIVE
	L	H	L	H	BA, CA, AP	READ/READA	Interrupt burst write by new burst read; Determine AP *5
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Interrupt burst write by new burst write; Determine AP
	L	L	H	H	BA, RA	ACT/MACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	
	L	L	L	H	X	REF/BREF	Illegal
	L	L	L	L	MODE	MRS	

(Continued)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Write Recovering	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	
	L	H	L	H	BA, CA, AP	READ/READA	Illegal
	L	H	L	L	BA, CA, AP	WRIT/WRITA	Start Write; Determine AP
	L	L	H	H	BA, RA	ACT/MACT	Illegal *1
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	
	L	L	L	H	X	REF/BREF	Illegal
	L	L	L	L	MODE	MRS	
Precharging	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	H	BA, CA, AP	READ/READA	Illegal *1
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT/MACT	
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	NOP *2
	L	L	L	H	X	REF/BREF	Illegal
	L	L	L	L	MODE	MRS	

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Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Function
Bank Activating	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal *2
	L	H	L	H	BA, CA, AP	READ/READA	
	L	H	L	L	BA, CA, AP	WRIT/WRITA	
	L	L	H	H	BA, RA	ACT/MACT	
	L	L	H	L	BA, AP	PRE/PALL/ MPRE	
	L	L	L	H	X	REF/SELF/BREF	Illegal
	L	L	L	L	MODE	MRS	
Refreshing/ Mode Register Setting	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	
	L	H	H	L	X	BST	Illegal
	L	H	L	X	X	READ/READA/ WRIT/WRITA	
	L	L	X	X	X	ACT/MACT/PRE/ PALL/MPRE/ REF/SELF/ BREF/MRS	

RA = Row Address BA = Bank Address
CA = Column Address AP = Auto Precharge

Note: Assuming CKE = H during the previous clock cycle and the current clock cycle. After illegal commands are asserted, following command and stored data should not be guaranteed.

*1: Illegal to bank in the specified state. Command entry may be legal depending on the state of bank selected by BA.

*2: NOP to bank in precharging or in idle state. Bank in active state may be precharged depending on BA.

*3: Illegal if any bank is not idle.

*4: MRS command should be issued on condition that all DQ are in High-Z.

*5: Requires appropriate DM masking.

■ BANK OPERATION COMMAND TABLE

Minimum clock latency or delay time for single bank operation

1st Command	2nd Command (same bank)														
	MRS	ACT	READ	READA	WRIT	WRITA	BST	PRE	PALL	REF	SELF	MACT	MPRE	BREF	BREFX
MRS	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	—
ACT	—	—	t_{RCD}	*4 t_{RCD}	t_{RCD}	*5 t_{RCD}	—	t_{RAS}	t_{RAS}	—	—	—	t_{RAS}	—	—
READ	—	—	1	1	*6 BL/2 +CL	*6 BL/2 +CL	1	*3 1	*3 1	—	—	—	*3 1	—	—
READA	*1, *2 BL/2 + t_{RP}	BL/2 + t_{RP}	—	—	—	—	BL/2 + t_{RP}	BL/2 + t_{RP}	BL/2 + t_{RP}	*1 BL/2 + t_{RP}	*1, *2 BL/2 + t_{RP}	BL/2 + t_{RP}	BL/2 + t_{RP}	BL/2 + t_{RP}	—
WRIT	—	—	*6 2 + t_{WTR}	*6 2 + t_{WTR}	1	1	1	*3 BL/2 + 1 + t_{WR}	*3 BL/2 + 1 + t_{WR}	—	—	—	*3 BL/2 + 1 + t_{WR}	—	—
WRITA	*1, *2 BL/2 + 1 + t_{DAL}	BL/2 + 1 + t_{DAL}	—	—	—	—	BL/2 +1 + t_{DAL}	BL/2 +1 + t_{DAL}	BL/2 +1 + t_{DAL}	*1 BL/2 +1 + t_{DAL}	*1, *2 BL/2 +1 + t_{DAL}	BL/2 + 1 + t_{DAL}	BL/2 +1 + t_{DAL}	BL/2 +1 + t_{DAL}	—
READ - BST	—	—	1	1	CL	CL	1	*3 1	*3 1	—	—	—	1	—	—
WRIT - BST	—	—	1 + t_{WTR}	1 + t_{WTR}	1	1		*3 1 + t_{WR}	*3 1 + t_{WR}	—	—	—	1 + t_{WR}	—	—
PRE	*1, *2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	*1 t_{RP}	*1, *2 t_{RP}	t_{RP}	1	t_{RP}	—
PALL	*2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	*2 t_{RP}	t_{RP}	1	t_{RP}	—
REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	—
SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	—
MACT	—	—	*7 t_{RCD}	*7 t_{RCD}	*7 t_{RCD}	*7 t_{RCD}	—	t_{RAS}	1 + t_{RAS}	—	—	—	1 + t_{RAS}	—	—
MPRE	*1, *2 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	*1 t_{RP}	*1, *2 t_{RP}	t_{RP}	1	t_{RP}	—
BREF	RC x t_{REFC}	RC x t_{REFC}	—	—	—	—	—	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	*8 t_{REFC}
BREFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	—

" - " : illegal

*1: Assume all banks are in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RAS} (Min.) is satisfied.

*4: ACT to READA interval must be longer than t_{RAS} - BL/2.

*5: ACT to WRITA interval must be longer than t_{RAS} - (1 + BL/2 + t_{WR}).

*6: Assume appropriate DM masking.

*7: 1st read or write access must be allowed for appropriate bank specified in the ACT and MACT commands of "■COMMAND TRUTH TABLE".

*8: BREFX command can be issued only when Background Refresh is in progress.

Minimum clock latency or delay time for multi bank operation

1st Command	2nd Command (other bank)														
	MRS	ACT	READ	READA	WRIT	WRITA	BST	PRE	PALL	REF	SELF	MACT	MPRE	BREF	BREFX
MRS	t_{MRD}	t_{MRD}	—	—	—	—	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	t_{MRD}	—
ACT	—	t_{RRD}	1	1	1	1	1	1	t_{RAS}	—	—	t_{RRD}	1	t_{RRD}	*7 t_{RRD}
READ	—	*1, *3 1	1	1	*5 BL/2 +CL	*5 BL/2 +CL	1	1	*4 1	—	—	*1, *3 1	1	1	*7 1
READA	*1, *2 BL/2 + t_{RP}	*1, *3 1	BL/2	BL/2	*5 BL/2 +CL	*5 BL/2 +CL	BL/2 + t_{RP}	1	*4 BL/2 + t_{RP}	*1 BL/2 + t_{RP}	*1 BL/2 + t_{RP}	*1, *3 1	1	1	*7 1
WRIT	—	*1, *3 1	*5 2 + t_{WTR}	*5 2 + t_{WTR}	1	1	1	1	*4 BL/2 + 1 + t_{WR}	—	—	*1, *3 1	1	1	*7 1
WRITA	*1 BL/2 + 1 + t_{DAL}	*1, *3 1	*5 BL/2 + 1 + t_{WTR}	*5 BL/2 + 1 + t_{WTR}	BL/2	BL/2	BL/2 +1 + t_{DAL}	1	*4 BL/2 + 1 + t_{DAL}	*1 BL/2 + 1 + t_{DAL}	*1 BL/2 + 1 + t_{DAL}	*1, *3 1	1	1	*7 1
READ - BST	—	*1, *3 1	1	1	CL	CL	1	1	*4 1	—	—	*1, *3 1	1	1	*7 1
WRIT - BST	—		1 + t_{WTR}	1 + t_{WTR}	1	1		1	*4 1 + t_{WR}	—	—				
PRE	*1, *2 t_{RP}	*1, *3 1	1	1	1	1	1	1	1	*1 t_{RP}	*1, *2 t_{RP}	*1, *3 1	1	1	*7 1
PALL	*1 t_{RP}	t_{RP}	—	—	—	—	t_{RP}	1	1	t_{RP}	t_{RP}	t_{RP}	1	t_{RP}	—
REF	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	—
SELFX	t_{REFC}	t_{REFC}	—	—	—	—	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	t_{REFC}	—
MACT	—	t_{RRD}	*6 1	*6 1	*6 1	*6 1	1	1	1+ t_{RAS}	—	—	t_{RRD}	1	t_{RRD}	*7 t_{RRD}
MPRE	*1, *2 t_{RP}	*1, *3 1	1	1	1	1	1	1	1	*1 t_{RP}	*1, *2 t_{RP}	*1, *3 1	1	1	*7 1
BREF	RC x t_{REFC}	t_{RRD}	1	1	1	1	1	1	RC x t_{REFC}	RC x t_{REFC}	RC x t_{REFC}	t_{RRD}	1	RC x t_{REFC}	*7 t_{REFC}
BREFX	t_{REFC}	t_{RRD}	1	1	1	1	1	1	t_{REFC}	t_{REFC}	t_{REFC}	t_{RRD}	1	t_{REFC}	—

" - " : illegal

*1: Assume other bank is in IDLE state.

*2: Assume output is in High-Z state.

*3: Assume t_{RRD} is satisfied.

*4: Assume t_{RAS} is satisfied.

*5: Assume appropriate DM masking.

*6: 1st read or write access must be allowed for appropriate bank specified in the ACT and MACT commands of "■COMMAND TRUTH TABLE".

*7: BREFX command can be issued only when Background Refresh is in progress.

■ COMMAND DESCRIPTION

1. DESELECT (DESL)

When $\overline{CS}$ is High at the CK rising edge, all input signals are neglected. Internal operation such as burst cycle is held.

2. NO OPERATION (NOP)

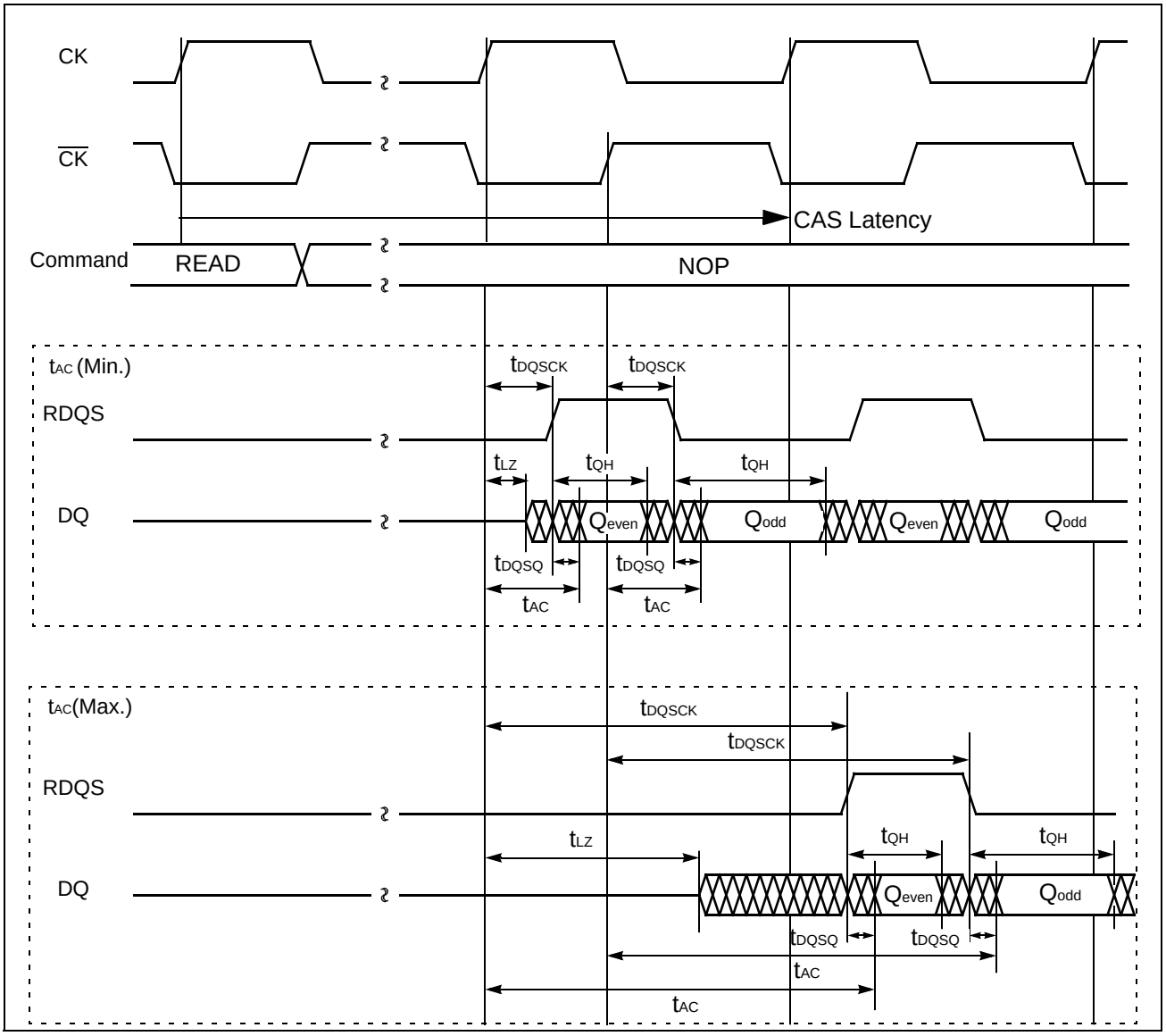
NOP disables address and data input and internal operation such as burst cycle is held.

3. BANK ACTIVE (ACT)

ACT activates the bank selected by BA and latch the row address through A0 to A12.

4. READ (READ)

READ initiates burst read operation to an activated row address. Address inputs of A[7:0] determine starting column address and A10 determines whether Auto Precharge is used or not. Initially RDQS output Low level then start toggling together with data output with respect to CL and BL. The read data output is edge-aligned with first rising edge of RDQS and successive read data output are edge-aligned to the successive edge of RDQS. The CK drives the rising edge of RDQS and Even data, and the $\overline{CK}$ drives the falling edge of RDQS and Odd data.

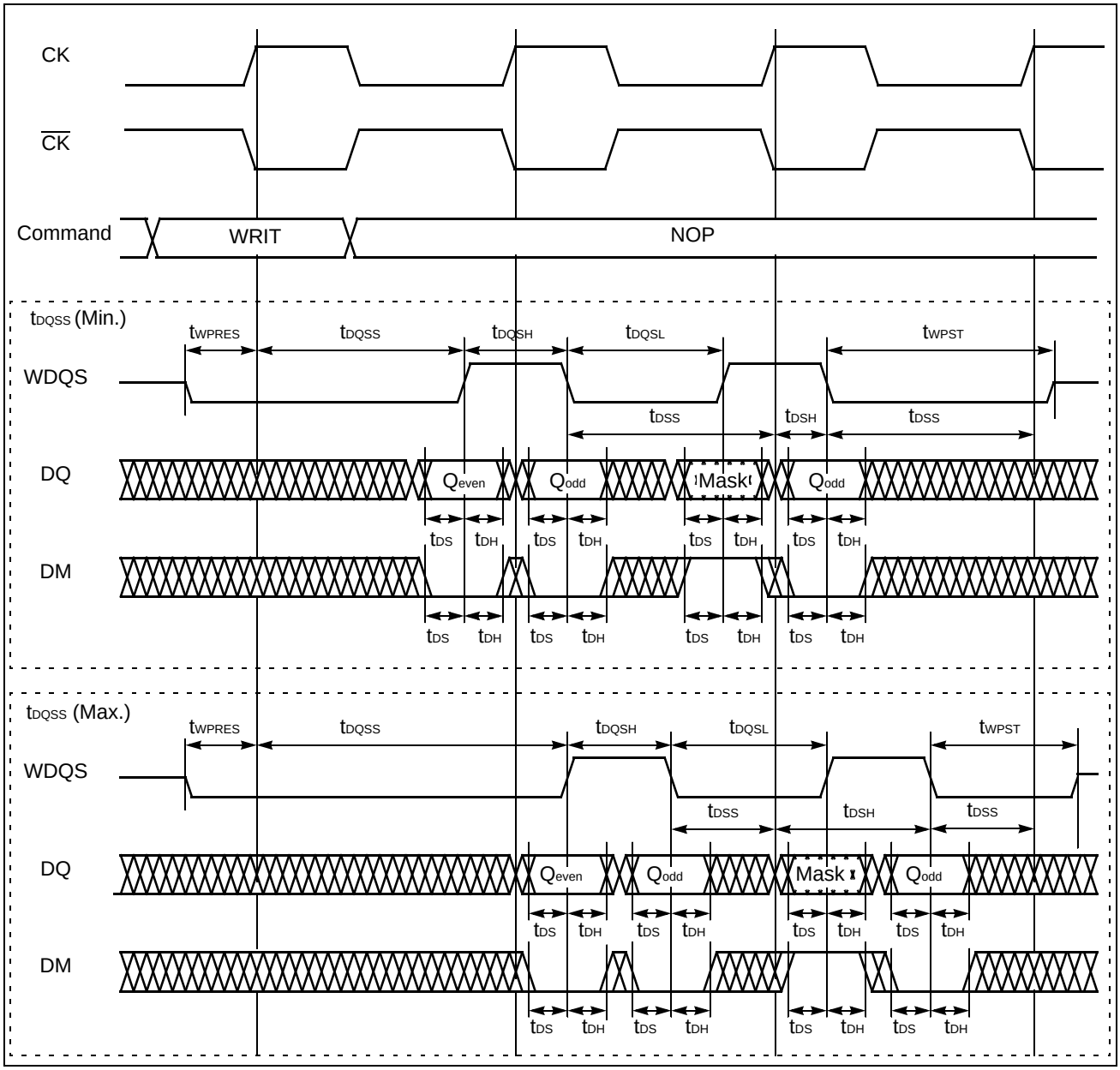


5. READ with Auto Precharge (READA)

READA commands can be issued by READ command with AP (A10) = H. Auto precharge is a feature which precharge the activated bank after the completion of burst read operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after BL/2 from READA command. READ with Auto precharge operation should not be interrupted by subsequent READ, READA, WRITE, WRITEA commands. Next ACTIVE (ACT) command can be issued after BL/2 + t_{RP} after READA command.

6. WRITE (WRIT)

WRIT initiates burst write operation to an active row address. Address inputs of A[7:0] determine starting column address and AP(A10) determines whether Auto Precharge is used or not. WDQS input must be provided in order to latch the input data. WDQS must be brought to Low to satisfy the specified time duration of the Write Preamble Setup Time to CK (t_{WPRES}). Input data window must be guaranteed with specified minimum setup and hold time against edge of WDQS input (t_{DS}, t_{DH}). The input data appearing on DQ is written into memory cell array subject to the DM input logic level appearing coincident with the input data. If a given signal on DM is registered Low, the corresponding data will be written into the cell array. And if a given signal on DM is registered High, the corresponding data will be masked and write will not be executed to that byte. After data input with respect to BL is completed, WDQS must be kept low for the specified minimum value of Write Postamble Time (t_{WPST}).



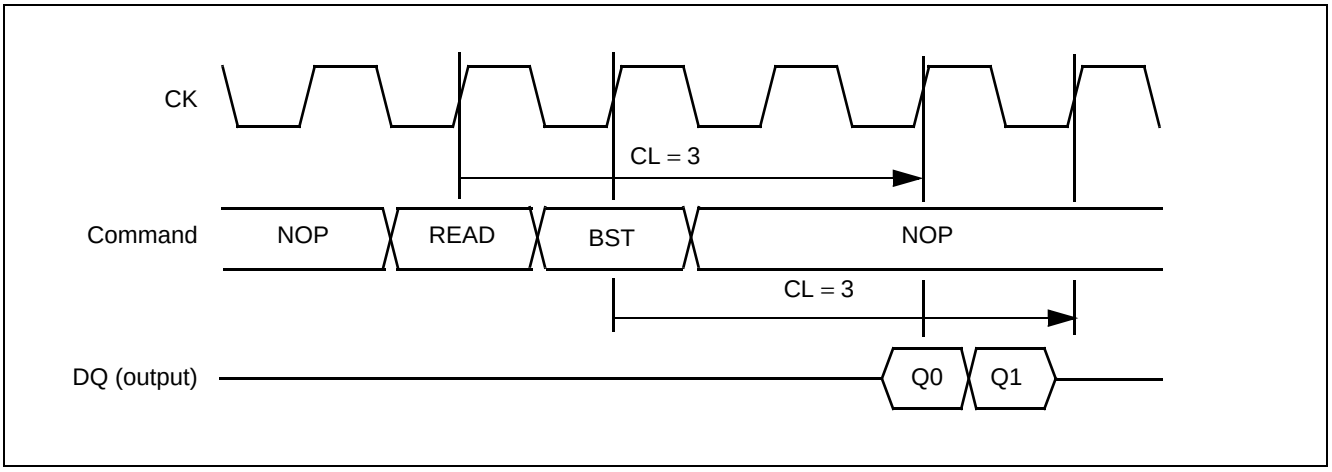
7. WRITE with Auto Precharge (WRITA)

WRITA commands can be issued by WRIT command with AP (A10) = H. Auto precharge is a feature which precharge the activated bank after the completion of burst write operation. The t_{RAS} is defined from between ACTIVE (ACT) command to the internal precharge which starts after 1+ BL/2 + t_{WR} from WRITA command. WRIT with Auto precharge operation should not be interrupted by subsequent READ, READA, WRIT, WRITA commands. Next ACTIVE (ACT) command can be issued after 1+ BL/2 + t_{DAL} after WRITA command.

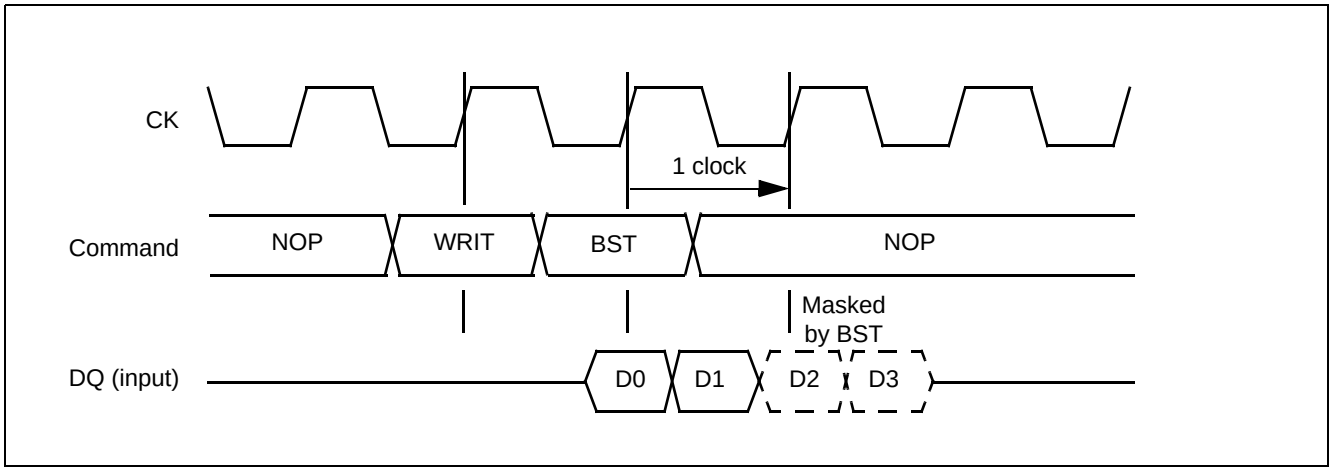
8. BURST TERMINATE (BST)

BST terminates the burst read or write operation. When a burst read is terminated by BST command, the data output will be in High-Z after CAS latency from the BST command. When a burst write is terminated by BST command, the data input after 1 clock from BST command will be masked.

Terminate read by BST @CL=3



Terminate write by BST



9. PRECHARGE SINGLE BANK (PRE)

PRECHARGE SINGLE BANK (PRE) command starts precharge operation for a bank selected by BA. A selected bank will be in IDLE state after specified time duration of t_{RP} from PRE command. A10 determines whether one or all banks are precharged. If AP(A10) = L, a bank to be selected by BA is precharged.

10. PRECHARGE ALL BANK (PALL)

PRECHARGE ALL BANKS (PALL) command starts precharge operation for all banks. All banks will be in IDLE state after specified time duration of t_{RP} from PALL command. A10 determines whether one or all banks are precharged. If AP(A10) = H, all banks are precharged and BA input is a “don't care”.

11. AUTO REFRESH (REF)

AUTO REFRESH (REF) command starts internal refresh operation which uses the internal refresh address counter. All banks must be precharged prior to the Auto-refresh command. Data retention capability depends on the Junction Temperature (Tj). Total 8,192 AUTO REFRESH (REF) commands must be asserted within the following refresh period of t_{REF}.

Tj Max (°C)	t_{REF} (ms)
+ 105	64
+ 125	16.7

12. SELF-REFRESH ENTRY (SELF)

SELF REFRESH ENTRY (SELF) commands can be issued by AUTO REFRESH (REF) command in conjunction with CKE = Low after last read data has been appeared on DQ. During Self Refresh mode, stored data can be retained without external clocking and all inputs except for CKE will be a “don't care”. Self refresh mode can be used when Tj is less than + 85°C. Auto Refresh must be issued to retain data when Tj is greater than + 85 °C.

13. SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum t_{IS} after CKE brought High, and then the NO OPERATION command (NOP) or the DESELECT command (DESL) should be asserted within one t_{REFC} period. CKE should be held High within one t_{REFC} period after t_{IS}. Refer to the “(15) Self Refresh Entry and Exit” in “■TIMING DIAGRAMS” for the detail. It is recommended to assert an Auto-refresh command just after the t_{REFC} period to avoid the violation of refresh period.

14. MODE REGISTER SET (MRS)

MODE REGISTER SET (MRS) commands to program the mode registers. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command. MRS command should only be issued on conditions that all DQs are in High-Z and all banks are in IDLE state. The contents of the mode registers is undefined after the power-up and Deep Power Down Exit. Therefore MRS must be issued to set each content of mode registers after initialization. Refer to the “Power Up Initialization” in “ ■FUNCTIONAL DESCRIPTION”.

15. POWER DOWN ENTRY (PD)

POWER DOWN ENTRY (PD) commands to drive the device in Power Down mode and maintains low power state as long as CKE is kept Low. During Power Down state, all inputs signals are a “don't care” except for CKE. Power Down mode must be entered on condition that all DQs are in High-Z.

16. POWER DOWN EXIT (PDX)

POWER DOWN EXIT (PDX) commands to resume the device from Power Down mode. Any commands can be detected 1 clock after PDX commands.

17. DEEP POWER DOWN ENTRY (DPD)

DEEP POWER DOWN ENTRY (DPD) commands to drive the device in Deep Power Down mode which is the lowest power consumption but all stored data and the contents of mode registers will be lost. During Deep Power Down state, all inputs signals except for CKE are a “don't care” and all DQs and RDQS will be in High-Z. Deep Power Down mode must be entered on conditions that all DQs are in High-Z and all banks are in IDLE state.

18. DEEP POWER DOWN EXIT (DPDX)

DEEP POWER DOWN EXIT (DPDX) commands to resume the device from Deep Power Down mode. Power up initialization procedure must be performed after DPDX commands. Refer to the “Power Up Initialization” in “■ FUNCTIONAL DESCRIPTION”.

19. MULTI BANK ACTIVE (MACT)

MULTI BANK ACTIVE (MACT) command activates 2 banks simultaneously selected by BA1. SA must be High to issue MACT command. BA1 determines the target bank group is either Bank 0 & 1 or Bank 2 & 3. And BA0 determines the bank where 1st read or write access can be performed. If MACT command is issued to Bank 0 (or Bank 2) with RA = N, same Row Address of RA = N is activated for Bank 1 (or Bank 3) and 1st read or write access must be allowed for RA=N of Bank 0 (or Bank 2). If MACT command is issued to Bank 1 (or Bank 3) with RA = N, next Row Address of RA = N + 1 is activated for Bank 0 (or Bank 2) and 1st read or write access must be allowed for RA = N of Bank 1 (or Bank 3). If MACT command is issued to Bank 1 (or Bank 3) with RA = FFFh, internal row address counter is wrap around therefore activated Row Address is FFFh for Bank 1 (or Bank 3) and 000h for Bank 0 (or Bank 2).

Command Truth Table of ACT and MACT

Command	Symbol	SA	BA1	BA0	Row Address A[12:0]	1st access		2nd access	
						Bank	RA	Bank	RA
BANK ACTIVE	ACT	L	L	L	RA = N	Bank 0	RA = N	NA	
			L	H		Bank 1	RA = N	NA	
			H	L		Bank 2	RA = N	NA	
			H	H		Bank 3	RA = N	NA	
MULTI BANK ACTIVE	MACT	H	L	L	RA = N	Bank 0	RA = N	Bank 1	RA = N
			L	H		Bank 1	RA = N	Bank 0	RA = N + 1
			H	L		Bank 2	RA = N	Bank 3	RA = N
			H	H		Bank 3	RA = N	Bank 2	RA = N + 1

The following memory map example enables to issue effective MACT command for 2-bank interleave access between Bank 0 and Bank 1 or Bank 2 and Bank 3.

Memory Map Example for 2-bank interleave access by MACT command

Bank	0	1	0	1	→	0	1	0	1	0	1	→	0	1	0	1
RA	000h		001h		→	N - 1		N		N + 1		→	FFFh		FFFh	
Bank	2	3	2	3	→	2	3	2	3	2	3	→	2	3	2	3
RA	000h		001h		→	N - 1		N		N + 1		→	FFFh		FFFh	

20. MULTI BANK PRECHARGE (MPRE)

MULTI BANK PRECHARGE (MPRE) command starts precharge operation for 2 banks selected by BA1. SA must be High to issue MPRE command. Selected 2 banks will be in IDLE state after specified time duration of t_{RP} from MPRE command. BA1 determines whether the target bank group is Bank 0 & 1 or Bank 2 & 3. If MPRE command is issued to BA1 = L, Bank 0 and Bank 1 will be precharged simultaneously. If MPRE command is issued to BA1 = H, Bank 2 and Bank 3 will be precharged simultaneously.

Command Truth Table of PRE, PALL and MPRE

Command	Symbol	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10 (AP)	A[9:0], A11, A12	SA	Precharged Bank
PRECHARGE SINGLE BANK	PRE	L	L	H	L	L	L	L	X	L	Bank 0
						L	H				Bank 1
						H	L				Bank 2
						H	H				Bank 3
PRECHARGE ALL BANK	PALL					X	X	H			All Banks
MULTI BANK PRECHARGE	MPRE					L	X	L		H	Bank 0 & 1
						H					Bank 2 & 3

21. BACKGROUND REFRESH ENTRY (BREF)

BACKGROUND REFRESH ENTRY (BREF) command starts internal refresh operation for 2 banks selected by BA1. SA must be High to issue BREF command and A10 determines either BACKGROUND REFRESH ENTRY (BREF) or EXIT (BREFX). 2 banks which will be refreshed must be precharged prior to the BREF command. When BREF command is issued, Refresh Count (RC) must be set through A[9:0] inputs as shown in the following table. RC defines how many refresh cycle is executed by one BREF command. RC can be set from 1 to 31 cycles. Refreshed banks will be in REFRESH state for a period specified by RC x t_{REFC}. While any read and write access must not be performed during AUTO REFRESH which initiates all banks refresh, background refresh can allow to read or write access to 2 banks which are not refreshed. BA1 determines the target bank group either Bank 0 & 1 or Bank 2 & 3. If BREF command is issued to BA1 = L, Bank 0 & 1 will be refreshed and Bank 2 & 3 can be accessible. If BREF command is issued to BA1 = H, Bank 2 & 3 will be refreshed and Bank 0 & 1 can be accessible. 8,192 BREF command must be asserted to both bank group of Bank 0 & 1 and Bank 2 & 3 within the refresh period of t_{REF}. When background refresh is in progress for one bank group, BREF command must not be issue to the other bank group.

22. BACKGROUND REFRESH EXIT (BREFX)

BACKGROUND REFRESH EXIT (BREFX) command terminates internal refresh operation for 2 banks initiated by BREF command for a period of RC x t_{REFC}. SA must be High to issue BREFX command. 2 banks will be IDLE state after t_{REFC} from BREFX command. BREFX command can be issued when background refresh is in progress.

Command Truth Table of BREF and BREFX

Command	Symbol	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10 (AP)	A[9:0], A11, A12	SA	Refreshed Bank
AUTO REFRESH	REF	L	L	L	H	X	X	X	X	L	All Banks
BACKGROUND REFRESH ENTRY	BREF					L	X	L	V (RC)	H	Bank 0 & 1
						H					Bank 2 & 3
BACKGROUND REFRESH EXIT	BREFX					X	X	H	X	H	Bank 0 & 1
											Bank 2 & 3

Refresh Count (RC) Definition Table

Refresh Count (RC)	A10	A[5:9], A11, A12	A4	A3	A2	A1	A0
ILLEGAL*	L	L	L	L	L	L	L
1							H
2						H	L
3							H
4					H	L	L
5							H
6						H	L
7							H
8				H	L	L	L
9							H
10						H	L
11							H
12					H	L	L
13							H
14						H	L
15							H
16			H	L	L	L	L
17							H
18						H	L
19							H
20					H	L	L
21							H
22						H	L
23							H
24				H	L	L	L
25							H
26						H	L
27							H
28					H	L	L
29							H
30						H	L
31							H

* : A[12:0] = 000h must not be set for RC.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage Relative to V_{SS}	V_{DD},V_{DDQ}	-0.5 to +2.3	V
Input / Output Voltage Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +2.3	V
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage*1	V_{DD}, V_{DDQ}	1.7	1.8	1.9	V
	V_{SS}, V_{SSQ}	0	0	0	V
DC Input High Voltage*2	$V_{IH\ (DC)}$	$V_{DDQ} \times 0.7$	—	V_{DDQ} + 0.3	V
AC Input High Voltage*2	$V_{IH\ (AC)}$	$V_{DDQ} \times 0.8$	—	V_{DDQ} + 0.3	V
DC Input Low Voltage*3	$V_{IL\ (DC)}$	-0.3	—	$V_{DDQ} \times 0.3$	V
AC Input Low Voltage*3	$V_{IL\ (AC)}$	-0.3	—	$V_{DDQ} \times 0.2$	V
Junction Temperature	T_j	-10	—	+125	°C

*1: V_{DDQ} must be less than or equal to V_{DD}.

*2: Maximum DC voltage on input or I/O pins is V_{DDQ} + 0.3 V. During voltage transitions, inputs may positive overshoot to V_{DDQ} + 1.0V for periods of up to 3 ns.

*3: Minimum DC voltage on input or I/O pins is -0.3 V. During voltage transitions, inputs may negative overshoot to V_{SSQ} - 1.0V for periods of up to 3 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ CAPACITANCE

(T_a = + 25 °C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance, Except for WDQS, DM	C_{IN1}	1	—	2.5	pF
Input Capacitance for WDQS, DM	C_{IN2}	2	—	4	pF
I/O Capacitance	$C_{I/O}$	2	—	4	pF

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(Under recommended operating conditions unless otherwise noted)

Parameter	Symbol	Condition		Value		Unit
				Min.	Max.	
Output High Voltage	$V_{OH(DC)}$	I_{OH} = -0.1 mA		V_{DDQ} – 0.2	—	V
Output Low Voltage	$V_{OL(DC)}$	I_{OL} = 0.1 mA		—	0.2	V
Input Leakage Current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0 V		– 5	5	µA
Output Leakage Current	I_{LO}	0 V ≤ V_{IN} ≤ V_{DDQ}, Data out disabled		– 5	5	µA
Operating One Bank Active-Precharge Current	I_{DD0}	t_{RC} = t_{RC} min, t_{CK} = t_{CK} min, CKE = V_{IH}, $\overline{CS}$ = V_{IH} addresses inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	65	mA
			Tj ≤ + 125 °C	—	75	mA
Precharge Standby Current	I_{DD2P}	All banks idle, CKE = V_{IL}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	6	mA
			Tj ≤ + 125 °C	—	9	
	I_{DD2N}	All banks idle, CKE = V_{IH}, $\overline{CS}$ = V_{IH}, t_{CK} = t_{CK} min, address and control inputs are SWITCHING; data bus inputs are STABLE	Tj ≤ + 105 °C	—	15	mA
			Tj ≤ + 125 °C	—	20	mA
Operating Burst Read Current	I_{DD4R}	One bank active, BL = 4, t_{CK} = t_{CK} min, Output pin open, Gapless data, address inputs are SWITCHING; 50% data change each burst transfer		—	300	mA
Operating Burst Write Current	I_{DD4W}	One bank active, BL = 4, t_{CK} = t_{CK} min, Gapless data, address inputs are SWITCHING; 50% data change each burst transfer		—	380	mA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RFC} min, t_{CK} = t_{CK} min, CKE = V_{IH}, address and control inputs are SWITCHING; data bus inputs are STABLE		—	120	mA

(Continued)

(Continued)

Parameter	Symbol	Condition	Value		Unit
			Min.	Max.	
Self Refresh Current	I_{DD6}	CKE = V_{IL}, $\overline{CS}$ = V_{IL}, address and control inputs are STABLE; data bus inputs are STABLE	—	6	mA
Deep Power Down Current	I_{DD8}	address and control inputs are STABLE; data bus inputs are STABLE	—	300	µA

Notes:
- All voltages are referenced to V_{SS}.
- After power on, initialization following power-up timing is required. DC characteristics are guaranteed after the initialization.
- I_{DD} depends on the output termination or load condition, clock cycle rate, signal clocking rate. The specified values are obtained with the output open condition.

2. AC Characteristics

(Under recommended operating conditions unless otherwise noted)*1, *2

Parameter			Symbol	Value		Unit
				Min.	Max.	
DQ Output Access Time from CK/$\overline{CK}$ (t_{CK} = t_{CK} min)*3, *4, *7			t_{AC}	2	6	ns
RDQS Output Access Time from CK/$\overline{CK}$ *3, *4			t_{DQSCK}	2	6	ns
Clock High Level Width *3			t_{CH}	2	—	ns
Clock Low Level Width *3			t_{CL}	2	—	ns
Delay between CK and $\overline{CK}$ *4			t_{DC}	0.45	0.55	t_{CK}
Clock Cycle Time	CL = 2		t_{CK}	15	—	ns
	CL = 3			7.4		
	CL = 4	Tj ≤ + 105 °C		4.6		
		Tj ≤ + 125 °C		5		
DQ and DM Input Setup Time*3		Tj ≤ + 105 °C	t_{DS}	0.4	—	ns
		Tj ≤ + 125 °C		0.5	—	ns
DQ and DM Input Hold Time*3		Tj ≤ + 105 °C	t_{DH}	0.4	—	ns
		Tj ≤ + 125 °C		0.5	—	ns
DQ and DM Input Pulse Width			t_{DIPW}	0.35	—	t_{CK}
Address and Control Input Setup Time *3			t_{IS}	0.9	—	ns
Address and Control Input Hold Time *3			t_{IH}	0.9	—	ns
Address and Control Input Pulse Width			t_{IPW}	0.6	—	t_{CK}
DQ Low-Z Time from CK/$\overline{CK}$ *3, *5			t_{LZ}	0	—	ns
DQ High-Z Time from CK/$\overline{CK}$ *3, *5, *6			t_{HZ}	—	6	ns
RDQS to DQ Skew *4			t_{DQSQ}	—	0.4	ns
DQ Output Hold Time from RDQS *3, *4			t_{QH}	t_{DC} – 0.5	—	ns
WRIT Command to 1st WDQS Latching Transition			t_{DQSS}	0.75	1.25	t_{CK}
WDQS Input High Level Width			t_{DQSH}	0.35	—	t_{CK}
WDQS Input Low Level Width			t_{DQSL}	0.35	—	t_{CK}
WDQS Falling Edge to CK Setup Time			t_{DSS}	0.2	—	t_{CK}
WDQS Falling Edge Hold Time from CK			t_{DSH}	0.2	—	t_{CK}
MRS Command Period			t_{MRD}	2	—	t_{CK}
Write Preamble Setup Time			t_{WPRES}	0	—	ns
Write Postamble Time			t_{WPST}	1	—	t_{CK}

(Continued)

(Continued)

(Under recommended operating conditions unless otherwise noted)*1, *2

Parameter		Symbol	Value		Unit
			Min.	Max.	
ACT to PRE, MPRE, PALL Command Period *7		t_{RAS}	37	8000	ns
ACT, MACT to ACT, MACT Command Period (Same Bank) *7		t_{RC}	59.2	—	ns
REF to ACT, REF Command Period		t_{REFC}	100	—	ns
ACT to READ or WRIT Command Period		t_{RCD}	20	—	ns
Precharge Period *7		t_{RP}	18	—	ns
ACT, MACT to ACT, MACT Command Period (Other Bank)*8		t_{RRD}	9.2	—	ns
Write Recovery Time		t_{WR}	12	—	ns
Data Input to ACT, REF Command Period	CL = 2	t_{DAL}	1 CLK + t_{RP}	—	ns
	CL = 3		2 CLK + t_{RP}		
	CL = 4		3 CLK + t_{RP}		
Internal Write to READ Command Delay		t_{WTR}	9.2	—	ns
Average Refresh Period *9	Tj ≤ + 105°C	t_{REFI}	—	7.8	µs
	Tj ≤ + 125°C			2.0	
Average Periodic Refresh Interval	Tj ≤ + 105°C	t_{REF}	—	64	ms
	Tj ≤ + 125°C			16.7	
Transition Time*10		t_T	—	1	ns

* 1: AC characteristics are measured after the Power up initialization procedure.

* 2: $V_{DD} \times 0.5$ is the reference level for 1.8 V I/O for measuring timing of input/output signals.

* 3: If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) − 0.5] ns should be added to t_{AC} (Max), t_{DQSCK} (Max) and t_{HZ} (max) spec values, [(t_T/2) − 0.5] ns should be subtracted from t_{LZ} (Min) and t_{QH} (Min) spec values, and (t_T - 1.0) ns should be added to t_{CH} (Min), t_{CL} (Min), t_{IS} (Min), t_{IH} (Min), t_{DS} (Min) and t_{DH} (Min) spec values.

* 4: The data valid window is defined as t_{QH} - t_{DQSQ}. The data valid window depends on t_{DC} which is defined between rising edge of CK and rising edge of $\overline{CK}$. The data valid window is guaranteed when t_{DC} is satisfied.

* 5: t_{AC}, t_{DQSCK}, t_{LZ} and t_{HZ}, are measured under output load circuit shown in " 3. Measurement Condition of AC Characteristics" in " ■ ELECRTRICAL CHARACTERISTICS" and Driver Strength (DS) = Normal, Pre Driver Strength (PDS) = Fast are assumed.

* 6: Specified where output buffer is no longer driven.

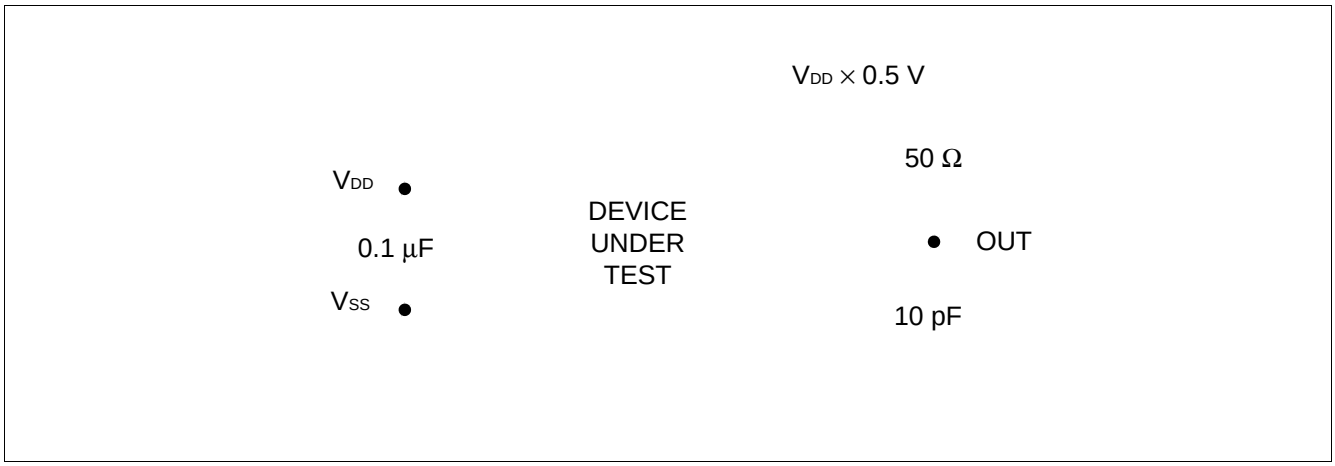
* 7: The sum of actual clock count of t_{RAS} and t_{RP} must be equal or greater than specified minimum t_{RC}.

* 8: t_{RRD} is applied to ACT (MACT) to BREF, ACT (MACT) to BREFX, BREF to ACT (MACT) and BREFX to ACT (MACT). Refer to the "■ BANK OPERATION COMMAND TABLE".

* 9: This value is for reference only.

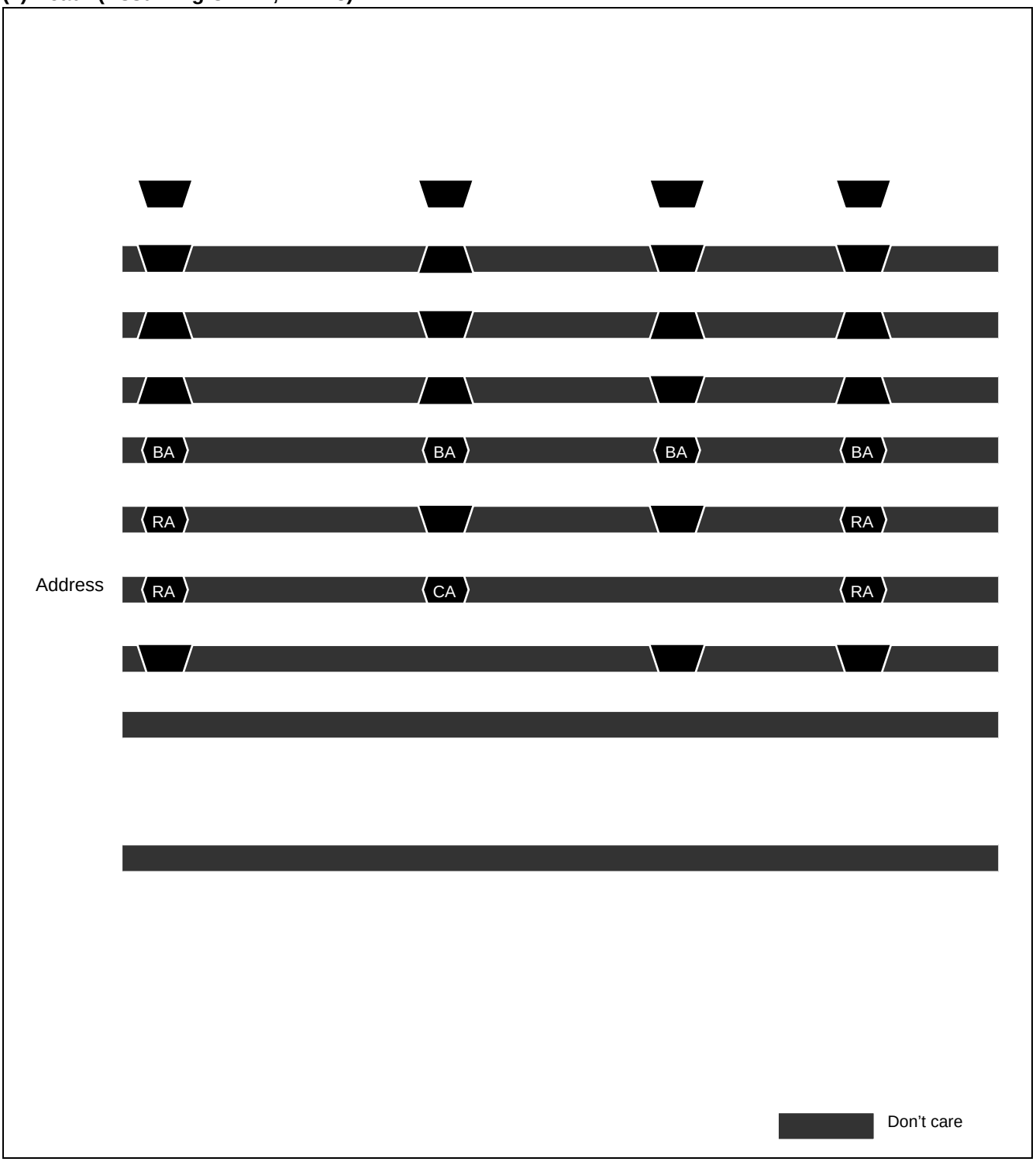
* 10: Transition times are measured between V_{IH} (AC) min and V_{IL} (AC) max.

3. Measurement Condition of AC Characteristics



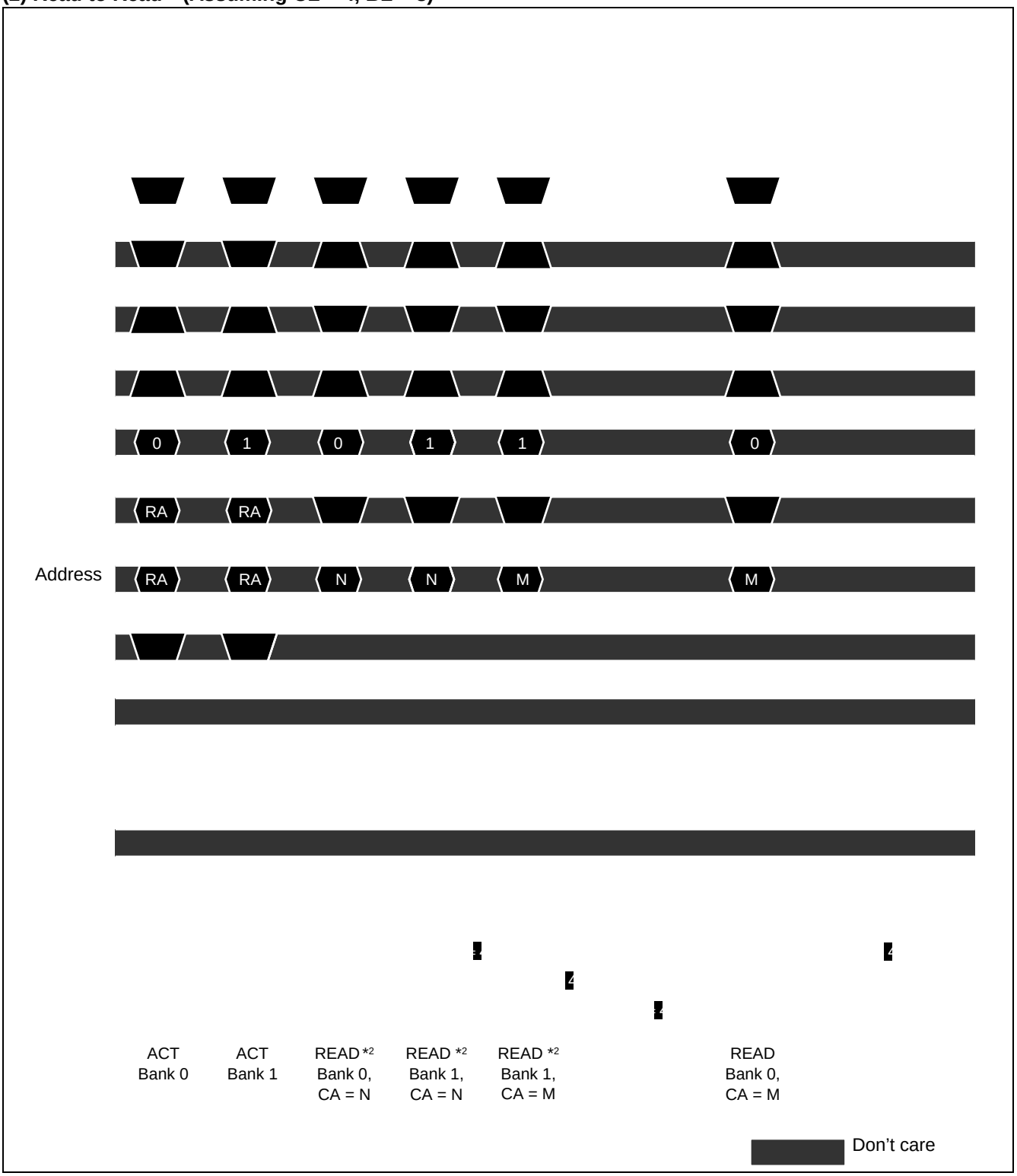
■ TIMING DIAGRAMS

(1) Read* (Assuming CL = 4, BL = 8)



* : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

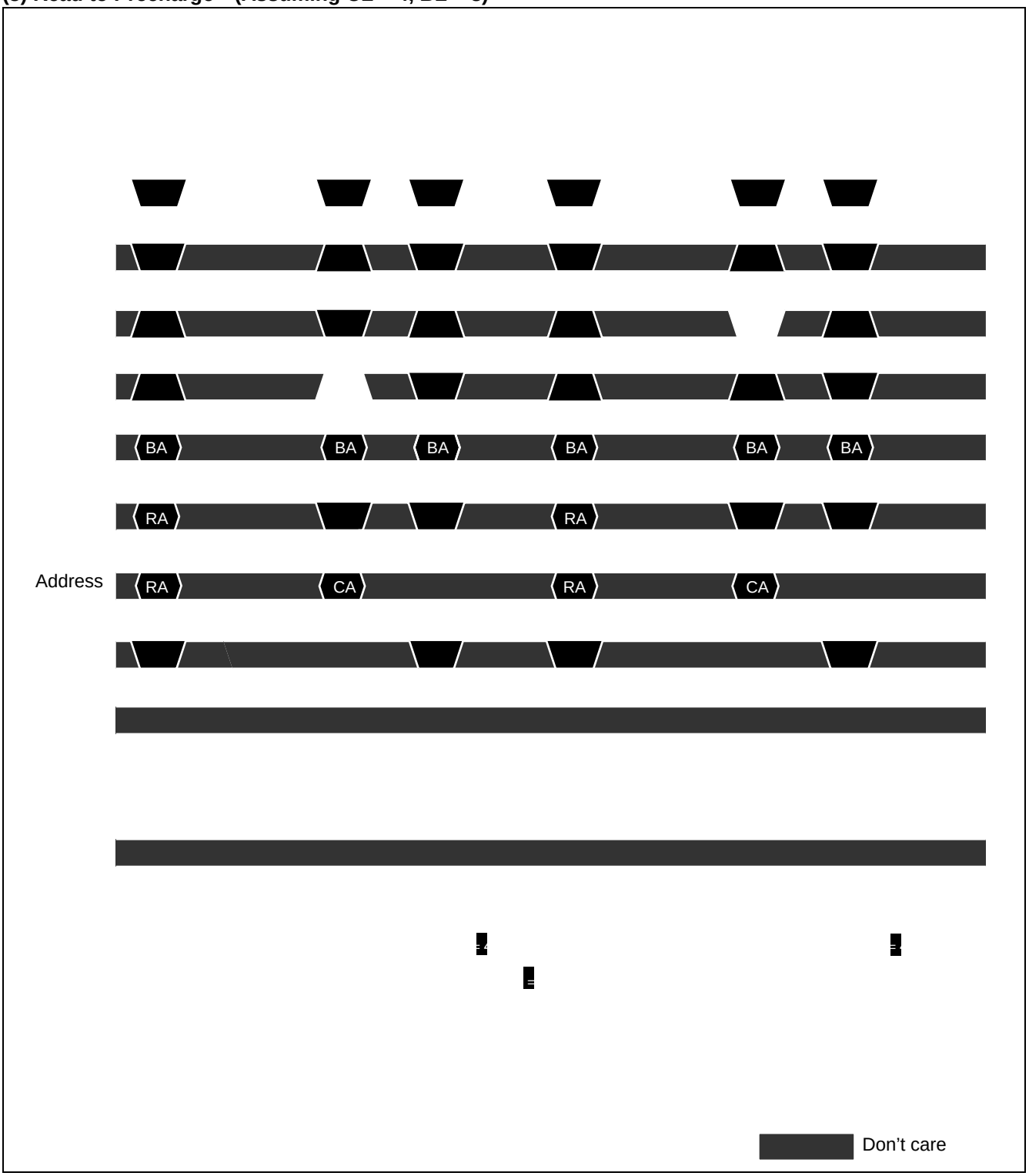
(2) Read to Read*1 (Assuming CL = 4, BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Previous burst read can be interrupted by subsequent burst read.

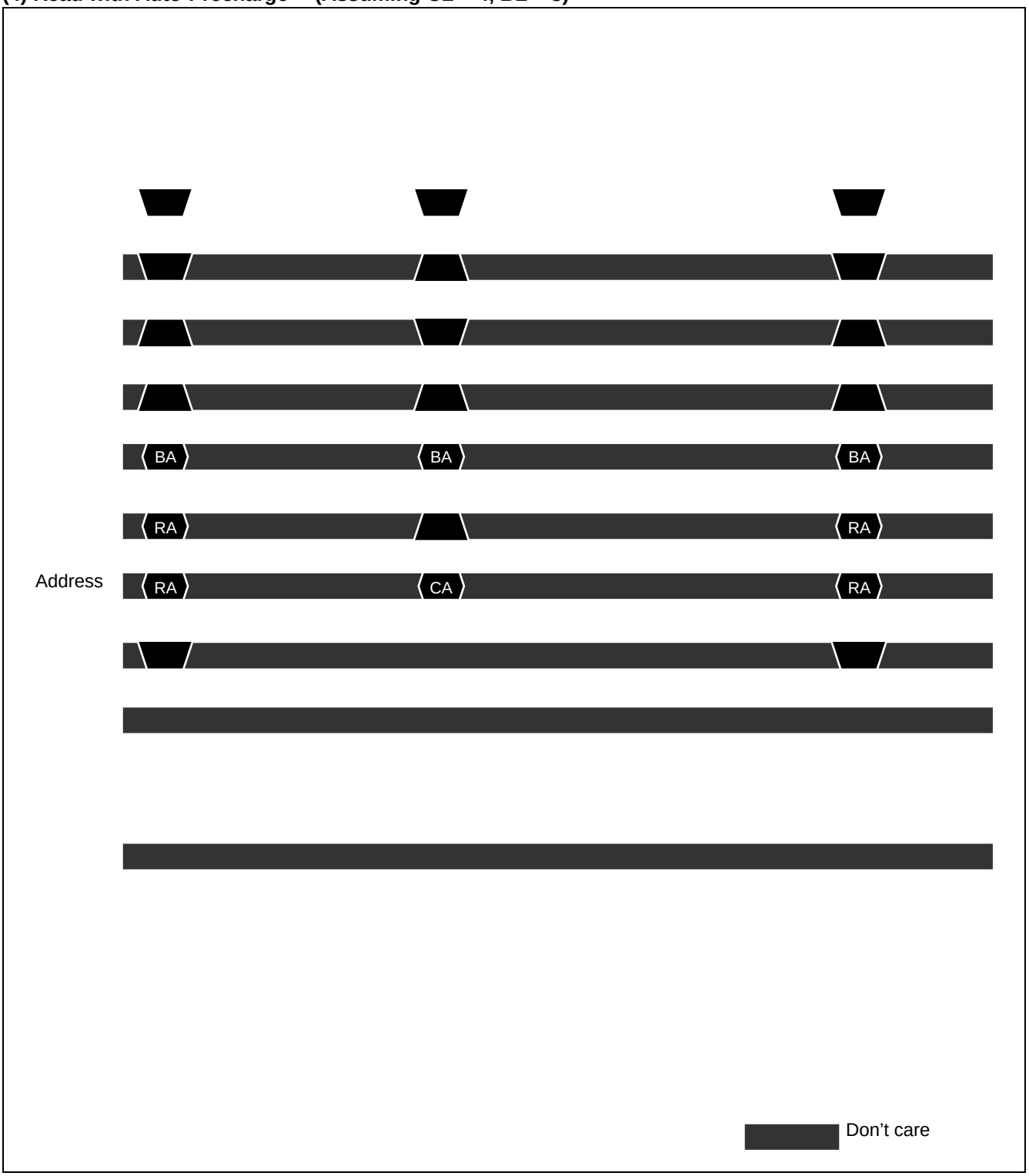
(3) Read to Precharge *1(Assuming CL = 4, BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst read operation can be terminated by PRE command. All DQ pins become High-Z after CL from PRE command.

(4) Read with Auto-Precharge *1 (Assuming CL = 4, BL = 8)

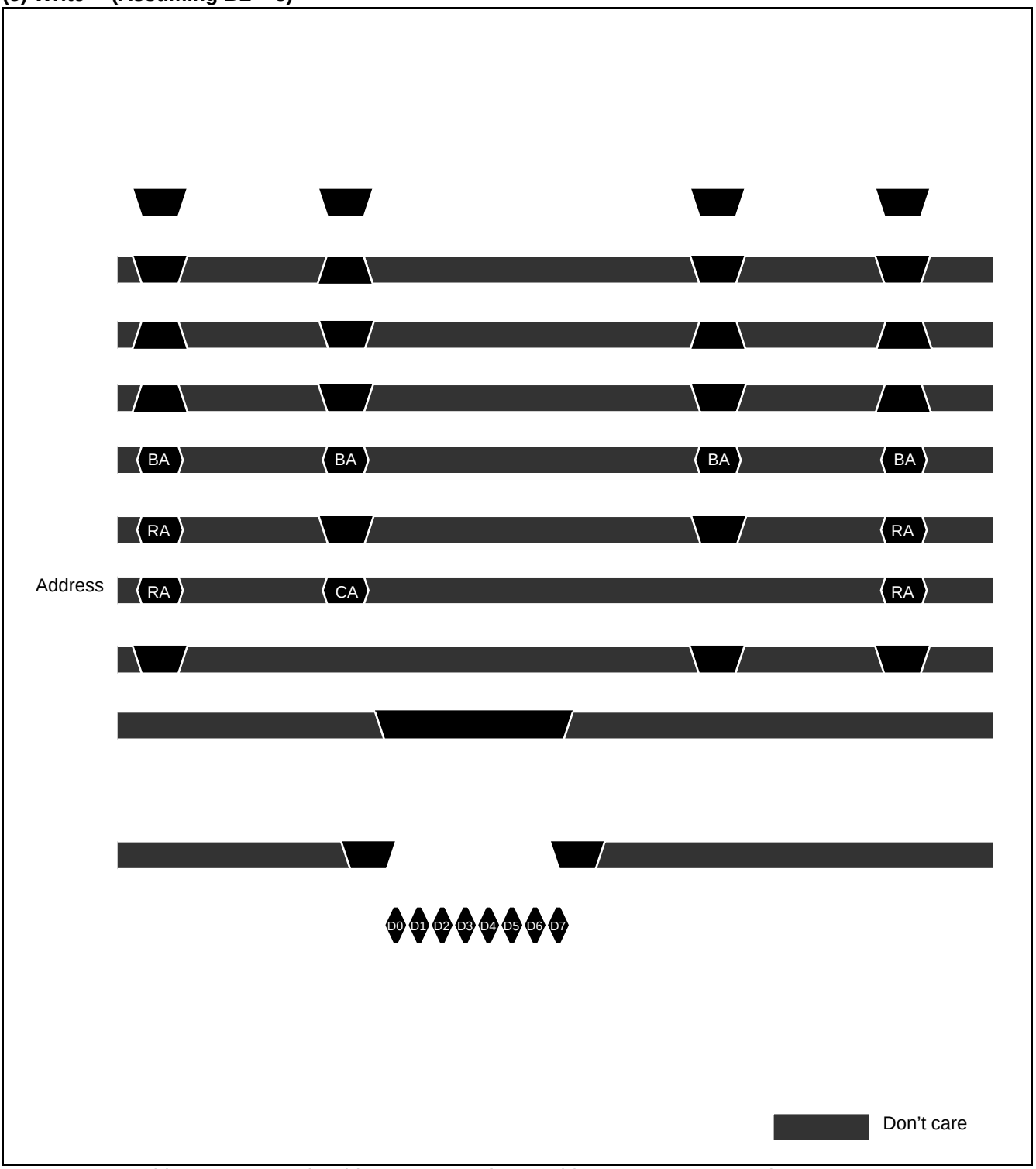


*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Internal precharge operation starts after BL/2 from READA command. t_{RAS} must be satisfied.

*3: Next ACT command can be issued after BL/2 + t_{RP} from READA command. t_{RC} must be satisfied.

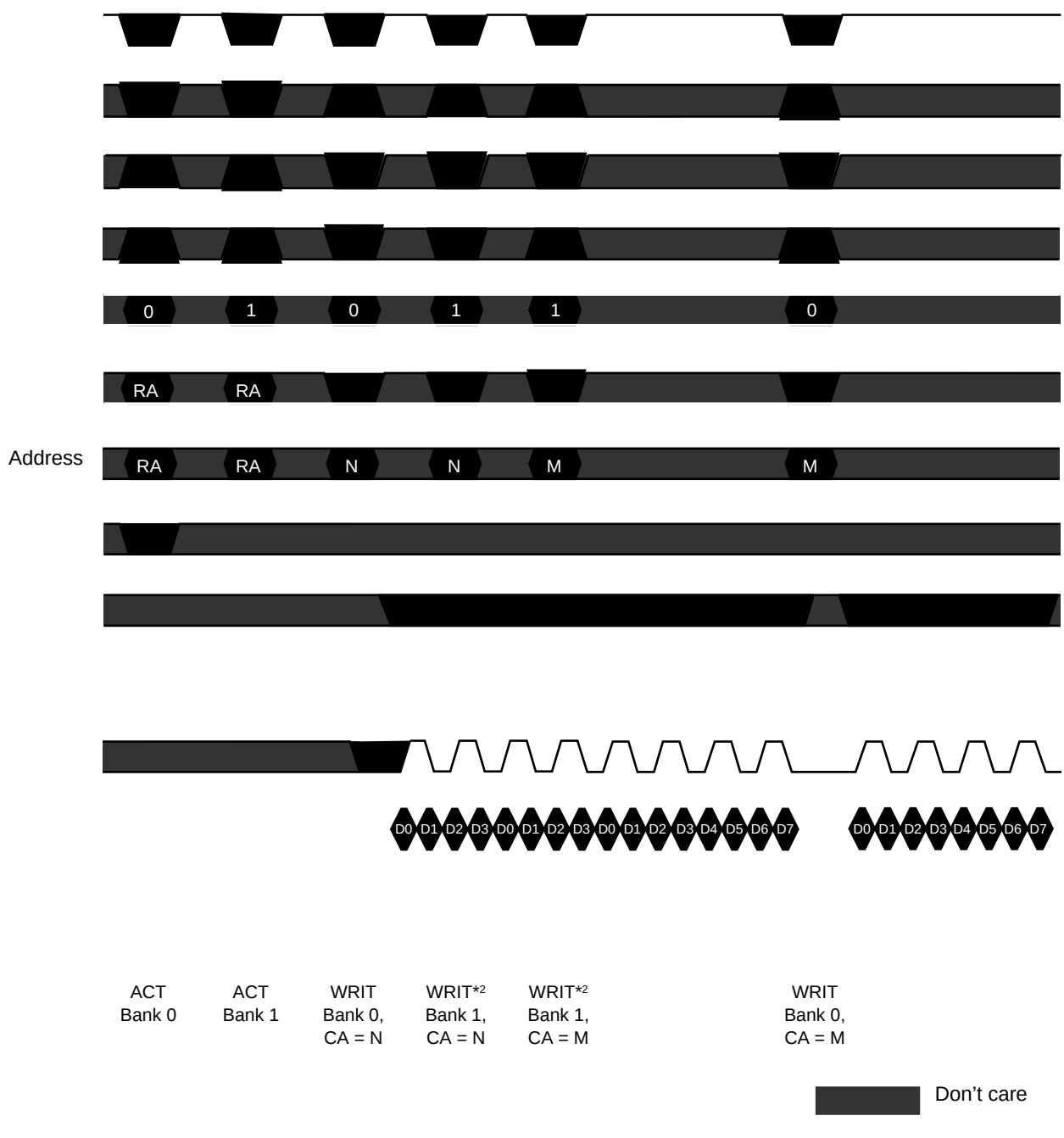
(5) Write *1 (Assuming BL = 8)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: Burst write operation should not be terminated by PRE command. PRE can be issued after 1 + BL/2 + t_{WR} from WRIT command.

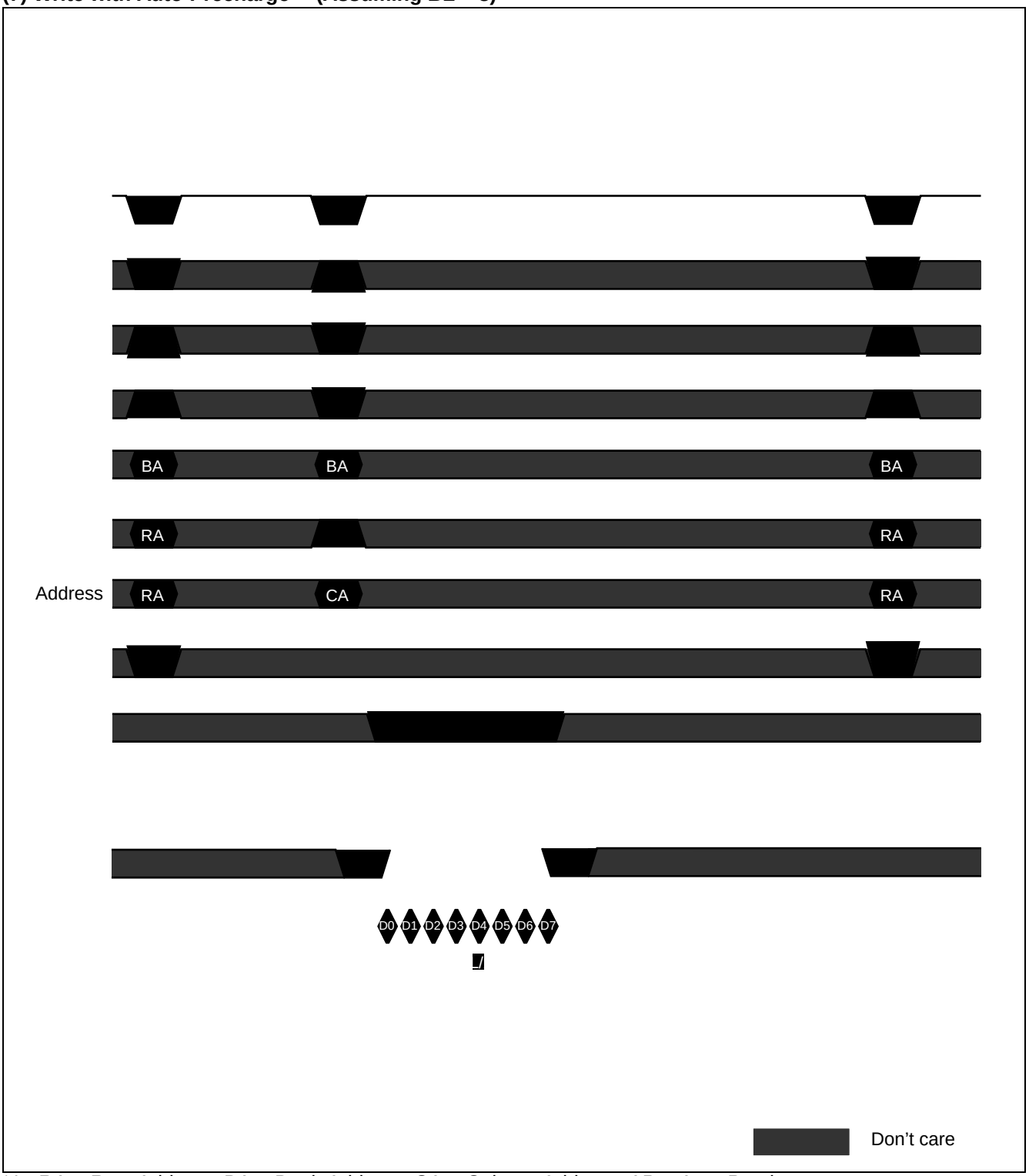
(6) Write to Write *1 (Assuming BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2 : Previous burst write can be interrupted by subsequent burst write.

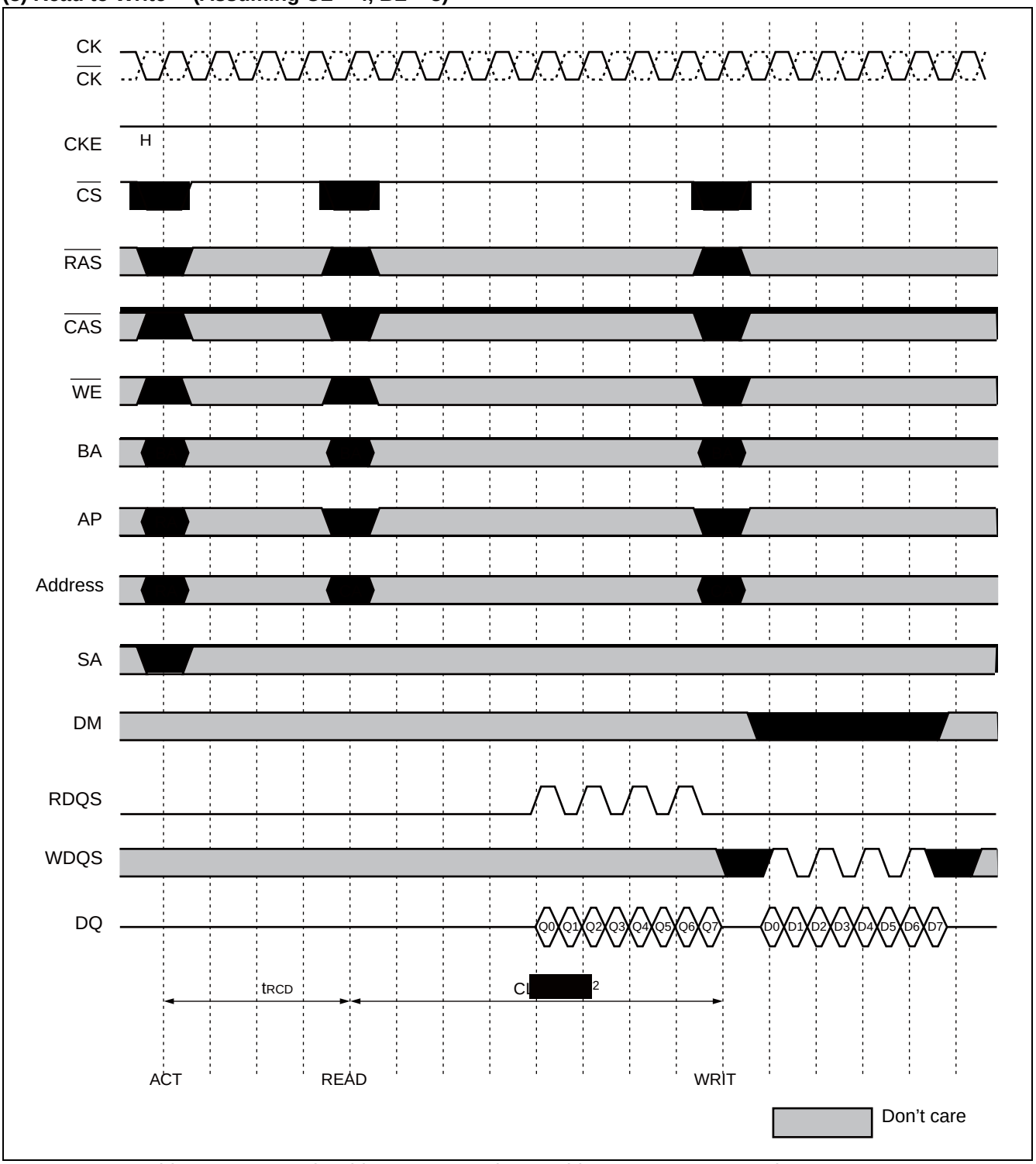
(7) Write with Auto-Precharge *1 (Assuming BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

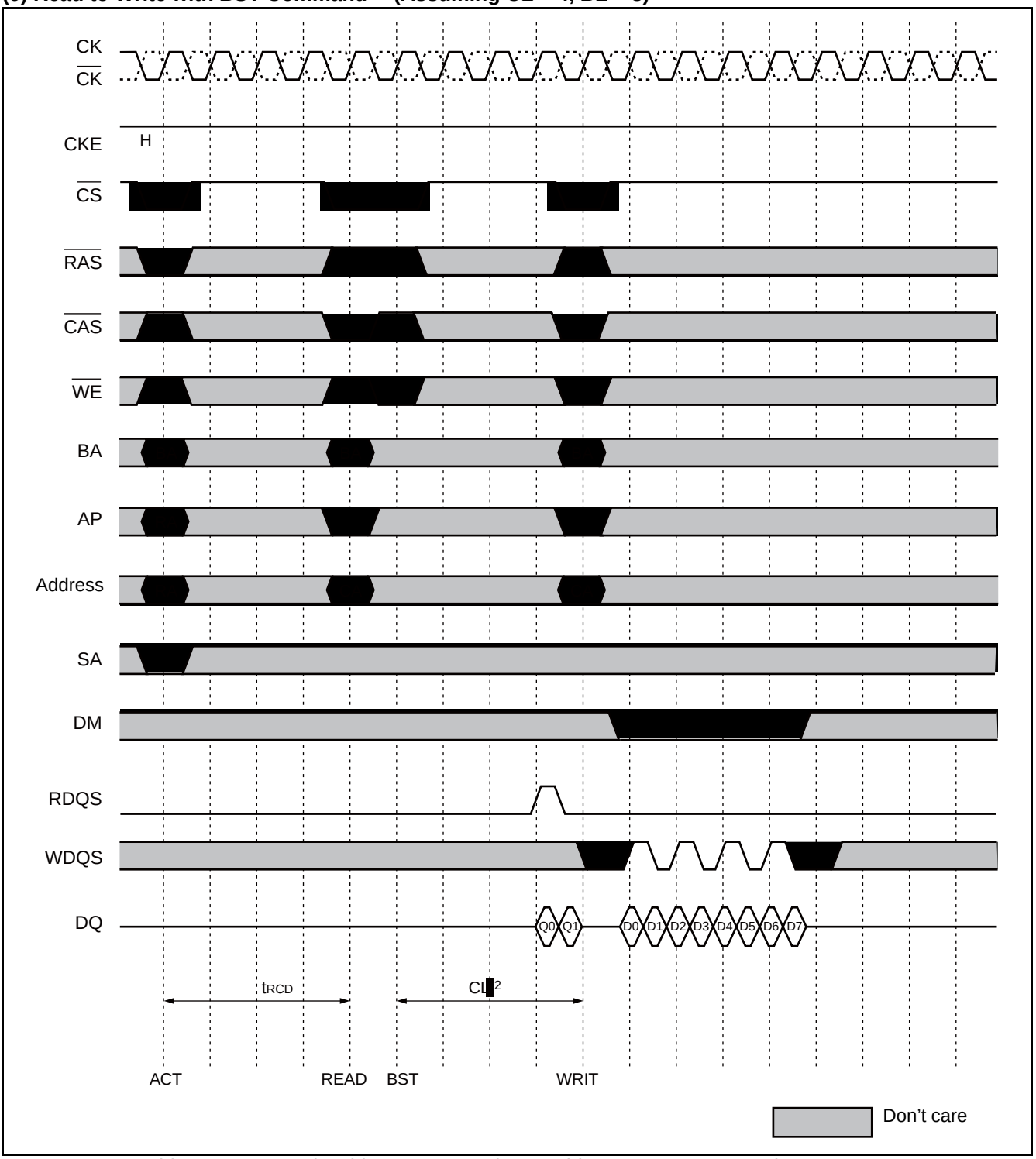
*2 : Next ACT command can be issued after 1 + BL/2 + t_{DAL} (Min) from WRITA command. t_{RC} must be satisfied.

(8) Read to Write *1 (Assuming CL = 4, BL = 8)



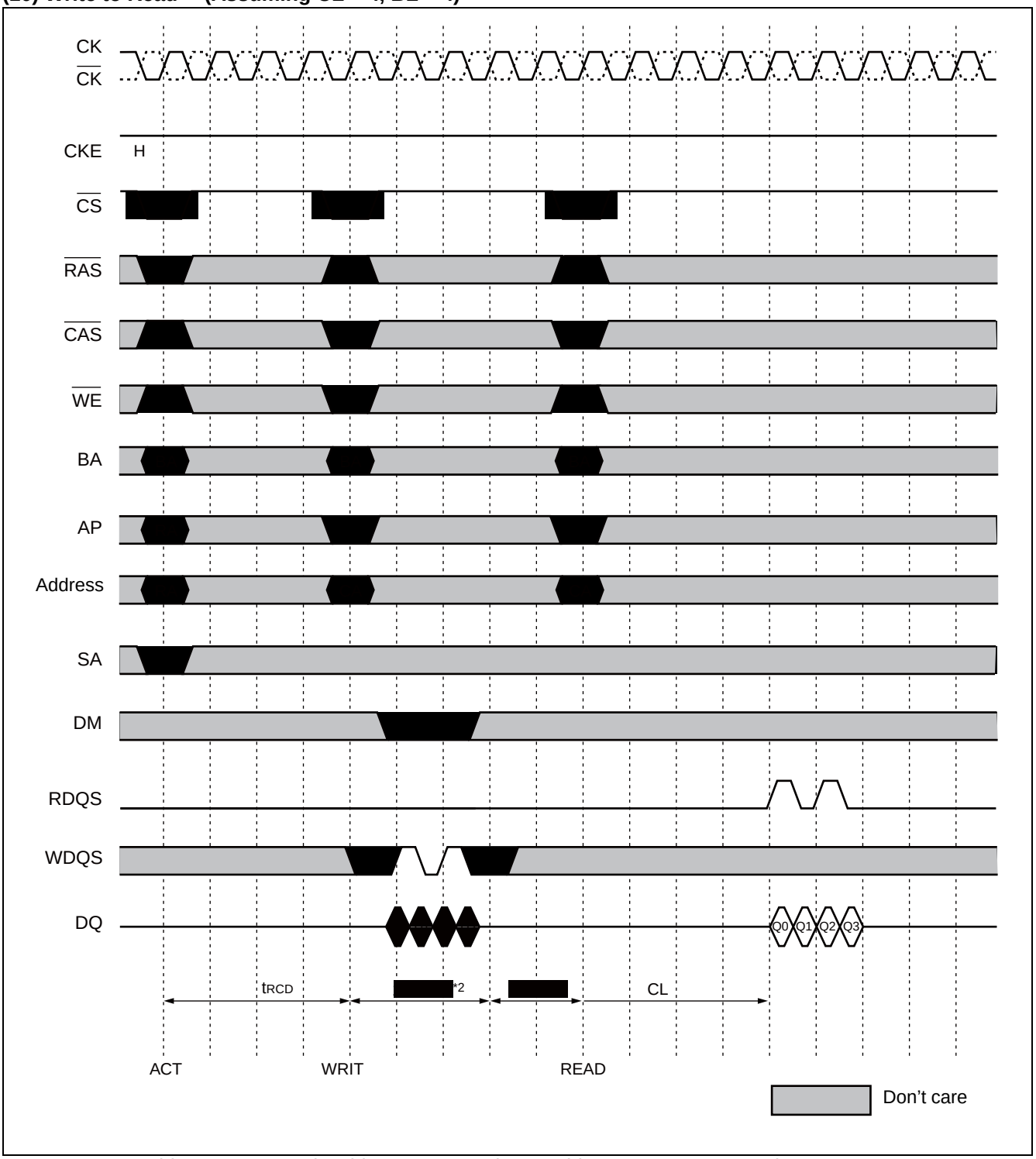
*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge
*2 : WRIT command can be issued after CL + BL/2 after READ command.

(9) Read to Write with BST Command *1 (Assuming CL = 4, BL = 8)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge
*2 : WRIT command can be issued after CL from burst read termination by BST command.

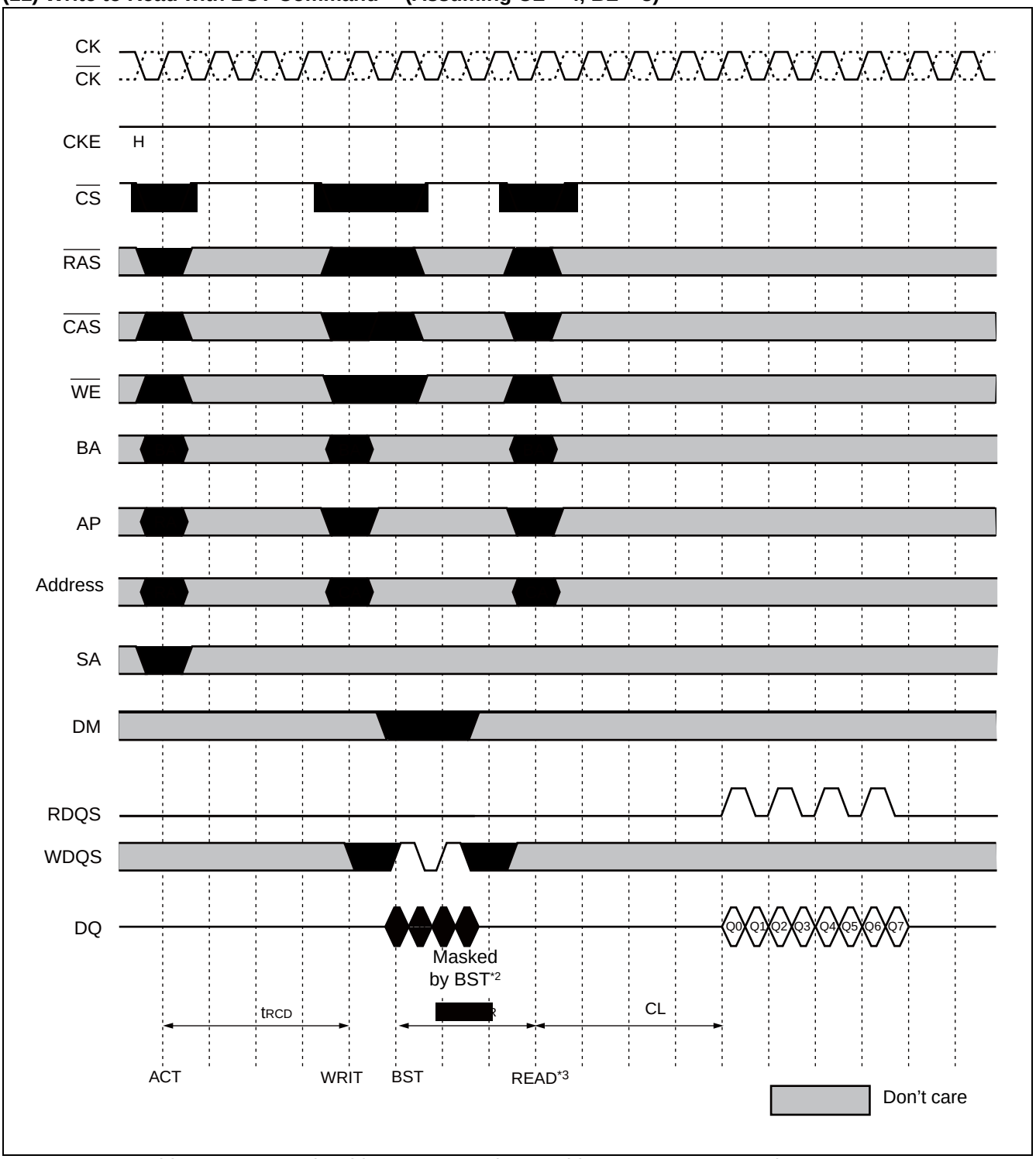
(10) Write to Read *1 (Assuming CL = 4, BL = 4)



*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

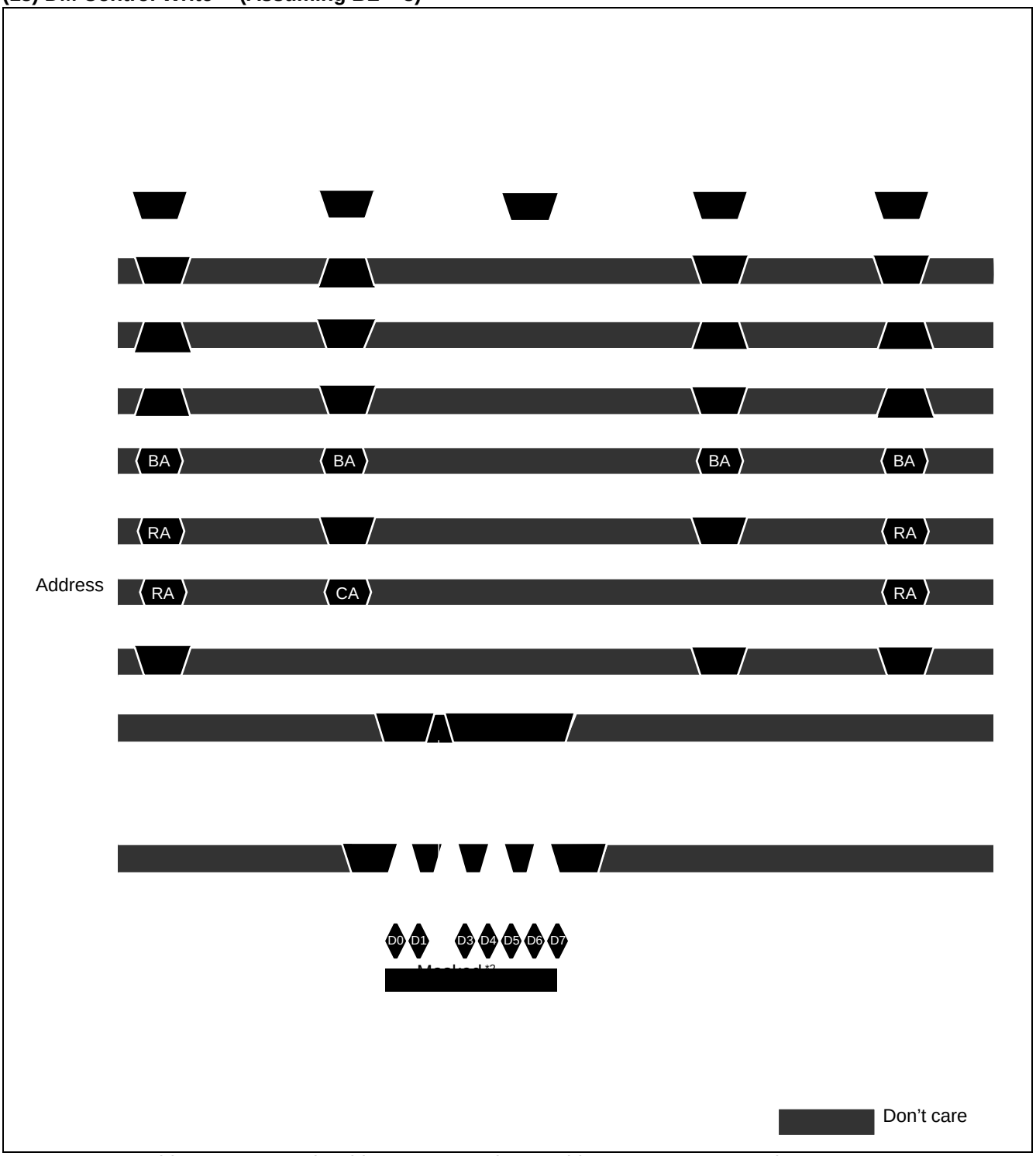
*2 : READ command can be issued after 1 + BL/2 + t_{WTR} from WRIT command.

(11) Write to Read with BST Command *1 (Assuming CL = 4, BL = 8)



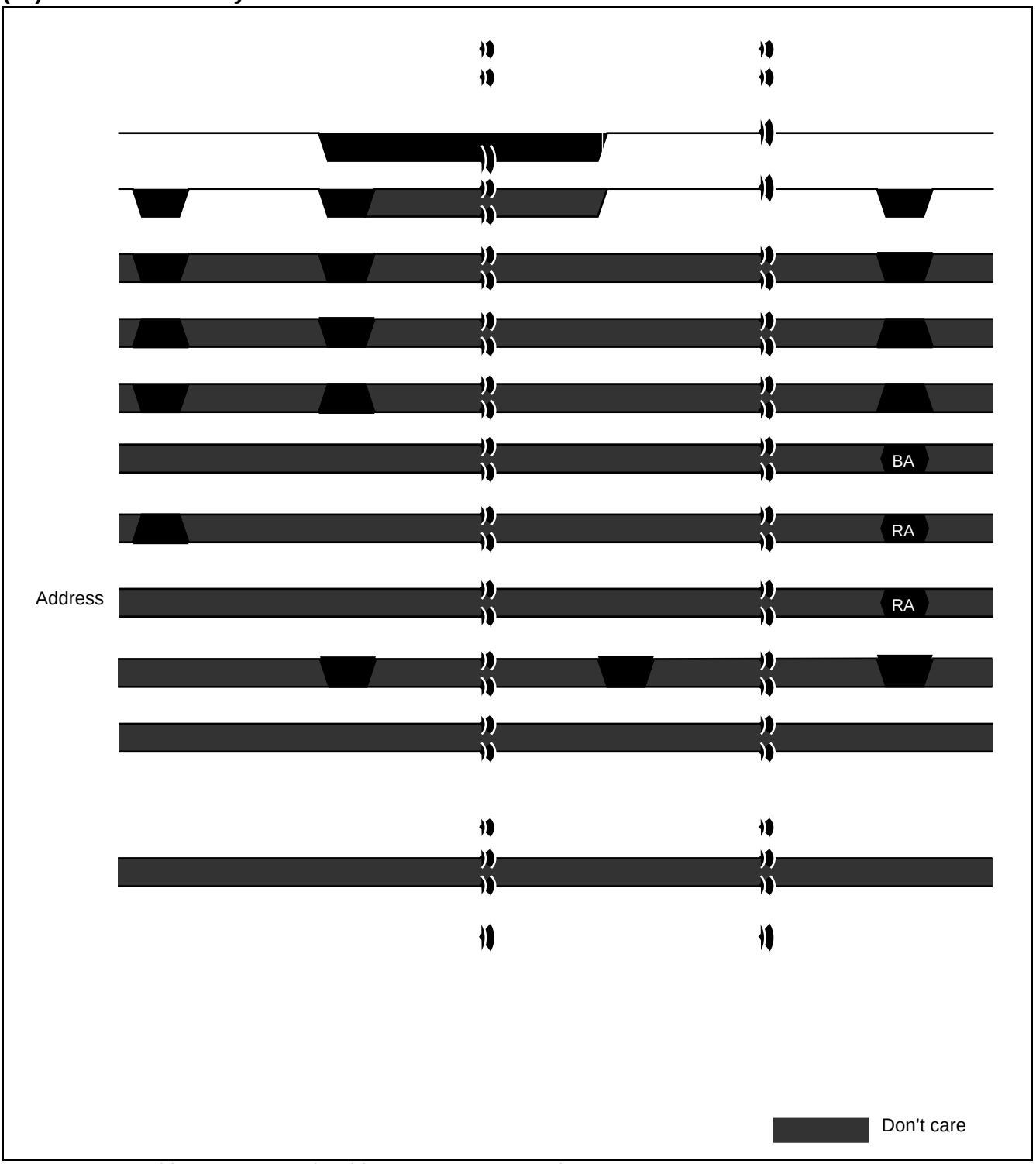
*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge
*2 : The data input after 1 clock from BST command will be masked.
*3 : READ command can be issued after 1 + t_{WTR} from burst write termination by BST command.

(13) DM Control Write *1 (Assuming BL = 8)



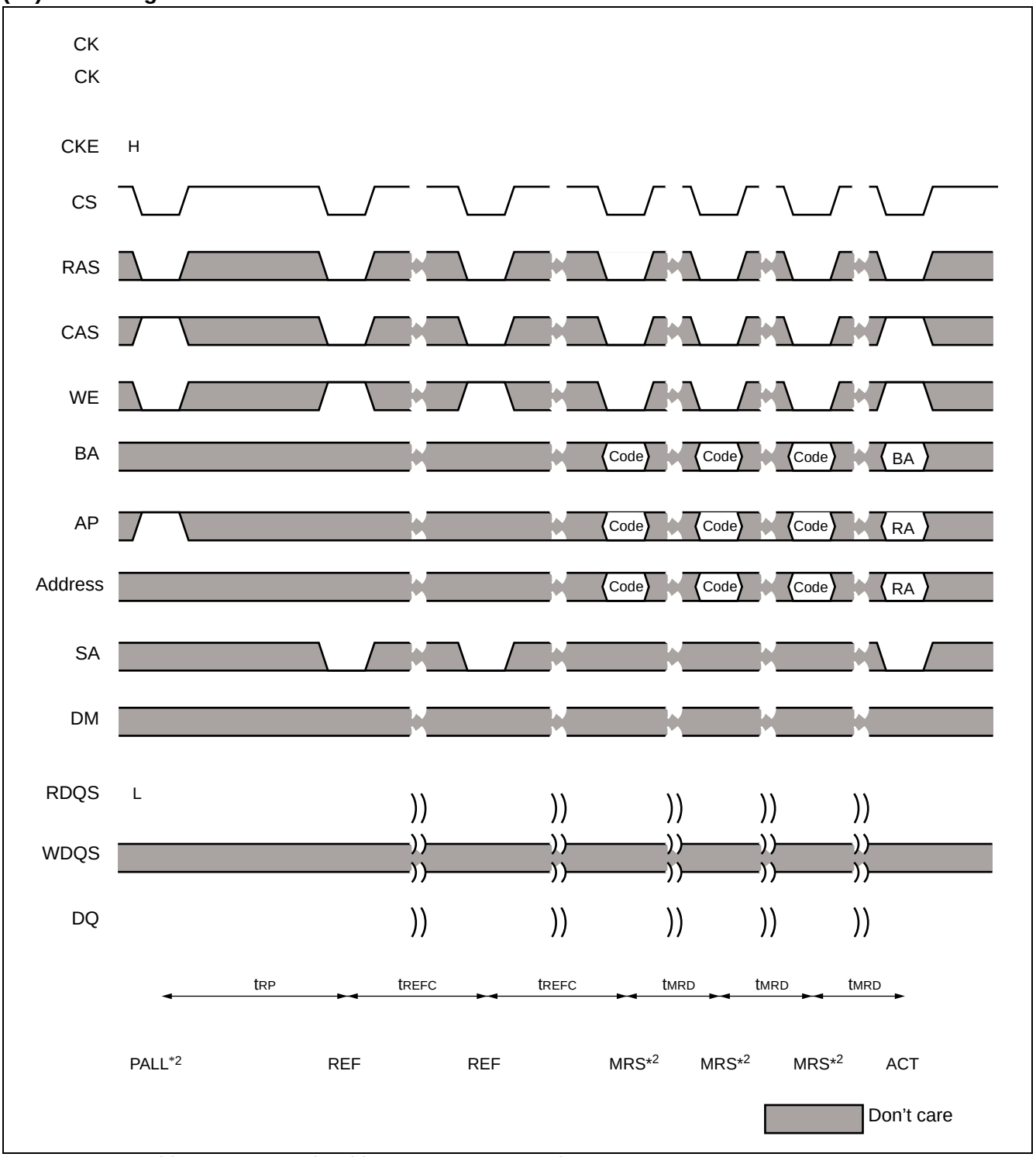
*1 : RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge
*2 : When DM is registered High, the corresponding data will be masked.

(15) Self Refresh Entry and Exit *1



*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge
*2 : All banks must be precharged prior to SELF REFRESH ENTRY (SELF) command.
*3 : SELF REFRESH EXIT (SELFX) command can be latched at the CK rising edge.
*4 : Either NOP or DESL command can be used during t_{REFC} period.
*5 : CKE should be held High during t_{REFC} period after SELFX command.

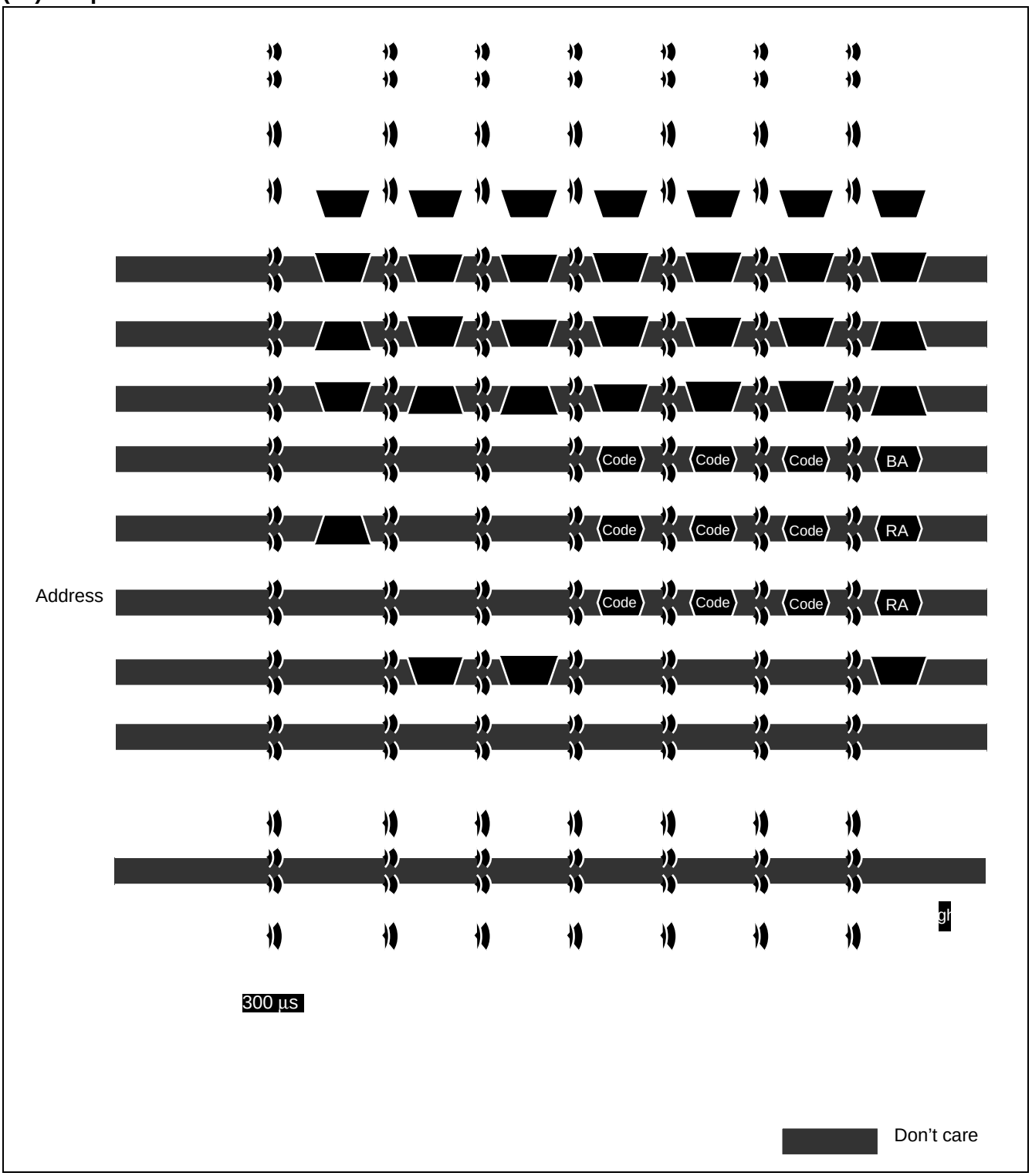
(16) Mode Register Set*1



*1 : RA = Row Address, BA = Bank Address, AP = Auto Precharge

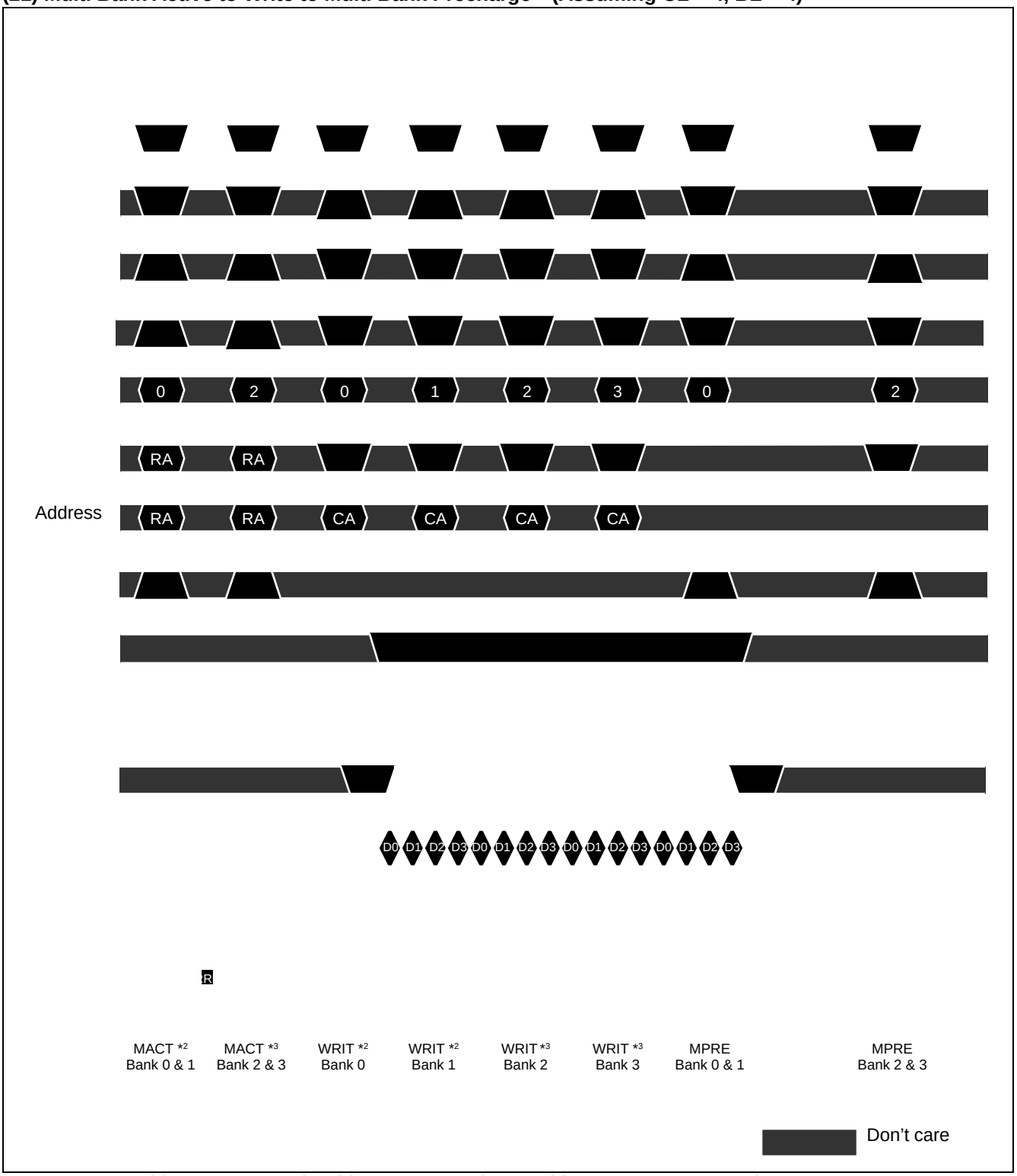
*2 : MODE REGISTER SET (MRS) command must be asserted after all banks have been precharged and all DQ are in High-Z.

(19) Deep Power Down Exit *1



*1: RA = Row Address, BA = Bank Address, AP = Auto Precharge
*2: Power up initialization procedure must be performed after DPDX command.

(21) Multi Bank Active to Write to Multi Bank Precharge*1 (Assuming CL = 4, BL = 4)



*1: RA = Row Address, BA = Bank Address, CA = Column Address, AP = Auto Precharge

*2: If MACT command is issued to Bank 0, 1st WRIT command must be issued to Bank 0 followed by 2nd WRIT command to Bank 1.

*3: If MACT command is issued to Bank 2, 1st WRIT command must be issued to Bank 2 followed by 2nd WRIT command to Bank 3.

MEMO

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