iC-LV
5-BIT OPTO ENCODER

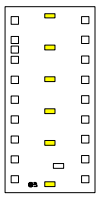
FEATURES

- High synchronism and technical reliability due to monolithic construction featuring on-chip photosensors
- Scanning with constant-light evaluation at a pitch of 600 µm
- Photocurrent amplifiers with high cut-off frequency
- Adjustable illumination control with 40 mA LED driver ensures constant receiver power over life
- Monitoring of safe operating range with alarm message (eg. EOL message on LED control error)
- Serial data output via extended SSI interface
- Parallel 5 bit data output as Gray or binary code
- Adjustable phase of MSB track selects for sense of Gray code direction
- Selectable all-track bit inversion
- Supports chain circuits of multiple devices including synchronisation options
- Integrated test aids
- Single 4 to 5.5 V supply, low power consumption
- Extended operating temperature range of -40 to 125 °C

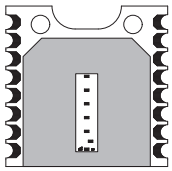
APPLICATIONS

- Scanning with constant-light evaluation for optical encoders
- Low-res singleturn encoders
- Multiturn encoders

CHIP

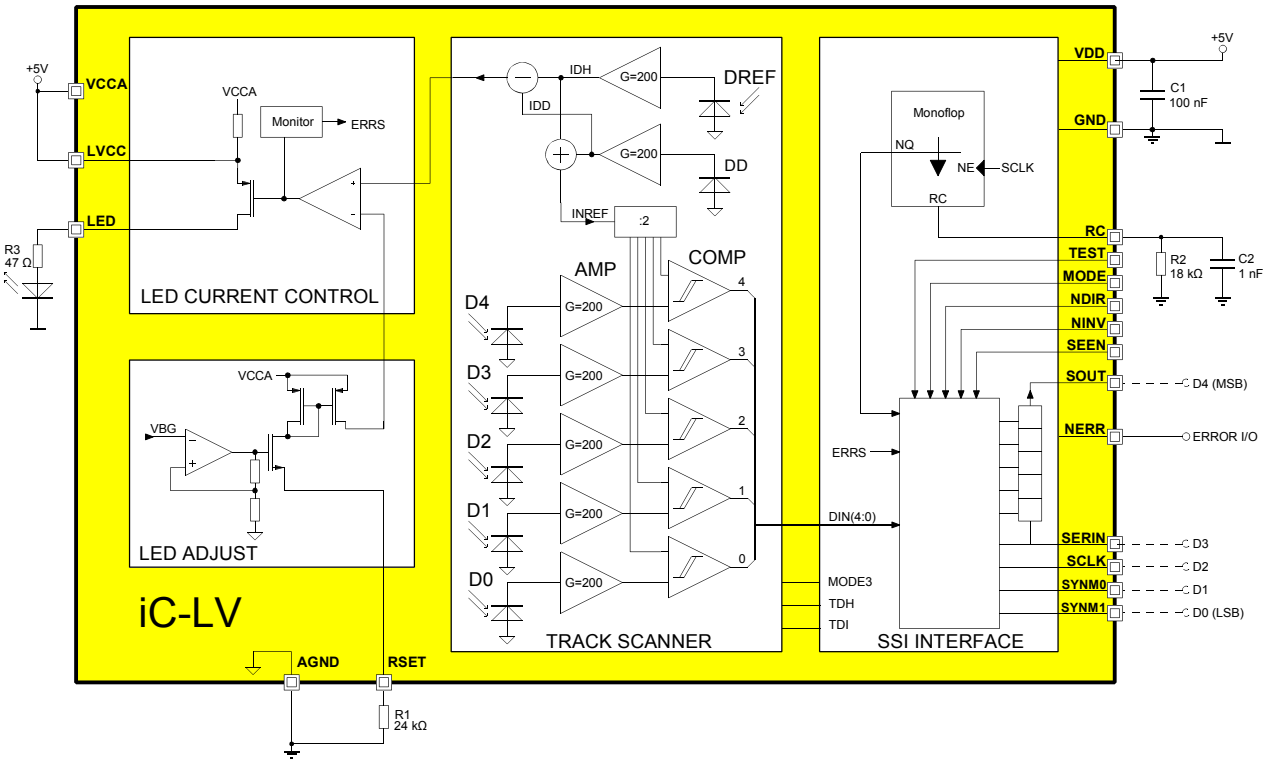


Chip
1.68 mm x 3.5 mm



16-pin BLCC
7.0 mm x 7.0 mm

BLOCK DIAGRAM



DESCRIPTION

iC-LV is an optoelectronic encoder IC for absolute linear and angle measuring systems such as glass scales and shaft encoders, for example. Photosensors, amplifiers and comparators for 5 tracks at a pitch of 600 µm and a reference photosensor operating the LED power control are monolithically integrated on the chip.

The internal comparator outputs switch to high when the amplified photocurrents exceed a given threshold (constant light evaluation). This threshold can be adjusted using an external resistor at RSET; alternatively, if RSET is not wired an internal resistor is used.

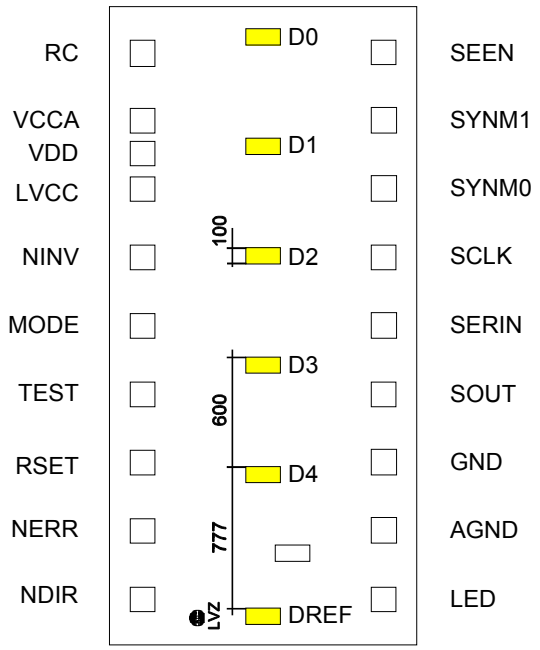
The internal or external resistor also establishes a setpoint for the LED current control which irrespective of temperature or the effects of aging keeps the optical receive power constant. A driver stage enables either a transmitting LED with a series resistor to be directly connected to the device or operates an external transistor to generate higher currents.

Track information can be read out in parallel (either in Gray or binary code) or serially via an SSI protocol. Here, any number of iC-LVs can be cascaded and synchronized with one another; data is then output as a binary word (requiring Gray code discs).

A watchdog generates an alarm message via the error output if the LED current control range is exceeded. The open-drain error output can be wired to a bus; the signal is then low active. The serial data output can also be complemented by the error bit.

All inputs and outputs are protected against destruction by ESD. Two different test modes can be selected by pin and permit a complete test of functions with the exception of the photosensors.

CHIP LAYOUT



PAD DESCRIPTION

Name	Function
RC	RC Network for SSI Monoflop (wiring is optional)
VCCA	+4...+5.5 V Analog Supply Voltage
VDD	+4...+5.5 V Digital Supply Voltage
LVCC	+4...+5.5 V LED Driver Supply Voltage
NINV	Bit-wise Inversion Input (low active)
MODE	Operating Mode Selection Input
TEST	Test Mode Enable Input (high active)
RSET	LED Power Control Adjustment (wiring is optional)
NERR	Error Output (low active)
NDIR	Reversal of Rotation Dir. Input (low active)
SEEN	Serial Error Bit Enable Input (high active)
SYNM1	Synchronisation Mode Input / Data Output D0
SYNM0	Synchronisation Mode Input / Data Output D1
SCLK	Clock Input (SSI) / Data Output D2
SERIN	Serial Data Input (SSI) / Data Output D3
SOUT	Serial Data Output (SSI) / Data Output D4
GND	Digital Ground
AGND	Analog Ground
LED	LED Power Control Output (high-side current source)

OPERATING MODES and PIN FUNCTIONS

Pin	Parallel Output Mode MODE = 0 TEST = 0	Serial Output Mode MODE = 1 TEST = 0 SYNM0 = X SYNM1 = 1 No Sync / No Sync Binary	Serial Output Mode MODE = 1 TEST = 0 SYNM0 = X SYNM1 = 0 Sync Out / SSI Out	Analog Test Mode MODE = 0 TEST = 1	Digital Test Mode MODE = 1 TEST = 1 SYNM0 = X SYNM1 = 1 No Sync	Digital Test Mode MODE = 1 TEST = 1 SYNM0 = X SYNM1 = 0 Sync Out / SSI Out
LED	LED Power Control Output (high-side current source)					
AGND	Analog Ground (reference for RC and RSET attachments)					
GND	Digital Ground					
SOUT	Data Output D4 (MSB)	Serial Data Output (SSI Interface)		Signal Output for Switch Threshold Measurement	Serial Data Output (SSI Interface)	
SERIN	Data Output D3	Serial Data Input (SSI Interface)				
SCLK	Data Output D2	Clock Input (SSI Interface)				
SYNM0	Data Output D1	Synchronisation Mode Input		Test Current Input DREF	Synchronisation Mode Input	
SYNM1	Data Output D0 (LSB)	Synchronisation Mode Input		Test Current Input D4...0	Synchronisation Mode Input	
SEEN	Gray/binary conversion (low active)	Serial Errorbit Enable Input / no function	Configuration of Phase Shift	no function	Serial Errorbit Enable Input	Configuration of Phase Shift
RC	RC Network for Monoflop					
VCCA	+4 ... +5.5 V Analog Supply Voltage					
VDD	+4 ... +5.5 V Digital Supply Voltage					
LVCC	+4 ... +5.5 V LED Driver Supply Voltage					
NINV	Bit-wise Inversion Input (low active)					
MODE	Operating Mode Selection Input					
TEST	Test Mode Enable Input (high active)					
RSET	LED Power Control Adjustment					
NERR	Error Output (illumination, low active)				Switch Threshold Measurement (Push-Pull Output)	
NDIR	Reversal of Rotation Dir. Input (low active)			IDDQ Test Enable (low active)	Reversal of Rotation Dir. Input (low active)	

ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VCC	Supply Voltage					V
G001	V()	Analog Supply Voltage VCCA			0.3	6	V
G002	V()	Digital Supply Voltage VDD			VCCA	VCCA	V
G003	V()	Voltage at LVCC, LED, SOUT, SERIN, SCLK, SYNM0, SYNM1, SEEN, NDIR, NERR, RSET, TEST, MODE, NINV, RC			-0.3	VCCA+0.3	V
G004	Ic()	Clamp Diode Current in LED, SOUT, SERIN, SCLK, SYNM0, SYNM1, SEEN, NDIR, NERR, RSET, TEST, MODE, NINV, RC	SERIN, SCLK, SYNM0, SYNM1 with input function		-4	4	mA
G005	I()	Current in SOUT, SERIN, SCLK, SYNM0, SYNM1, RSET, RC	SERIN, SCLK, SYNM0, SYNM1 with input function		-4	4	mA
G006	I()	Current in LVCC to LED	V(LVCC) ≤ VCCA		0	50	mA
E001	Vd()	ESD Susceptibility at all pins	MIL-STD-883, Method 3015, HBM 100 pF discharged through 1.5 kΩ			2	kV
TG1	Tj	Operating Junction Temperature			-40	125	°C
TG2	Ts	Storage Temperature Range	see package specification				°C

THERMAL DATA

Operating Conditions: VCCA, VDD, LVCC= 4..5.5V

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range	see package specification					°C

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCA, VDD, LVCC = 4 ... 5.5 V, Tj = -40 ... +125 °C, unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	V()	Permissible Supply Voltage VCCA, VDD, LVCC				4	5	5.5	V
002	I()	Supply Current in VCCA, VDD	LED control active: R(RSET/AGND) = 24 kΩ, MODE = hi, TEST = lo; I(D0..4) ≤ 8nA				2	5	mA
003	Vcz()hi	Clamp Voltage hi vs. GNDA at all pins	I() = 4 mA					11	V
004	Vc()hi	Clamp Voltage hi at inputs: RC, NINV, MODE, TEST, RSET, NERR, NDIR, SEEN, SYNM1, SYNM0, SCLK, SERIN, SOUT	Vc()hi = V() - V(VDD), I() = 4 mA			0.3		1.2	V
005	Vc()lo	Clamp Voltage lo at all pins	I() = -4 mA			-1.2		-0.3	V
TTL Inputs: SYNM1, SYNM0, SCLK, SERIN, SEEN, NDIR, TEST, MODE, NINV									
006	Vt()hi	Threshold Voltage hi	MODE = hi					2	V
007	Vt()lo	Threshold Voltage lo	MODE = hi			0.8			V
008	Vt()hys	Threshold Voltage Hysteresis	MODE = hi			300	500		mV
009	Ipu()	Pull-up Current in SCLK, SERIN, SEEN, NDIR, MODE, NINV	V() = 0 ... VCCA - 1V, MODE = hi			-62	-30	-4	µA
010	Ipu()	Pull-up Current in SYNM1, SYNM0	V() = 0 ... VCCA - 1V, MODE = hi			-80		-4	µA
011	Ipd()	Pull-down Current in TEST	V() = 1 V ... VCCA, MODE = hi			3	31	75	µA
Outputs D0 to D4: SYNM1, SYNM0, SCLK, SERIN, SOUT									
012	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA MODE = lo					500	mV
013	Vs()lo	Saturation Voltage lo	I() = 4 mA I() = 1.6 mA					500 400	mV mV
Error Output NERR									
014	Vs()lo	Saturation Voltage lo	I() = 4 mA I() = 1.6 mA					500 400	mV
015	R()pu	Permissible Pull-up Load					10		kΩ
Current Comparators, Tracks 0...4									
301	IDREF	Reference Sensor Photocurrent					100		nA
302	IDD	Compensation Sensor Dark Current					20		pA
303	Hys	Switch Hysteresis Referred to Reference Current IDREF	I(D0...4) = IDD ... IDREF			14	17	20	%

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCCA, VDD, LVCC = 4 ... 5.5 V, Tj = -40 ... +125 °C, unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Photosensors and Amplifiers D0...4, DREF									
401	S(λ)	Spectral Sensitivity	λ = 880 nm				0.3		A/W
402	λar	Spectral Application Range	Se(λar) = 0.1 × S(λ)max			400		1050	nm
403	Aph()	Active Photosensor Area				0.200 × 0.100			mm²
404	dθ/dA	Permissible Irradiance	application range					1000	µW/cm²
405	fo	Upper Cut-off Frequency	sinusoidal waveform, I(D0...4) = 8 ... 80 nA, I(DREF) = 80 nA			200			kHz
406	Δtp()	Propagation Delay Difference (Delay Skew)	square waveform, R(RSET/AGND) = 24 kΩ I(D0...4) = 8 ... 100 nA, I(DREF) = 100 nA					0.5	µs
407	CM()	Common Mode Referred to Reference Photocurrent I(DREF)				0.85	1	1.15	
LED Power Control and DREF Reference Sensor									
501	Aph()	Active Photosensor Area DREF				0.200 × 0.100			mm²
502	I(LED)	Permissible LED Output Current				0		40	mA
503	Vs(LED)	Saturation Voltage at LED	I(LED) = 40 mA					1.1	V
504	tr(LED)	Rise Time LED Current	I(LED) = 0 ... 100 %				60	1500	µs
505	R()	Link Resistance LVCC to VDD				2	5	10	kΩ
Monoflop RC									
601	C(RC)	Permissible Capacitor at RC				0.1		1000	nF
602	R(RC)	Permissible Resistor at RC				15		1000	kΩ
603	tmf	Monoflop Time	R2 = 1 nF, C2 = 18 kΩ, tmf = 1.16 x R x C (±15 %)			16	21	24	µs
604	tmf	Monoflop Time	no external RC network			11.5	21	29.5	µs
SSI Interface									
701	f(SCLK)	Permissible Clock Rate						2	MHz
702	tp()	Propagation Delay SCLK to SOUT					85		ns
703	tp()	Propagation Delay SERIN to SOUT	mode "Sync Out"				85		ns
Analog Test Mode SYNM0, SYNM1									
801	CR1()	Test Current Ratio I(SYNM1)/I(D0..4)	TEST = hi, MODE = lo: analog test mode active, I() = 2 ... 200 µA				1000		
802	CR2()	Test Current Ratio I(SYNM0)/I(DREF)	TEST = hi, MODE = lo: analog test mode active, I() = 2 ... 200 µA				1000		
Control Adjustment RSET									
E01	V()	Reference Voltage	I(RSET) = -100 ... -20 µA			0.95	1.16	1.25	V
E02	Ibias()	Permissible Bias Current				-100		-20	µA
E03	Ibias()	Equivalent Internal Bias Current	RSET open	27			50		µA
E04	Isc()	Short-Circuit Current	V(RSET) = 0				1.3	2.6	mA

OPERATING REQUIREMENTS: Logic

Operating Conditions: VCCA, VDD, LVCC = 4 ... 5.5 V, Tj = -40 ... +125 °C,
input levels lo = 0 ... 0.45 V, hi = 2.4 V ... VDD, see Fig. 1 for reference levels

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
I1	t_{set}	Setup Time: SERIN stable before SCLK hi → loi	mode "No Sync"	2	30		ns
I2	t_{hold}	Hold Time: SERIN stable after SCLK hi → lo	mode "No Sync"	2	30		ns

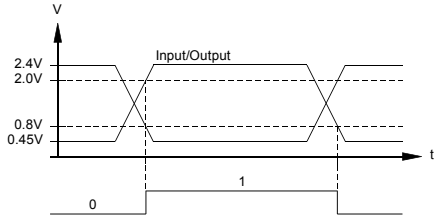


Figure 1: Reference levels

DESCRIPTION OF FUNCTIONS

Illumination control

The integrated LED power control with a driver stage keeps the photocurrent of reference photosensor DREF constant. This compensates for aging, dirt and drops in efficiency of the transmitting LED with rises in temperature.

The photocurrent of reference sensor DREF and the dark current of compensation sensor DD are amplified in the receiver. The amplified currents are subtracted from one another, yielding an actual value to feed the LED power control. The current adjusted by resistor R1 at pin RSET generates the bias for the control; the voltage at pin RSET is kept constant (see Electrical Characteristics No. E01). If pin RSET remains open an internal bias current is used which is equivalent to an external resistor of ca. 24 kΩ.

If there is an optical feedback loop from the LED to reference sensor DREF the power driver alters the LED current until the optical power received complies with the given setpoint. The photocurrent generated by reference sensor DREF – and thus also the level of illumination for the overall system – is kept constant.

A monitoring circuit detects when and if the LED control range is overshot or undershot and signals this by switching error output NERR to low and via the error bit during serial communication (when SEEN is high and no synchronization is selected).

Resistor R3 connected in series to the transmitting LED limits the current and governs the operating limits of the LED power control.

At the same time the amplified dark current of compensation sensor DD and the reference photocurrent of sensor DREF are added together. The resulting current, named INREF, is used to provide the switching threshold for the track comparators. This enables operation of iC-LV with an external light source instead of using power-controlled LED.

Track evaluation

The switching threshold supplied to the track comparators lies at half of INREF, ie. in the center between a full light and no light condition, and adjusts automatically to changes in illumination. This enables the device to be operated without the LED power control with a constant illumination level only. The hysteresis of the current comparators is also photocurrent tracked and increases noise immunity.

The most significant bit (MSB) can be inverted by connecting pin NDIR to ground (GND). If the pin remains open, an internal pull-up current source generates a high level. When Gray code discs are used, inverting the MSB track is tantamount to changing the direction of rotation.

Modes of operation

iC-LV has various modes of operation which are preselected using pin MODE. MODE = 0 selects operation as an optoelectronic encoder IC with a parallel output; MODE = 1 (default) makes a number of serial operating modes available.

Parallel Output Mode (MODE = 0)

In parallel output mode the 5 tracks with sensor D4 (MSB) to sensor D0 (LSB or least significant bit) are output in parallel to pins SYNM1 (LSB), SYNM0, SCLK, SERIN and SOUT (MSB).

The wiring of pin NDIR determines the count direction. With NDIR connected to GND the MSB is output inverted so that the count direction can be altered when reading Gray-coded discs.

By connecting pin NINV to GND the output of all bits can be inverted. If this is not required, NINV can be left open. NDIR and NINV can be used either together or independently of one another. If both pins are connected to GND all bits – with the exception of the MSB – are output inverted.

By connecting pin SEEN to GND the bits can be output in binary format following a Gray to binary code conversion. This is done after the bits have been inverted, where relevant. If pin SEEN is left unconnected the output is in Gray code.

Serial Output Mode (MODE = 1, default)

In serial output mode pin SCLK is the clock input hooked up to an SSI master supplying an intermittently active clock signal with a high level during idle time, pin SERIN is the serial data input and pin SOUT the serial data output.

Various serial operational modes and output formats can be configured using pins SYNM0 and SYNM1 (high when not wired).

SYNM (1:0)	Serial Operational Modes	Data Output Format
1 1	No Sync (default)	5 bit Gray (option: +1 error bit)
1 0	No Sync Binary	5 bit binary
0 1	Sync Out	4 bit binary (corrected by ±1)
0 0	SSI Out	4 bit binary (corrected by ±1)

In **No Sync** mode an LED control error bit (low active) can be added to the serial data by releasing it via pin SEEN. In **No Sync Binary** mode pin SEEN has no function.

In both **No Sync** and **No Sync Binary** mode iC-LV operates without synchronization, i.e. it stores the 5 track values on the first falling edge seen at SCLK after a long idle time and then transmits the track data via pin SOUT on each of the 5 following rising edges at SCLK. At the same time pin SERIN reads in data from a pre-positioned iC-LV which can then be passed on. Here, iC-LV operates as a 5-bit shift register (or 6-bit if the error bit is active during No Sync mode) whose flipflops accept input data on a falling edge and output stored data on a rising edge.

In **No Sync Binary** mode data is converted from Gray to binary before being output. In this mode of operation it is not possible to output a serial error bit; no data from SERIN is accepted on the first and second rising edge at SCLK.

If pin NDIR is connected to GND a change in count direction with Gray codes can be initiated by inverting the MSB. By connecting pin NINV to GND all track data can be output inverted. Both pins NINV and NDIR are high when not connected.

In modes **SSI out** and **Sync out** iC-LV operates with synchronization, classing the LSB of its own code disc as a synchronization bit. The data read in from the code disc is converted into binary code and, if necessary, corrected by +1 or -1 depending on the MSB of the pre-positioned device also read in.

Each LSB has the same resolution as the MSB of the pre-positioned iC-LV, operated at a 16-fold faster speed, and is assembled so that it either trails (SEEN is high, default) or leads (SEEN is low) by up to 90°. The phase position must be configured for each individual code disc using pin SEEN (trail/lead). This phase shift applies to data converted into binary code and is not immediately visible on the code discs.

If data is read out serially and synchronized elsewhere a smaller phase shift must be adjusted. In this instance data transmission times must be taken into account.

The synchronization process ensures that synchronous with the flipping of the MSB from the pre-positioned iC-LV track data is switched forward to the next data word expected on that code disc. Once the track data has been captured on the first falling edge at SLCK, the data word is synchronized with the MSB of the predecessor during the first low and first high period on the SCLK line (the MSB is possibly subject to change within this time).

The synchronization result is switched straight through to the output so that a synchronized MSB is available for each following gear. This allows the track data to be synchronized with MSBs on the first falling as well as on the first rising edge.

In synchronization modes iC-LV functions as a 4-bit shift register, i.e. the synchronization bit is not clocked out with the track data. Serial data is read in on a falling edge and output on a rising edge. In **SSI Out** mode the MSB is blanked out by a high until the first rising edge and thus output on this first rising edge, making this mode SSI compatible.

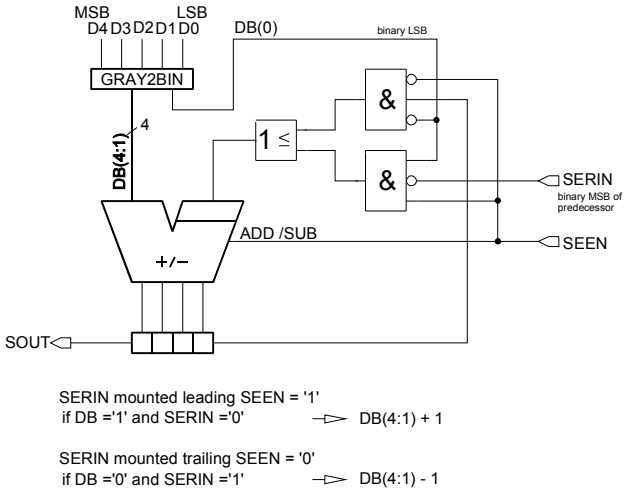


Figure 2: Synchronization

If inverted Gray codes are used on the code discs a code inversion can be initiated by connecting NINV to GND. By connecting NDIR to GND the MSB bit is output inverted to reverse the count direction of the Gray code.
Here it should be noted that inverting the MSB output causes a 180° change in the phase position, i.e. a trailing 90° synchronization track becomes a leading 90° track and vice versa. This can be compensated for by a suitable setting of pin SEEN or by assembling the code disc in a suitable zero position.

Test modes

iC-LV has two different test modes which are activated by connecting pin TEST to VDD. Pin MODE designates which test mode is activated. Connected to VDD (or not connected at all), this initiates the digital test mode; if connected to GND the analog test mode is selected.

Analog Test Modes (MODE = 0)

Sensor emulation and comparator switching threshold test: To test the track evaluation and switching thresholds a test current is supplied at pin SYNM0 for reference sensor DREF and at SYNM1 for the track sensors. The current reduction ratio is 1:1000.

Alternatively, testing can be carried out by illumination as the supplied test currents are added to the photocurrents. The track to be measured at SOUT is selected via a 5-bit shift register. To this end a suitable bit stream is clocked in via SCLK (clock low active) and SERIN (level). If more than one track is selected, the comparator output signals are EXORed. The 5-bit shift register addresses track sensors D4 to D0 via bits 4 to 0. When measurement commences the shift register should be filled up with zero.

IDDQ test: This test is initiated by connecting pin NDIR (default high) to GND.

Digital Test Modes (MODE = 1, open)

Logic test: Digital test mode is largely identical to the serial operating modes. One difference is that data input at pin SERIN is first clocked through a 5-bit shift register before being clocked through the output shift register. This enables various bit sequences to be first clocked into the test register. Following an idle time on the clock line of t > tmf (see Electrical Characteristics No. 603) the test data is stored on the first falling edge on SCLK instead of the track values.

This allows various sensor input stimuli to be generated. In the synchronized operating modes the data word is synchronized with pin SERIN as in normal operating mode. Configuration of the various serial operating modes is also as in normal operating mode. No stimuli can be clocked in in **No Sync Binary** mode.

TP: So that the switching thresholds of the input interfaces (SYNM0, SYNM1, SERIN, SCLK, NDIR, NINV, SEEN) can be measured the signals are EXORed and output at pin NERR. To this end pin NERR is switched as a push-pull output.

APPLICATIONS INFORMATION

If a stable SSI output level is required all MSBs used in the synchronization chain must be switched to the relevant outputs on the first falling edge. The iC-LV chain should also be synchronized in its entirety before the first rising edge of SCLK.

To guarantee functionality it is sufficient for synchronization to be completed by the second falling edge of SCLK; SOUT is, however, then not stable for half a clock cycle. Despite this limitation it is also possible to synchronize with MSBs which are only output on the first rising SCLK edge (e.g. from external SSI-compatible devices).

Figure 3 gives signal patterns for a cascade of three iC-LVs.

In the synchronization modes all of the information is output after just 4 rising clock edges per chained iC-LV.

In keeping with the required SSI clock frequency the time span of the internal monoflop, used to detect idle times on the clock line, can be adjusted by externally connecting pin RC to an RC network. Should pin RC remain unconnected, tmf (Electrical Characteristics No. 603) is taken as the internal time span.

Note: iC-LV stores input data received at SERIN on the falling edge of SCLK and outputs data via SOUT on the rising edge of SCLK.

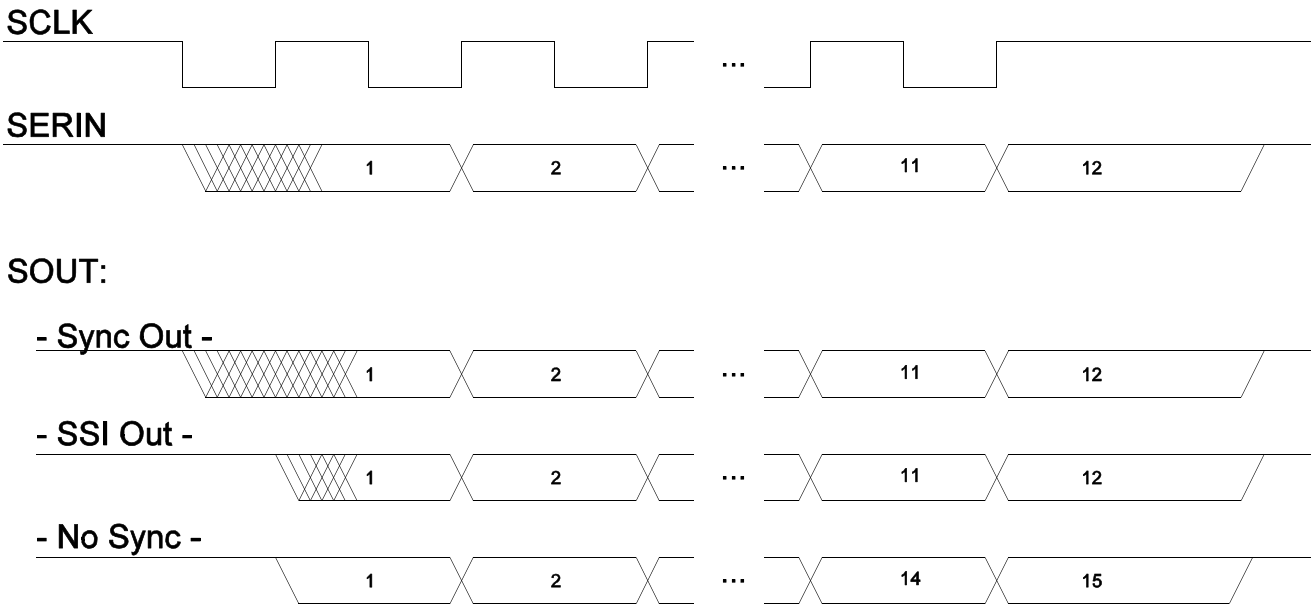


Figure 3: SOUT in the various modes of operation.

ORDERING INFORMATION

Type	Package	Order designation
iC-LV	-	iC-LV chip
iC-LV	BLCC LV4C	iC-LV BLCC LV4C

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel +49-6135-9292-0
Fax +49-6135-9292-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: **http://www.ichaus.de/support_distributors.php**