C-MEDIA ELECTRONICS INC.
Ver. 1.2
6F, No. 100, Sec. 4, Civil Boulevard, Taipei, Taiwan
TEL: (02)8773-1100 FAX: 886-2-8773-2211
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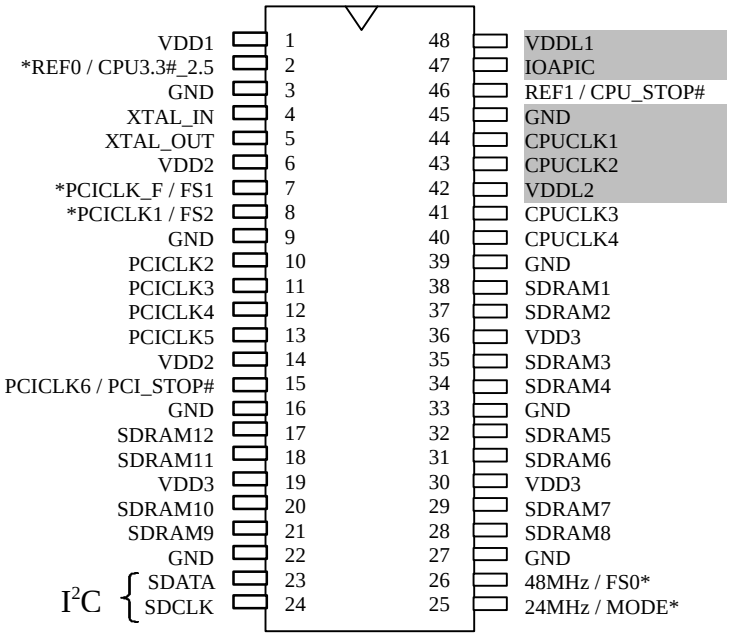
CMA8864-04 (3 DIMM) I²C, Mixed Voltage clock Synthesizer with Buffer for PENTIUM™ & II CPU/PCI system (CK3D)

FEATURES

- **Supports Pentium and Pentium II CPUs.**
- **Two (2) copies of CPUCLK clock powered with VDDL2, two (2) copies of CPUCLK powered with VDD3..**
- **Twelve (12) SDRAM clocks powered by VDD3.**
- **Seven (7) copies of PCI clock (1/2 CPU clock or asynchronous 2/5 CPU clock).**
- **IOAPIC clock @14.318MHz driven by VDDL1.**
- **24/48 MHz outputs (3.3V TTL)**
- **Two Ref. Clock @ 14.318MHz (3.3V TTL).**
- **60mA buffer switching current @3.3V.**
- **Optional common or mixed power supply mode**
  - ✧ **VDD1, 2, 3 = VDDL2, 1 = 3.3V**
  - ✧ **VDD1, 2, 3 = 3.3V; VDDL2, 1 = 2.5V**
- **< 250ps skew between CPU/SDRAM buffers.**
- **<500ps skew between PCI buffers.**
- **Power management controlled by CPU_STOP#, PCI_STOP#.**
- **I²C Serial configuration interface.**
- **48 pins SSOP package.**

PIN CONFIGURATIONS



POWER GROUPS

VDD1=REF, XTAL_IN, XTAL_OUT, PLL CORE

VDD2=PCICLK

VDD3=SDRAM, 24/48MHz, CPUCLK3- 4

VDDL1=IOAPIC

VDDL2=CPUCLK1-2

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PIN DESCRIPTION

NAME	TYPE	NO.	DESCRIPTION
VDD1	P	1	Analog 3.3V power supply for PLL core, REF, XTAL_IN/_OUT.
REF0 / CPU3.3#_2.5	I/O	2	14.318MHz clock output. / Indicates VDDL2 power supply, 0=3.3V CPU, 1=2.5V CPU.
GND	G	3, 9, 16, 22, 27, 33, 39, 45	Ground.
XTAL_IN	I	4	Crystal input.
XTAL_OUT	O	5	Crystal output.
VDD2	P	6, 14	3.3V I/O power supply for PCICLK.
PCICLK_F / FS1	I/O	7	PCI clock output free-running, TTL compatible 3.3V. / Frequency select pin, latched input, internal pull-High.
PCICLK1 / FS2	I/O	8	PCI clock output TTL compatible 3.3V. / Frequency select pin, latched input, internal pull-High.
PCICLK2-5	O	10, 11, 12, 13	PCI clock output TTL compatible 3.3V.
PCICLK6 / PCI_STOP#	I/O	15	PCI clock output TTL compatible 3.3V. / halts PCICLK at logic 0 level when input low, MODE=0 (Mobil mode)
SDRAM12-1	O	17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM clock output.
VDD3	P	19, 30, 36	3.3V I/O power supply for SDRAM, 24/48MHz.
SDRAM10:1	O	20, 21, 28, 29, 31, 32, 34, 35,37, 38	SDRAM clock outputs powered by VDD3.
SDATA	I	23	Data input pin for I^2C bus.
SDCLK	I	24	Clock input pin for I^2C bus.
24MHz / MODE	I/O	25	24MHz clock output 3.3V. MODE=1 / Pin 15 = PCICLK6 / Pin 46 = REF1 MODE=0 / Pin 15 = CPI_STOP# / Pin 46 = CPU_STOP#
48MHz / FS0	I/O	26	48MHz clock output 3.3V. / Frequency select pin, latched input, internal pull-High.
CPUCLK4	O	40	CPU and Host clock output 3.3V output, powered by VDD3.
CPUCLK3	O	41	CPU and Host clock output 3.3V output, powered by VDD3.
VDDL2	P	42	2.5V/3.3V I/O power supply.
CPUCLK2	O	43	CPU and Host clock output 2.5V/3.3V output, powered by VDDL2.
CPUCLK1	O	44	CPU and Host clock output 2.5V/3.3V output, powered by VDDL2.
REF1 / CPU_STOP#	I/O	46	14.318MHz clock output. / halts CPUCLK at logic 0 level when input low, MODE=0 (Mobil mode)
IOAPIC	I/O	47	14.318MHz clock output 2.5V/3.3V, powered by VDDL1.
VDDL1	P	48	2.5V/3.3V I/O power supply.

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CPU CLOCK FREQUENCY TABLE (in MHz)

SEL2	SEL1	SEL0	CPU, SDRAM	PCI
1	1	1	66.8	33.4 (1/2 CPU)
1	1	0	60	30 (1/2 CPU)
1	0	1	75	37.5 (1/2 CPU)
1	0	0	83.3	33.3 (2/5 CPU)
0	1	1	68.5	34.25 (1/2 CPU)
0	1	0	83.3	41.65 (1/2 CPU)
0	0	1	75	30 (2/5 CPU)
0	0	0	50	25 (1/2 CPU)

I²C SERIAL CONTROL

I²C Specification

Address assignment	7 bit									
Transfer type	Slaver / Receiver									
Transfer rate	100kbits/s (standard mode)									
Data byte format	8 bits									
Address format	A6	A5	A4	A3	A2	A1	A0	R/Ws	+8 bits dummy Command Code	+8 bits dummy Command Code
	1	1	0	1	0	0	1	0		
General call	No respond									

SERIAL CONTROL REGISTERS

A) The serial bits will be read in the following order :

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

B) The PIN# column lists the affected pin number where application. The values in the @Pup column gives the state at true power up. Registers are set to the values shown only on the true power up.

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Byte 0 : Function and Frequency Select Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description				
7	--	0	Must be 0 for normal operation.				
			0 -- ¡ Ó5% frequency modulation.				
			1 -- ¡ Ó5% frequency modulation.				
6	--	0	Bit6	Bit5	Bit4	CPU, SDRAM	PCI
5	--	0	1	1	1	66.8	33.4 (1/2 CPU)
4	--	0	1	1	0	60	30 (1/2 CPU)
			1	0	1	75	37.5 (1/2 CPU)
			1	0	0	83.3	33.3 (2/5 CPU)
			0	1	1	68.5	34.5 (1/2 CPU)
			0	1	0	83.3	41.65 (1/2 CPU)
			0	0	1	75	30 (2/5 CPU)
			0	0	0	50	25 (1/2 CPU)
3	--	0	0 -- Frequency is selected by hardware select, latched inputs.				
			1 -- Frequency is selected by Bit 6 : 4.				
2	--	0	Must be 0 for normal operation.				
			0 -- Frequency modulation center spread type.				
			1 -- Frequency modulation down spread type.				
1	--	0	0 -- Normal.				
			1 -- Frequency modulation enabled type.				
0	--	0	0 -- Normal.				
			1 -- Tristate all outputs.				

Byte 1 : CPU Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	26	1	48MHz (Active/Inactive)
6	25	1	24MHz (Active/Inactive)
5	--	X	Reserved
4	--	X	Reserved
3	40	1	CPUCLK4 (Active/Inactive)
2	41	1	CPUCLK3 (Active/Inactive)
1	43	1	CPUCLK2 (Active/Inactive)
0	44	1	CPUCLK1 (Active/Inactive)

Byte 2 : PCI Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	7	1	PCICLK_F (Active/Inactive)
5	15	1	PCICLK6 (Active/Inactive)
4	13	1	PCICLK5 (Active/Inactive)
3	12	1	PCICLK4 (Active/Inactive)
2	11	1	PCICLK3 (Active/Inactive)
1	10	1	PCICLK2 (Active/Inactive)
0	8	1	PCICLK1 (Active/Inactive)

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Byte 3 : SDRAM Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	28	1	SDRAM8 (Active/Inactive)
6	29	1	SDRAM7 (Active/Inactive)
5	31	1	SDRAM6 (Active/Inactive)
4	32	1	SDRAM5 (Active/Inactive)
3	34	1	SDRAM4 (Active/Inactive)
2	35	1	SDRAM3 (Active/Inactive)
1	37	1	SDRAM2 (Active/Inactive)
0	38	1	SDRAM1 (Active/Inactive)

Byte 4 : Additional SDRAM Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	--	X	Reserved
3	17	1	SDRAM12 (Active/Inactive)
2	18	1	SDRAM11 (Active/Inactive)
1	20	1	SDRAM10 (Active/Inactive)
0	21	1	SDRAM9 (Active/Inactive)

Byte 5 : Peripheral Active/Inactive Register (1=enable, 0=disable)

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	47	1	IOAPIC (Active/Inactive)
3	--	X	Reserved
2	--	X	Reserved
1	46	1	REF1 (Active/Inactive)
0	2	1	REF0(Active/Inactive)

Byte 6 : Reserved Optional Register for Future Requirements

Bit	PIN#	@Pup	Description
7	--	X	Reserved
6	--	X	Reserved
5	--	X	Reserved
4	--	X	Reserved
3	--	X	Reserved
2	--	X	Reserved
1	--	X	Reserved
0	--	X	Reserved

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BUFFER SPECIFICATION

Buffer Name	Vcc Range (V)	Impedance (£)	Buffer Type
CPU	2.375 - 2.9	15 - 45	1
IOAPIC	2.375 - 2.9	10 - 30	2
24/48MHz, REF1, 2	3.315 - 3.465	20 -60	3
,REF0, SDRAM	3.315 - 3.465	10 - 24	4
PCI	3.315 - 3.465	12 - 55	5

Type 1 : CPU clock buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-27		mA
Iohmax	Pull-up Current	Vout=2.6V		-27	mA
Iolmin	Pull-down Current	Vout=1.2V	27		mA
Iolmax	Pull-down Current	Vout=0.3V		27	mA
trh	2.5V Type 1 output Rise Edge Rate	2.5V @2.0V-0.4V 10pF load	1/1	4/1	V/ns
tfh	2.5V Type 1 output Fall Edge Rate	2.5V @2.0V-0.4V 20pF load	1/1	4/1	V/ns

Type 2 : IOAPIC (2.5V) clock buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.4V	-36		mA
Iohmax	Pull-up Current	Vout=2.7V		-29	mA
Iolmin	Pull-down Current	Vout=1.0V	36		mA
Iolmax	Pull-down Current	Vout=0.2V		28	mA
trh	2.5V Type 2 output Rise Edge Rate	2.5V @0.4V-2.0V 10pF load	1/1	4/1	V/ns
tfh	2.5V Type 2 output Fall Edge Rate	2.5V @2.0V-0.4V 20pF load	1/1	4/1	V/ns

Type 3 : FD, USB, REF1, 2 (3.3V) clock buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-29		mA
Iohmax	Pull-up Current	Vout=3.315V		-23	mA
Iolmin	Pull-down Current	Vout=1.95V	29		mA
Iolmax	Pull-down Current	Vout=0.4V		27	mA
trh	3.3V Type 3 output Rise Edge Rate	3.3V @0.4V-2.4V 10pF load	0.5	2.0	V/ns
tfh	3.3V Type 3 output Fall Edge Rate	3.3V @2.4V-0.4V 20pF load	0.5	2.0	V/ns

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Type 4 : REF0, SDRAM (3.3V) clock buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=2.0V	-54		mA
Iohmax	Pull-up Current	Vout=3.315V		-46	mA
Iolmin	Pull-down Current	Vout=1.0V	54		mA
Iolmax	Pull-down Current	Vout=0.4V		53	mA
trh	3.3V Type 4 output Rise Edge Rate	3.3V @0.4V-2.4V 20pF load	1.5	4/1	V/ns
tfh	3.3V Type 4 output Fall Edge Rate	3.3V @2.4V-0.4V 30pF load	1.5	4/1	V/ns

Type 5 : PCI clock buffer Operating Characteristics

Symbol	Parameter	Condition	Min.	Max.	Units
Iohmin	Pull-up Current	Vout=1.0V	-33		mA
Iohmax	Pull-up Current	Vout=3.315V		-33	mA
Iolmin	Pull-down Current	Vout=1.95V	30		mA
Iolmax	Pull-down Current	Vout=0.4V		38	mA
trh	3.3V Type 5 output Rise Edge Rate	3.3V @0.4V-2.4V 20pF load	1/1	4/1	V/ns
tfh	3.3V Type 5 output Fall Edge Rate	3.3V @2.4V-0.4V 30pF load	1/1	4/1	V/ns

AC / DC SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Power Supply Voltage	VDD=3.3V±5% VDD3=3.3V±5% VDDL=2.5V+16%, -5%
Applied Input Voltage (VSS)	-0.3V
Ambient Temperature	55 to 125°C
Storage Temperature	-65 to 150°C
Maximum Power pplySu	7V

NOTICE : This device contains circuitry to protect the inputs against damage due to high static voltage or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range :

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD)

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DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITION
Idd	Dynamic Supply Current	-	TBD	mA	CPU=66.6MHz, PCI=33.3MHz
Vil	Input Low Voltage	VSS-0.3	0.8	VDC	
Vih	Input High Voltage	2.0	VDD-0.3	VDC	VDD=3.3V± 5%
Iil	Input Leakage Current	-5	+5	uA	0<Vin<VDD
Voh2	2.5V Output High Voltage	2.0	-	V	VDDL=2.375V to 2.9V, Ioh=-1mA
Vol2	2.5V Output Low Voltage	-	0.4	V	VDDL=2.375V to 2.9V, Iol=1mA
Voh3	3.3V Output High Voltage	2.4	-	V	VDD3=3.3V± 5%, Ioh=-1mA
Vol3	3.3V Output Low Voltage	-	0.4	V	VDD3=3.3V± 5%, Iol=1mA
Vpoh	PCI bus Output High Voltage	2.4	-	V	VDD2=3.3V± 5%, Ioh=-1mA
Vpol	PCI bus Output High Voltage	-	0.55	V	VDD2=3.3V± 5%, Iol=1mA
Ioz	Tristate Leakage Current	-	10	uA	
Isc	Short Circuit Current	25	-	mA	1 output at a time - 30 seconds

AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	Typ.	MAX.	UNIT	CONDITION
$T_{Hrise,}$ T_{Hfall}	Host clock Rise and Fall Time	0.4		1.6	ns	20pf load/CPU and PCI outputs
T_{HCP}	Host Clock Period	15/16.7	-	-	ns	Measured at 1.25V, 66/60MHz
T_{HCH}	Host Clock High Time	5.2/6.0		-	ns	Measured at 2.0V, 66/60MHz
T_{HCL}	Host Clock Low Time	5.0/5.8	-	-	ns	Measured at 0.4V, 66/60MHz
Duty Cycle	Duty cycle	45	50	55	%	Refer to Notes below
T_{HSKW}	Buffer out Skew All Host CLK	-	-	250	ps	Refer to Notes below
T_{JAB}	Jitter absolute, Host clock	-	-	250	ps	Refer to Notes below
T_{STB}	Host/PCI clock stabilization from power-up	-	-	3	ms	Refer to Notes below, VDDL=3.3V
Toff	Host to PIC Offset	1.0	-	4.0	ns	Refer to Notes below
T_{HSSKW}	Host to SDRAM skew	-	-	250	ps	Refer to Notes below
T_{PCP}	PCI clock period	30/33.3	-	-	ns	Measured at 1.5V, 66/60MHz
T_{PCH}	PCI clock High Time	12/13.3	-	-	ns	Measured at 2.4, 66/60MHz
T_{PCL}	PCI clock Low Time	12/13.3	-	-	ns	Measured at 0.4, 66/60MHz
T_{PSKW}	Buffer out skew all PCICLK	-	-	500	ps	Refer to Notes below
Iol	Switching Current Low	TBD	60	TBD	mA	Vol=1.5V
Ioh	Switching Current High	TBD	60	TBD	mA	Voh=1.5V

Notes : **Clock period, Jitter, Offset and skew are measured on the rising edge clocks at 1.25V for the 2.5V clocks and 1.5V for the 3.3V clocks.**

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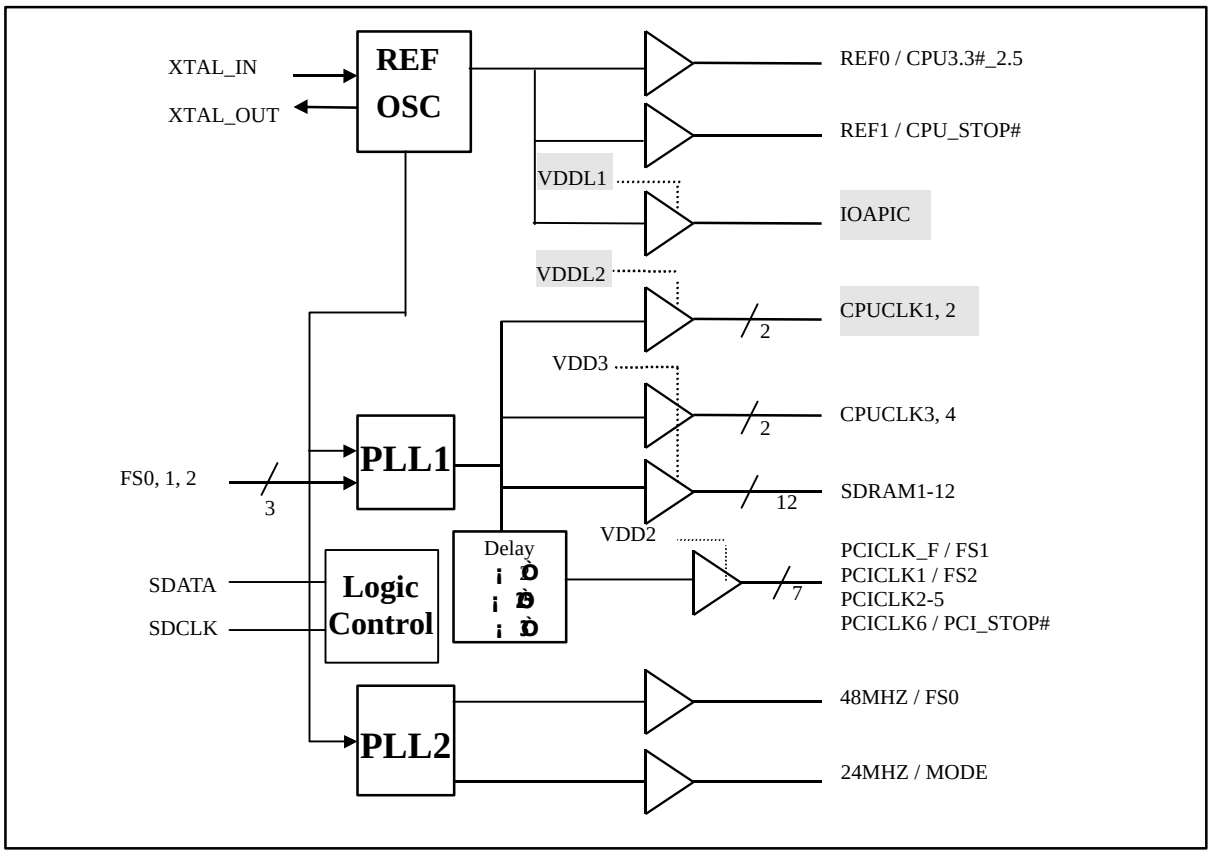
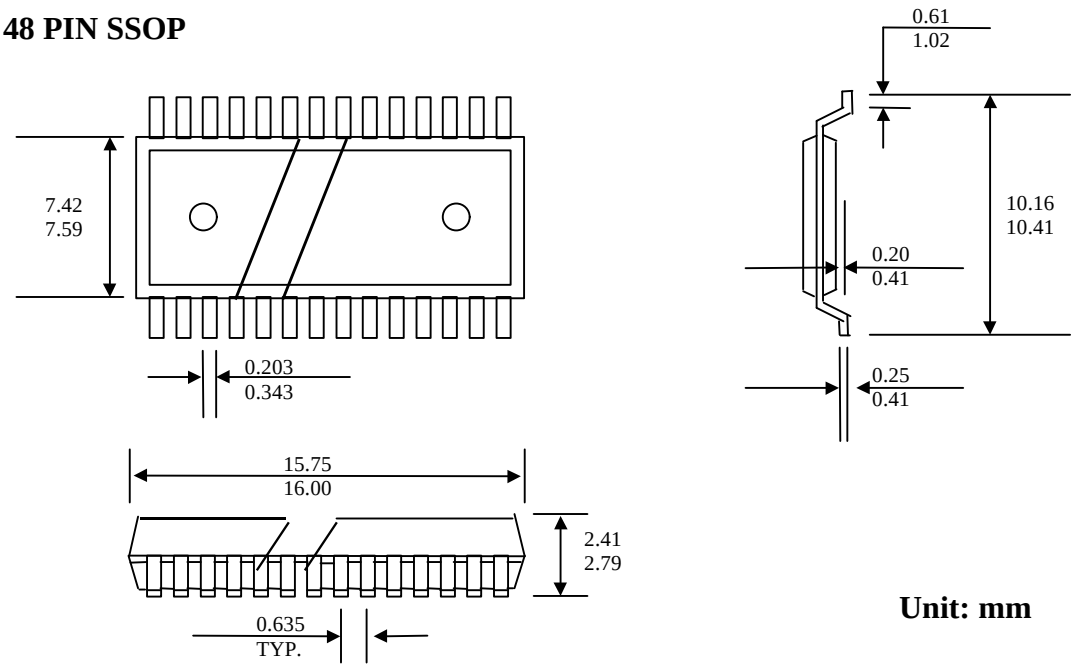
BLOCK DIAGRAM



PACKAGE DIMENSION

48 PIN SSOP



Unit: mm