

# INTELLIGENT INTERACTIVE SYNTHESIZER

## SURFACE MOUNT MODEL: FSW2476-50

### WIDE BANDWIDTH

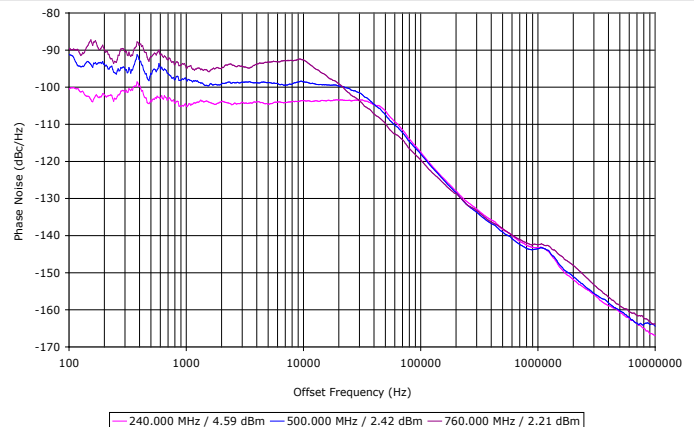
### 240 - 760 MHz

#### FEATURES:

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patent Pending REL-PRO® Technology
- ▶ Small Size, Surface Mount



#### Phase Noise



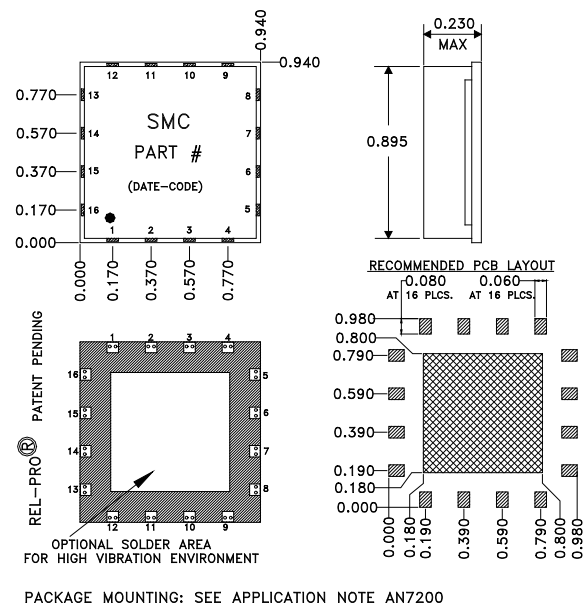
#### SPECIFICATIONS (Rev. B 03/29/07)

Frequency	240 - 760 MHz		
Step Size	500 kHz		
Reference Input Frequency	10 MHz *		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	15
	VCO	+5	45
	Tune	+25	10
Output Power	0 dBm (Min.)		
Spurious Suppression	70 dB (Typ.)		
Harmonic Suppression	12 dB (Typ.)		
Settling Time	10 mSec (Max.) **		
Output Impedance	50 Ohms (Nom.)		
Typical Phase Noise	Offset	Phase Noise	
	@ 1 kHz	-90 dbc/Hz	
	@ 10 kHz	-93 dbc/Hz	
	@ 100 kHz	-120 dbc/Hz	
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		

\* Reference input frequency is programmable in multiples of the step size, 10 MHz is the default setting. 150 MHz (Max.)

\*\* From the rising edge of LE to stable lock detect

Package # 273LF



#### Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (Tune)	+28 V
Bias Voltage (VCO)	+5.5 V
DC Voltage Applied to RF Out	±25 V

#### Pin-Out

Pin 1 - Reset *	Pin 7 - Vcc (Digital)	Pin 15 - Data In
Pin 2,3 - NC	Pin 8 - Vcc (Tune)	Pin 16 - Clock In
Pin 4 - Error flag	Pin 9 - Vcc (VCO)	All Others - Ground
Pin 5 - Latch Enable In	Pin 13 - RF Out	
Pin 6 - Ref. In	Pin 14 - Lock Detect Out	NC - No Connection

\* A logic low on this input will reset the internal controller. Leave unconnected for normal operation.

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 Pending: 60/493075; 60/501371 & 60/501790; 60/527957 & 60/528670; 60/563481; 60/564173; 60/589090; 60/601823; 60/605791; EV31369834;  
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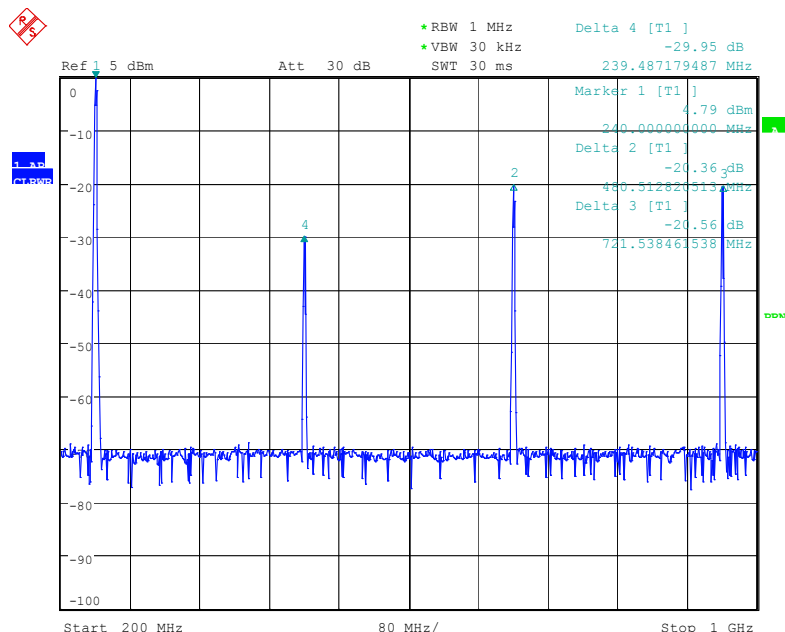
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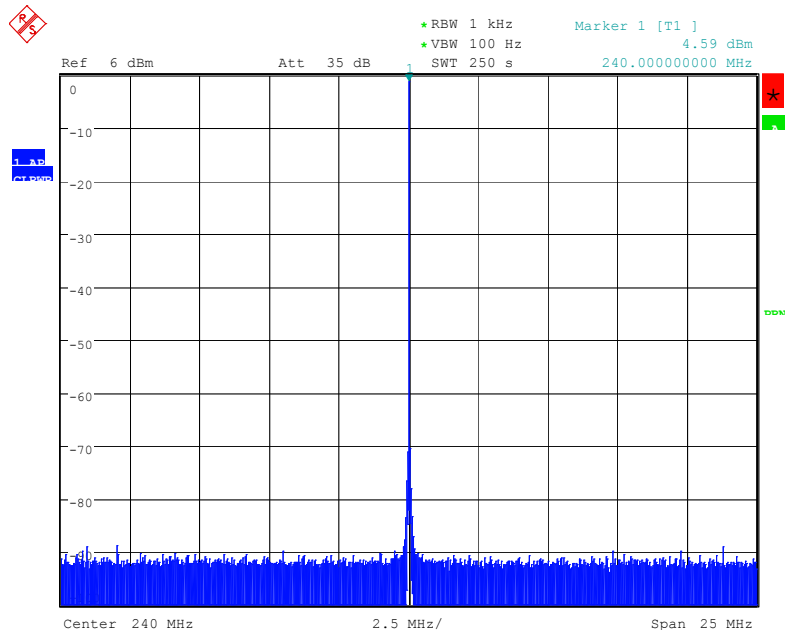
WIDE BANDWIDTH

240 - 760 MHz

### HARMONIC SUPPRESSION



### REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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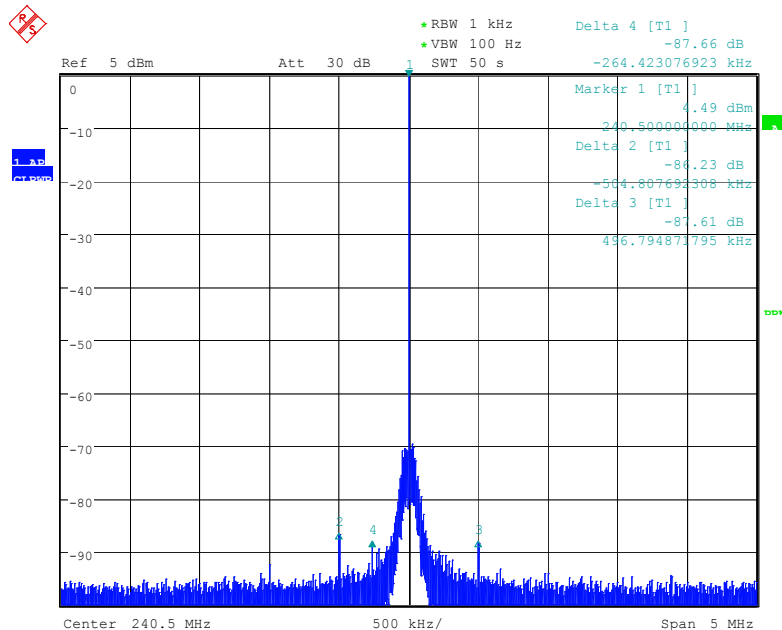
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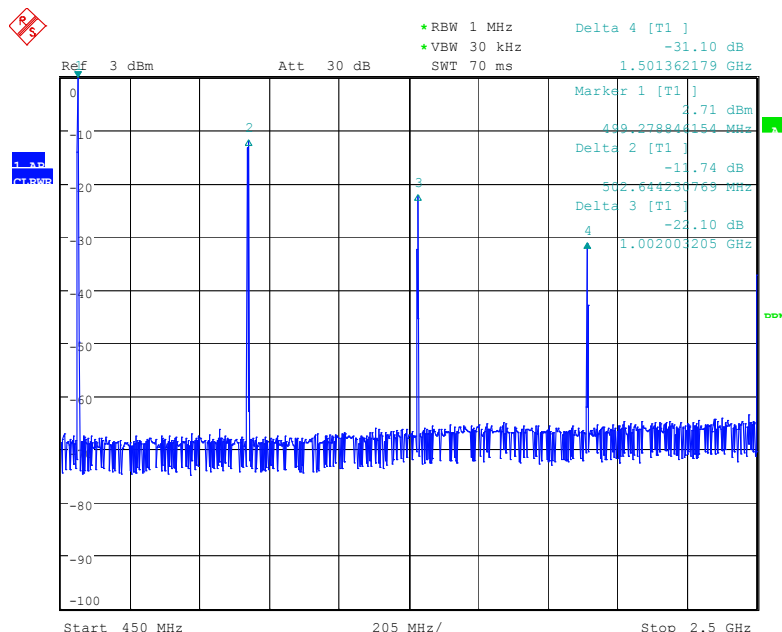
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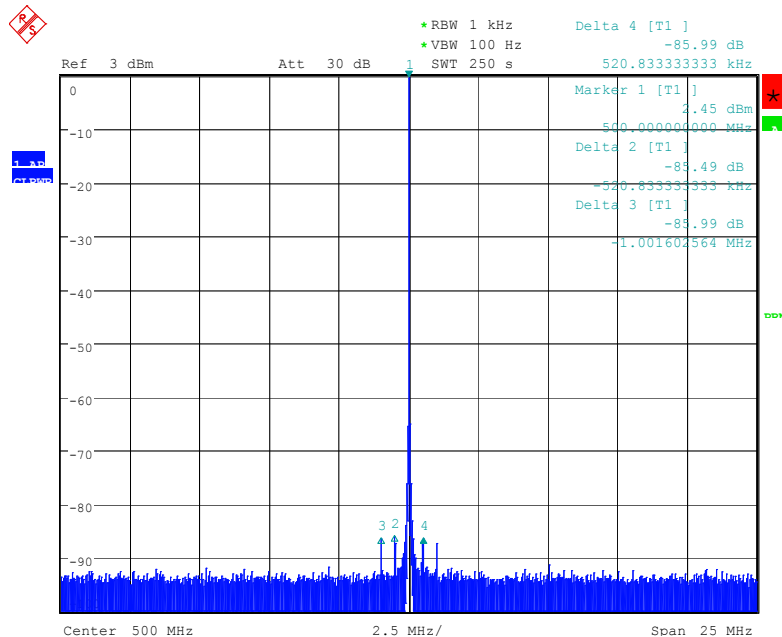
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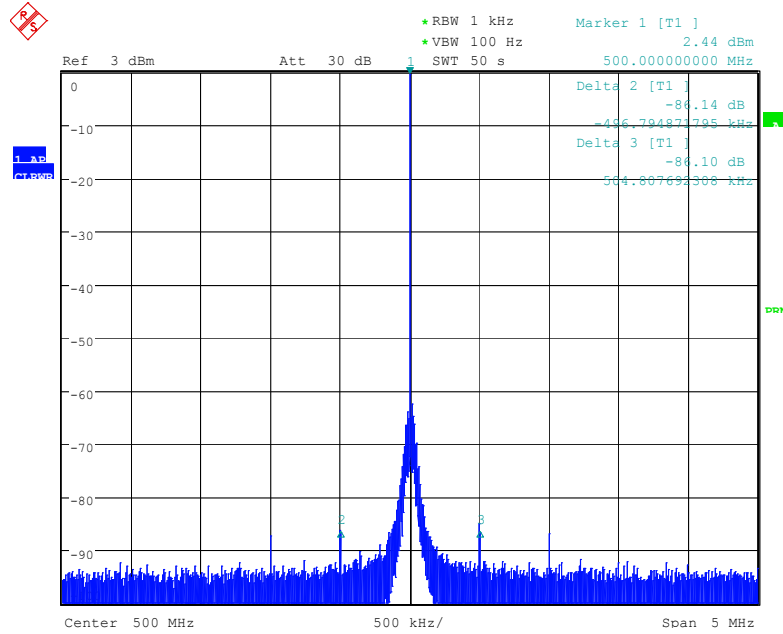
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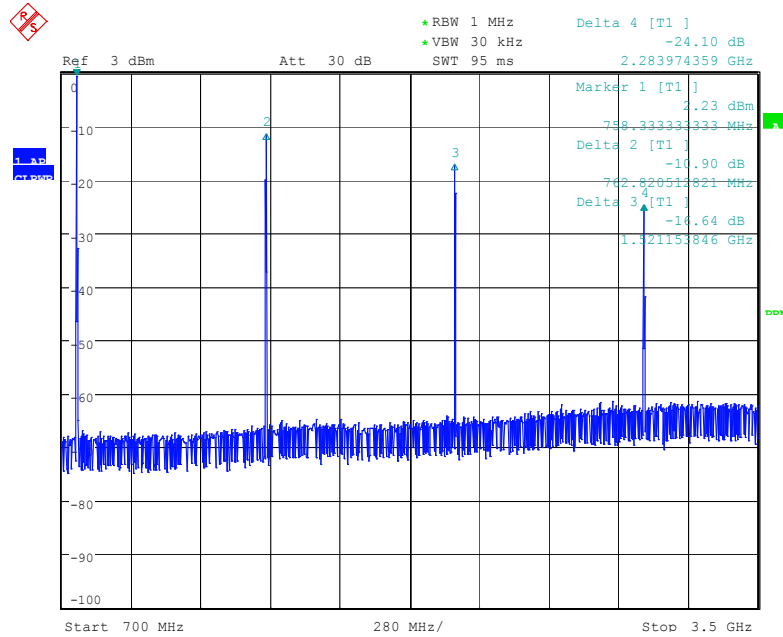
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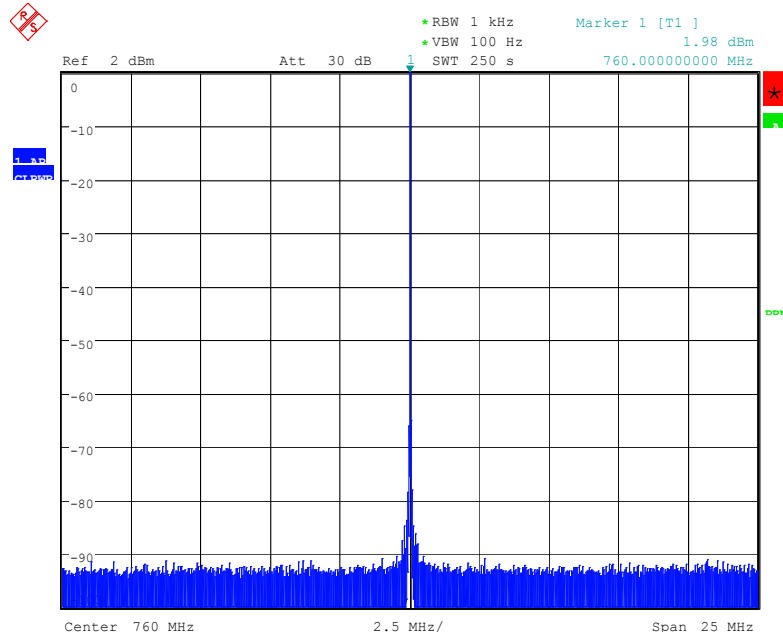
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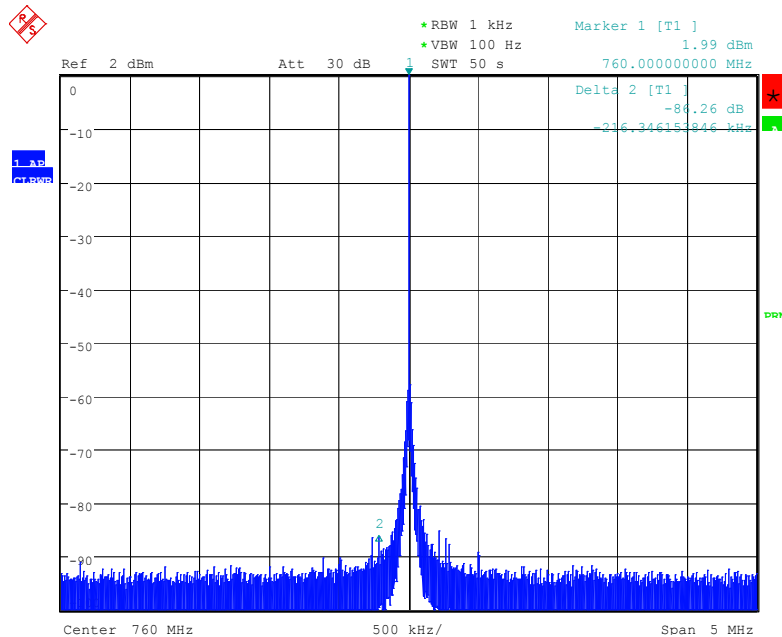
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