

FEATURES

- Supports NTSC (M) and PAL (B, D, G, H, I)
- CCIR 601, square pixel and 4Fsc operation
- 4:2:2 YCrCb and 4:1:1 YCrCb digital input formats
- Two on-chip 8-bit video DACs
- Internally generates SYNC and color burst signals
- Internal vertical interpolation filter
- Analog composite or Y/C output
- High-resolution mode supports Video CD, V2.0
- 16 CLUT RAM (programmable)
- Four modes of video/graphics operation: graphics, video, chroma key and external key
- Color bar generation test function
- Suspend function
- 64-lead PQFP package
- Single +3.3 V power supply

GENERAL DESCRIPTION

The SPT2210 is a single-chip video encoder that is capable of converting digital video data (YCrCb) into analog NTSC or PAL video signals. Two digital input formats are supported: 4:2:2 (YCrCb) and 4:1:1 (YCrCb). It internally generates the proper SYNC and color burst signals for NTSC (525 lines/60 Hz) and PAL (625/50 Hz) video standards operating in any one of three sample rate modes: CCIR 601, square pixel and 4Fsc.

Composite or Y/C S-Video analog video output is generated via two 8-bit internal video DACs. In addition, the

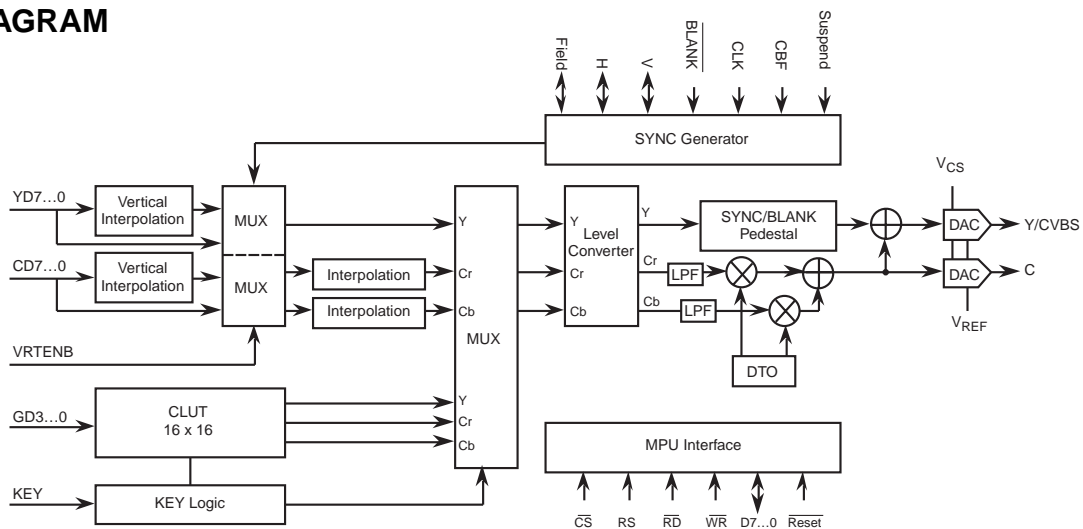
APPLICATIONS

- Video cameras
- Digital video tape recorders
- Video conference equipment
- Video frame grabbers
- Set-top boxes
- Video projection and displays
- Video printers
- Video game machines
- Multimedia PCs

SPT2210 supports external or chroma key functions for color graphics pixel-by-pixel overlay. It has a 16-color lookup-table overlay palette which is fully programmable. It also has an on-chip vertical interpolation filter that can be activated to reduce jaggy noise and flicker. The chip also features an internal test color bar pattern generator.

The SPT2210 operates from a single +3.3 V supply and is built in a 0.5 μm CMOS process. It is available in a 64-lead PQFP package and operates over the commercial temperature range.

BLOCK DIAGRAM



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GENERAL DESCRIPTION OF FUNCTIONS

VIDEO MODES

The SPT2210 supports NTSC and PAL video standards in Y/C (4:2:2) and Y/C (4:1:1) input formats. Table I shows the video modes supported.

Table I – Supported Video Modes

Video Mode	Active Number of Pixels	Input Clock Frequency
NTSC Square Pixel Y/C (4:2:2/4:1:1)	640 x 483	12.2727 MHz
NTSC CCIR 601 Y/C (4:2:2/4:1:1)	720 x 483	13.5000 MHz
NTSC 4Fsc Y/C (4:2:2/4:1:1)	768 x 483	14.3182 MHz
PAL Square Pixel Y/C (4:2:2/4:1:1)	640 x 573	12.1875 MHz
PAL Square Pixel Y/C (4:2:2/4:1:1)	768 x 573	14.7500 MHz
PAL CCIR 601 Y/C (4:2:2/4:1:1)	720 x 573	13.5000 MHz
PAL 4Fsc Y/C (4:2:2/4:1:1)	948 x 573	17.7345 MHz

VERTICAL INTERPOLATION

The SPT2210 has a vertical interpolation filter that is used to reduce jaggy noise and flicker. It also supports the high-resolution mode for Video CD, version 2.0.

TWO-CHANNEL D/A CONVERTER OUTPUT

Digital video signals are output on two 8-bit D/A converters. Y/C (S-Video) output or composite video output can be selected. The Y/C video outputs are current sources, capable of driving a 75 Ω load to 1 V_{P-P}, referenced to ground. If both composite and S-Video are required simultaneously, a simple circuit (using the SPT9400 video driver) may be added.

FOUR-BIT TITLE/GRAPHICS MULTIPLEXING FUNCTION

Graphics from a 16-entry color lookup table can be arbitrarily displayed. In chroma mode it is possible to superimpose graphics and video input by specifying transparent colors. In the external key mode it is possible to display graphics in the areas specified pixel by pixel.

HOST INTERFACE

The operational modes and parameters of the SPT2210 can be changed via a MPU host parallel interface. The following parameters can be changed:

- Low-pass filter
- Switching between Y/C output and composite output
- Switching between two's complement or offset binary data format
- Selecting between seven video modes
- 50%, Y, Y/C and color enable/disable
- Color bar test pattern
- Color kill (monochrome only out)
- Graphics mode control
- Software reset
- Select Y/C 4:2:2 or 4:1:1 input format
- Change of the Cr/Cb sampling order
- Interpolation field changeover
- Vertical interpolation filter bypass
- Free run or reset of subcarrier phase
- Turn off/on NTSC setup
- Suspend mode
- Input logic polarity set
- V Blank_ timing adjust
- H Blank_ timing adjust

EXTERNAL SETTING PINS

In addition to host interface control, the SPT2210 can be operated independent of host interface using external pin control. The external pin controls available are listed below:

- Select between seven video modes
- Sync/Blank I/O mode
- Output of the built-in color bars
- Free run or reset of subcarrier phase
- Switching between Y/C output and composite output
- Turn off/on NTSC setup

See the External Setting Pin Descriptions section for operation.

Table II – Y/C Video Encoder Pin Functions

Signal Name	Pin Numbers	I/O	Function
Digital Video Inputs and Controls			
YD7...0	1-8	I	Luminance Digital Input (YD0 = LSB) (TTL Level)
CD7...0	57-64	I	Color Difference Digital Input (CD0 = LSB) (TTL Level)
CBF	11	I	Cr/Cb Sampling Order Control (TTL Level)
BLANK_	12	I	External Blanking Control Signal Input (TTL Level)
FIELD	16	I	Field Indicator Signal (TTL Level)
V	13	I/O	Vertical Synchronization Signal Input (TTL Level)
H	14	I/O	Horizontal Synchronization Signal Input (TTL Level)
KEY	17	I	Keying Signal Input (TTL Level)
GD3...0	18-21	I	CLUT Ram Address (GD0 = LSB) (TTL Level)
VRTENB	15	I	Vertical Interpolation Enable (TTL Level)
SUSPEND	43	I	Suspend Mode Enable/Disable
Video Outputs			
Y	53	O	Luminance or Composite Video Analog Signal Output (1 V _{P-P})
C	49	O	Chrominance Video Analog Signal Output (1 V _{P-P}) (Includes burst)
V _{REF}	46	I	Internal D/A Reference Voltage Input
V _{CS}	47	I	Internal D/A Output Signal Amplitude Control Voltage
MPU Interface and Clock			
D7...0	29-32,36-39	I/O	Address/Data Bus (TTL Level)
CS_	22	I	Chip Select (TTL Level)
RS	23	I	Register Select (TTL Level)
RD_	24	I	Read from Data Bus (TTL Level)
WR_	25	I	Write to Data Bus (TTL Level)
RESET_	26	I	Reset Signal Input (TTL Level)
CLK	34	I	System Clock Input (Pixel Clock)
TEST	42	I	Test Mode Enable/Disable
Power Supply Connections			
V _{DD}	10,28,35,41,56	-	+3.3 V Power Supply for Digital Circuitry
AV _{DD}	44,52	-	+3.3 V Power Supply for Analog Circuitry
GND	9,27,33,40,55	-	Ground for Digital Circuitry
AGND	45,48,54	-	Ground for Analog Circuitry

DESCRIPTION OF PIN FUNCTIONS

DIGITAL VIDEO INPUTS AND CONTROLS

YD7...0 Pins

The luminance signal digital data is input on YD7...0 (TTL level). The input can be in either offset binary or two's complement format. The range of the input data is bounded from 16 to 235. Any data less than 16 is converted to 16 and data greater than 235 is converted to 235. The active pixels will be output after completion of the back porch as shown in figure 2. YD7 is the MSB and YD0 is the LSB.

CD7...0 Pins

The color difference digital data is input on CD7...0 (TTL level). The input can be in either offset binary or two's complement format. The input range of the offset binary mode is from 16 to 240, and the input range of the two's complement mode is from -112 to +112. Signal data is bounded to these minimum and maximum limits.

As a means of dealing with abnormal data, color kill is carried out when 00(H) or FF(H) is detected for two successive clocks or more at CD7...0 (automatic color kill mode). Color kill is immediately cancelled when data other than 00(H) or FF(H) are entered.

The order of Cr and Cb is determined by the combination of the CBF pin (described below) and the Cr/Cb inversion bit, D2 (data bit 2), of the command register CR1. In normal setup mode (Cr/Cb inversion bit = 0 and CBF pin = 1) and 4:2:2 format, the input is started with the Cb data and, after that, Cr and Cb are repeated alternately. (Refer to figure 1.)

In the 4:1:1 format only (with normal CBF setup) the first and the second data positions in time are used, and the third and fourth data are ignored (or not present). (Refer to figure 1.) The first data is repeated again after the fourth data. The active pixels are output after the back porch as shown in figure 2. CD7 is the MSB and CD0 is the LSB.

CBF Pin

This is the Cr/Cb control pin. It determines the sampling order of Cr/Cb. When the command register CR1, data bit 2, (Cr/Cb inversion) is low (clear), the CBF pin is input as positive true logic. (See the Command Register Descriptions.) When CBF is high, the SPT2210 samples the data as Cb after the leading edge of HSYNC_ and the back porch has occurred. When CBF is low, the SPT2210 samples the data as Cr after the leading edge of HSYNC_ and the back porch has occurred.

When the command register CR1, data bit 2, (Cr/Cb Inversion) is high (set), the CBF pin is input as negative logic. (See the Command Register Descriptions.) In this mode the CBF pin is read as inverted.

Figure 1 – Y/C Data Input Format (CBF=High, CR1:D2=0)

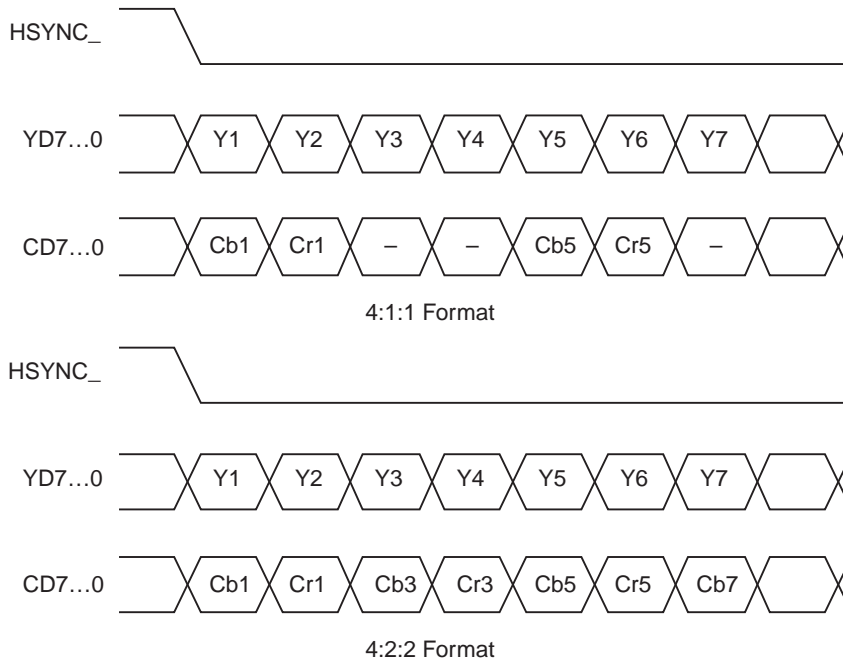
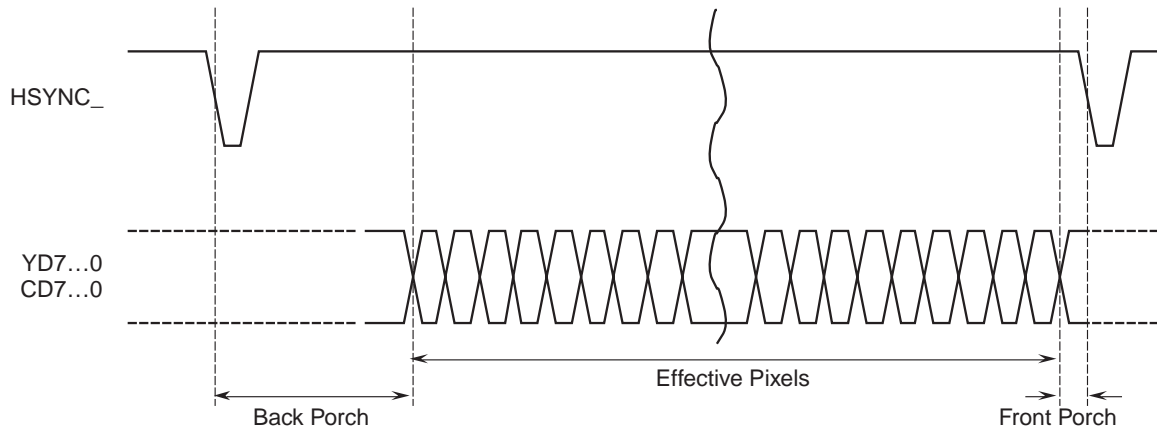
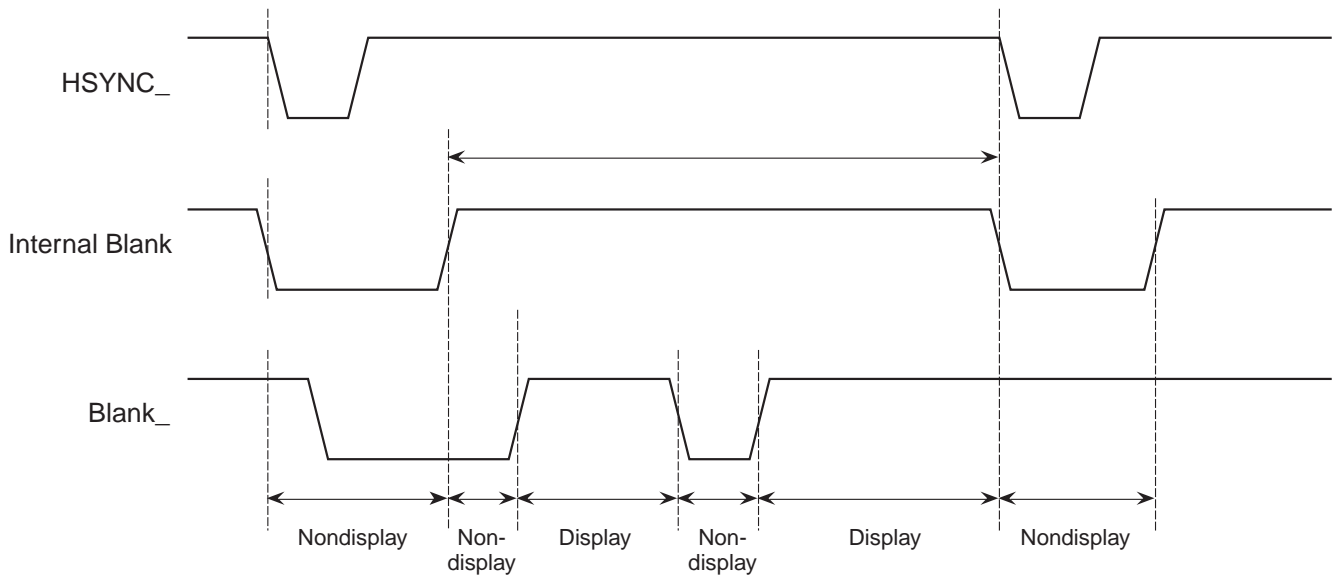


Figure 2 – Y/C Data Input Timing



Operation Mode	Number of Effective Pixels	Back Porch	Front Porch
NTSC CCIR 601	720 Clocks	122 Clocks	16 Clocks
NTSC Square Pixel	640 Clocks	120 Clocks	20 Clocks
NTSC 4Fsc	768 Clocks	124 Clocks	18 Clocks
PAL CCIR 601	720 Clocks	132 Clocks	12 Clocks
PAL Square Pixel (14.75)	768 Clocks	152 Clocks	24 Clocks
PAL 4Fsc	948 Clocks	164 Clocks	23 Clocks
PAL Square Pixel (12.18)	640 Clocks	120 Clocks	20 Clocks

Figure 3 – Set of BLANK_ Terminal and Display/Nondisplay



Blank_ Pin

This is the input pin for the external blanking control signal (TTL level). The SPT2210 samples BLANK_ at the rising edge of CLK. When BLANK_ is high, the output proceeds with normal operation and when it is low the output signal gets blanked (i.e., no display). The specification of the blank state can be performed on a pixel-by-pixel basis.

The chip has an internal blanking function that operates independent of the external blanking signal. Figure 3 shows operation of the internal blanking in conjunction with external blanking. Table III delineates the internal blanking that is generated regardless of the level of the blank pin, upon detection of HSYNC_.

Table III – Internal Blanking Periods for NTSC and PAL

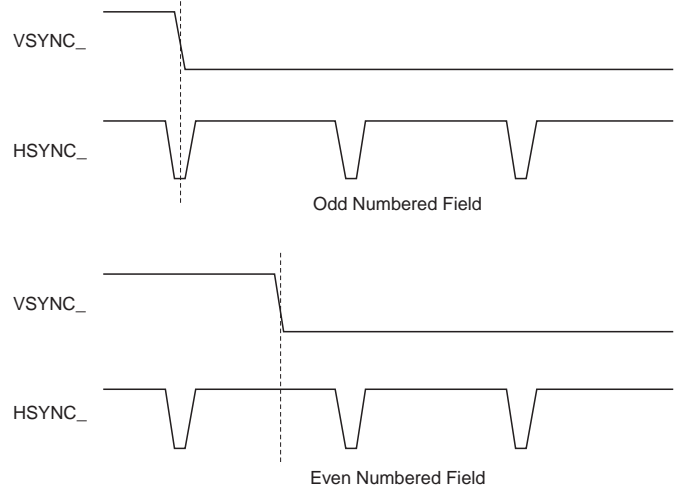
	NTSC	PAL
Lines	1 to 20	1 to 23
Lines	263 to 283	310 to 335
Line(s)	525	623 to 625

V Pin

This input pin provides the timing to generate the vertical signal out of the SPT2210. The mode of operation for this pin is controlled by Command Register, CR5. The sampling of the sync signal occurs on the rising edge of clock. When the Vsync input signal is asserted during an Hsync signal the field is considered to be odd, else the field is even. (Refer to figure 4.)

When in the blank operational mode the field is determined by the field input signal.

Figure 4 – Sync Signal Input Timing



H Pin

This input pin provides the timing to generate the horizontal signal out of the SPT2210. The mode of operation for this pin is controlled by Command Register, CR5. The sampling of the sync signal occurs on the rising edge of clock. When the timing for Hsync/Hblank input is different from the number of clock cycles shown in table IV, the phase of the subcarrier will be put into free-run.

Since the horizontal blanking period in Figure 2 is determined internally, the width and the trailing edge of HSYNC_ are not detected. The active pixels are output after the completion of the back porch as shown in figure 2.

Table IV – Expected Line Clock Count for Various Modes

Video Mode	Clocks
NTSC 4Fsc	910
NTSC Square Pixel	780
NTSC CCIR 601	858
PAL 4Fsc	1135
PAL Square Pixel ($f_s = 14.75$ MHz)	944
PAL Square Pixel ($f_s = 12.1875$ MHz)	780
PAL CCIR 601	864

FIELD

This is an input signal controlled by CR5. It is sampled on the leading edge of the clock cycle. It indicates the field odd or even and is required in the Blank mode. High level indicates ODD and low level indicates EVEN field.

TEST

This is an input signal. During normal operation it is set to a logic low. Test functions of the device are enabled by taking this pin to a logic high.

SUSPEND

This input pin is set to a logic low for normal operation. When set to a logic high, the SPT2210 suspends operation and no output is active. This includes taking in data from either the MPU data ports or video data.

KEY Pin

This is the external key input pin (TTL level). Input from this pin is enabled when the external key mode is activated by setting the command register CR1 bits to D1 = 1 and D0 = 1. (See the Command Register Descriptions section.) When KEY is high, the colors of the contents of color lookup table (CLUT) that is specified by means of GD3...0 are displayed. When KEY is low, the data of YD7...0 and CD7...0 are output. This mode is called the external key mode.

GD3...0 Pins

These are the graphic data input pins (TTL level). This 4-bit input port specifies which one of the 16 color entries in the CLUT is to be output for the current pixel. If GD3...0 is all low when the SPT2210 is in chroma mode, the CLUT output is transparent and the data of the YD7...0 and CD7...0 ports are output. (This assumes that the transparent color was not changed in Address 0H of the CLUT.) Refer to the Color Lookup Table (CLUT) Description section.

VRTENB Pin

This is the vertical interpolation enable signal input pin (TTL level). When VRTENB is high, vertical interpolation is enabled and when it is low, vertical interpolation is disabled.

N/C Pins

These are no connect pins.

VIDEO OUTPUTS

Y Pin

This is the luminance or composite analog output signal pin. The Y output pin is a current source capable of driving a 75 Ω load terminated to ground to 1 V_{P-P} . The encoded analog luminance or composite signal is output on this pin.

C Pin

This is the chroma analog output signal pin. The C output pin is a current source capable of driving a 75 Ω load terminated to ground to 1 V_{P-P} . The chroma signal is output on this pin.

V_{REF} Pin

This is the reference voltage input pin for the internal D/A converters. A 0.1 μ F capacitor and voltage divider of 6.8 k Ω and 5.1 k Ω resistors should be connected to this pin from +3.3 V.

V_{CS} Pin

This is the control voltage for the output amplitude of the internal D/A converters. The D/A output amplitude can be adjusted from 1.0 to 1.4 V_{P-P} using this pin.

MPU INTERFACE AND CLOCK

D7...0 Pins

These are the address and data input/output bus pins (TTL level). This is a bidirectional 8-bit bus. D7 is the MSB and D0 is the LSB. When the CS_ (chip select) pin is high, the D7...0 bus is in a high impedance state.

The SPT2210 features the ability to run without an external MPU host. In this mode, D7...0 and RS (Register Select) pins can be used as external setting pins. The D7...0 pins and RS pin become external setting pins when CS_, RD_ (Read Enable) and WR_ (Write Enable) are low for three clock cycles or more. Refer to the External Setting Pin Descriptions section for more details.

CS_ Pin

This is the chip select input pin (TTL level). The SPT2210 is selected for read/write operation when this pin is low. The CS_ pin is also used in enabling the external pin mode. Refer to the External Setting Pin Descriptions section for more details.

RS_ Pin

This is the register select input pin (TTL level). The D7...0 pins operate as either address or data registers (except when operating as external setting pins). The RS_ pin determines the mode in which D7...0 will operate. When RS_ is low the D7...0 bus is switched to the address bus mode, and when it is high the bus is switched to the data bus mode. The RS_ pin is also used as an external pin in the external pin mode. Refer to the External Setting Pin Descriptions section for more details.

RD_ Pin

This is the read enable input pin (TTL level). The data on D7...0 is read out of the SPT2210 on the leading edge of a high-to-low transition of RD_. If RS_ is high, the data is read from the internal register specified by the last address write. If RS_ is low, the current address value is read from the address register. The RD_ pin is also used in enabling the external pin mode. Refer to the External Setting Pin Descriptions section for more details.

WR_ Pin

This is the write enable input pin (TTL level). The data on D7...0 is written into the address or command register on the leading edge of a high-to-low transition of RD_. If RS_ is high, the data is written into the internal command register specified by the last address write. If RS_ is low, the data is written into the address register. The WR_ pin is also used in enabling the external pin mode. Refer to the External Setting Pin Descriptions section for more details.

Reset Pin

This is the reset input pin (TTL level). The reset input is sampled on the leading edge of the system clock (CLK). The SPT2210 is initialized by holding the RESET_ pin low for a minimum of five clock cycles. The SPT2210 will come out of reset five clock cycles after the RESET_ pin has been brought back high.

CLK Pin

This is the system clock input pin (TTL level). The YD7...0, CD7...0, GD3...0, BLANK_, V, H, Field and KEY pins are all sampled on the rising edge of the CLK signal. Additionally, when an asynchronous access from the MPU is processed, the access is synchronized with this clock and then the processing is carried out.

When the clock is switched over to another operating frequency (i.e., changing video modes), the SPT2210 should be reset once to ensure proper operation. In this case, the command registers will need to be set again.

V_{DD} Pins

These are the +3.3 V power supply pins for the digital circuitry.

AV_{DD} Pins

These are the +3.3 V power supply pins for the analog circuitry. V_{DD} and AV_{DD} are completely independent of each other. Be sure to keep the following operating condition:

$$|V_{DD} - AV_{DD}| \leq 0.5 \text{ V.}$$

GND Pins

These are the ground pins for the digital circuitry.

AGND Pins

These are the ground pins for the analog circuitry. Since GND and AGND are completely independent of each other, it is necessary to keep them at the same electric potential by externally tying them together through a ferrite bead.

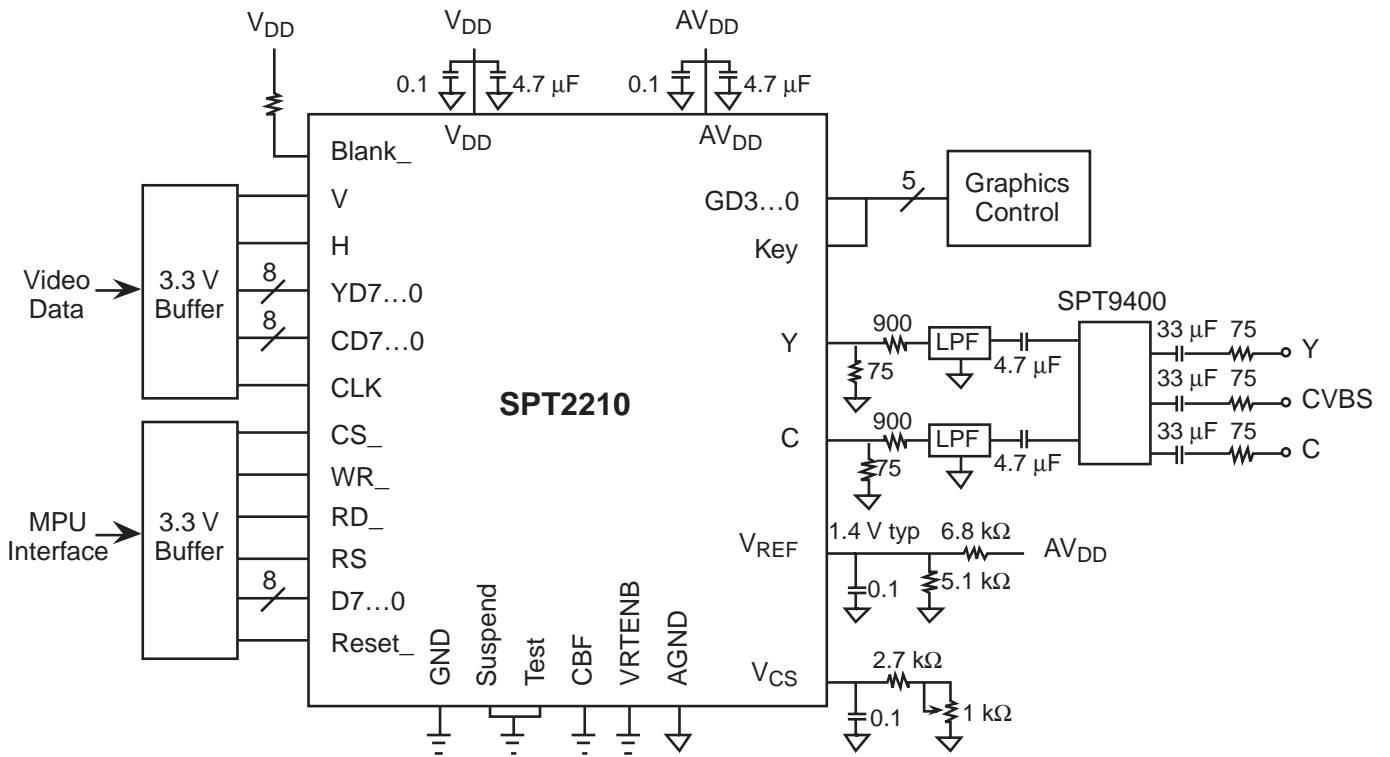
Internal Pullup and Pulldown Resistors

The following pins are either pulled up or down with an internal resistor of approximately 100 k Ω :

Pins with internal pulldown: CD7...0, YD7...0, GD3...0, KEY, VRTENB, TEST, SUSPEND.

Pins with internal pullup: RESET_, BLANK_, V, H, CS_, RD_, WR_, D7...0, CBF, RS, CLK.

Figure 5 – Typical Interface Circuit



REGISTER FUNCTIONS

GENERAL DESCRIPTION

There are two general types of registers in the SPT2210. One type is a command register and the other is a color lookup table (CLUT). Table V shows the register mapping for both types of registers. A third register is the address register that enables access to command registers and the CLUT.

Table V – Register Map

Address	Register Name	Default Value	
00H	Command Register 1	02H	
01H	Command Register 2	01H	
02H	Command Register 3	00H	
03H	Suspend	00H	
04H	HV I/O	00H	
05H	HV Timing	00H	
06H	Background Control	00H	
07-0FH	Reserved	----	
10H	CLUT Entry 0	00,80,80	Transparent
11H	CLUT Entry 1	28,70,F0	100% Blue
12H	CLUT Entry 2	50,F0,58	100% Red
13H	CLUT Entry 3	6C,E0,C8	100% Magenta
14H	CLUT Entry 4	90,20,38	100% Green
15H	CLUT Entry 5	A8,10,A8	100% Cyan
16H	CLUT Entry 6	D0,90,10	100% Yellow
17H	CLUT Entry 7	EC,80,80	100% White
18H	CLUT Entry 8	Not Used	
19H	CLUT Entry 9	1C,78,B8	50% Blue
1AH	CLUT Entry 10	30,B8,70	50% Red
1BH	CLUT Entry 11	40,B0,A8	50% Magenta
1CH	CLUT Entry 12	50,50,58	50% Green
1DH	CLUT Entry 13	60,48,90	50% Cyan
1EH	CLUT Entry 14	74,88,48	50% Yellow
1FH	CLUT Entry 15	80,80,80	50% White

COMMAND REGISTER DESCRIPTIONS

Tables VI through XV give detailed descriptions for programming the SPT2210 command registers.

COMMAND REGISTER DESCRIPTIONS

COMMAND REGISTER CR1

CR1 (Address = 00H)



Table VI – Command Register CR1 Description Table

Address	Bit #	Function	Bit Setting /Description		Default
00H	7	Software reset	0	Normal operation	02H
			1	Reset; all registers returned to default	
	6	Test bar	0	Normal operation	
			1	Color test bar is generated	
	5	Not used	0	Use fixed at 0	
			1		
	4	Not used	0	Use fixed at 0	
			1		
	3	Color kill	0	Normal operation	
			1	Monochromatic (black and white) image is output	
	2	Cr/Cb inversion	0	According to the order specified by the CBF pin	
			1	According to the order specified by the inverted CBF pin	
	1,0	Chroma key control. Set multiplex mode of YD7...0 and CD7...0 video input, and GD3...0 graphics input		See table VII	

Table VII – Multiplexing Mode (Command Register 1)

D1	D0	Mode	Operation
0	0	Graphics Mode	GD3...0 is displayed irrespective of the KEY terminal pin state. The transparent color cannot be specified in this mode.
0	1	Video Mode	YD7...0 and CD7...0 are always selected irrespective of the state of the KEY terminal.
1	0	Chroma Key Mode	YD7...0 and CD7...0 are displayed only at the parts in which transparent colors are specified by means of GD3...0. GD3...0 is displayed in all other parts.
1	1	External Key Mode	YD7...0 and CD7...0 are displayed when the KEY terminal pin is set to logic 0. GD3...0 is displayed when the KEY terminal is set to logic 1. Transparent colors cannot be specified in this mode.

COMMAND REGISTER DESCRIPTIONS

COMMAND REGISTER CR2

CR2 (Address = 01H)

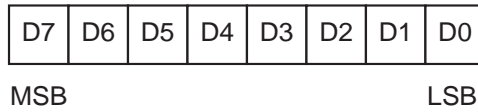


Table VIII – Command Register CR2 Description Table

Address	Bit #	Function	Bit Setting/Description		Default
01H	7	Low pass filter bypass (U/V filters)	0	Enabled	01H
			1	Disabled (bypassed)	
	6	Not used	0	Use fixed at 0	
			1		
	5	Not used	0	Use fixed at 0	
			1		
	4	Composite video enable	0	Component mode: Luminance signal output through the Y pin	
			1	Composite mode: Composite signal output through the Y pin	
	3	Color data format on CD7...0	0	Offset binary	
			1	Two's complement	
2,1,0	Video mode selection		See table IX		

Table IX – Video Mode (Command Register 2)

D2	D1	D0	Operation Mode
0	0	0	NTSC 4Fsc
0	0	1	NTSC square pixel
0	1	0	NTSC CCIR 601 525/60
0	1	1	Setting disabled
1	0	0	PAL 4Fsc
1	0	1	PAL square pixel, $f_S = 14.7500$ MHz
1	1	0	PAL CCIR 601 625/50
1	1	1	PAL square pixel, $f_S = 12.1875$ MHz

COMMAND REGISTER DESCRIPTIONS

COMMAND REGISTER CR3

CR3 (Address = 02H)

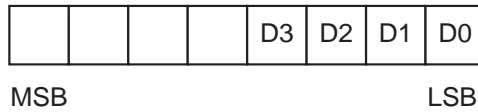


Table X – Command Register CR3 Description Table

Address	Bit #	Function	Bit Setting /Description		Default
02H	7-4	Not used	Fix at 0		00H
	3	Odd/even vertical interpolation field	0	Start at ODD field	
			1	Start at EVEN field	
	2	Vertical interpolation bypass	0	Normal operation	
			1	Vertical interpolation is bypassed	
	1	Phase free run (NTSC only)	0	Subcarrier phase is reset every odd frame	
			1	Subcarrier free run (i.e., not reset)	
	0	Setup enable (NTSC only)	0	Setup enabled	
1			No setup		

SUSPEND REGISTER

(Address = 03H)

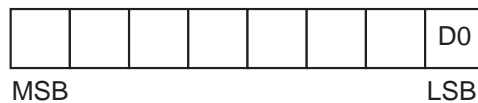


Table XI – Suspend Register Description Table

Address	Bit #	Function	Bit Setting /Description		Default
03H	7-1	Not used	Fix at 0		00H
	0	Suspend mode	0	Normal operation	
			1	Suspend	

COMMAND REGISTER DESCRIPTIONS

H/V I/O REGISTER

(Address = 04H)

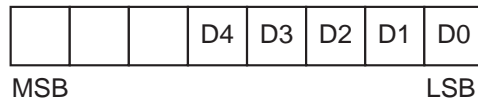


Table XII – H/V I/O Register Description Table

Address	Bit #	Function	Bit Setting /Description		Default
04H	7-5	Not used	Fix at 0		00H
	4	Field polarity	0	Positive logic. High level = Odd field	
			1	Negative logic. High level = Even field	
	3	V signal (VSYNC and VBLNK) polarity	0	Positive logic	
			1	Negative logic	
	2	H signal (HSYNC and HBLNK) polarity	0	Positive logic	
			1	Negative logic	
	1	Blank I/O	0	HBLNK/VBLNK/FIELD output mode	
			1	HBLNK/VBLNK/FIELD input mode	
	0	Timing I/O	0	HSYNC/VSYNC input mode	
1			HBLNK/VBLNK/FIELD I/O mode		

H/V TIMING REGISTER

(Address = 05H)

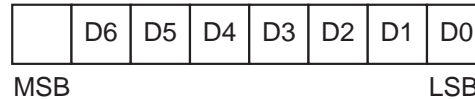


Table XIII – H/V Timing Register Description Table

Address	Bit #	Function	Bit Setting /Description		Default
05H	7	Not used	Fix at 0		00H
	6-5	Vertical Blank timing	00	1V=240H	
			01	1V=241H	
			10	1V=242H	
			11	Not used	
4-0	Horizontal Blank timing	See table XIV			

Table XIV – Horizontal Blank Timing Control (H/V Timing Register)

D4....D0	HBLNK Timing	D4....D0	HBLNK Timing
01111	+15 clocks from the original point.	10001	-1 clock from the original point.
01110	+14 clocks from the original point.	10010	-2 clocks from the original point.
⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮
00001	+1 clock from the original point.	11110	-14 clocks from the original point.
00000	+0 (Default: original point)	11111	-15 clocks from the original point.

COMMAND REGISTER DESCRIPTIONS

BACKGROUND CONTROL

(Address = 06H)

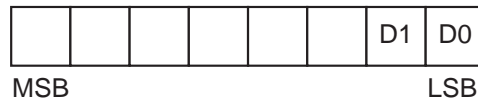


Table XV – Background Control Description Table

Address	Bit #	Function	Bit Setting /Description		Default
06H	7-2	Not used	Fix at 0		00H
	1	Half Y/C and 50% Color Enable. Input Y value is reduced by 50% and C is replaced with CLUT15 Cb/Cr data	0	Half Y/C and 50% Color Disable	
			1	Half Y/C and 50% Color Enable	
	0	Half Y/C Enable. Input Y/C value is reduced by half.	0	Half Y/C Disable	
			1	Half Y/C Enable	

ACCESSING THE COMMAND REGISTERS

Access to the command registers for read or write purposes is performed in the following sequence. It requires the correct setting of the control lines and setting the data on the bidirectional 8-bit data bus.

Command Register Read and Write Operation

Address Setup:

- Set CS_, RS low.
- Set the data bus to the address required, then set WR_ low.
- Set WR_ high, then CS_ and RS high.

This completes the address write and points to the register that may be read from or written to.

Register Read:

- After completing address setup, Set CS_ low, RS high.
- Set RD_ low, this enables the data from the pointed-to register onto the data bus.
- Set RD_, CS_ and RS high.

This completes the register read operation; subsequent reads from the same register may be performed, if the address has not been changed.

Register Write:

- After completing address setup, set CS_ low, RS high.
- Set the data required onto the data bus, then set WR_ low.
- Set WR_, CS_ and RS high, then release data bus input data.

This completes the register write operation; subsequent writes to the same register may be performed, if the address has not been changed.

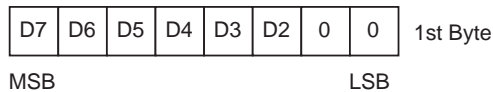
COLOR LOOKUP TABLE (CLUT) DESCRIPTION

CLUT FORMAT AND DATA LIMITS

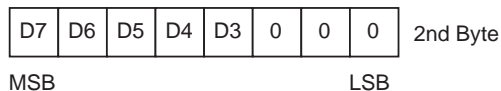
The CLUT has 16 entries and is set up in YCrCb three-byte format. (See below.) The upper 6 bits in the Y data are used (lower two are filled with zero) and the upper 5 bits in the Cr/Cb data are used (lower 3 bits are filled with zero). Therefore the setting ranges are Y = 00H to FCH (midpoint value = 80H) and Cr and Cb = 00H to F8H (midpoint value = 80H).

The numerical values of Cr and Cb are expressed in offset binary form, irrespective of the setting of bit D3 in Command Register 2. Since no limit processing is carried out in connection with the CLUT data entries, it is necessary to set Y within the limits of 16 to 236 (10H to ECH) and Cr/Cb within the limits of 16 to 240 (10H to F0H).

Bit composition of Y (address=10H~1FH)



Bit composition of Cr (offset binary, address=10H~1FH)



Bit composition of Cb (offset binary, address=10H~1FH)



TRANSPARENT COLOR

Transparent colors can be used in chroma key mode (See Combining Video and Graphics Signals for more details.) Transparent colors can be entered in the CLUT with the following data values for Y, Cr and Cb:

$$Y = 00H, Cr = 80H, Cb = 80H$$

When these data values are selected in the CLUT, the graphics data becomes transparent and the SPT2210 displays the video YD7...0 and CD7...0 data instead.

COLOR SPACE CONVERSION FROM RGB TO YCRCB FOR CLUT ENTRY

The SPT2210 CLUT stores data in YCrCb format only. RGB graphics data must be converted in the host before loading the CLUT. The conversion for RGB to YCrCb is shown here:

$$Y = 0.2990 \times R + 0.5770 \times G + 0.1140 \times B$$

$$Cr = 0.5000 \times R - 0.4187 \times G - 0.0813 \times B + 128$$

$$Cb = 0.1684 \times R - 0.3316 \times G + 0.5000 \times B + 128$$

Example: Assume that each RGB data is 8 bits in length and that their values are R = 120, G = 96, B = 96. The

values of Y, Cr and Cb are given by the following calculations:

$$Y = 0.2990 \times 120 + 0.5770 \times 96 + 0.1140 \times 96 = 102$$

$$Cr = 0.5000 \times 120 - 0.4187 \times 96 - 0.0813 \times 96 + 128 = 140$$

$$Cb = 0.1684 \times 120 - 0.3316 \times 96 + 0.5000 \times 96 + 128 = 124$$

Since the SPT2210 CLUT only uses the upper 6 bits in the Y data and the upper 5 bits in the Cr/Cb data, it is necessary to round the results above. The second bit is rounded in the Y calculation and the third bit is rounded in the Cr and Cb calculation. The results are shown below:

$$Y = 102 = 01100110 \text{ (binary)} \text{ results in } 01101000 \text{ (binary)} = 104$$

$$Cr = 140 = 10001100 \text{ (offset binary)} \text{ results in } 10010000 \text{ (offset binary)} = 144$$

$$Cb = 124 = 01111100 \text{ (offset binary)} \text{ results in } 10000000 \text{ (offset binary)} = 128$$

ACCESSING THE COLOR LOOKUP TABLE

The method for accessing the CLUT is different from the method for accessing the command registers because each entry of the CLUT has a length of 3 bytes at each address. The CLUT is accessed by means of three successive bytes after writing the address. Note that Y, Cr and Cb cannot be accessed individually in the CLUT. They must be accessed in units of three bytes sequentially.

Color Lookup-table Register Read and Write Operation

Address Setup:

- Set CS_, RS low.
- Set the data bus to the address required (10H – 1FH), then set WR_ low.
- Set WR_ high, then CS_ and RS high.

This completes the address write and points to the CLUT registers that may be read from or written to.

Register Read:

- After completing address setup, Set CS_ low, RS high.
- Set RD_ low; this enables the data from the pointed-to register onto the data bus (first byte, Y data).
- Set RD_ high, then set RD_ low; this enables the data from the pointed-to register onto the data bus (second byte, Cr data).
- Set RD_ high, then set RD_ low; this enables the data from the pointed-to register onto the data bus (third byte, Cb data).
- Set RD_, CS_ and RS high.

This completes the three-byte sequence of CLUT register read operation at the specified address.

Register Write:

After completing address setup, set CS_ low, RS high.
 Set the data required onto the data bus, then set WR_ low and then back high; this will write the Y data.
 Set the data required onto the data bus, then set WR_ low and then back high; this will write the Cr data.
 Set the data required onto the data bus, then set WR_ low and then back high; this will write the Cb data.
 Set WR_, CS_ and RS high, then release data bus input data.

This completes the three-byte sequence of the CLUT register write operation at the specified address.

COMBINING VIDEO AND GRAPHICS SIGNALS

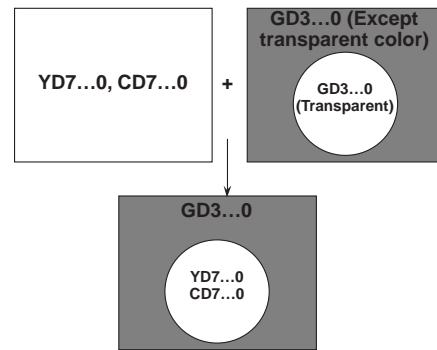
EXTERNAL KEY MODE

The external key mode is selected by setting the command register CR1, bits D1...0 = 11 (binary). In this mode it is possible to combine the video signals (YD7...0, CD7...0) with the graphics signals (GD3...0). When the KEY pin is high, in conformity with the timing shown in figure 8, the graphics signals (out of the CLUT and referenced by GD3...0) are output (i.e., displayed). This can be done on a pixel-by-pixel basis.

CHROMA MODE

The chroma key mode is selected by setting the command register CR1, bits D1...0 = 10 (binary). In this mode the graphics signal image becomes the front image, and the Y/C image becomes the rear image. The Y/C image is displayed in the portions of the display in which the transparent colors are specified in the graphics image data stream. Figure 6 illustrates the combining of video and graphics images in the chroma mode.

Figure 6 – Multiplex in Chroma Mode



VERTICAL INTERPOLATION

The SPT2210 has a vertical interpolation filter that is used to reduce jaggy noise and flicker. It also supports the high resolution mode for Video CD, version 2.0.

INTERPOLATION FIELD SELECTION

The vertical interpolation filter is active for each odd or even field as specified in command register CR3, bit D3. However, vertical interpolation is not active for NTSC line 21 and PAL line 25 when the ODD field is selected (CR3, bit D3 = 0) and NTSC line 285 and PAL line 336 when the EVEN field is selected (CR3, D3 = 1).

INTERPOLATION BYPASS

Vertical interpolation is automatically enabled and disabled for the proper even/odd field depending on the field selection specified in CR3, bit D3. The VRTENB pin enables interpolation, in conjunction with the even/odd field algorithm, as shown in figures 7 and 8. The interpolation filter may be bypassed altogether by setting bit D2 in command register CR3 or setting the VRTENB pin to logic low.

Figure 7 – Vertical Interpolation Timing CR3 D2=0, D3=1; Even Field

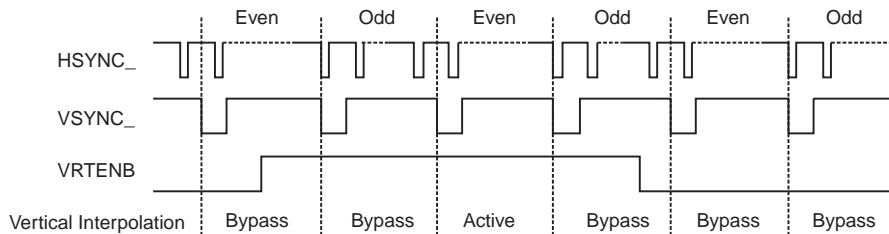
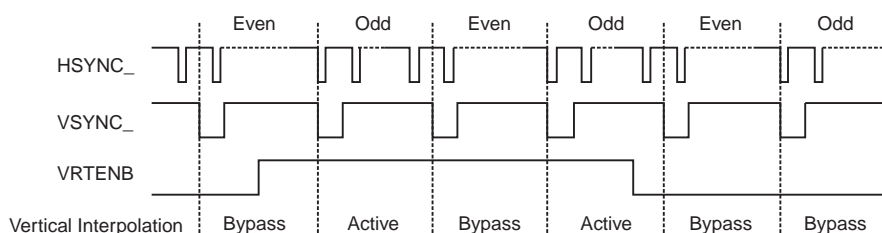


Figure 8 – Vertical Interpolation Timing CR3 D2=0, D3=0; Odd Field



EXTERNAL SETTING PIN DESCRIPTIONS

The SPT2210 has the capability of operating without a host interface and allowing certain programmable settings to be accessed via external pins. When the RD_, WR_ and CS_ pins are all held (or tied) low for a minimum of three clock pulses, the D7...0 bus and the RS pin can be used for external setting of various modes and functions. (When these pins are not used as external setting pins, they are ordinary pins for host interface.)

Table XVI below shows the pin function assignments and settings for the D7...0 and RS pins.

Figure 9 – Multiplexing in the External Key Mode

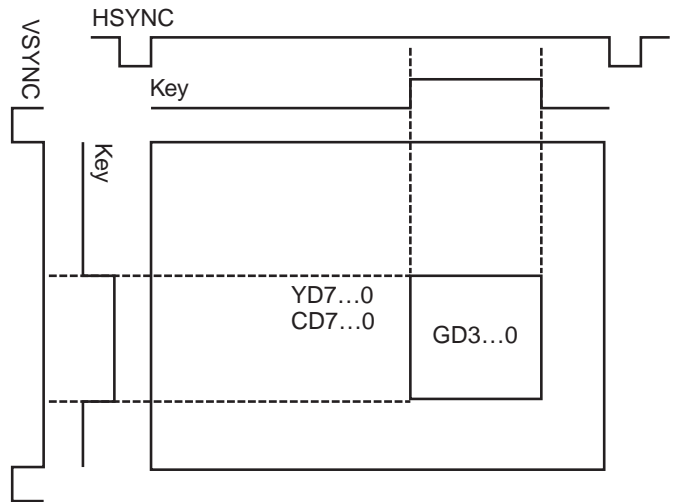


Table XVI – D7...0 and RS Pin External Setting Description Table

Pin #	Function	Bit Setting			Description
D7	Composite video mode	0			Y/C (S-Video)
		1			Composite video
D6	Color bars	0			Normal operation
		1			Generate color bars
D5	Phase reset (NTSC only)	0			Subcarrier phase is reset at every odd frame
		1			Free run; subcarrier phase is not reset
D4,3	SYNC/BLNK I/O	D4	D3		SYNC, BLNK, I/O
		0	0		BLNK Input
		0	1		SYNC Input
		1	0		BLNK Output
		1	1		Reserved
D2...0	Video mode setting	D2	D1	D0	Mode
		0	0	0	NTSC 4Fsc
		0	0	1	NTSC Square Pixel
		0	1	0	NTSC CCIR 601 525/60
		0	1	1	Setting disabled
		1	0	0	PAL 4Fsc
		1	0	1	PAL Square Pixel ($f_S=14.7500$ MHz)
		1	1	0	PAL CCIR 601 625/50
		1	1	1	PAL Square Pixel ($f_S=12.1875$ MHz)
RS	Setup (NTSC only)	0			Setup enabled
		1			No setup

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25 °C

Supply Voltages

V _{DD}	V _{SS} -0.3 to V _{SS} +4.6 V
AV _{DD}	V _{SS} -0.3 to V _{SS} +4.6 V

Input/Output Voltages

Digital Inputs	V _{SS} -0.3 to V _{DD} +0.3 V
Digital Outputs	V _{SS} -0.3 to V _{DD} +0.3 V

Temperature

Operating Temperature	0 to 70 °C
Junction Temperature	150 °C
Lead Temperature (soldering 10 seconds)	300 °C
Storage Temperature	-40 to +125 °C

Note:1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, AV_{DD}=V_{DD}=+5.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNIT
Analog Outputs						
Differential Linearity					±0.5	LSB
Integral Linearity					±1.0	LSB
Output Full-Scale Current				13		mA
Digital Inputs						
Reset Pin						
V _{IH}			0.7 x V _{DD}			V
V _{IL}					0.3 x V _{DD}	V
I _{IH}	V _{IH} = V _{DD}		-10		10	µA
I _{IL}	V _{IL} = V _{SS}		-10		10	µA
Digital Outputs						
V _{OH}	I _{OH} = -4 mA		2.4			V
V _{OL}	I _{OL} = 4 mA			0.4		V
Power Supply						
V _{DD}			3.0		3.6	V
AV _{DD}			3.0		3.6	V
V _{DD} -AV _{DD}			-0.5		+0.5	V
I _{DD}	V _{DD} =+3.3 V, f=17.73 MHz			50		mA
Timing Characteristics						
CS Setup (TCSS)			10			ns
CS Hold (TCSH)			10			ns
RS Setup (TRSS)			10			ns
RS Hold (TRSH)			10			ns
RDWR_ Pulse Low (TRWL)			1 X TCC			
RDWR_ Pulse High (TRWH)			1 X TCC			
Delay to Data Bus Valid (TDBV)	C _L =50 pF				25	ns
Output Data Delay Time (TDLY)	C _L =50 pF		3		20	ns
Data Output Disable (TDOD)					20	ns
Data Output Hold (TDOH)			3			ns
Write Data Setup (TWDS)			10			ns
Write Data Hold (TWDH)			10			ns
Clock Cycle (TCC)			56			ns
Clock Pulse High (TCH)			20			ns
Clock Pulse Low (TCL)			20			ns
Input Data/Cont Setup (TIS)			10			ns
Input Data/Cont Hold (TIH)			10			ns
Reset Pulse Width (TRSW)			5 X TCC			ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at $T_A = +25\text{ }^\circ\text{C}$, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at $T_A = +25\text{ }^\circ\text{C}$. Parameter is guaranteed over specified temperature range.

Figure 10 – MPU Interface Timing

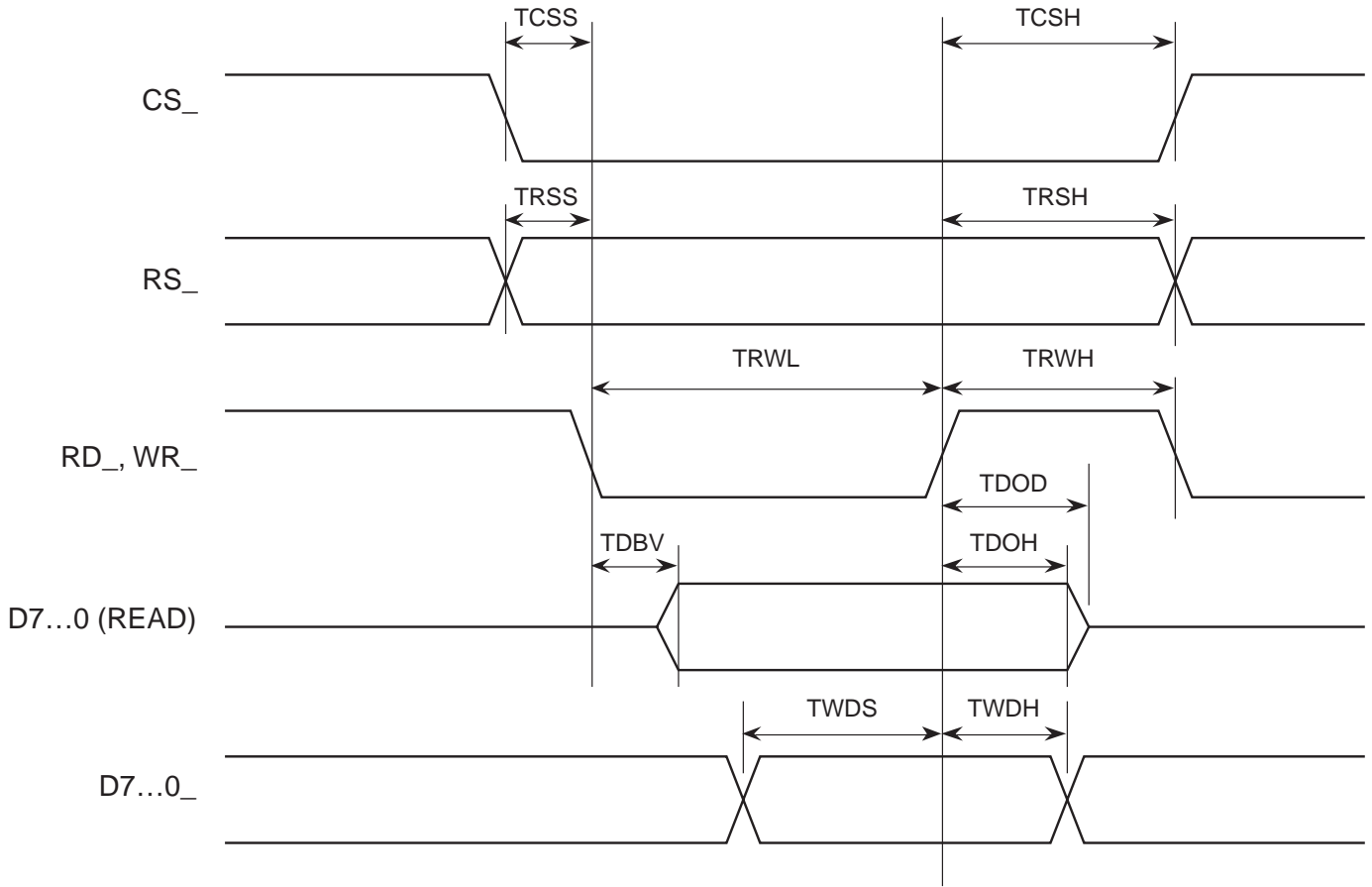
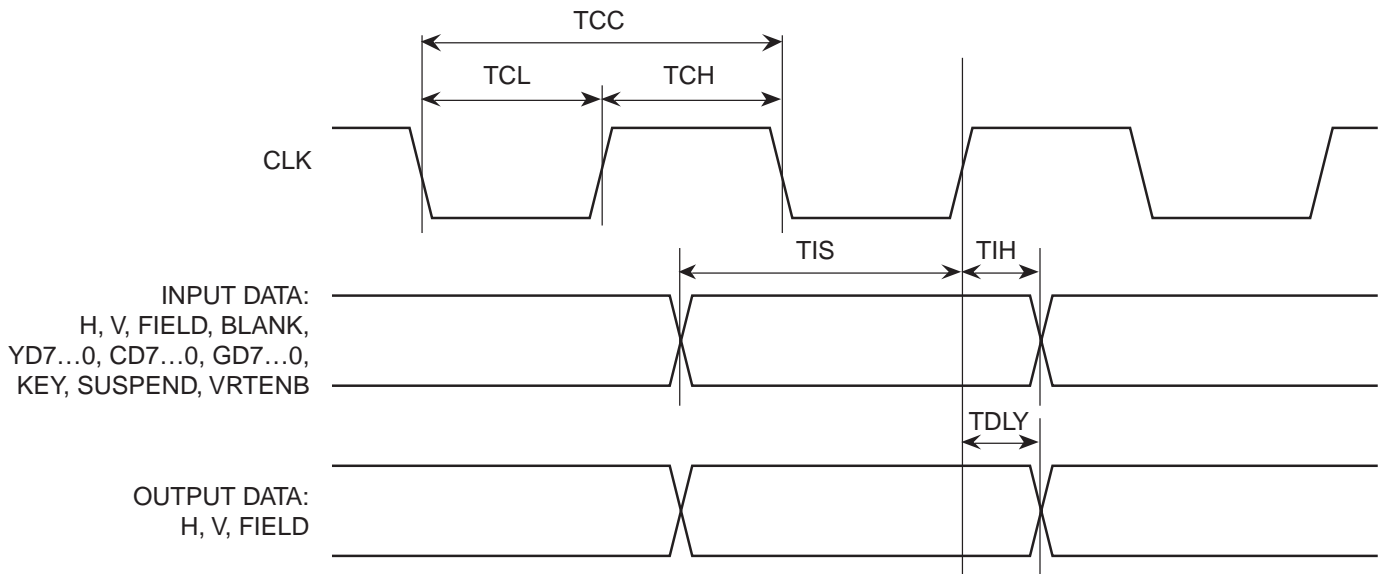
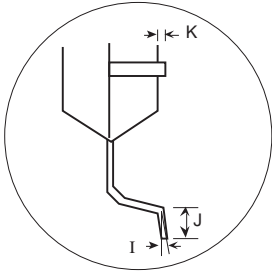
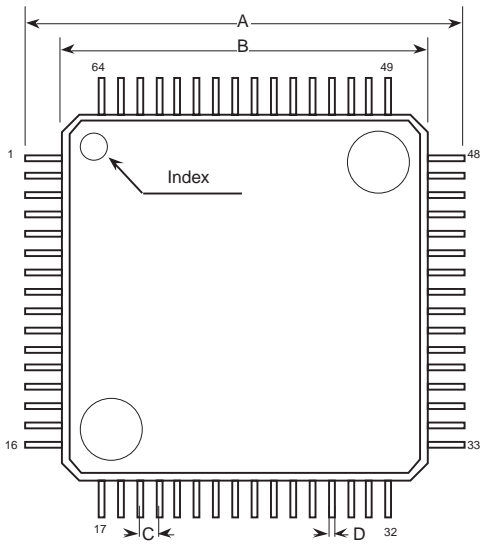


Figure 11 – AC Data Timing



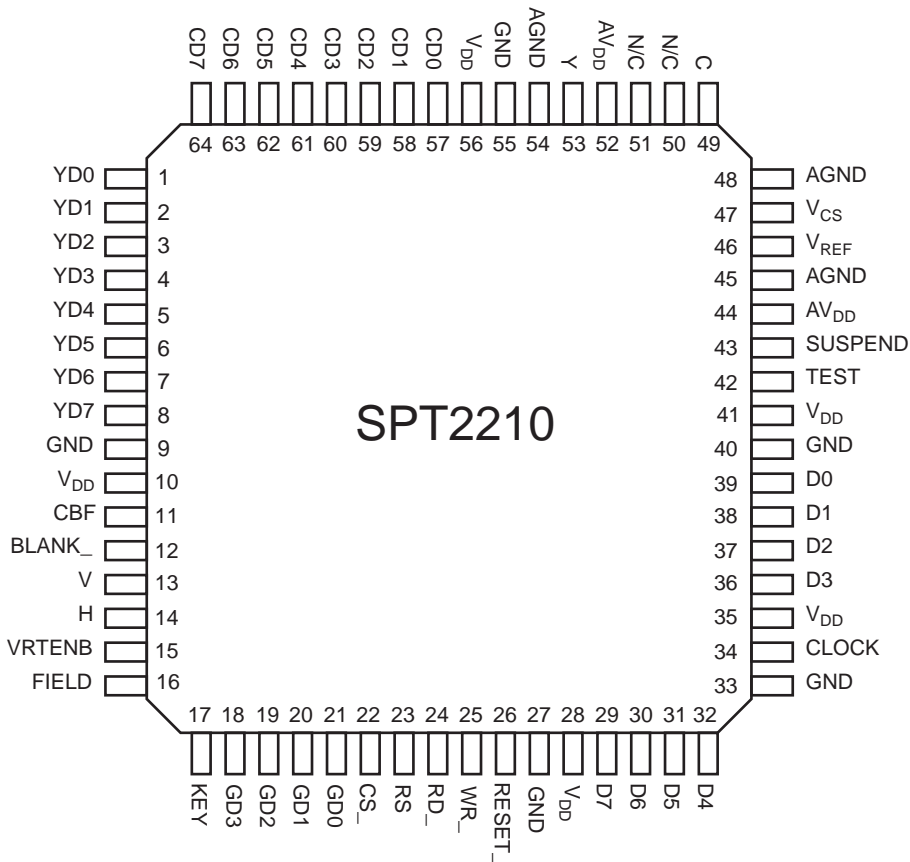
PACKAGE OUTLINE

64-LEAD PQFP



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.465	0.480	11.80	12.20
B	0.390	0.398	9.90	10.10
C	0.017	0.023	0.42	0.58
D	0.006	0.010	0.15	0.26
E	0.295 typ		7.5 typ	
F	0.465	0.480	11.80	12.20
G	0.055	0.067	1.40	1.70
H	0.0049	0.0052	0.125	0.132
I	0-10°		0-10°	
J	0.012	0.028	0.30	0.70
K	0.000	0.008	0.00	0.20

PIN ASSIGNMENTS



ORDERING INFORMATION

PART NUMBER	DESCRIPTION	TEMPERATURE RANGE	PACKAGE TYPE
SPT2210SCT	Y/C Video Encoder	0 to +70 °C	64L PQFP

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Signal Processing Technologies believes that ultrasonic cleaning of its products may damage the wire bonding, leading to device failure. It is therefore not recommended, and exposure of a device to such a process will void the product warranty.