



TP6311QG

1/8 - 1/16 Duty VFD Controller/ Driver

DataSheet

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TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

General Specification

The TP6311QG is a FIP (Fluorescent indicator Panel or Vacuum Fluorescent Display) controller/driver that is driven on a 1/8 – to 1/16 duty factor. It consists of 12 segment output lines, 8 grid output lines, 8 segment/grid output drive lines, a display memory, a control circuit, and a key scan circuit. Serial data is input to the TP6311QG through a three-line serial interface. This FIP controller/driver is ideal as a peripheral device of a single-chip microcomputer.

FEATURE

- Many display modes (12-segment & 16-digit to 20-segment & 8-digit)
- Key scanning (12 × 4 matrices)
- Dimming circuit (eight steps)
- High-voltage output ($V_{DD} - 35V$ max)
- LED ports (5 chs, 20 mA max)
- General-purpose input port (4 bits)
- No external resistor necessary for driver outputs (P-ch open-drain + pull-down resistor output)
- Serial interface (CLK, STB, D_{IN} , D_{OUT})



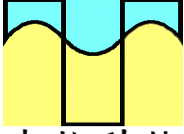
TP6311QG

1/8 - 1/16 Duty VFD Controller/ Driver

Contents :

1. General Specification	<i>P. 2</i>	<i>--- P. 2</i>
2. Pin Configurations and Package Type	<i>P. 4</i>	<i>--- P. 6</i>
3. Pin Descriptions	<i>P. 7</i>	<i>--- P. 8</i>
4. Functional Block Diagram	<i>P. 9</i>	<i>--- P. 9</i>
5. Function Descriptions	<i>P. 10</i>	<i>--- P. 17</i>
6. Absolute Maximum Ratings	<i>P. 18</i>	<i>--- P. 18</i>
7. DC Electrical Characteristic	<i>P. 19</i>	<i>--- P. 20</i>
8. AC Electrical Characteristic	<i>P. 21</i>	<i>--- P. 22</i>
9. Application Notes	<i>P. 23</i>	<i>--- P. 23</i>

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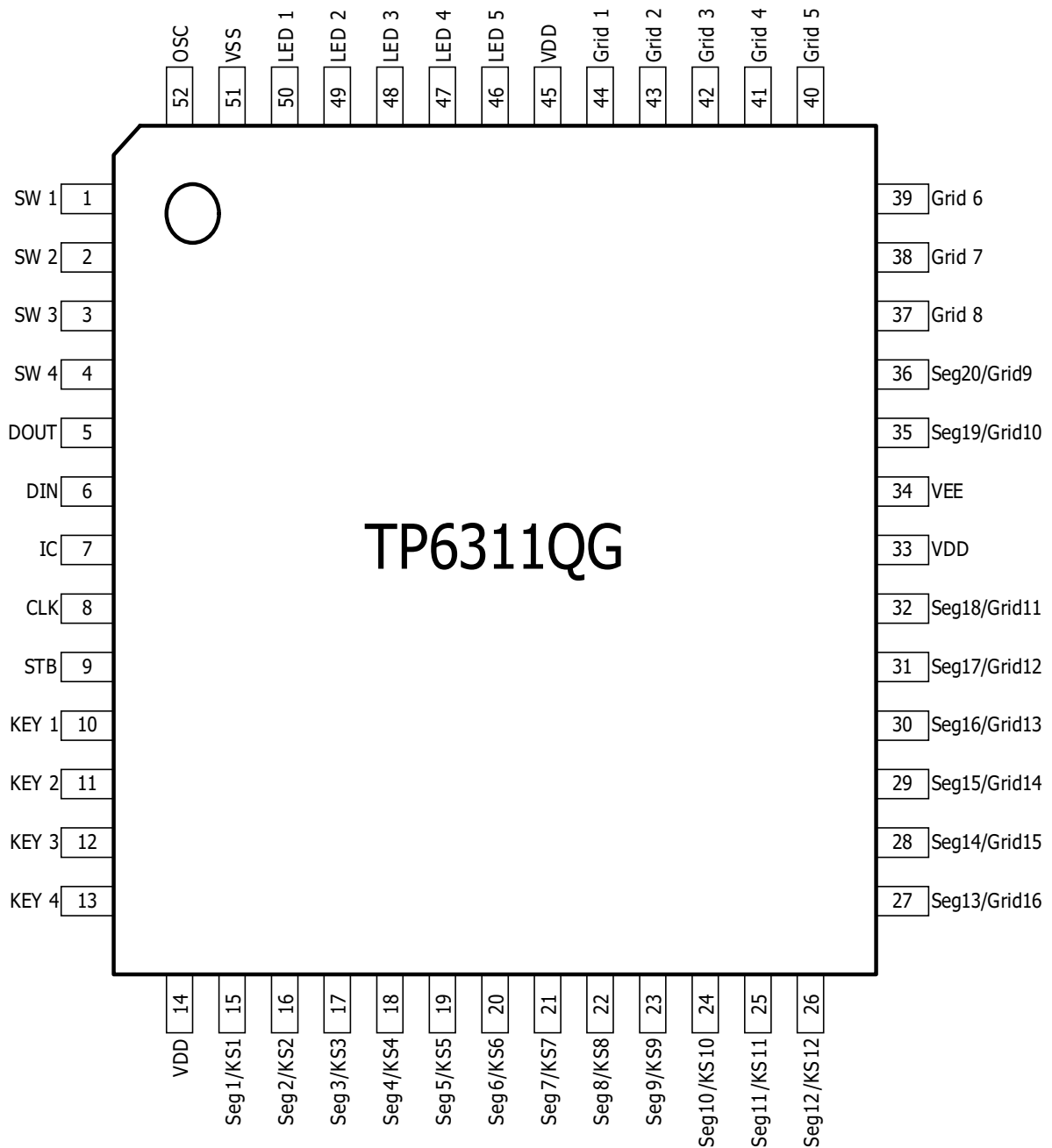


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Pin Configurations and Package Type

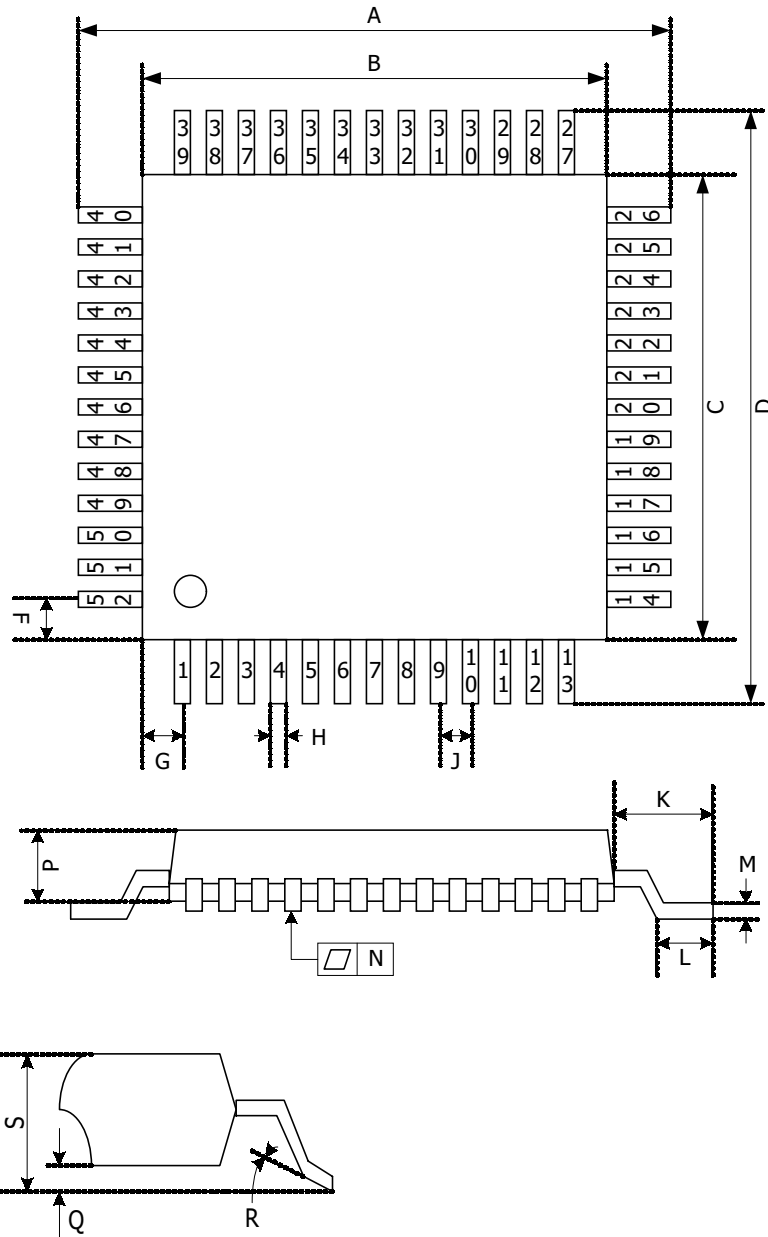


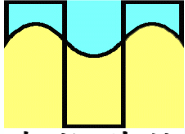
Use all the power pins. Leave the IC pin open.

TP6311QG

1/8 - 1/16 Duty VFD Controller/ Driver

52 PIN PLASTIC QFP (14 × 14)



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1/8 - 1/16 Duty VFD Controller/Driver

ITEM	MILLMETERS	INCHES		ITEM	MILLMETERS	INCHES	
A	17.6± 0.4	0.693± 0.016		K	1.8± 0.2	0.071	+0.008 -0.009
B	14.0± 0.2	0.551	+0.009 -0.008	L	0.8± 0.2	0.031	+0.009 -0.008
C	14.0± 0.2	0.551	+0.009 -0.008	M	0.15	+0.10 -0.05	0.006 +0.004 -0.003
D	17.6± 0.4	0.693± 0.016		N	0.10	0.004	
F	1.0	0.039		P	2.6	0.102	
G	1.0	0.039		Q	0.1± 0.1	0.004± 0.004	
H	0.40± 0.10	0.016	+0.004 -0.005	R	5° ± 5°	5° ± 5°	
I	0.20	0.008		S	3.0 MAX.	0.119 MAX.	
J	1.0 (T.P.)	0.039 (T.P.)					

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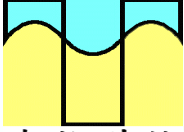
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Pin Descriptions

Pin Function

Pin No	Symbol	Pin Name	Description
6	DIN	Date input	Input serial data at rising edge of shift clock, starting from lower bit.
5	DOUT	Date output	Outputs serial data at falling edge of shift clock, starting from lower bit. This is N-ch open-drain output pin.
9	STB	Strobe	Initializes serial interface at rising or falling edge to make TP6311QG waiting for reception of command. Data input after STB has fallen is processed as command. While command data is processed, current processing is stopped, and serial interface is initialized. While STB is high, CLK is ignored.
8	CLK	Clock input	Reads serial data at rising edge, and outputs data at falling edge.
52	OSC	Oscillator pin	Connect resistor for determining oscillation frequency to this pin.
15 to 26	Seg1/KS1 to Seg12/KS12	High-voltage output (segment)	Segment output pins (Dual function as key source)
44 to 37	Grid1 to Grid8	High-voltage output (grid)	Grid output pins
27 to 32 35 to 36	Seg13/Grid16 to Seg20/Grid9	High-voltage output (segment/grid)	These pins are selectable for segment or grid output.
50 to 46	LED1 to LED5	LED output	CMOS output. +20 mA max
10 to 13	Key1 to Key4	Key data input	Data input to these pins is latched at end of display cycle.
1 to 4	SW1 to SW4	Switch input	These pins constitute 4-bit general-purpose input port.

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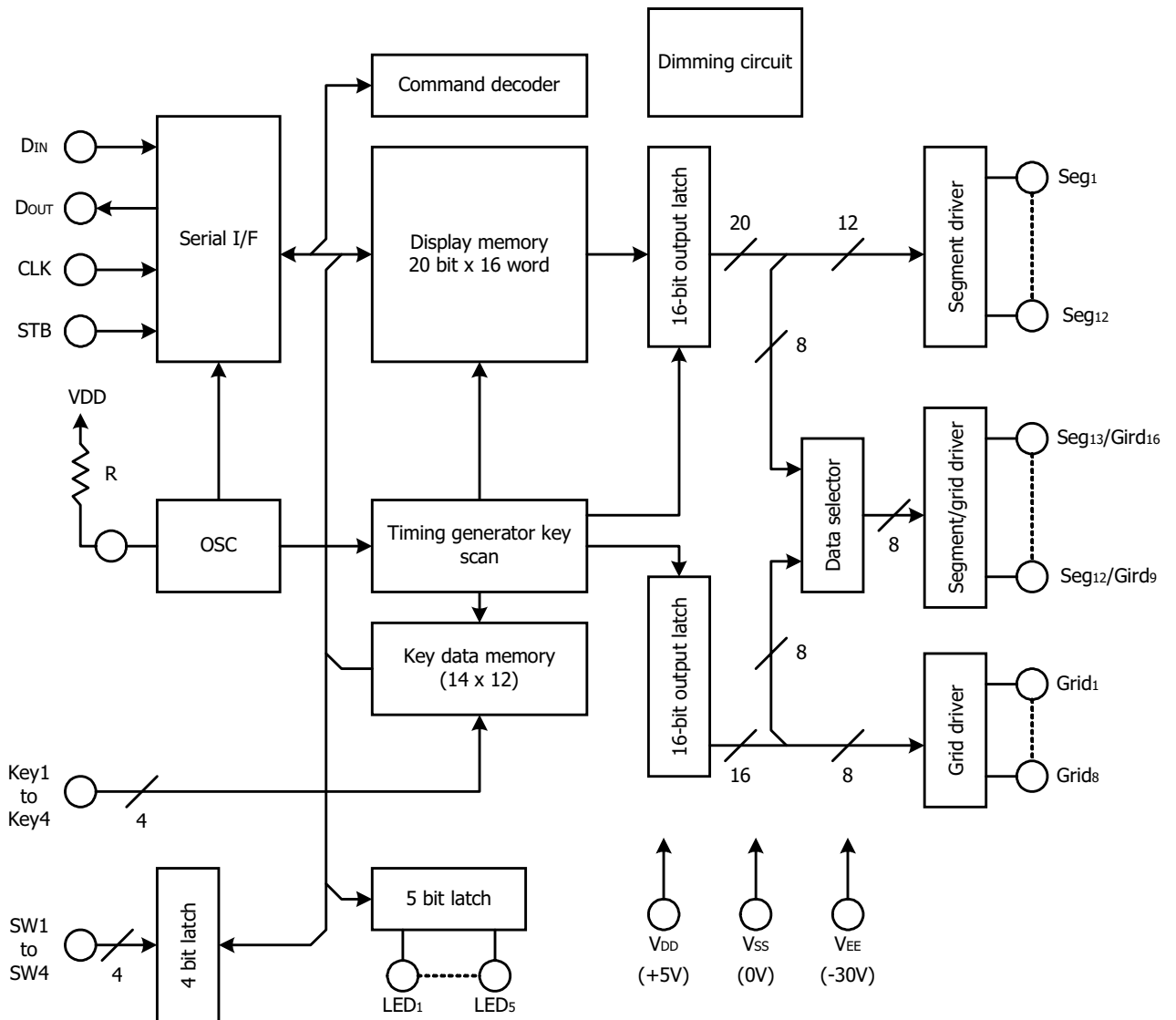
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14, 33,45	VDD	Logic power	5V \pm 10%
51	VSS	Logic ground	Connect this pin to GND of system.
34	VEE	Pull-down level	VDD – 35 V max
7	IC	Internally connected	Be sure to leave this pin open (this pin is at VDD level).

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1/8 - 1/16 Duty VFD Controller/Driver

Functional Block Diagram



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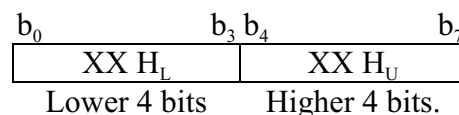
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Function Descriptions

Display RAM Address and Display Mode

The display RAM stores the data transmitted from an external device to the TP6311QG through the serial interface, and is assigned addresses as follows, in units of 8 bits:

Seg ₁	Seg ₄	Seg ₈	Seg ₁₂	Seg ₁₆	Seg ₂₀	
00H _L	00H _U	01H _L	01H _U	02H _L		DIG1
03H _L	03H _U	04H _L	04H _U	05H _L		DIG2
06H _L	06H _U	07H _L	07H _U	08H _L		DIG3
09H _L	09H _U	0AH _L	0AH _U	0BH _L		DIG4
0CH _L	0CH _U	0DH _L	0DH _U	0EH _L		DIG5
0FH _L	0FH _U	10H _L	10H _U	11H _L		DIG
12H _L	12H _U	13H _L	13H _U	14H _L		DIG7
15H _L	15H _U	16H _L	16H _U	17H _L		DIG8
18H _L	18H _U	19H _L	19H _U	1AH _L		DIG9
1BH _L	1BH _U	1CH _L	1CH _U	1DH _L		DIG10
1EH _L	1EH _U	1FH _L	1FH _U	20H _L		DIG11
21H _L	21H _U	22H _L	22H _U	23H _L		DIG12
24H _L	24H _U	25H _L	25H _U	26H _L		DIG13
27H _L	27H _U	28H _L	28H _U	29H _L		DIG14
2AH _L	2AH _U	2BH _L	2BH _U	2CH _L		DIG15
2DH _L	2DH _U	2EH _L	2EH _U	2FH _L		DIG16



Only the lower 4 bits of the addresses assigned to Seg17 through Seg20 are valid, and the higher 4 bits are ignored.

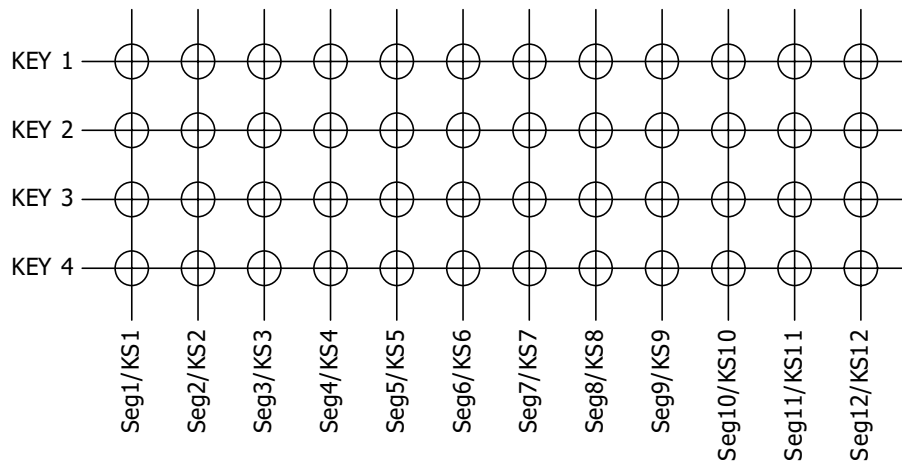


TP6311QG

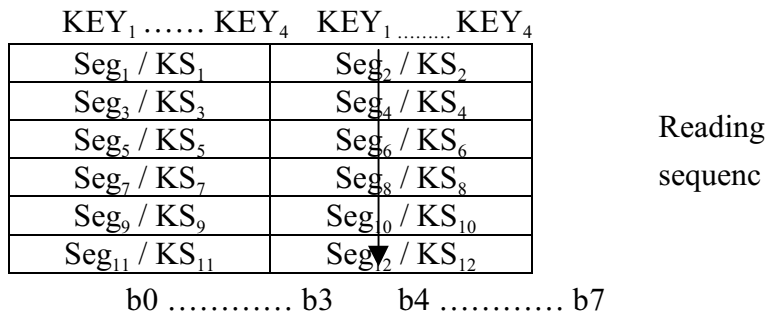
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Key Matrix and Key-Input Data Storage RAM

The key matrix is of 12 × 4 configuration, as shown below.



The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.



When the most significant bit of data (Seg12 b7) has been read, the least significant bit of the next data (Seg1 b0) is read.

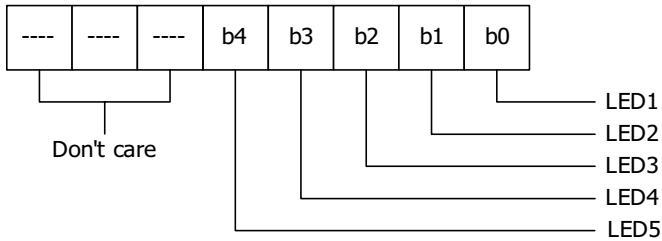


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LED PORT

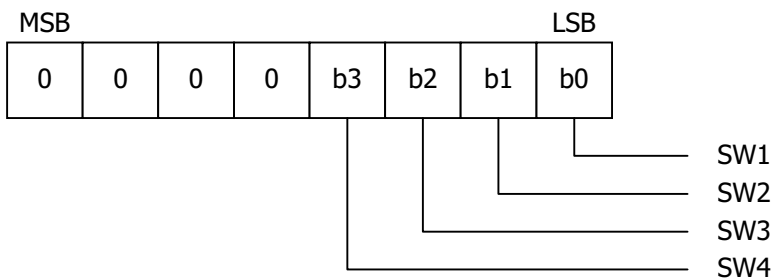
Data is written to the LED port by a write command, starting from the least significant bit of the port. When a bit of this port is 0, the corresponding LED lights ; when the bit is 1, the LED goes off. The data of bits 6 through 8 is ignored.



On power application, all the LEDs remain dark.

SW Data

The SW data is read by a read command, starting from the least significant bit. Bits 5 through 8 of the SW data are 0.





TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

Command

A command sets the display mode and status of the FIP driver.

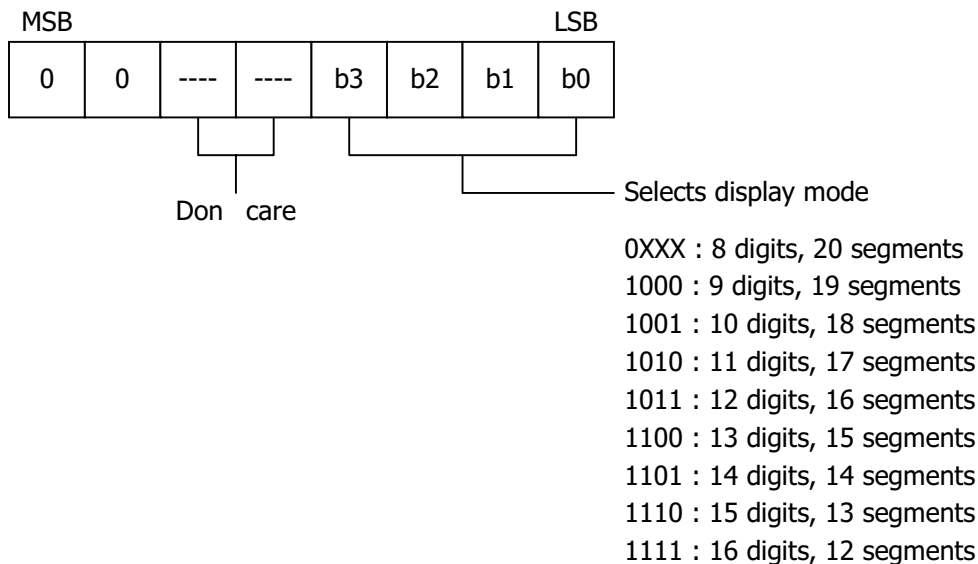
The first 1 byte input to the TP6311QG through the Din pin after the STB pin has fallen is regarded as a command.

If STB is made high while a command/data is transmitted, serial communication is initialized, and the command/data being transmitted is invalid (however, the command/data already transmitted remains valid).

(1) Display mode setting command

This command initializes the TP6311QG and selects the number of segments and number of grids (1/8 to 1/16 duty, 12 segments to 20 segments).

On power application, the 16-digit, 12-segment mode is selected.

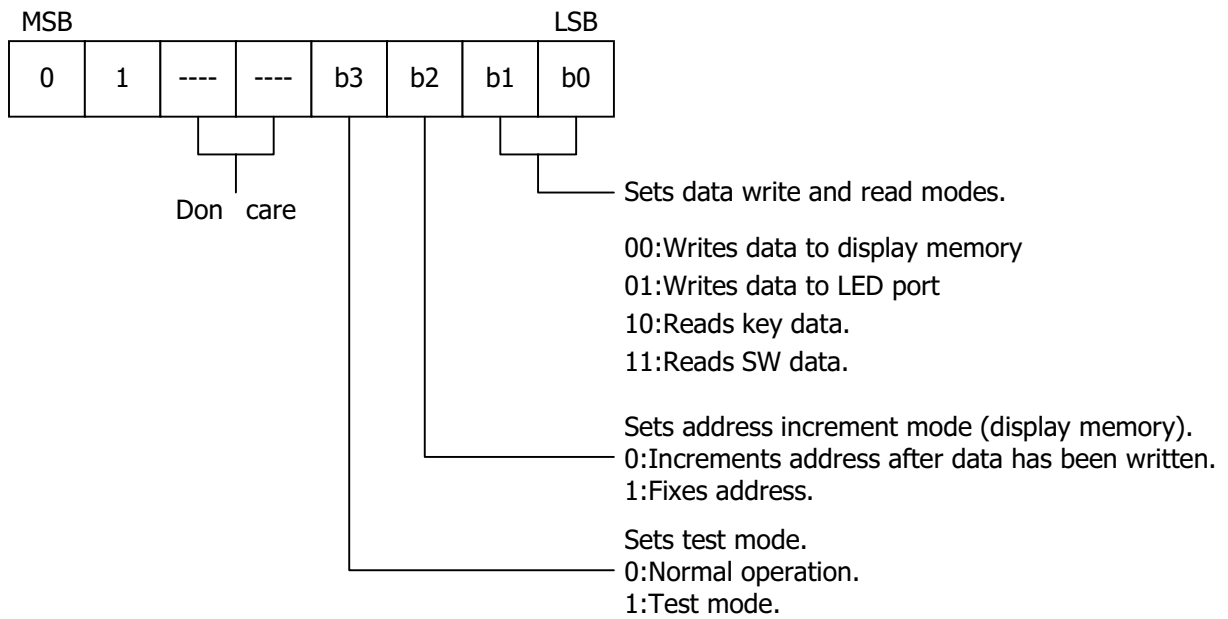


TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

(2) Data setting command

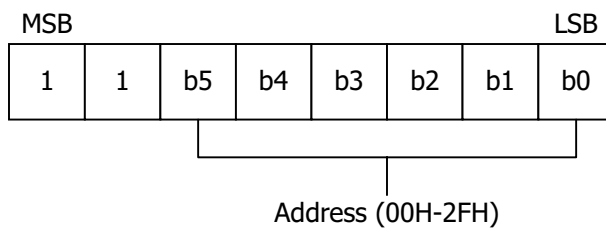
This command sets data write and read modes.



On power application, the normal operation mode and address increment mode set.

(3) Address setting command

This command sets an address of the display memory.



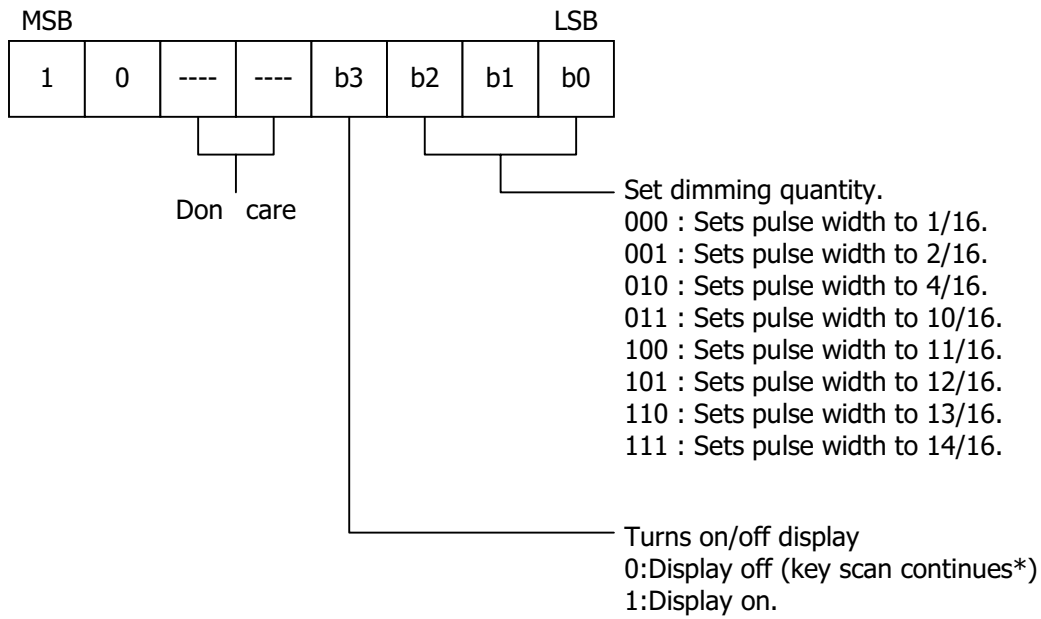
If address 30H or higher is set, the data is ignored, until a correct address is set.

On power application, the address is set to 00H.

TP6311QG

1/8 - 1/16 Duty VFD Controller/ Driver

(4) Display control command



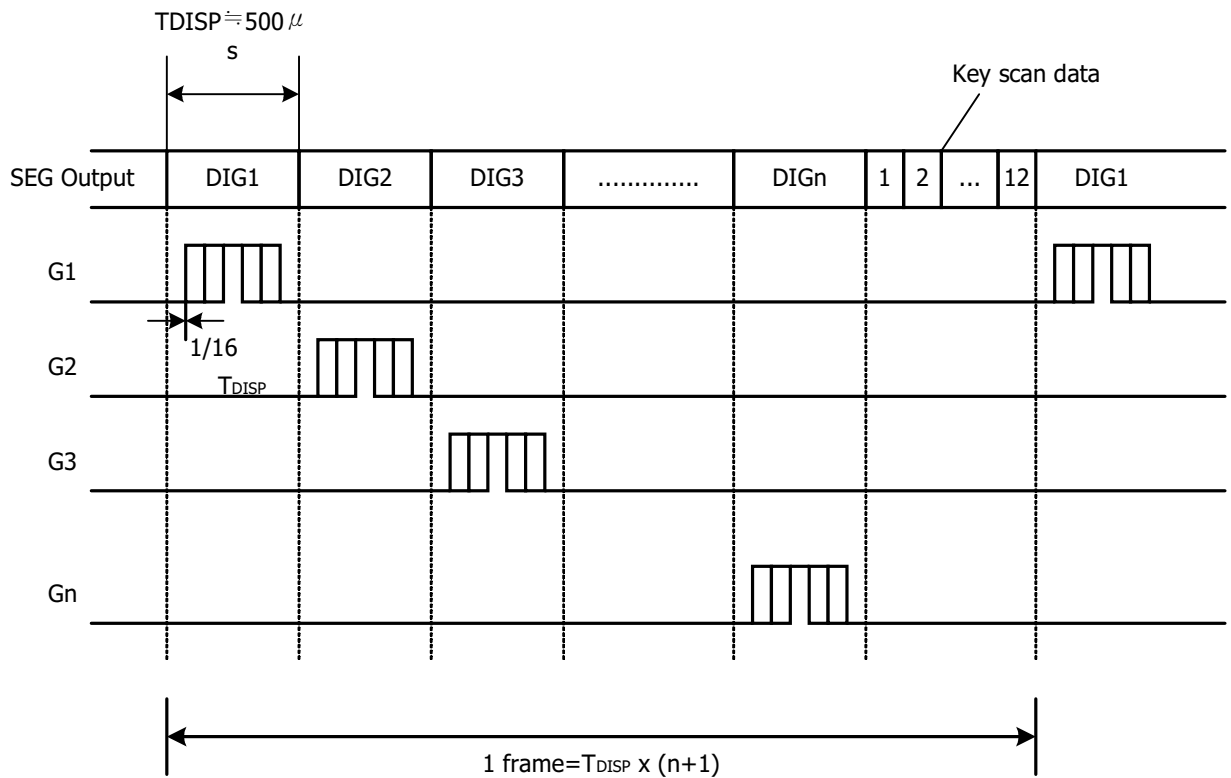
On power application, the 14/16-pulse width is set and the display is turned off.

* : On power application, key scanning is stopped..

TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

Key Scanning and Display Timing



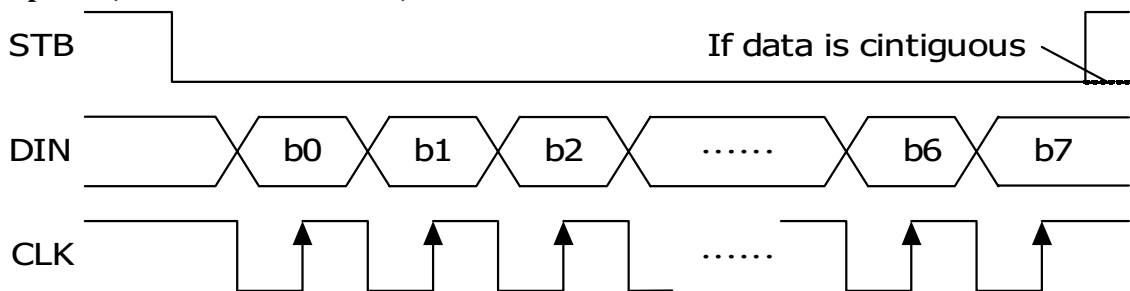
One cycle of key scanning consists of two frames, and data of 12×4 matrices is stored in RAM.

TP6311QG

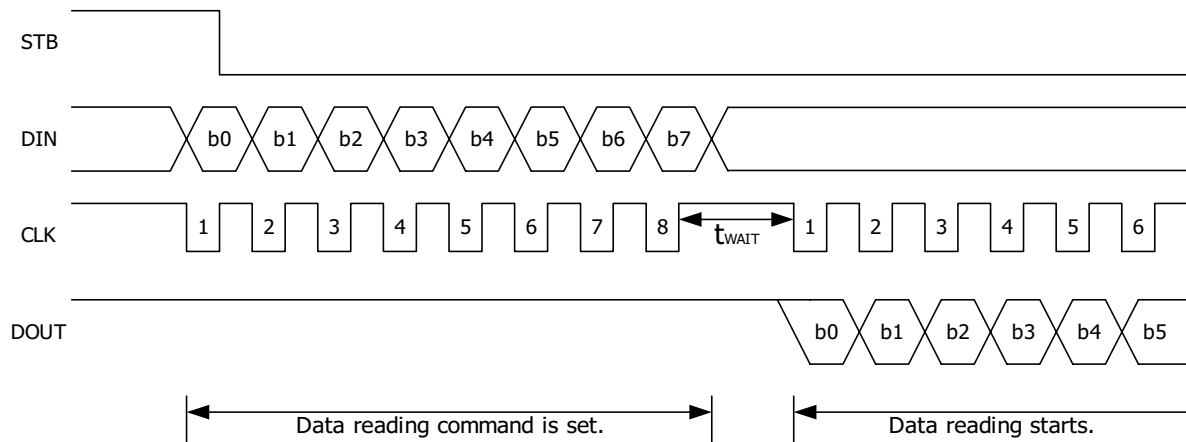
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Serial Communication Format

Reception (command/data write)



Transmission (data read)



Because the DOUT pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1k Ω to 10 k Ω).

*:When data is read, a wait time t_{WAIT} of 1 μ s is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.



TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATING (Ta=25°C, Vss=0 V)

PARAMETER	SYMBOL	RATINGS	UNIT
Logic Supply Voltage	V _{DD}	-0.5 to + 7.0	V
Driver Supply Voltage	V _{EE}	V _{DD} +0.5 to V _{DD} -40	V
Logic Input Voltage	V _{i1}	-0.5 to V _{DD} +0.5	V
FIP Driver Output Voltage	V _{o2}	V _{EE} -0.5 to V _{DD} +0.5	V
LED Driver Output Current	I _{o1}	25	mA
FIP Driver Output Current	I _{o2}	-40 (grid) -15 (segment)	mA
Power Dissipation	P _D	1200*	mW
Operating Ambient Temperature	T _{opt}	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +150	°C

* Derate at -9.6 mW/°C at Ta=25°C or higher.



TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

DC Electrical Characteristic

RECOMMENDED OPERATING CONDITION (Ta=-20

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Logic Supply Voltage	VDD	4.5	5	5.5	V	
High-Level input Voltage	Vih	0.6VDD		VDD	V	
Low-Level input Voltage	Vil	0		0.3VDD	V	
Driver Supply Voltage	VEE	0		VDD-35	V	

Maximum power consumption Pmax.=FIP driver dissipation + R_L dissipation + LED driver dissipation + dynamic power consumption.

Where segment current = 3 mA, grid current = 15ma, and LED current = 20 mA,

FIP driver dissipation = number of segments x 6 + number of grids/(number of grids + 1) x 30 (mW)

R_L dissipation = (V_{DD}-V_{EE})²/50 x (segment+1) (mW)

LED driver dissipation = number of LEDs x 20(mW)

Dynamic power consumption = V_{DD} x 5(mW)



TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

Example

Where $V_{EE} = -30\text{ V}$, $V_{DD} = 5\text{ V}$, and in 16-segment and 12-digit modes,

FIP driver dissipation = $16 \times 6 + 12/13 \times 35 =$	128
R_L dissipation = $35^2/50 \times 17 =$	417
LED driver dissipation = $5 \times 20 =$	100
Dynamic power consumption = $5 \times 5 =$	25

Total 670 mW

ELECTRICAL SPECIFICATIONS(Ta= -20 to + 70°C ,VDD= 4.5 to 5.5V ,VS

=0V,VEE =VDD - 35V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High-Level Output Voltage	V_{OH1}	$0.9 V_{DD}$			V	LED ₁ - LED ₅ , $I_{OH1} = -1\text{ mA}$
Low-Level Output Voltage	V_{OL1}			1	V	LED ₁ - LED ₅ , $I_{OL1} = 20\text{ mA}$
Low-Level Output Voltage	V_{OL2}			0.4	V	D _{OUT} , $I_{OL2} = 4\text{ mA}$
High-Level Output Current	I_{OH21}	-3			mA	$V_o = V_{DD} - 2\text{V}$, Seg ₁ to Seg ₁₂
High-Level Output Current	I_{OH22}	-15			mA	$V_o = V_{DD} - 2\text{V}$, Grid ₁ to Grid ₈ , Seg ₁₃ /Seg ₁₆ to Seg ₂₀ /Seg ₉
Driver Leakage Current	I_{OLEAK}			-10	μA	$V_o = V_{DD} - 35\text{V}$, Driver off
Output Pull-Down Resistor	R_L	50	100	150	kΩ	Driver output
Input Current	I_i			±1	μA	$V_i = V_{DD} - V_{SS}$
High-Level Output Voltage	V_{IH}	$0.6 V_{DD}$			V	
Low-Level Output Voltage	V_{IL}			$0.3 V_{DD}$	V	
Hysteresis Voltage	V_H		0.35		V	CLK, DIN, STB
Dynamic Current Consumption	I_{DDdyn}			5	mA	Under no load, display off



TP6311QG

1/8 - 1/16 Duty VFD Controller/Driver

AC Electrical Characteristic

SWITCHING CHARACTERISTICS($T_a = -20$ to $+70^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{EE} = -30\text{V}$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillation Frequency	t_{OSC}	350	500	650	kHz	$R = 56\text{k}\Omega$
Propagation Delay Time	t_{PLZ}			300	ns	CLK \Rightarrow DOUT CL = 15pF, RL = 10k Ω
	t_{PZL}			100	ns	
Rise Time	t_{TZH1}			2	μs	CL = 300 PF Seg1 to Seg12 Grid1 to Grid8 Seg13/Grid15 to Seg20/Grid9
	t_{TZH2}			0.5	μs	
Fall Time	t_{THZ}			120	μs	CL = 300 pF, Segn, Gridn
Maximum Clock Frequency	f_{max}	1			MHZ	Duty = 50%
Input Capacitance	C1			15	pF	

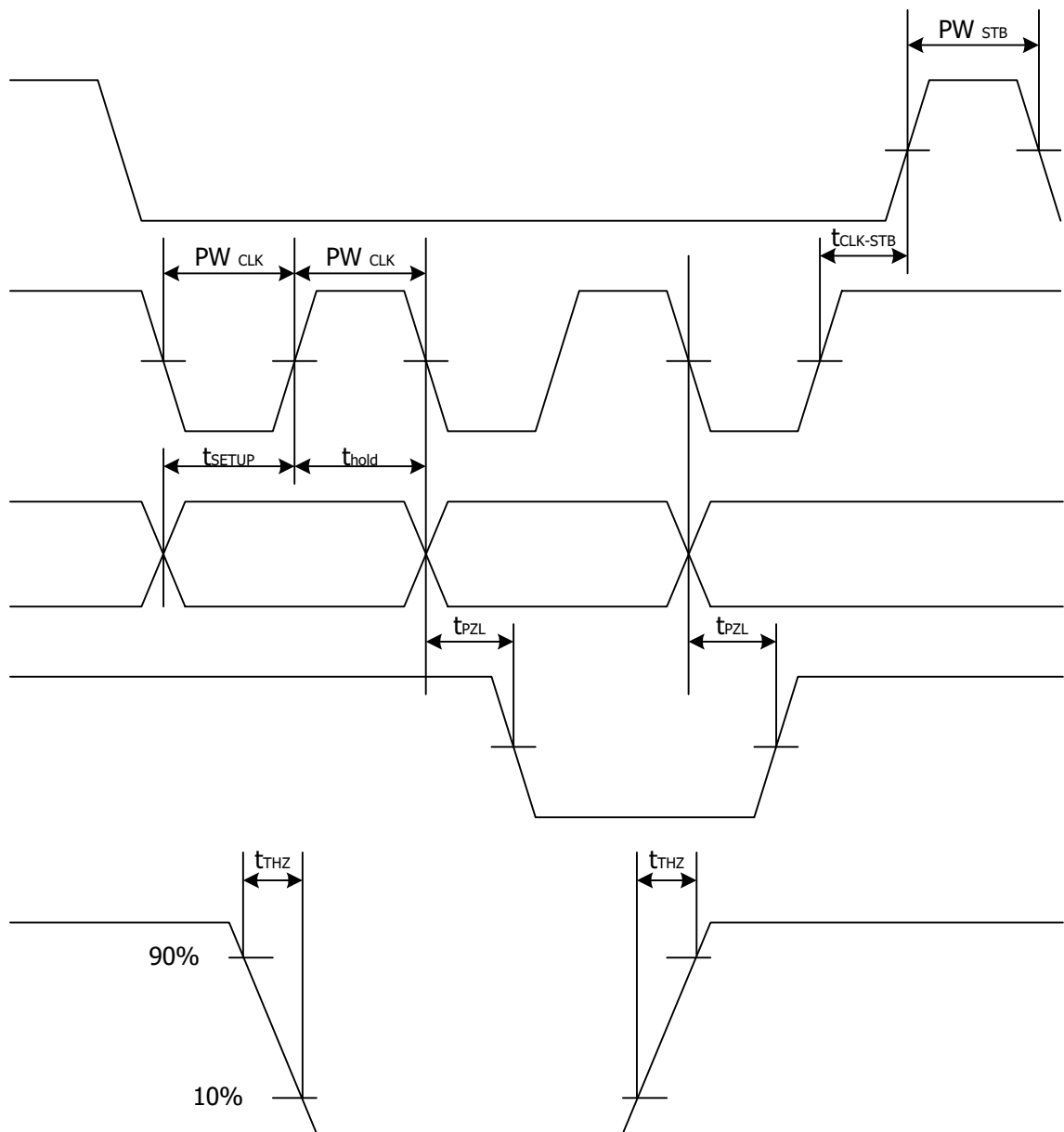
TIMING CONDITIONS($T_a = -20$ to $+70^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Pulse Width	PW_{CLK}	400			ns	
Strobe Pulse Width	PW_{STB}	1			μs	
Data Setup Time	t_{SETUP}	100			ns	
Data Hold Time	t_{HOLD}	100			ns	
Clock-Strobe Time	$t_{CLK-STB}$	1			μs	CLK $\uparrow \rightarrow$ STB \uparrow
Wait Time	t_{WAIT}	1			μs	CLK $\uparrow \rightarrow$ CLK \downarrow

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1/8 - 1/16 Duty VFD Controller/Driver

Switching Characteristic Waveform



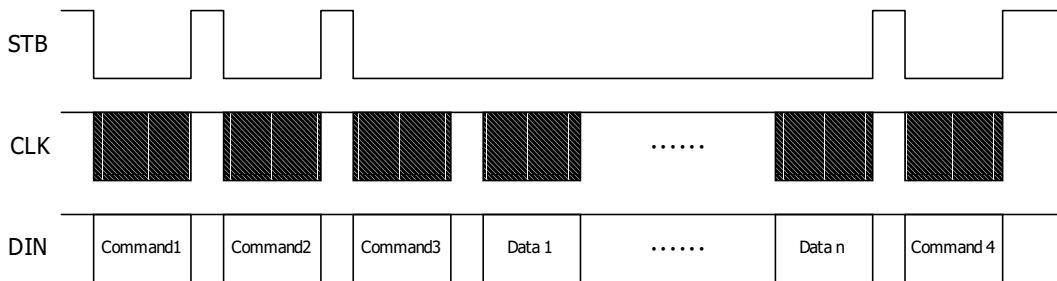


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1/8 - 1/16 Duty VFD Controller/Driver

Application Notes

Updating display memory by incrementing address.



Command1: sets display mode

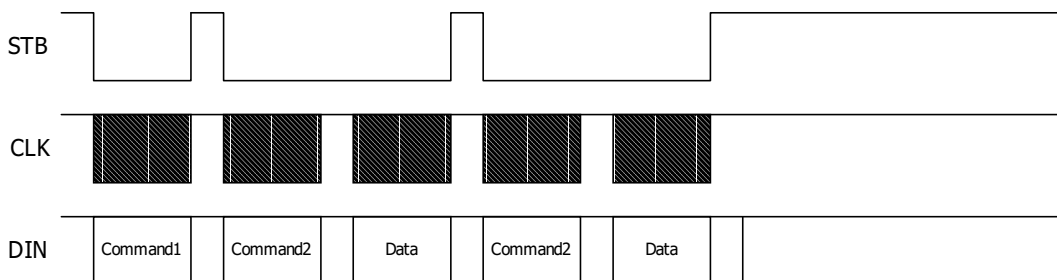
Command2: sets data

Command3: sets address

Data 1 to n : transfers display data (48 bytes max.)

Command4: controls display

Updating specific address



Command1: sets data

Command2: sets address

Data: display data