SHARC Processor

Preliminary Technical Data

ADSP-21462W/ADSP-21465W/ADSP-21467

SUMMARY

Note: This datasheet is preliminary. This document contains material that is subject to change without notice.

High performance 32-bit/40-bit floating point processor optimized for high performance audio processing

Single-instruction, multiple-data (SIMD) computational architecture

On-chip memory—5 Mbits of on-chip RAM, 4 Mbits of on-chip ROM

Automotive applications—the ADSP-21462W and the ADSP-21465W are available exclusively as automotive products

Code compatible with all other members of the SHARC family

The ADSP-21462W/ADSP-21465W/ADSP-21467 are available with unique audiocentric peripherals such as the digital applications interface, DTCP (digital transmission content protection protocol), serial ports, precision clock generators, S/PDIF transceiver, asynchronous sample rate converters, input data port, and more.

For complete ordering information, see Automotive Products on Page 59 and Ordering Guide on Page 59.

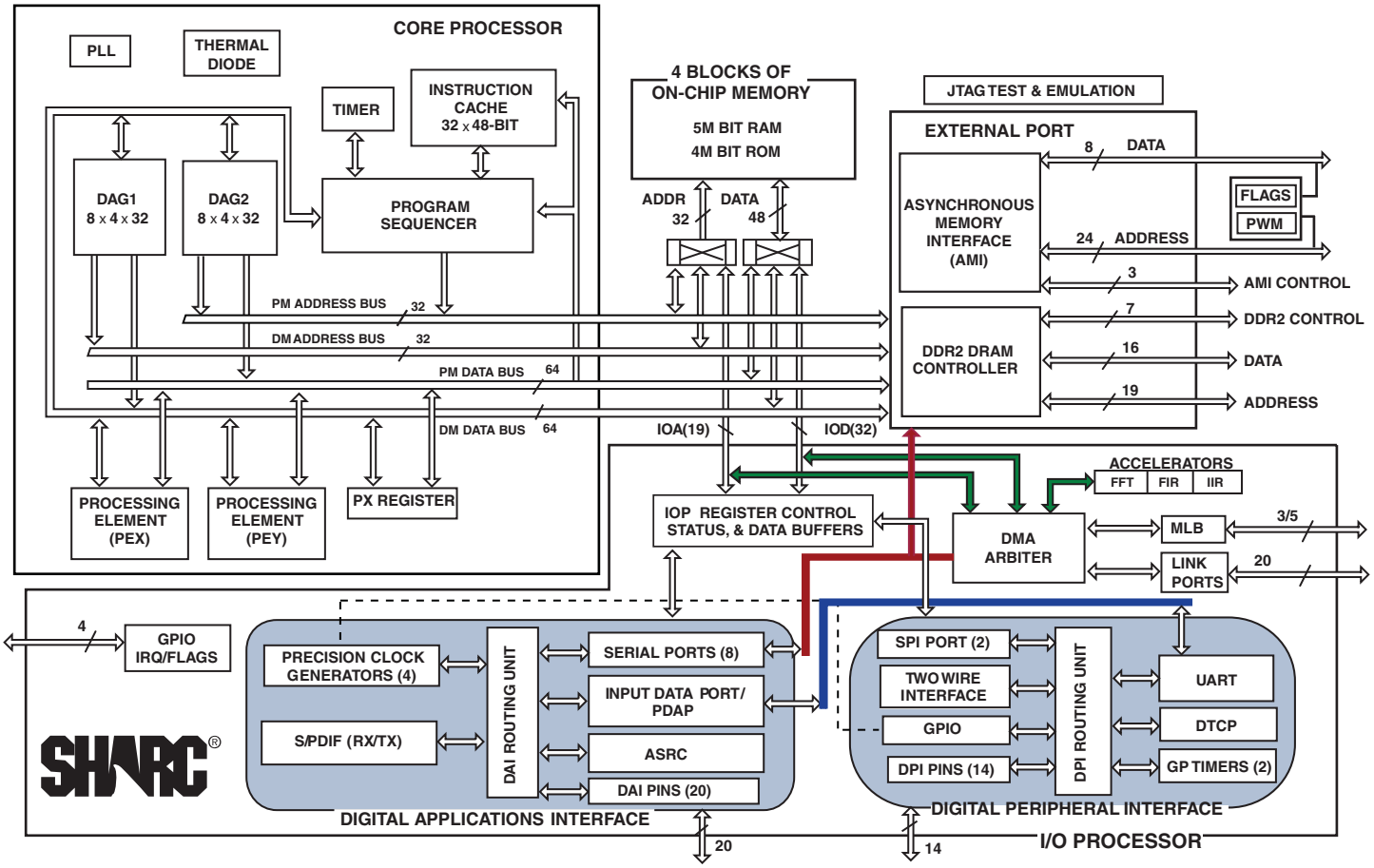

Figure 1. Functional Block Diagram

Rev. PrA

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KEY FEATURES—PROCESSOR CORE

- At up to 450 MHz core instruction rate, the processor performs at 2.7 GFLOPS/900 MMACs
- 5 Mbits on-chip RAM, 4 Mbits on-chip ROM for simultaneous access by the core processor and DMA
- DDR2 DRAM interface (16-bit) operating at maximum frequency of half the core clock frequency
- Dual data address generators (DAGs) with modulo and bit-reverse addressing
- Zero-overhead looping with single-cycle loop setup, providing efficient program sequencing
- VISA (variable instruction set) execution support
- Single instruction multiple data (SIMD) architecture provides:
  - Two computational processing elements
  - Concurrent execution
  - Code compatibility with other SHARC family members at the assembly level
  - Parallelism in buses and computational units allows:
    - Single cycle executions (with or without SIMD) of a multiply operation, an ALU operation, a dual memory read or write, and an instruction fetch
- Transfers between memory and core at a sustained 7.2 Gbytes/second bandwidth
- FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention
- IIR accelerators perform dedicated IIR filtering with high-performance, fixed- and floating-point processing capabilities with no core intervention
- FIR accelerators perform dedicated FIR filtering with high-performance, fixed- and floating-point processing capabilities with no core intervention
- Program sequencer can execute code directly from external memory bank 0 (SRAM, as well as DDR2 DRAM). This allows more options to a user in terms of code storage.
- New opcodes of 16 and 32 bits are supported in addition to the existing 48 bit opcodes. Variable Instruction Set Architecture (VISA) execution from external DDR2 DRAM memory is also supported.

INPUT/OUTPUT FEATURES

- Two 8-bit wide link ports can connect to the link ports of other SHARCs or peripherals. Link ports are bidirectional programmable ports having eight data lines, an acknowledge line and a clock line
- DMA controller supports
  - 67 DMA channels for transfers between internal memory and a variety of peripherals
  - DMA transfers at peripheral clock speed, in parallel with full-speed processor execution
- External port provides glueless connection to 16-bit wide synchronous DDR2 DRAM using a dedicated DDR2 DRAM controller, and 8-bit wide asynchronous memory devices using asynchronous memory interface (AMI)
  - Programmable wait state options (for AMI) 2 to 31 DDR2_CLK cycles
  - Delay-line DMA engine maintains circular buffers in external memory with tap/offset based reads
  - 16-bit data access for synchronous DDR2 DRAM memory
  - 8-bit data access for asynchronous memory
  - 4 memory select lines allows multiple external memory devices
- Digital audio interface (DAI) includes eight serial ports, four precision clock generators, an input data port, an S/PDIF transceiver, and a signal routing unit
- Digital peripheral interface (DPI) includes, two timers, one UART, and two SPI ports, a DTCP cipher (ADSP-21462W and ADSP-21465W), and a two-wire interface port
  - Outputs of PCG A and B can be routed through DAI pins
  - Outputs of PCG C and D can be driven on to DAI as well as DPI pins
- Eight dual data line serial ports — each has a clock, frame sync, and two data lines that can be configured as either a receiver or transmitter pair
- TDM support for telecommunications interfaces including 128 TDM channel support for newer telephony interfaces such as H.100/H.110
- Up to 16 TDM stream support, each with 128 channels per frame
- Companding selection on a per channel basis in TDM mode
- Input data port (IDP), configurable as eight channels of serial data or seven channels of serial data and up to a 20-bit wide parallel data channel
- Signal routing unit provides configurable and flexible connections between the various peripherals and the DAI/DPI components
- 4 independent asynchronous sample rate converters (ASRC). Each converter has separate serial input and output ports, a de-emphasis filter providing up to –128 dB SNR performance, stereo sample rate converter and supports left-justified, I2S, TDM, and right-justified modes and 24-, 20-, 18-, and 16-audio data word lengths.
- An MLB (media local bus) interface allows the processor to support for both 3-pin as well as 5-pin media local bus protocols (ADSP-21462W and ADSP-21465W).
- 2 muxed flag/$\overline{\text{IRQ}}$ lines
- 1 muxed flag/$\overline{\text{IRQ}}$ /$\overline{\text{AMI\_MS}}$ pin
- 1 muxed flag/Timer expired line /$\overline{\text{AMI\_MS}}$ pin
- S/PDIF-compatible digital audio receiver/transmitter supports EIAJ CP-340 (CP-1201), IEC-958, AES/EBU standards
  - Left-justified, I^2S or right-justified serial data input with 16-, 18-, 20- or 24-bit word widths (transmitter)
- Pulse-width modulation provides:
  - 16 PWM outputs configured as four groups of four outputs supports center-aligned or edge-aligned PWM waveforms
- PLL has a wide variety of software and hardware multiplier/divider ratios
- Thermal diode to monitor die temperature
- Available in 19 mm by 19 mm PBGA package (see Ordering Guide on Page 59)

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REVISION HISTORY

11/08—Revision PrA

Initial version

GENERAL DESCRIPTION

The ADSP-21462W/ADSP-21465W/ADSP-21467 SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x DSPs as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. These new processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with its large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1. SHARC Family Features

Feature	ADSP-21462W	ADSP-21465W	ADSP-21467
Frequency	400 MHz	400 MHz	450 MHz
RAM	5M bits	5M bits	5M bits
ROM[1]	4M bits	4M bits	4M bits
Audio Decoders in ROM	No	Yes	Yes
Pulse-Width Modulation	Yes	Yes	Yes
S/PDIF	Yes	Yes	Yes
DTCP[2]	Yes	Yes	No
DDR2 Memory Interface	1/2 CCLK Max	1/2 CCLK Max	1/2 CCLK Max
DDR2 Memory Bus Width	16 bits	16 bits	16 bits
Direct DMA from SPORTs to external memory	Yes	Yes	Yes
FIR accelerator	Yes	Yes	Yes
IIR accelerator	Yes	Yes	Yes
FFT accelerator	Yes	Yes	Yes
MLB Interface	Yes	Yes	No
IDP	Yes	Yes	Yes
Serial Ports	8	8	8
SRU	2	2	2
DDR2 Memory Interface	Yes	Yes	Yes
UART	1	1	1
DAI and DPI	20/14 pins	20/14 pins	20/14 pins
Link ports	2	2	2
S/PDIF transceiver	1	1	1

Table 1. SHARC Family Features (Continued)

Feature	ADSP-21462W	ADSP-21465W	ADSP-21467
AMI interface with 8-bit support	Yes	Yes	Yes
SPI	2	2	2
TWI	Yes	Yes	Yes
Package	324-ball PBGA	324-ball PBGA	324-ball PBGA
SRC Performance	128 dB	128 dB	128 dB

[1] Audio decoding algorithms include PCM, Dolby Digital EX, Dolby Prologic IIx, DTS 96/24, Neo:6, DTS ES, MPEG-2 AAC, MP3, and functions like bass management, delay, speaker equalization, graphic equalization, and more. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The ADSP-21462W and ADSP-21465W processors provide the Digital Transmission Content Protection protocol, a proprietary security protocol. Contact your Analog Devices sales office for more information.

As shown in the functional block diagram on Page 1, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. Fabricated in a state-of-the-art, high speed, CMOS process, the processor achieves an instruction cycle time of 2.22 ns at 450 MHz (ADSP-21467) and 2.5 ns at 400 MHz (ADSP-21462W, ADSP-21465W). With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz (ADSP-21467) and 2.4 GFLOPS running at 400 MHz (ADSP-21462W, ADSP-21465W).

Table 2 shows performance benchmarks for the ADSP-2146x processors.

Table 2. Processor Benchmarks

Benchmark Algorithm	Speed (at 450 MHz)
1024 Point Complex FFT (Radix 4, With Reversal)	20.44 µs
FIR Filter (per Tap)[1]	1.11 ns
IIR Filter (per Biquad)[1]	4.43 ns
Matrix Multiply (Pipelined)	
[3 × 3] × [3 × 1]	10.0 ns
[4 × 4] × [4 × 1]	17.78 ns
Divide (y/×)	6.67 ns
Inverse Square Root	10.0 ns

[1] Assumes two files in multichannel SIMD mode

The ADSP-21462W/ADSP-21465W/ADSP-21467 continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1 illustrates the following architectural features:

- Two processing elements, each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Two programmable interval timers with external event counter capabilities
- On-chip SRAM
- JTAG test access port
- FFT, FIR, IIR accelerators

The block diagram of the processor on Page 1 also illustrates the following architectural features:

- DMA controller
- Digital applications interface that includes four precision clock generators (PCG), an S/PDIF-compatible digital audio receiver/transmitter with four independent asynchronous sample rate converters, an input data port (IDP) with eight serial ports, DTCP cipher, eight serial interfaces, a 20-bit parallel input port (PDAP), and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, one UART, two serial peripheral interfaces (SPI), a 2-wire interface (TWI), and a flexible signal routing unit (DPI SRU).

FAMILY CORE ARCHITECTURE

The ADSP-21462W/ADSP-21465W/ADSP-21467 is code compatible at the assembly level with the ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-21462W/ADSP-21465W/ADSP-21467 shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, and ADSP-2116x SIMD SHARC processors, as detailed in the following sections.

SIMD Computational Engine

The ADSP-21462W/ADSP-21465W/ADSP-21467 contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0-R15 and in PEY as S0-S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21462W/ADSP-21465W/ADSP-21467 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1 on page 1). With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21462W/ADSP-21465W/ADSP-21467 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus

data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Zero-Overhead Hardware Circular Buffer Support

The ADSP-21462W/ADSP-21465W/ADSP-21467's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the processors contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21462W/ADSP-21465W/ADSP-21467 can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Variable Instruction Set Architecture

In addition to supporting the standard 48-bit instructions from previously existing SHARC family of processors, the ADSP-21462W/ADSP-21465W/ADSP-21467 support new instructions of 16 and 32 bits in addition to the existing 48 bit instructions. This feature, called Variable Instruction Set Architecture (VISA), is based on dropping redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer will now support fetching these 16-bit and 32-bit instructions as well in addition to the standard 48-bit instructions, both from internal as well as external memory. Source modules will need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

FFT Accelerator

FFT accelerator implements radix-2 complex/real input, complex output FFT with no core intervention.

FIR Accelerators

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

IIR Accelerators

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

MEMORY

The ADSP-21462W/ADSP-21465W/ADSP-21467 adds the following architectural features to the SIMD SHARC family core.

On-Chip Memory

The processors contain 5 Mbits of internal RAM. Each block can be configured for different combinations of code and data storage (see Table 3 on Page 7). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The ADSP-21462W/ADSP-21465W/ADSP-21467 memory architecture, in combination with its separate on-chip buses, allow two data transfers from the core and one from the I/O processor, in a single cycle.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory map in Table 3 displays the internal memory address space of the ADSP-21462W/ADSP-21465W/ADSP-21467.

The 48-bit space section describes what this address range looks like to an instruction that retrieves 48-bit memory.

The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

EXTERNAL MEMORY

The external port on the ADSP-21462W/ADSP-21465W/ADSP-21467 SHARC provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal DDR2 memory controller. The 16-bit DDR2 DRAM controller connects to industry-standard synchronous DRAM devices, while the second 8-bit asynchronous memory controller is intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types. Non DDR2 DRAM external memory address space is shown in Table 4.

External Memory Execution

In the ADSP-21462W/ADSP-21465W/ADSP-21467, the program sequencer can execute code directly from external memory bank 0 (SRAM, as well as DDR2 DRAM). This allows more options to a user in terms of code and data storage. With external execution, programs run at slower speeds since 48-bit instructions are fetched in parts from a 16-bit external bus coupled with the inherent latency of fetching instructions from DDR2 DRAM. VISA mode and SIMD mode accesses are supported for DDR2 space. However, external memory execution from DDR2 space is different for VISA and non-VISA mode.

Table 3. ADSP-21462W/ADSP-21465W/ADSP-21467 Internal Memory Space

IOP Registers 0x0000 0000–0x0003 FFFF			
Long Word (64 bits)	**Extended Precision Normal or Instruction Word (48 bits)**	**Normal Word (32 bits)**	**Short Word (16 bits)**
BLOCK 0 ROM 0x0004 0000–0x0004 7FFF	BLOCK 0 ROM 0x0008 0000–0x0008 AAA9	BLOCK 0 ROM 0x0008 0000–0x0008 FFFF	BLOCK 0 ROM 0x0010 0000–0x0011 FFFF
Reserved 0x0004 8000–0x0004 8FFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0009 0000–0x0009 1FFF	Reserved 0x0012 0000–0x0012 3FFF
BLOCK 0 RAM 0x0004 9000–0x0004 EFFF	BLOCK 0 RAM 0x0008 C000-0x0009 3FFF	BLOCK 0 RAM 0x0009 2000-0x0009 DFFF	BLOCK 0 RAM 0x0012 4000–0x0013 BFFF
Reserved 0x0004 F000–0x0004 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0009 E000–0x0009 FFFF	Reserved 0x0013 C000–0x0013 FFFF
BLOCK 1 ROM 0x0005 0000–0x0005 7FFF	BLOCK 1 ROM 0x000A 0000–0x000A AAA9	BLOCK 1 ROM 0x000A 0000–0x000A FFFF	BLOCK 1 ROM 0x0014 0000-0x0015 FFFF
Reserved 0x0005 8000–0x0005 8FFF	Reserved 0x000B 000–0x000B 1FFF	Reserved 0x000B 0000–0x000B 1FFF	Reserved 0x0016 0000-0x0016 3FFF
BLOCK 1 RAM 0x0005 9000–0x0005 EFFF	BLOCK 1 RAM 0x000A C000-0x000B 3FFF	BLOCK 1 RAM 0x000B 2000-0x000B DFFF	BLOCK 1 RAM 0x0016 4000-0x0017 BFFF
Reserved 0x0005 F000–0x0005 FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x000B E000–0x000B FFFF	Reserved 0x0017 C000–0x0017 FFFF
BLOCK 2 RAM 0x0006 0000–0x0006 3FFF	BLOCK 2 RAM 0x000C 0000–0x000C 5554	BLOCK 2 RAM 0x000C 0000-0x000C 7FFF	BLOCK 2 RAM 0x0018 0000–0x0018 FFFF
Reserved 0x0006 4000–0x0006 FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x000C 8000–0x000D FFFF	Reserved 0x0019 0000–0x001B FFFF
BLOCK 3 RAM 0x0007 0000–0x0007 3FFF	BLOCK 3 RAM 0x000E 0000–0x000E 5554	BLOCK 3 RAM 0x000E 0000–0x000E 7FFF	BLOCK 3 RAM 0x001C 0000–0x001C FFFF
Reserved 0x0007 4000–0x0007 FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x000E 8000–0x000F FFFF	Reserved 0x001D 0000–0x001F FFFF

DDR2 Support

The ADSP-21462W/ADSP-21465W/ADSP-21467 supports a 16-bit DDR2 interface operating at a maximum frequency of half the core clock. Execution from external memory is supported. External memory devices up to 2 Gbits in size can be supported. Delay line DMA functionality supported.

DDR2 DRAM Controller

The DDR2 DRAM controller provides an 16-bit interface to up to four separate banks of industry-standard DDR2 DRAM devices. Fully compliant with the DDR2 DRAM standard, each bank can has its own memory select line (DDR2_CS3-DDR2_CS0), and can be configured to contain between 32M bytes and 256M bytes of memory. DDR2 DRAM external memory address space is shown in Table 5

A set of programmable timing parameters is available to configure the DDR2 DRAM banks to support memory devices.

Table 5. External Memory for DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	62M	0x0020 0000 – 0x03FF FFFF
Bank 1	64M	0x0400 0000 – 0x07FF FFFF
Bank 2	64M	0x0800 0000 – 0x0BFF FFFF
Bank 3	64M	0x0C00 0000 – 0x0FFF FFFF

Table 4. External Memory for Non DDR2 DRAM Addresses

Bank	Size in Words	Address Range
Bank 0	14M	0x0020 0000 – 0x00FF FFFF
Bank 1	16M	0x0400 0000 – 0x04FF FFFF
Bank 2	16M	0x0800 0000 – 0x08FF FFFF
Bank 3	16M	0x0C00 0000 – 0x0CFF FFFF

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap. In case of 32-bit wide external memory, two 48-bit instructions will be stored in three 32-bit wide memory locations. For example, if 2k instructions are placed in 32-bit wide external memory starting at the bank 0 normal-word base address 0x0030 0000 (corresponding to instruction address 0x0020 0000) and ending at address 0x0030 0BFF (corresponding to instruction address 0x0020 07FF), then data buffers can be placed starting at an address that is offset by 3k 32-bit words (for example, starting at 0x0030 0C00).

Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 14M word window and banks 1, 2, and 3 occupy a 16M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

The asynchronous memory controller is capable of a maximum throughput of TBD Mbps using a TBD MHz external bus speed. Other features include 8 to 32-bit packing and unpacking, booting from bank select 1, and support for delay line DMA.

Shared External Memory

The ADSP-21462W/ADSP-21465W/ADSP-21467 processor supports connecting to common shared external DDR2 memory with other ADSP-2146x processors to create shared external bus processor systems. This support includes:

- Distributed, on-chip arbitration for the shared external bus
- Fixed and rotating priority bus arbitration
- Bus time-out logic
- Bus lock

Multiple processors can share the external bus with no additional arbitration logic. Arbitration logic is included on-chip to allow the connection of up to TBD processors.

Bus arbitration is accomplished through the $\overline{\text{BR6-1}}$ signals and the priority scheme for bus arbitration is determined by the setting of the RPBA pin. Table 6 on Page 13 provides descriptions of the pins used in multiprocessor systems.

INPUT/OUTPUT FEATURES

The ADSP-21462W and ADSP-21465W I/O processors provide 67 channels of DMA, while ADSP-21467 I/O processors provide 36 channels of DMA as well as an extensive set of peripherals. These include a 20 lead digital applications interface, which controls:

- Eight serial ports
- S/PDIF receiver/transmitter
- Four precision clock generators
- Input data port/parallel data acquisition port
- Four asynchronous sample rate converters

The ADSP-21462W/ADSP-21465W/ADSP-21467 processor also contains a 14 lead digital peripheral interface, which controls:

- Two general-purpose timers
- Two serial peripheral interfaces
- One universal asynchronous receiver/transmitter (UART)
- An I^2C®-compatible 2-wire interface
- Two PCGs (C and D) can also be routed through DPI

DMA Controller

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21462W/ADSP-21465W/ADSP-21467's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the parallel data acquisition port (PDAP) or the UART.

Sixty-seven channels of DMA are available on the ADSP-21462W and ADSP-21465W devices, and thirty-six channels on the ADSP-21467. The breakdown is as follows: 16 via the serial ports, eight via the input data port, two for the

UART, two for the SPI interface, two for the external port, two for DTCP (or memory-to-memory data transfer when DTCP is not used), two for the link port, two for the FFT/FIR/IIR accelerators, and up to 31 DMA channels for the media local bus interface on the ADSP-21462W and ADSP-21465W.

Programs can be downloaded to the ADSP-21462W/ADSP-21465W/ADSP-21467 using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Delay Line DMA

The ADSP-21462W/ADSP-21465W/ADSP-21467 processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

Scatter/Gather DMA

The ADSP-21462W/ADSP-21465W/ADSP-21467 processor provides scatter/gather DMA functionality.

This allows processor DMA reads/writes to/from non-contingeous memory blocks.

Digital Applications Interface (DAI)

The digital applications interface (DAI) provides the ability to connect various peripherals to any of the DAI pins (DAI_P20–1).

Programs make these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI also includes eight serial ports, four precision clock generators (PCG), S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

Serial Ports

The ADSP-21462W/ADSP-21465W/ADSP-21467 features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

The serial ports operate at a maximum data rate of 56.25 Mbps. Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard DSP serial mode
- Multichannel (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left-justified sample pair mode

Left-justified sample pair mode is a mode where in each frame sync cycle two samples of data are transmitted/received—one sample on the high segment of the frame sync, the other on the low segment of the frame sync. Programs have control over various attributes of this mode.

Each of the serial ports supports the left-justified sample pair and I^2S protocols (I^2S is an industry-standard interface commonly used by audio codecs, ADCs, and DACs such as the Analog Devices AD183x family), with two data pins, allowing four left-justified sample pair or I^2S channels (using two stereo devices) per serial port, with a maximum of up to 32 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For the left-justified sample pair and I^2S modes, dataword lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding selection on a per channel basis. Serial port clocks and frame syncs can be internally or externally generated.

The serial ports also contain frame sync error detection logic where the serial ports detect frame syncs that arrive early (for example frame syncs that arrive while the transmission/reception of the previous word is occurring). All the serial ports also share one dedicated error interrupt.

S/PDIF-Compatible Digital Audio Receiver/Transmitter and Synchronous/Asynchronous Sample Rate Converter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left justified, I^2S or right justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources such as the SPORTs, external pins, the precision clock generators (PCGs), and are controlled by the SRU control registers.

The sample rate converter (ASRC) contains four ASRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The ASRC block is used to perform synchronous or asyn-

chronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

Digital Transmission Content Protection

The DTCP specification defines a cryptographic protocol for protecting audio entertainment content from illegal copying, intercepting, and tampering as it traverses high performance digital buses, such as the IEEE 1394 standard. Only legitimate entertainment content delivered to a source device via another approved copy protection system (such as the DVD content scrambling system) will be protected by this copy protection system. This feature is available on the ADSP-21462W and ADSP-21465W processors only. Licensing through DTLA is required for these products. Visit www.dtcp.com for more information.

Digital Peripheral Interface (DPI)

The digital peripheral interface provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), and two general-purpose timers.

Serial Peripheral (Compatible) Interface

The ADSP-2146x SHARC processors contain two serial peripheral interface ports (SPIs). The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

The UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supporting bit rates ranging from (f_{PCLK}/ 1,048,576) to (f_{PCLK}/16) bits per second.
- Supporting data formats from 7 to 12 bits per frame.
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor.

In conjunction with the general-purpose timer functions, autobaud detection is supported.

Timers

The ADSP-21462W/ADSP-21465W/ADSP-21467 has a total of three timers: a core timer that can generate periodic software interrupts and two general purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and each general-purpose timer has one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables both general-purpose timers independently.

2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the I^2C bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

Pulse-Width Modulation

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on

two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs each. Therefore, this module generates 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single update mode or double update mode. In single update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the mid-point of the PWM period. In double update mode, a second updating of the PWM registers is implemented at the mid-point of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

Link Ports

Two 8-bit wide link ports can connect to the link ports of other DSPs or peripherals. Link ports are bidirectional ports having eight data lines, an acknowledge line and a clock line. Link ports can operate at a maximum frequency of 166 MHz.

MediaLB

The ADSP-21462W and ADSP-21465W have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame.

ROM Based Security

The ADSP-21462W/ADSP-21465W/ADSP-21467 has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code when enabled. When using this feature, the processor does not boot-load any external code, executing exclusively from internal SRAM/ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features and external boot modes are only available after the correct key is scanned.

SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

Program Booting

The internal memory of the ADSP-2146x boots at system power-up from an 8-bit EPROM via the external port, link port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOTCFG2–0) pins (see Table 8 on Page 17).

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and DDR2 DRAM controller, or performing a Boot. The functionality of the CLKOUT/$\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference*.

Power Supplies

The processors have separate power supply connections for the internal (V_{DD_INT}), external (V_{DD_EXT}), and analog (V_{DD_A}/V_{SS_A}) power supplies. The internal and analog supplies must meet the V_{DD_INT} specifications. The external supply must meet the V_{DD_EXT} specification. All external supply pins must be connected to the same power supply.

Note that the analog supply pin (V_{DD_A}) powers the processor's internal clock generator PLL. To produce a stable clock, it is recommended that PCB designs use an external filter circuit for the V_{DD_A} pin. Place the filter components as close as possible to the V_{DD_A}/V_{SS_A} pins. For an example circuit, see Figure 2. (A recommended ferrite chip is the muRata BLM18AG102SN1D).

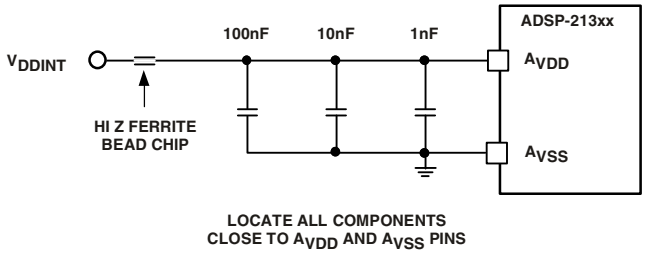

Figure 2. Analog Power (V_{DD_A}) Filter Circuit

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for V_{DD_INT} and V_{SS}. Use wide traces to connect the bypass capacitors to the analog power (V_{DD_A}) and ground (V_{SS_A}) pins. Note that the V_{DD_A} and V_{SS_A} pins specified in Figure 2 are inputs to the processor and not the analog ground plane on the board—the V_{SS_A} pin should connect directly to digital ground (V_{SS}) at the chip

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2146x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate "Emulator Hardware User's Guide".

DEVELOPMENT TOOLS

The ADSP-21462W/ADSP-21465W/ADSP-21467 processors are supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-2146x processors.

EZ-KIT Lite Evaluation Board

For evaluation of the processors, use the EZ-KIT Lite® board being developed by Analog Devices. The board comes with on-chip emulation capabilities and is equipped to enable software development. Multiple daughter cards are available.

Designing an Emulator-Compatible DSP Board (Target)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG Test Access Port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the processor, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The processor must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

Evaluation Kit

Analog Devices offers a range of EZ-KIT Lite® evaluation platforms to use as a cost effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++® development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board Flash device to store user-specific boot code, enabling the board to run as a standalone unit without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom defined system. Connecting one of Analog Devices JTAG emulators to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2146x architecture and functionality. For detailed information on the ADSP-21462W/ADSP-21465W/ADSP-21467 family core architecture and instruction set, refer to the *ADSP-2136x/ADSP-2146x SHARC Processor Programming Reference*.

PIN FUNCTION DESCRIPTIONS

The following symbols appear in the Type column of Table 6:
A = asynchronous, I = input, O = output, S = synchronous,
(A/D) = active drive, (O/D) = open drain, and T = three-state,
(pd) = pull-down resistor, (pu) = pull-up resistor.

Table 6. Pin List

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
AMI_ADDR_{23-0}	I/O/T	✓		High-Z/ driven low (boot)	**External Address.** The ADSP-21462W/ADSP-21465W/ADSP-21467 outputs addresses for external memory and peripherals on these pins. The data pins can be multiplexed to support the PDAP (I) and PWM (O). After reset, all AMI_ADDR_{23-0} pins are in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the AMI_ADDR_{23-0} pins for parallel input data.
AMI_DATA_{7-0}	I/O/T	✓		High-Z	**External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), the PDAP (I), FLAGS (I/O) and PWM (O). After reset, all AMI_DATA pins are in EMIF mode and FLAG(0-3) pins will be in FLAGS mode (default).
DAI_P_{20-1}	I/O with fixed weak pull-up on input path [1, 2]	✓		High-Z	**Digital Applications Interface Pins**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audiocentric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determine the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. The DAI SRU provides the connection from the serial ports, the S/PDIF module, input data ports (2), and the precision clock generators (4), to the DAI_P20–1 pins.
DPI_P_{14-1}	I/O with fixed weak pull-up only on input path[1, 2]	✓		High-Z	**Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. The DPI SRU provides the connection from the timers (2), SPIs (2), UART (1), flags (12), and general-purpose I/O (9) to the DPI_P14–1 pins.
AMI_ACK	I (pu)	✓			**Memory Acknowledge (AMI_ACK).** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access.
$\overline{AMI\_RD}$	O/T	✓		High-Z	**AMI Port Read Enable.** $\overline{AMI\_RD}$ is asserted whenever the ADSP-21462W/ADSP-21465W/ADSP-21467 reads a word from external memory. $\overline{AMI\_RD}$ has fixed internal pull-up resistor[1, 2].
$\overline{AMI\_WR}$	O/T	✓		High-Z	**External Port Write Enable.** $\overline{AMI\_WR}$ is asserted when the ADSP-21462W/ADSP-21465W/ADSP-21467 writes a word to external memory. $\overline{AMI\_WR}$ has fixed internal pull-up resistor[1, 2].
$DDR2\_ADDR_{15-0}$	O/T		✓	High-Z/ Driven low	**DDR2 Address pins.** DDR2 address pins.
$DDR2\_BA_{2-0}$	O/T		✓	High-Z/ Driven low	**DDR2 Bank Address Input pins.** Define which bank an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA2–0 define which mode register including MR, EMR, EMR(2), and EMR(3) is loaded during the LOAD MODE command.

Table 6. Pin List (Continued)

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
$\overline{\text{DDR2\_CAS}}$	O/T		✓	High-Z/ Driven high	**DDR2 Column Address Strobe.** Connect to **$\overline{\text{DDR2\_CAS}}$** pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
DDR2_CKE	O/T		✓	High-Z/ Driven low	**DDR2 Clock Enable Output to DDR2.** Active high signal. Connect to DDR2 CKE signal.
$\overline{\text{DDR2\_CS}}_{3\text{-}0}$	O/T		✓	High-Z/ Driven high	**DDR2 Chip Select.** All commands are masked when $\overline{\text{DDR2\_CS}}_{3\text{-}0}$ is driven high. $\overline{\text{DDR2\_CS}}_{3\text{-}0}$ are decoded emory address lines. Each $\overline{\text{DDR2_CS}}_{3\text{-}0}$lines select the corresponding bank.
$\text{DDR2\_DATA}_{15\text{-}0}$	I/O/T		✓	High-Z	**DDR2 Data In/Out.** Connect to corresponding DDR2_DATA pins.
$\text{DDR2\_DM}_{1\text{-}0}$	O/T		✓	High-Z/ Driven high	**DDR2 Input Data Mask.** Mask for the DDR2 write data if driven high. Sampled on both edges of DDR2_DQS at DDR2 side. DM0 corresponds to DDR2_DATA 7–0 and DM1 corresponds to DDR2_DATA 15–8.
$\text{DDR2\_DQS}_{1\text{-}0}$ $\overline{\text{DDR2\_DQS}}_{1\text{-}0}$	I/O/T (Differential)		✓	High-Z	**Data Strobe.** Output with Write Data. Input with Read Data. DQS0 corresponds to DDR2_DATA 7–0 and DQS1 corresponds to DDR2_DATA 15–8.
$\overline{\text{DDR2\_RAS}}$	O/T		✓	High-Z/ Driven high	**DDR2 Row Address Strobe.** Connect to $\overline{\text{DDR2\_RAS}}$ pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform.
$\overline{\text{DDR2\_WE}}$	O/T		✓	High-Z/ Driven high	**DDR2 Write Enable.** Connect to $\overline{\text{DDR2\_WE}}$ pin, in conjunction with other DDR2 command pins, defines the operation for the DDR2 to perform
DDR2_CLK0, $\overline{\text{DDR2\_CLK0}}$, DDR2_CLK1, $\overline{\text{DDR2\_CLK1}}$	O/T (Differential)		✓	High-Z/ driven low	**DDR2 Clock.** Free running, minimum frequency not guaranteed during reset.
DDR2_ODT	O/T		✓	High-Z/ Driven low	**DDR2 On Die Termination.** ODT pin when driven high (along with other requirements) enables the DDR2 termination resistances.
$\overline{\text{AMI\_MS}}_{0\text{–}1}$	O/T	✓		High-Z	**Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory on the AMI interface. The $\overline{\text{MS}}_{1\text{-}0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{1\text{-}0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. The $\overline{\text{MS1}}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference.*
FLAG[0]/$\overline{\text{IRQ0}}$	I/O	✓		High-Z	**FLAG0/Interrupt Request0.**
FLAG[1]/$\overline{\text{IRQ1}}$	I/O	✓		High-Z	**FLAG1/Interrupt Request1.**
FLAG[2]/$\overline{\text{IRQ2}}$/ $\overline{\text{AMI\_MS2}}$	I/O	✓		High-Z	**FLAG2/Interrupt Request2/Async Memory Select2.**
FLAG[3]/TIMEX P/ $\overline{\text{AMI\_MS3}}$	I/O	✓		High-Z	**FLAG3/Timer Expired/Async Memory Select3.**
$\text{LDAT0}_{7\text{–}0}$ $\text{LDAT1}_{7\text{–}0}$	I/0	✓		High-Z	**Link Port Data (Link Ports 0-1)**.
LCLK0 LCLK1	I/O	✓		High-Z	**Link Port Clock (Link Ports 0–1).**
LACK0 LACK1	I/O	✓		High-Z	**Link Port Acknowledge (Link Port 0-1).**
THD_P	I				**Thermal Diode Anode**
THD_M	O				**Thermal Diode Cathode**

Table 6. Pin List (Continued)

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
TDI	I (pu)	✓			**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a fixed internal pull-up resistor[1, 2].
TDO	O /T	✓		High-Z	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
TMS	I (pu)	✓			**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a fixed internal pull-up resistor[1, 2].
TCK	I (pu)	✓			**Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device.
$\overline{\text{TRST}}$	I (pu)	✓			**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. $\overline{\text{TRST}}$ has a fixed internal pull-up resistor[1, 2].
$\overline{\text{EMU}}$	O/T (pu)	✓		High-Z	**Emulation Status.** Must be connected to the ADSP-21462W/ADSP-21465W/ADSP-21467 Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a fixed internal pull-up resistor[1, 2].
CLK_CFG_{1-0}	I	✓			**Core to CLKIN Ratio Control.** These pins set the start up clock frequency. See Table 9 for a description of the clock configuration modes. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset.
BOOT_CFG_{2-0}	I	✓			**Boot Configuration Select.** These pins select the boot mode for the processor. The BOOTCFG pins must be valid before reset is asserted. See Table 8 for a description of the boot modes.
$\overline{\text{RESET}}$	I (pu)	✓			**Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
XTAL	O	✓			**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal.
CLKIN	I	✓			**Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency.
CLKOUT/ $\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$	I/O (pu)	✓			**Clock Out/Reset Out/Running Reset In.** The functionality can be switched between the PLL output clock and reset out by setting Bit 12 of the PMCTL register. The default is reset out. This pin also has a third function as $\overline{\text{RUNRSTIN}}$ which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-2146x SHARC Processor Hardware Reference.*
MLBCLK	I (pd)	✓		High-Z	**Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface. 49.152 MHz at Fs=48 kHz
MLBDAT	I/O (pd) in 3 pin mode. Input in 5 pin mode.	✓		High-Z	**Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin will be an input only.

Table 6. Pin List (Continued)

Name	Type	LVTTL	SSTL18	State During and After Reset	Description
MLBSIG	I/O (pd) in 3 pin mode. Input in 5 pin mode	✓		High-Z	**Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin will be input only.
MLBDO	O (pd)	✓		High-Z	**Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode.
MLBSO	O (pd)	✓		High-Z	**Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode.
BR_{6-1}	I/O	✓		High-Z/ Driven low	**Bus request.** Bus request pins for external DDR2 bus arbitration.
RPBA	I	✓			**Rotating priority bus arbitration.**
ID_{2-0}	I	✓			**Chip ID**

[1] Pull-up/pull-down resistor can not be enabled/disabled and the value of the pull-up/pull-down resistor cannot be programmed.
[2] Range of fixed pull-up resistor can be between 26k-63kΩ. Range of fixed pull-down resistor can be between 31k-85kΩ.

DATA MODES

The address and data pins of the external memory interface are muxed (using bits in the SYSCTL register) to support the external memory interface data (input/output), the PDAP (input only), and the FLAGS (input/output). Table 7 provides the pin settings.

Table 7. Function of Data Pins

DATA PIN MODE	AMI_ADDR [23:8]	AMI_ADDR [7:0]	AMI_DATA [7:0]
000	AMI_ADDR [23:0]		AMI_DATA [7:0]
001	Reserved		
010	Reserved		
011	FLAGS/PWM [15–0]	FLAGS [15–0]	
100	Reserved		
101	PDAP (DATA + CTRL)		FLAGS [7–0]
110	Reserved		
111	Three-state all pins		

BOOT MODES

Table 8. Boot Mode Selection

BOOTCFG2–0	Booting Mode
000	SPI Slave Boot
001	SPI Master Boot
010	AMI user boot (for 8-bit Flash boot)
011	Reserved
100	Link Port 0 Boot
101	Reserved

CORE INSTRUCTION RATE TO CLKIN RATIO MODES

For details on processor timing, see Timing Specifications and Figure 3 on Page 21.

Table 9. Core Instruction Rate/ CLKIN Ratio Selection

CLKCFG1–0	Core to CLKIN Ratio
00	6:1
01	32:1
11	Reserved
10	16:1

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Min	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	TBD[2]	TBD[2]	V
V_{DD_EXT}	External (I/O) Supply Voltage	3.14	3.46	V
V_{DD_DDR2}[3]	DDR2 Controller Supply Voltage	1.71	1.89	V
V_{REF}	DDR2 Reference Voltage	0.84	0.96	V
V_{IH}[4]	High Level Input Voltage @ V_{DD_EXT} = max	2.0	3.6	V
V_{IL}[4]	Low Level Input Voltage @ V_{DD_EXT} = min	-0.3	0.8	V
V_{IH_CLKIN}[5]	High Level Input Voltage @ V_{DD_EXT} = max	TBD	TBD	V
V_{IL_CLKIN}[5]	Low Level Input Voltage @ V_{DD_EXT} = min	TBD	TBD	V
V_{IL_DDR2} (DC)	DC Low Level Input Voltage	-0.3	V_{REF} - 0.12	V
V_{IH_DDR2} (DC)	DC High Level Input Voltage	V_{REF} + 0.13	V_{DD_DDR2} + 0.3	V
V_{IL_DDR2} (AC)	AC Low Level Input Voltage		V_{REF} - 250	mV
V_{IH_DDR2} (AC)	AC High Level Input Voltage	V_{REF} + 250		mV
T_J	Junction Temperature 208-Lead PBGA @ $T_{AMBIENT}$ 0 °C to +70 °C	0	125	°C

[1] Specifications subject to change without notice.
[2] The expected value is 1.1V and initial customer designs should design with a programmable regulator that can be adjusted from 0.95V to 1.15V +/-50mV
[3] Applies to DDR2 signals.
[4] Applies to input and bidirectional pins: AMI_ADDR23–0, AMI_DATA7–0, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{SPIDS}}$, BOOTCFGx, CLKCFGx, CLKOUT ($\overline{\text{RUNRSTIN}}$), $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$.
[5] Applies to input pin CLKIN.

ELECTRICAL CHARACTERISTICS

Parameter[1]	Description	Test Conditions	Min	Typical	Max	Unit
V_{OH}[2]	High Level Output Voltage	@ V_{DD_EXT} = min, I_{OH} = –1.0 mA[3]	2.4			V
V_{OL}[2]	Low Level Output Voltage	@ V_{DD_EXT} = min, I_{OL} = 1.0 mA[3]			0.4	V
I_{OH_DDR2}[4]	Output Source DC Current	@ V_{OH_DDR2} (DC) = V_{DD_DDR2} -0.28 V	TBD			mA
I_{OL_DDR2}[4]	Output Sink DC Current	@ V_{OL_DDR2} (DC)=0.28			TBD	mA
V_{OH_DDR2}		@	TBD			mA
V_{OL_DDR2}		@			TBD	mA
I_{IH}[5, 6]	High Level Input Current	@ V_{DD_EXT} = max, V_{IN} = V_{DD_EXT} max			10	µA
I_{IL}[5]	Low Level Input Current	@ V_{DD_EXT} = max, V_{IN} = 0 V			10	µA
I_{ILPU}[6]	Low Level Input Current Pull-up	@ V_{DD_EXT} = max, V_{IN} = 0 V			TBD	µA
I_{OZH}[7, 8]	Three-State Leakage Current	@ V_{DD_EXT} = max, V_{IN} = V_{DD_EXT} max			10	µA
I_{OZL}[7]	Three-State Leakage Current	@ V_{DD_EXT} = max, V_{IN} = 0 V			10	µA
I_{OZLPU}[8]	Three-State Leakage Current Pull-up	@ V_{DD_EXT} = max, V_{IN} = 0 V			TBD	µA
$I_{DD\text{-}INTYP}$[9, 10]	Supply Current (Internal)	TBD			TBD	mA
C_{IN}[11, 12]	Input Capacitance	TBD			TBD	pF

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: AMI_ADDR23-0, AMI_DATA7-0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{\text{EMU}}$, TDO, CLKOUT.
[3] See Output Drive Currents on Page 53 for typical drive current capabilities.
[4] Applies to DDR2_ADDR18-0, $\overline{\text{DDR2\_CAS}}$, $\overline{\text{DDR2\_CS3-0}}$, DDR2_DQ1-0, DDR2_DM1-0, DDR2_DQS1-0, DDR2_DATA15-0, $\overline{\text{DDR2\_RAS}}$, $\overline{\text{DDR2\_WE}}$, DDR2_CLK0, $\overline{\text{DDR2\_CLK0}}$, DDR2_CLK1 and, $\overline{\text{DDR2\_CLK1}}$.
[5] Applies to input pins: BOOTCFGx, CLKCFGx, TCK, $\overline{\text{RESET}}$, CLKIN.
[6] Applies to input pins with internal pull-ups: $\overline{\text{TRST}}$, TMS, TDI.
[7] Applies to three-statable pins: FLAG3–0.
[8] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{\text{EMU}}$.
[9] Typical internal current data reflects nominal operating conditions.
[10] See Engineer-to-Engineer Note “Estimating Power Dissipation for ADSP-2146x SHARC Processors” for further information.
[11] Applies to all signal pins.
[12] Guaranteed, but not tested.

MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note "Estimating Power Dissipation for ADSP-2146x SHARC Processors" for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 54.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 10 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 10. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +1.32V
Analog (PLL) Supply Voltage (V_{DD_A})	TBD
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +4.6V
DDR2 Controller Supply Voltage (V_{DD_DDR2})	–0.5 V to +2.7V
Input Voltage	–0.5 V to +3.8V
Output Voltage Swing	–0.5 V to V_{DD_EXT} +0.5V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C
Junction Temperature under Bias	125°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21462W/ADSP-21465W/ADSP-21467's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, and serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLKCFG1–0 pins (see Table 9 on Page 17). To determine switching frequencies for the serial ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports).

Figure 3 shows core to CLKIN ratios of 6:1, 16:1, and 32:1 with external oscillator or crystal. Note that more ratios are possible and can be set through software using the power management control register (PMCTL). For more information, see the *ADSP-2136x SHARC Processor Programming Reference*.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

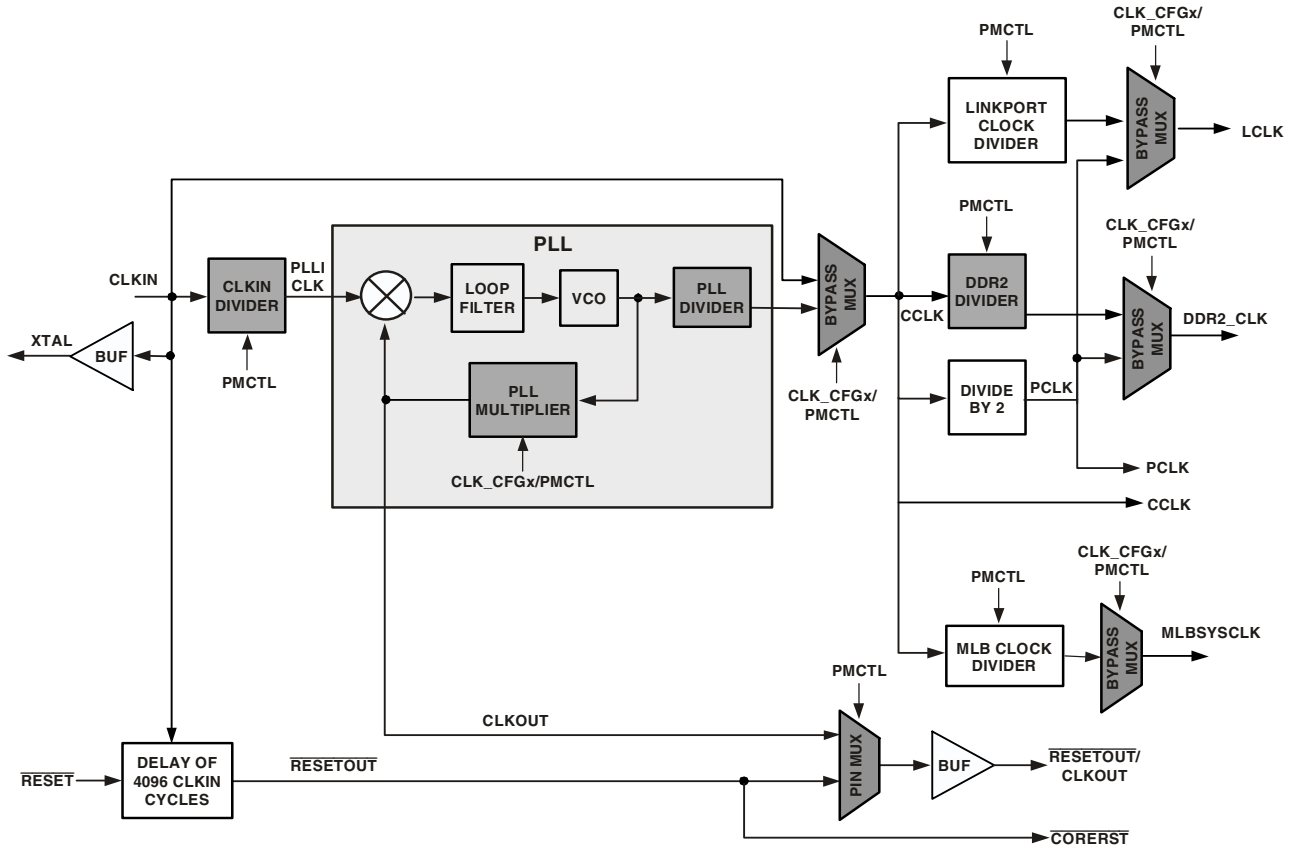

Figure 3. Core Clock and System Clock Relationship to CLKIN

Core clock frequency can be calculated as:

$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div (2 \times PLLN)$$

Note that in the user application, the PLL multiplier value should be selected in such a way that the VCO frequency falls in between 160 MHz and 800 MHz. The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$

where:

f_{VCO} is the VCO frequency

PLLM is the multiplier value programmed

f_{INPUT} is the input frequency to the PLL in MHz.

f_{INPUT} = CLKIN when the input divider is disabled

f_{INPUT} = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of various clock periods shown in Table 12 which are a function of CLKIN and the appropriate ratio control shown in Table 11.

Table 11. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CCLK	Core Clock	$1/t_{CCLK}$

Table 12. Clock Periods

Timing Requirements	Description[1]
t_{CK}	CLKIN Clock Period
t_{CCLK}	(Processor) Core Clock Period
t_{PCLK}	(Peripheral) Clock Period = 2 × t_{CCLK}
t_{SCLK}	Serial Port Clock Period = (t_{PCLK}) × SR
t_{DDR2_CLK}	DDR2 DRAM Clock Period = (t_{CCLK}) × SDR
t_{SPICLK}	SPI Clock Period = (t_{PCLLK}) × SPIR

[1] where:
SR = serial port-to-core clock ratio (wide range, determined by SPORT CLKDIV bits in DIVx register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPIBAUD register setting)
SDR=DDR2 DRAM-to-Core Clock Ratio (Values determined by bits 20-18 of the PMCTL register)

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 41 on Page 53 under Test Conditions for voltage reference levels.

Switching Characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing

The timing requirements for processor startup are given in Table 13.

Table 13. Power Up Sequencing Timing Requirements (Processor Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DD_EXT} or V_{DD_DDR2} On	0		ms
$t_{EVDD-DDR2VDD}$	V_{DD_EXT} on Before V_{DD_DDR2}	TBD		ms
$t_{DDR2VDD\_IVDD}$	V_{DD_DDR2} on Before V_{DD_INT}	TBD		ms
t_{CLKVDD}[1]	CLKIN Valid After V_{DD_INT} Valid	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted	10[2]		ms
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted	20[3]		ms
Switching Characteristic				
$t_{CORERST}$	Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted	$4096 \times t_{CK} + 2 \times t_{CCLK}$ [4, 5]		ms

[1] Valid V_{DD_INT} assumes that the supply is fully ramped to its 1 volt rail. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's datasheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on t_{SRST} specification in Table 15. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

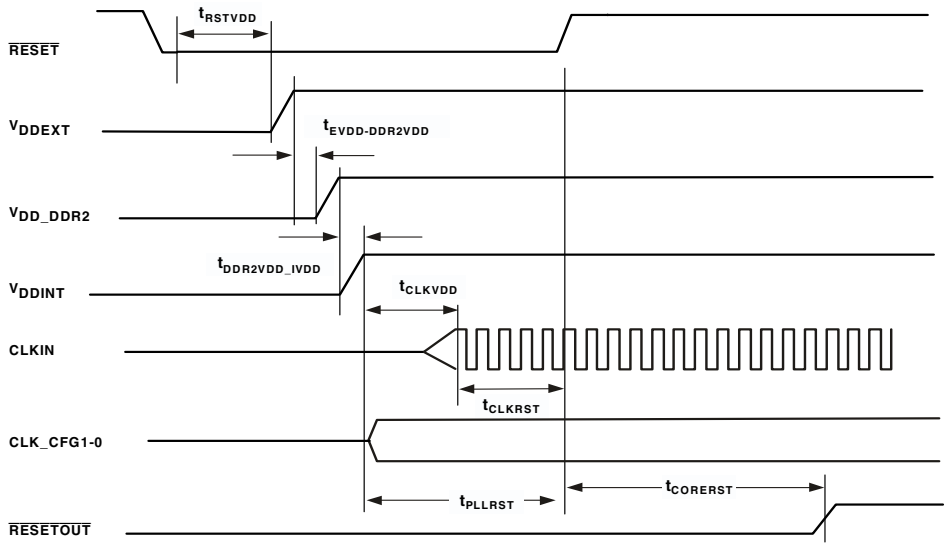

Figure 4. Power-Up Sequencing

Clock Input

Table 14. Clock Input

Parameter		400 MHz Min	400 MHz Max	450 MHz Min	450 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period	TBD[1]	TBD[2]	TBD[1]	TBD[2]	ns
t_{CKL}	CLKIN Width Low	TBD[1]	TBD[2]	TBD[1]	TBD[2]	ns
t_{CKH}	CLKIN Width High	TBD[1]	TBD[2]	TBD[1]	TBD[2]	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		TBD		TBD	ns
t_{CCLK}[3]	CCLK Period	2.5[1]	TBD	2.22[1]	TBD	ns

[1] Applies only for CLKCFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLKCFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification t_{CCLK}.

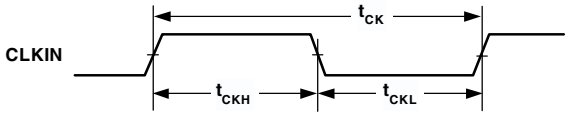

Figure 5. Clock Input

Clock Signals

The ADSP-2146x can use an external clock or a crystal. See the CLKIN pin description in Table 6. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 6 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 28.125 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 450 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register. In case of ADSP-21462W and ADSP-21465W, the maximum clock speed of 400 MHz is arrived at by using a 25 MHz crystal with the default multiplier of 16:1.

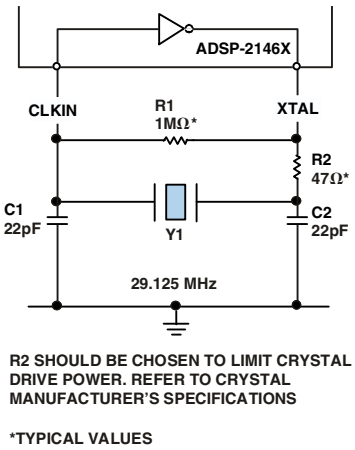

Figure 6. 450 MHz Operation (Fundamental Mode Crystal)

Reset

Table 15. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}[1]	$\overline{\text{RESET}}$ Pulse Width Low	TBD	TBD	ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN Low	TBD	TBD	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 ms while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).

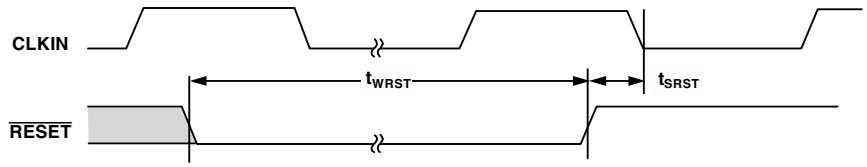

Figure 7. Reset

Running Reset

The following timing specification applies to CLKOUT/$\overline{\text{RESETOUT}}$/RUNRSTIN pin when it is configured as $\overline{\text{RUNRSTIN}}$.

Table 16. Running Reset

Parameter		Min	Max	Unit
Timing Requirements				
$t_{WRUNRST}$	Running $\overline{\text{RESET}}$ Pulse Width Low	TBD	TBD	ns
$t_{SRUNRST}$	Running $\overline{\text{RESET}}$ Setup Before CLKIN High	TBD	TBD	ns

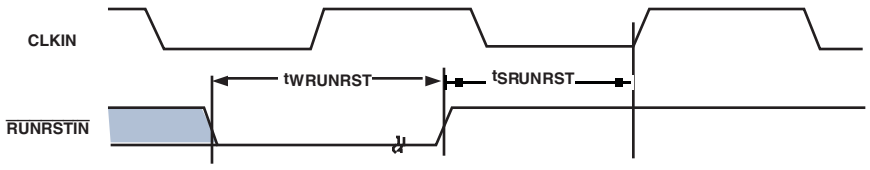

Figure 8. Running Reset

Interrupts

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts as well as the DAI_P20-1 and DPI_P14-1 pins when they are configured as interrupts.

Table 17. Interrupts

Parameter		Min	Max	Unit
Timing Requirement				
t_{IPW}	$\overline{\text{IRQx}}$ Pulse Width	TBD	TBD	ns

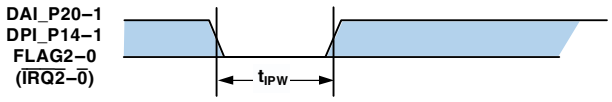

Figure 9. Interrupts

Core Timer

The following timing specification applies to FLAG3 when it is configured as the core timer (CTIMER).

Table 18. Core Timer

Parameter		Min	Max	Unit
Switching Characteristic				
t_{WCTIM}	CTIMER Pulse Width	TBD	TBD	ns

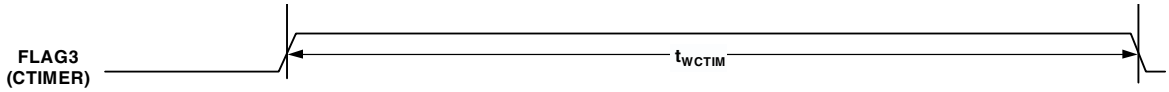

Figure 10. Core Timer

Timer PWM_OUT Cycle Timing

The following timing specification applies to Timer0 and Timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 19. Timer PWM_OUT Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	TBD	TBD	ns

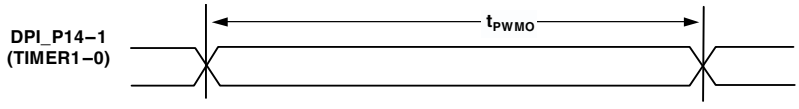

Figure 11. Timer PWM_OUT Timing

Timer WDTH_CAP Timing

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

Table 20. Timer Width Capture Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{PWI}	Timer Pulse Width	TBD	TBD	ns

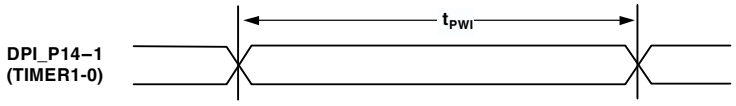

Figure 12. Timer Width Capture Timing

Pin to Pin Direct Routing (DAI and DPI)

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

Table 21. DAI Pin to Pin Routing

Parameter		Min	Max	Unit
Timing Requirement				
t_{DPIO}	Delay DAI/DPI Pin Input Valid to DAI Output Valid	TBD	TBD	ns

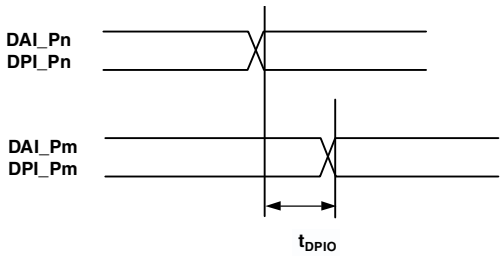

Figure 13. DAI Pin to Pin Direct Routing

Precision Clock Generator (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers) there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

Table 22. Precision Clock Generator (Direct Pin Routing)

Parameter		Min	Max	Unit
Timing Requirements				
t_{PCGIW}	Input Clock Period	TBD	TBD	ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	TBD	TBD	ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	TBD	TBD	ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	TBD	TBD	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	TBD	TBD	ns
$t_{DTRIGFS}$	PCG Frame Sync Delay After PCG Trigger	TBD	TBD	ns
t_{PCGOW}[1]	Output Clock Period	TBD	TBD	ns

D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-2146x SHARC Processor Hardware Reference, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

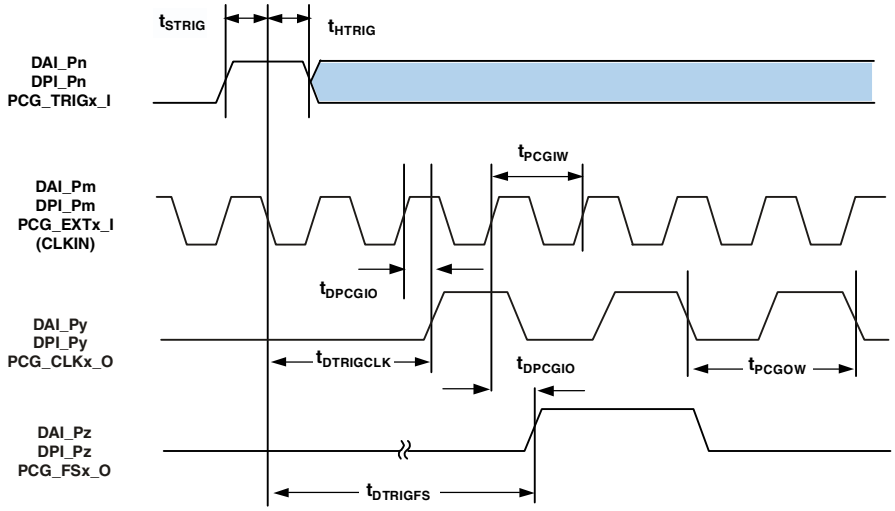

Figure 14. Precision Clock Generator (Direct Pin Routing)

Flags

The timing specifications provided below apply to AMI_ADDR23-0 and AMI_DATA7-0 when configured as FLAGS. See Table 6 on page 13 for more information on flag use.

Table 23. Flags

Parameter		Min	Max	Unit
Timing Requirement				
t_{FIPW}	DPI_P14-1, AMI_ADDR23-0, AMI_DATA7-0, FLAG3–0 IN Pulse Width	TBD	TBD	ns
Switching Characteristic				
t_{FOPW}	DPI_P14-1, AMI_ADDR23-0, AMI_DATA7-0, FLAG3–0 OUT Pulse Width	TBD	TBD	ns

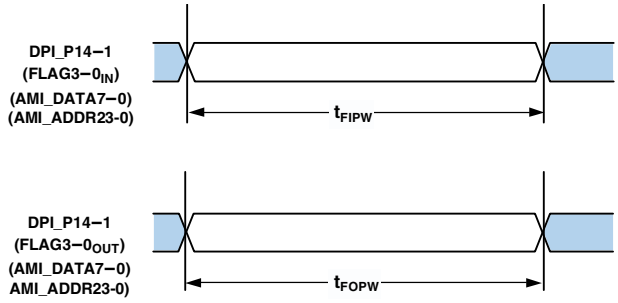

Figure 15. Flags

DDR2 SDRAM Read Cycle Timing

Table 24. DDR2 SDRAM Read Cycle Timing, $V_{DD\text{-}DDR2}$ nominal 1.8V

Parameter	Symbol	Minimum	Maximum	Unit
Timing Requirements				
TBD	TBD	TBD	TBD	TBD

TBD

Figure 16. DDR2 SDRAM Controller Input AC Timing

DDR2 SDRAM Write Cycle Timing

Table 25. DDR2 SDRAM Write Cycle Timing, $V_{DD\text{-}DDR2}$ nominal 1.8V

Parameter	Symbol	Minimum	Maximum	Unit
Switching Characteristics				
TBD	TBD	TBD	TBD	TBD

TBD

Figure 17. DDR2 SDRAM Controller Output AC Timing

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 26. Memory Read—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]	TBD	TBD	ns
t_{DRLD}	$\overline{\text{AMI\_RD}}$ Low to Data Valid[1]	TBD	TBD	ns
t_{SDS}	Data Setup to $\overline{\text{AMI\_RD}}$ High	TBD	TBD	ns
t_{HDRH}	Data Hold from $\overline{\text{AMI\_RD}}$ High[3, 4]	TBD	TBD	ns
t_{DAAK}	AMI_ACK Delay from Address, Selects[2, 5]	TBD	TBD	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_RD}}$ Low[4]	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DRHA}	Address Selects Hold After $\overline{\text{AMI\_RD}}$ High	TBD	TBD	ns
t_{DARL}	Address Selects to $\overline{\text{AMI\_RD}}$ Low[2]	TBD	TBD	ns
t_{RW}	$\overline{\text{AMI\_RD}}$ Pulse Width	TBD	TBD	ns
t_{RWR}	$\overline{\text{AMI\_RD}}$ High to $\overline{\text{AMI\_WR}}$, $\overline{\text{AMI\_RD}}$, Low	TBD	TBD	ns

W = (number of wait states specified in AMICTLx register) × t_{DDR2_CLK}.
HI = RHC + IC (RHC = (number of Read Hold Cycles specified in AMICTLx register) x t_{DDR2_CLK}
IC = (number of idle cycles specified in AMICTLx register) x t_{DDR2_CLK}).
H = (number of hold cycles specified in AMICTLx register) x t_{DDR2_CLK}.

[1] Data delay/setup: System must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{\text{AMI_MS}}$x, is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[4] Data hold: User must meet t_{HDRH} in asynchronous access mode. See Test Conditions on Page 53 for the calculation of hold times given capacitive and dc loads.
[5] AMI_ACK delay/setup: User must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.

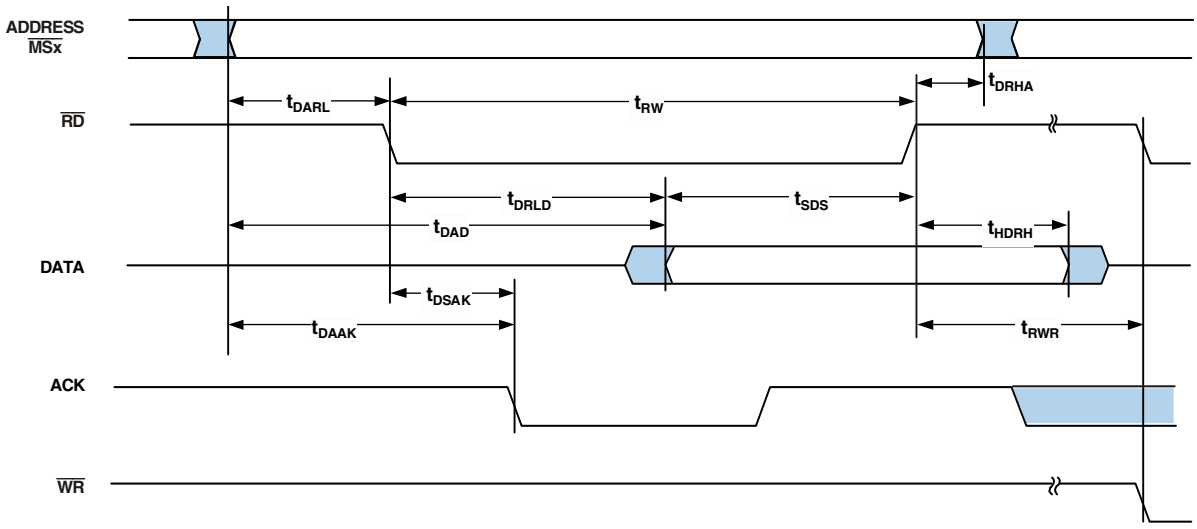

Figure 18. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

Table 27. Memory Write—Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	AMI_ACK Delay from Address, Selects[1, 2]	TBD	TBD	ns
t_{DSAK}	AMI_ACK Delay from $\overline{\text{AMI\_WR}}$ Low [1, 3]	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DAWH}	Address, Selects to $\overline{\text{AMI\_WR}}$ Deasserted[2]	TBD	TBD	ns
t_{DAWL}	Address, Selects to $\overline{\text{AMI\_WR}}$ Low[2]	TBD	TBD	ns
t_{WW}	$\overline{\text{AMI\_WR}}$ Pulse Width	TBD	TBD	ns
t_{DDWH}	Data Setup Before $\overline{\text{AMI\_WR}}$ High	TBD	TBD	ns
t_{DWHA}	Address Hold After $\overline{\text{AMI\_WR}}$ Deasserted	TBD	TBD	ns
t_{DWHD}	Data Hold After $\overline{\text{AMI\_WR}}$ Deasserted	TBD	TBD	ns
t_{DATRWH}	Data Disable After $\overline{\text{AMI\_WR}}$ Deasserted[4]	TBD	TBD	ns
t_{WWR}	$\overline{\text{AMI\_WR}}$ High to $\overline{\text{AMI\_WR}}$, $\overline{\text{AMI\_RD}}$ Low	TBD	TBD	ns
t_{DDWR}	Data Disable Before $\overline{\text{AMI\_RD}}$ Low	TBD	TBD	ns
t_{WDE}	$\overline{\text{AMI\_WR}}$ Low to Data Enabled	TBD	TBD	ns

W = (number of wait states specified in AMICTLx register) × t_{SDDR2_CLK}H = (number of hold cycles specified in AMICTLx register) x t_{DDR2_CLK}

[1] AMI_ACK delay/setup: System must meet t_{DAAK}, or t_{DSAK}, for deassertion of AMI_ACK (low). For asynchronous assertion of AMI_ACK (high) user must meet t_{DAAK} or t_{DSAK}.
[2] The falling edge of $\overline{\text{AMI\_MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, AMI_DATA, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 53 for calculation of hold times given capacitive and dc loads.

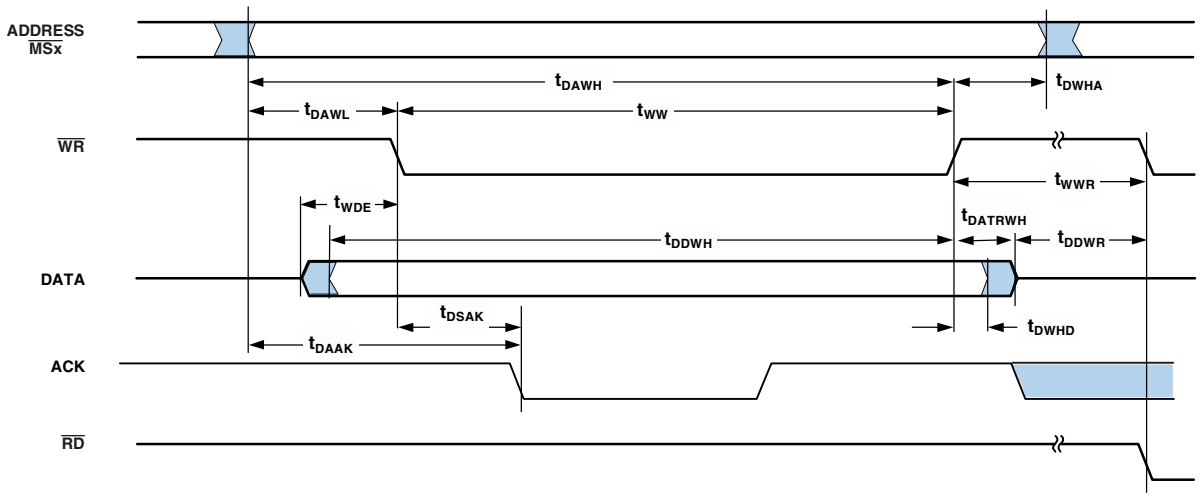

Figure 19. Memory Write—Bus Master

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = t_{LCLK}-

$_{TWH}$ min– t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

Setup Skew = TBD ns max

Hold Skew = TBD ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 28. Link Ports – Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	TBD	TBD	ns
t_{HLDCL}	Data Hold After LCLK Low	TBD	TBD	ns
t_{LCLKIW}	LCLK Period	TBD	TBD	ns
$t_{LCLKRWL}$	LCLK Width Low	TBD	TBD	ns
$t_{LCLKRWH}$	LCLK Width High	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DLALC}	LACK Low Delay After LCLK High[1]	TBD	TBD	ns

[1] LACK goes low with tDLALC relative to rise of LCLK after first byte, but does not go low if the receiver's link buffer is not about to fill.

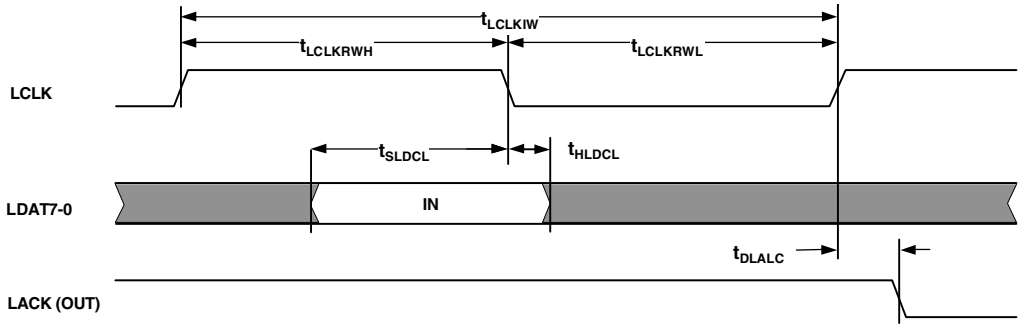

Figure 20. Link Ports—Receive

Table 29. Link Ports – Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	TBD	TBD	ns
t_{HLACH}	LACK Hold After LCLK High	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DLDCH}	Data Delay After LCLK High	TBD	TBD	ns
t_{HLDCH}	Data Hold After LCLK High	TBD	TBD	ns
$t_{LCLKTWL}$	LCLK Width Low	TBD	TBD	ns
$t_{LCLKTWH}$	LCLK Width High	TBD	TBD	ns
t_{DLACLK}	LCLK Low Delay After LACK High	TBD	TBD	ns

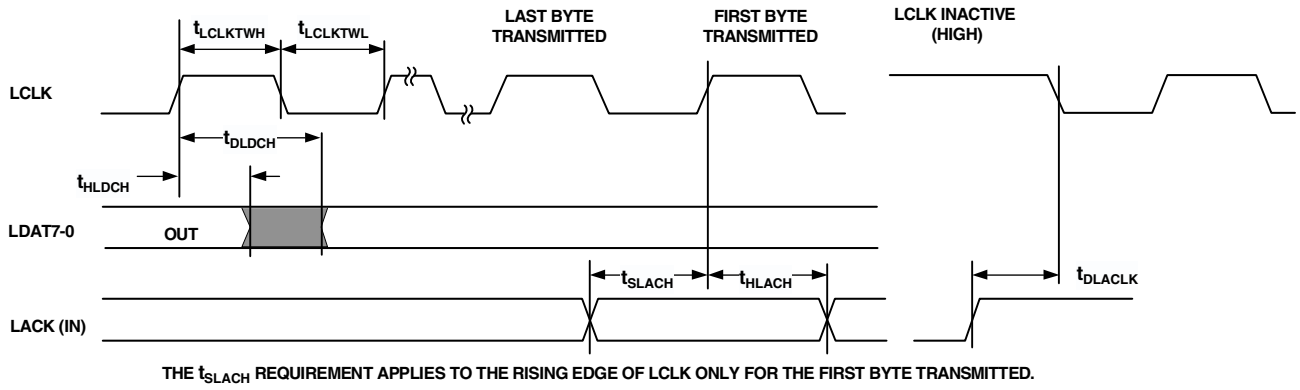

Figure 21. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Serial port signals (SCLK, FS, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 30. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HFSE}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{SDRE}[1]	Receive Data Setup Before Receive SCLK	TBD	TBD	ns
t_{HDRE}[1]	Receive Data Hold After SCLK	TBD	TBD	ns
t_{SCLKW}	SCLK Width	TBD	TBD	ns
t_{SCLK}	SCLK Period	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DFSE}[2]	FS Delay After SCLK (Internally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HOFSE}[2]	FS Hold After SCLK (Internally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{DDTE}[2]	Transmit Data Delay After Transmit SCLK	TBD	TBD	ns
t_{HDTE}[2]	Transmit Data Hold After Transmit SCLK	TBD	TBD	ns

[1] Referenced to sample edge.
[2] Referenced to drive edge.

Table 31. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}[1]	FS Setup Before SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{HFSI}[1]	FS Hold After SCLK (Externally Generated FS in either Transmit or Receive Mode)	TBD	TBD	ns
t_{SDRI}[1]	Receive Data Setup Before SCLK	TBD	TBD	ns
t_{HDRI}[1]	Receive Data Hold After SCLK	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DFSI}[2]	FS Delay After SCLK (Internally Generated FS in Transmit Mode)	TBD	TBD	ns
t_{HOFSI}[2]	FS Hold After SCLK (Internally Generated FS in Transmit Mode)	TBD	TBD	ns
t_{DFSIR}[2]	FS Delay After SCLK (Internally Generated FS in Receive Mode)	TBD	TBD	ns
t_{HOFSIR}[2]	FS Hold After SCLK (Internally Generated FS in Receive Mode)	TBD	TBD	ns
t_{DDTI}[2]	Transmit Data Delay After SCLK	TBD	TBD	ns
t_{HDTI}[2]	Transmit Data Hold After SCLK	TBD	TBD	ns
t_{SCKLIW}	Transmit or Receive SCLK Width	TBD	TBD	ns

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

Table 32. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}[1]	Data Enable from External Transmit SCLK	TBD	TBD	ns
t_{DDTTE}[1]	Data Disable from External Transmit SCLK	TBD	TBD	ns
t_{DDTIN}[1]	Data Enable from Internal Transmit SCLK	TBD	TBD	ns

[1] Referenced to drive edge.

Table 33. Serial Ports—External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$[1]	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0	TBD	TBD	ns
$t_{DDTENFS}$[1]	Data Enable for MCE = 1, MFD = 0	TBD	TBD	ns

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified sample pair as well as DSP serial mode, and MCE = 1, MFD = 0.

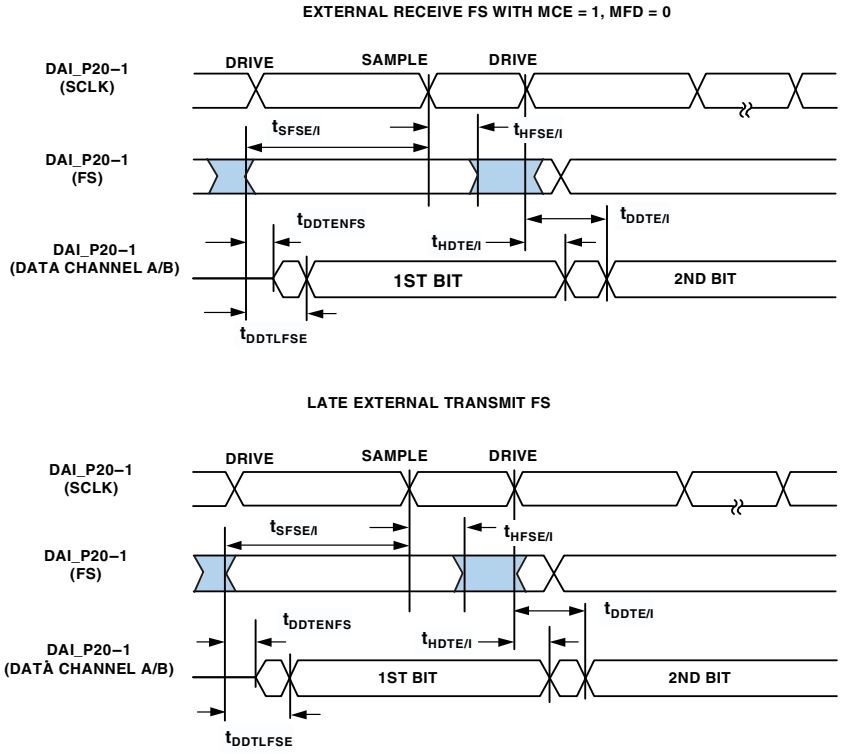

Figure 22. External Late Frame Sync[1]

[1] This figure reflects changes made to support left-justified sample pair mode.

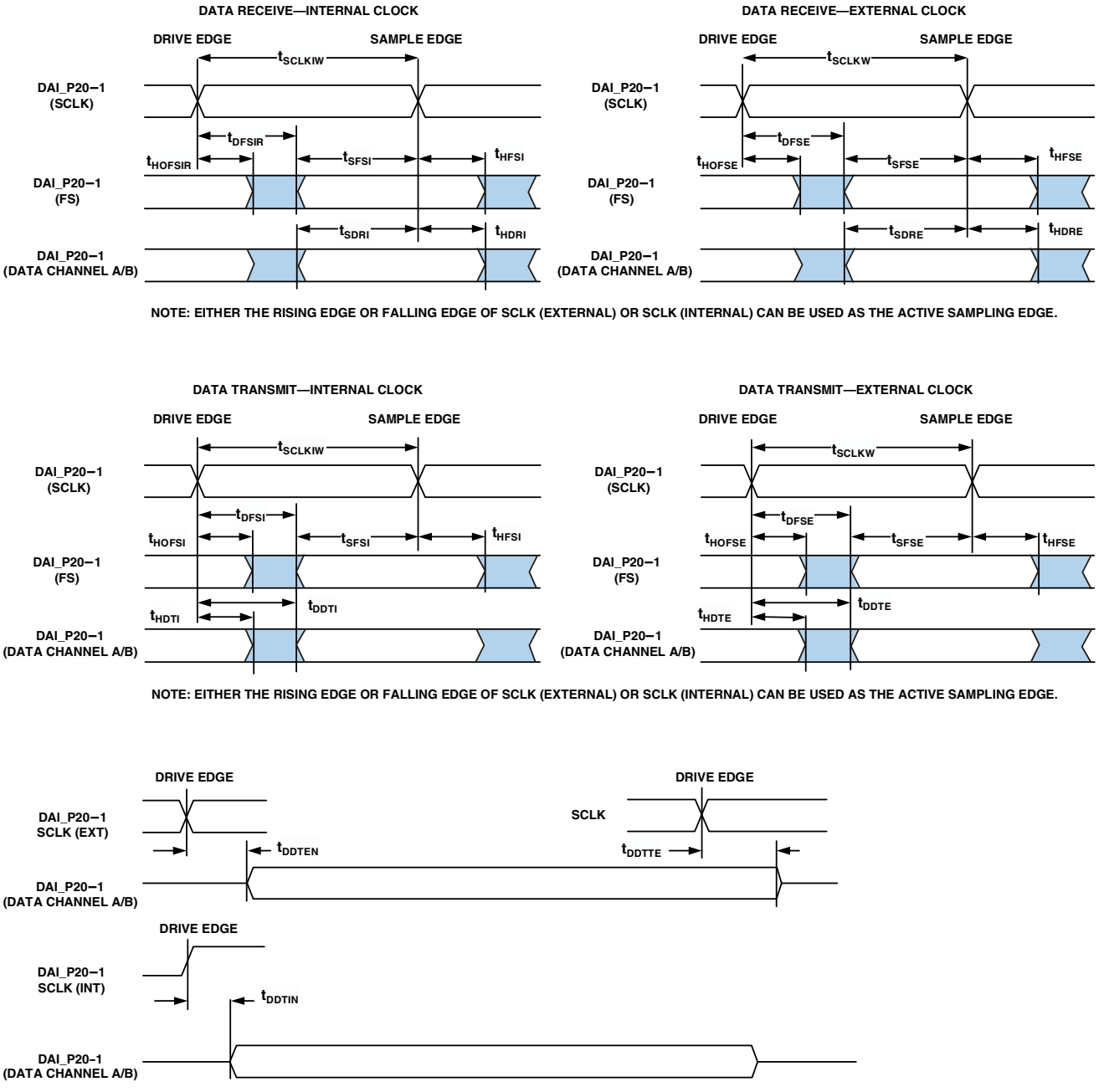

Figure 23. Serial Ports

Input Data Port (IDP)

The timing requirements for the IDP are given in Table 34. IDP signals (SCLK, FS, and SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 34. Input Data Port (IDP)

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{IDPCLKW}$	Clock Width	TBD	TBD	ns
t_{IDPCLK}	Clock Period	TBD	TBD	ns

[1] AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

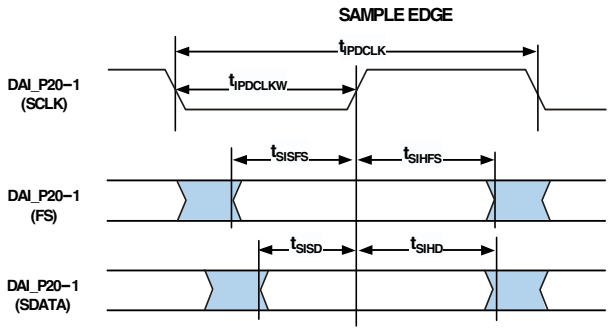

Figure 24. IDP Master Timing

Sample Rate Converter—Serial Input Port

The ASRC input signals (SCLK, FS, and SDATA) are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 35 are valid at the DAI_P20–1 pins.

Table 35. ASRC, Serial Input Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SRCSD}[1]	SDATA Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHD}[1]	SDATA Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SRCCLKW}$	Clock Width	TBD	TBD	ns
t_{SRCCLK}	Clock Period	TBD	TBD	ns

[1] AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

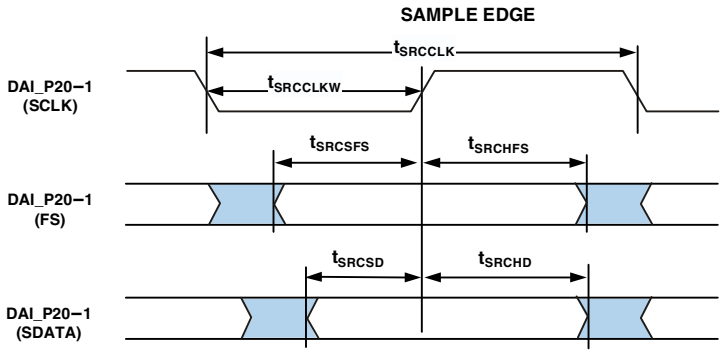

Figure 25. ASRC Serial Input Port Timing

Sample Rate Converter—Serial Output Port

For the serial output port, the frame-sync is an input and it should meet setup and hold times with regard to SCLK on the output port. The serial data output, SDATA, has a hold time and delay specification with regard to SCLK. Note that SCLK rising edge is the sampling edge and the falling edge is the drive edge.

Table 36. ASRC, Serial Output Port

Parameter		Min	Max	Unit
Timing Requirements				
t_{SRCSFS}[1]	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SRCHFS}[1]	FS Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SRCCLKW}$	Clock Width	TBD	TBD	ns
t_{SRCCLK}	Clock Period	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{SRCTDD}[1]	Transmit Data Delay After SCLK Falling Edge	TBD	TBD	ns
t_{SRCTDH}[1]	Transmit Data Hold After SCLK Falling Edge	TBD	TBD	ns

[1] AMI_DATA, SCLK, and FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

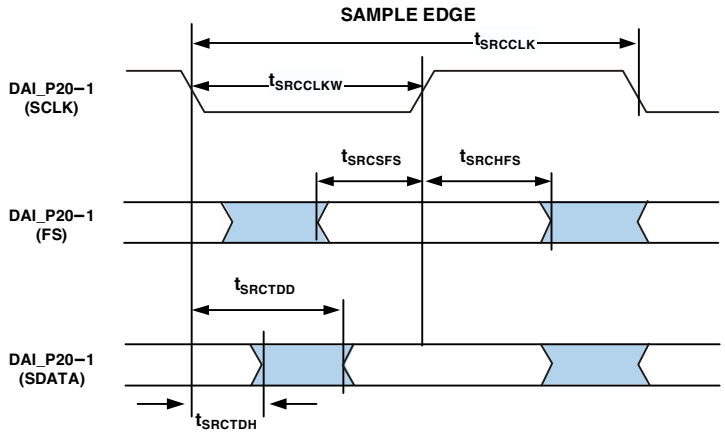

Figure 26. ASRC Serial Output Port Timing

Parallel Data Acquisition Port (PDAP)

The timing requirements for the PDAP are provided in Table 37. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-2146x SHARC Processor Hardware Reference*. Note that the most significant 16 bits of external PDAP data can be provided through the DATA7-0 pins. The remaining four bits can only be sourced through DAI_P4–1. The timing below is valid at the DATA7–0 pins.

Table 37. Parallel Data Acquisition Port (PDAP)

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPCLKEN}$[1]	PDAP_CLKEN Setup Before PDAP_CLK Sample Edge	TBD	TBD	ns
$t_{HPCLKEN}$[1]	PDAP_CLKEN Hold After PDAP_CLK Sample Edge	TBD	TBD	ns
t_{PDSD}[1]	PDAP_DAT Setup Before SCLK PDAP_CLK Sample Edge	TBD	TBD	ns
t_{PDHD}[1]	PDAP_DAT Hold After SCLK PDAP_CLK Sample Edge	TBD	TBD	ns
t_{PDCLKW}	Clock Width	TBD	TBD	ns
t_{PDCLK}	Clock Period	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{PDHLDD}	Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word	TBD	TBD	ns
t_{PDSTRB}	PDAP Strobe Pulse Width	TBD	TBD	ns

[1] Source pins of AMI_DATA are DATA7–0 or DAI pins. Source pins for SCLK and FS are: 1) DAI pins, 2) CLKIN through PCG, or 3) DAI pins through PCG.

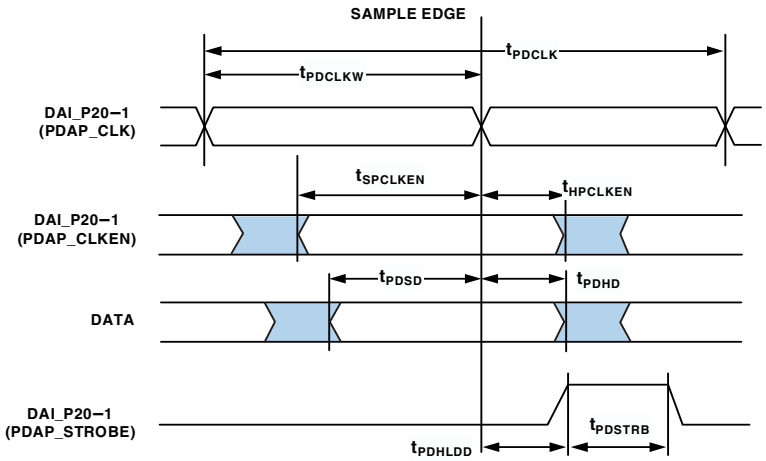

Figure 27. PDAP Timing

Pulse-Width Modulation Generators (PWM)

The following timing specifications apply when the AMI_ADDR23-8 pins are configured as PWM.

Table 38. Pulse-Width Modulation (PWM) Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{PWMW}	PWM Output Pulse Width	TBD	TBD	ns
t_{PWMP}	PWM Output Period	TBD	TBD	ns

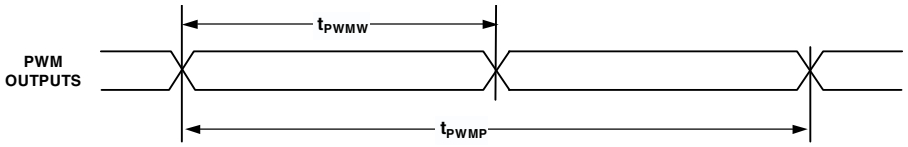

Figure 28. PWM Timing

S/PDIF Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I²S, or right justified with word widths of 16-, 18-, 20-, or 24-bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter-Serial Input Waveforms

Figure 29 shows the right-justified mode. LRCLK is high for the left channel and low for the right channel. Data is valid on the rising edge of SCLK. The MSB is delayed 12-bit clock periods (in 20-bit output mode) or 16-bit clock periods (in 16-bit output mode) from an LRCLK transition, so that when there are 64 SCLK periods per LRCLK period, the LSB of the data will be right-justified to the next LRCLK transition.

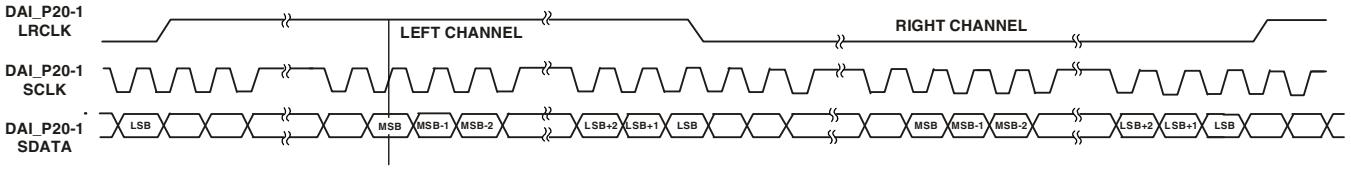

Figure 29. Right-Justified Mode

Figure 30 shows the default I²S-justified mode. LRCLK is low for the left channel and HI for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition but with a single SCLK period delay.

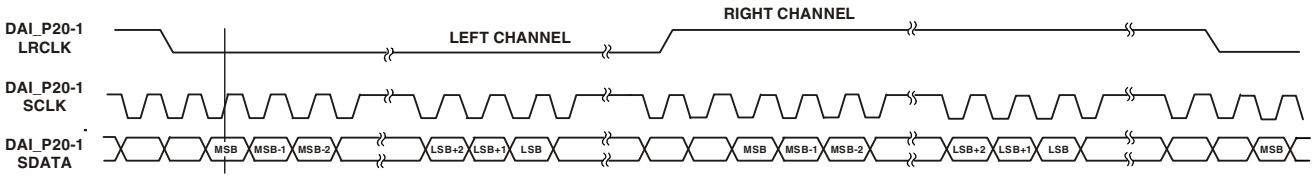

Figure 30. I²S-Justified Mode

Figure 31 shows the left-justified mode. LRCLK is high for the left channel and LO for the right channel. Data is valid on the rising edge of SCLK. The MSB is left-justified to an LRCLK transition with no MSB delay.

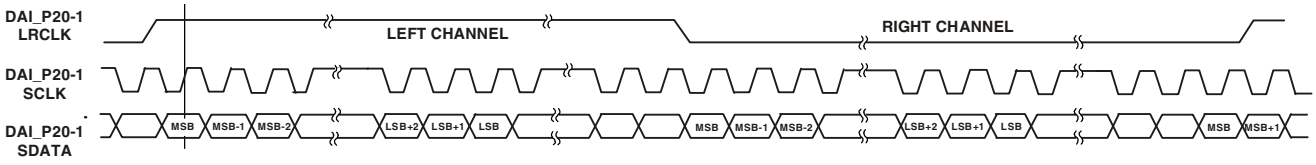

Figure 31. Left-Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 39. Input signals (SCLK, FS, SDATA) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

Table 39. S/PDIF Transmitter Input Data Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{SISFS}[1]	FS Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHFS}[1]	FS Hold After SCLK Rising Edge	TBD	TBD	ns
t_{SISD}[1]	SData Setup Before SCLK Rising Edge	TBD	TBD	ns
t_{SIHD}[1]	SData Hold After SCLK Rising Edge	TBD	TBD	ns
$t_{SITXCLKW}$	Transmit Clock Width	TBD	TBD	ns
$t_{SITXCLK}$	Transmit Clock Period	TBD	TBD	ns
$t_{SISCLKW}$	Clock Width	TBD	TBD	ns
t_{SISCLK}	Clock Period	TBD	TBD	ns

[1] AMI_DATA, SCLK, FS can come from any of the DAI pins. SCLK and FS can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

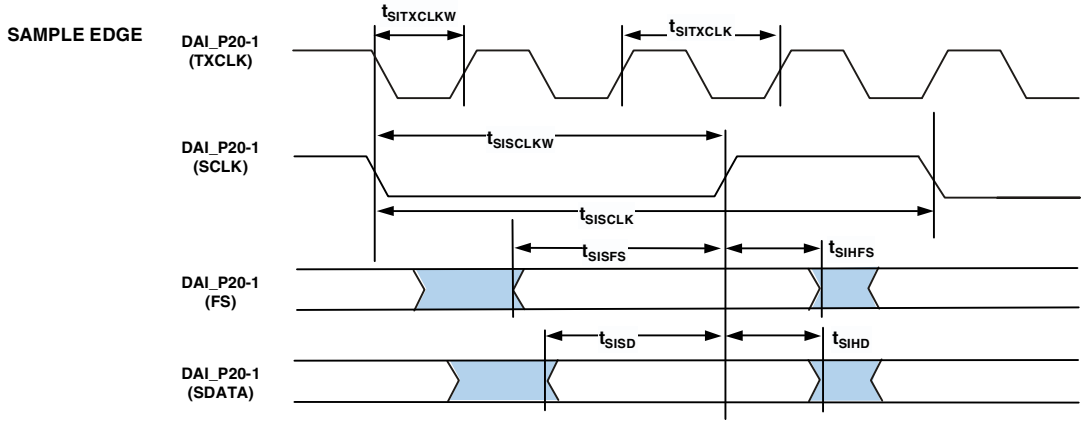

Figure 32. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter has an oversampling clock. This TxCLK input is divided down to generate the biphase clock.

Table 40. Over Sampling Clock (TxCLK) Switching Characteristics

Parameter	Min	Max	Unit
TxCLK Frequency for TxCLK = 384 × FS	TBD	TBD	MHz
TxCLK Frequency for TxCLK = 256 × FS	TBD	TBD	MHz
Frame Rate	TBD	TBD	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the TBD × FS clock.

Table 41. S/PDIF Receiver Internal Digital PLL Mode Timing

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	LRCLK Delay After SCLK	TBD	TBD	ns
t_{HOFSI}	LRCLK Hold After SCLK	TBD	TBD	ns
t_{DDTI}	Transmit Data Delay After SCLK	TBD	TBD	ns
t_{HDTI}	Transmit Data Hold After SCLK	TBD	TBD	ns
t_{SCLKIW}[1]	Transmit SCLK Width	TBD	TBD	ns

[1] SCLK frequency is TBD x FS where FS = the frequency of LRCLK.

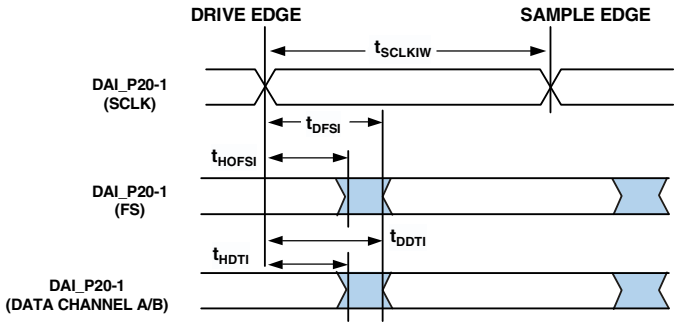

Figure 33. S/PDIF Receiver Internal Digital PLL Mode Timing

SPI Interface—Master

The ADSP-21462W/ADSP-21465W/ADSP-21467 contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 42 and Table 43 applies to both.

Table 42. SPI Interface Protocol—Master Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSPIDM}	Data Input Valid To SPICLK Edge (Data Input Setup Time)	TBD	TBD	ns
t_{HSPIDM}	SPICLK Last Sampling Edge To Data Input Not Valid	TBD	TBD	ns
Switching Characteristics				
$t_{SPICLKM}$	Serial Clock Cycle	TBD	TBD	ns
t_{SPICHM}	Serial Clock High Period	TBD	TBD	ns
t_{SPICLM}	Serial Clock Low Period	TBD	TBD	ns
$t_{DDSPIDM}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)	TBD	TBD	
$t_{HDSPIDM}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	TBD	TBD	ns
t_{SDSCIM}	FLAG3–0IN (SPI device select) Low to First SPICLK Edge	TBD	TBD	ns
t_{HDSM}	Last SPICLK Edge to FLAG3–0IN High	TBD	TBD	ns
t_{SPITDM}	Sequential Transfer Delay	TBD	TBD	ns

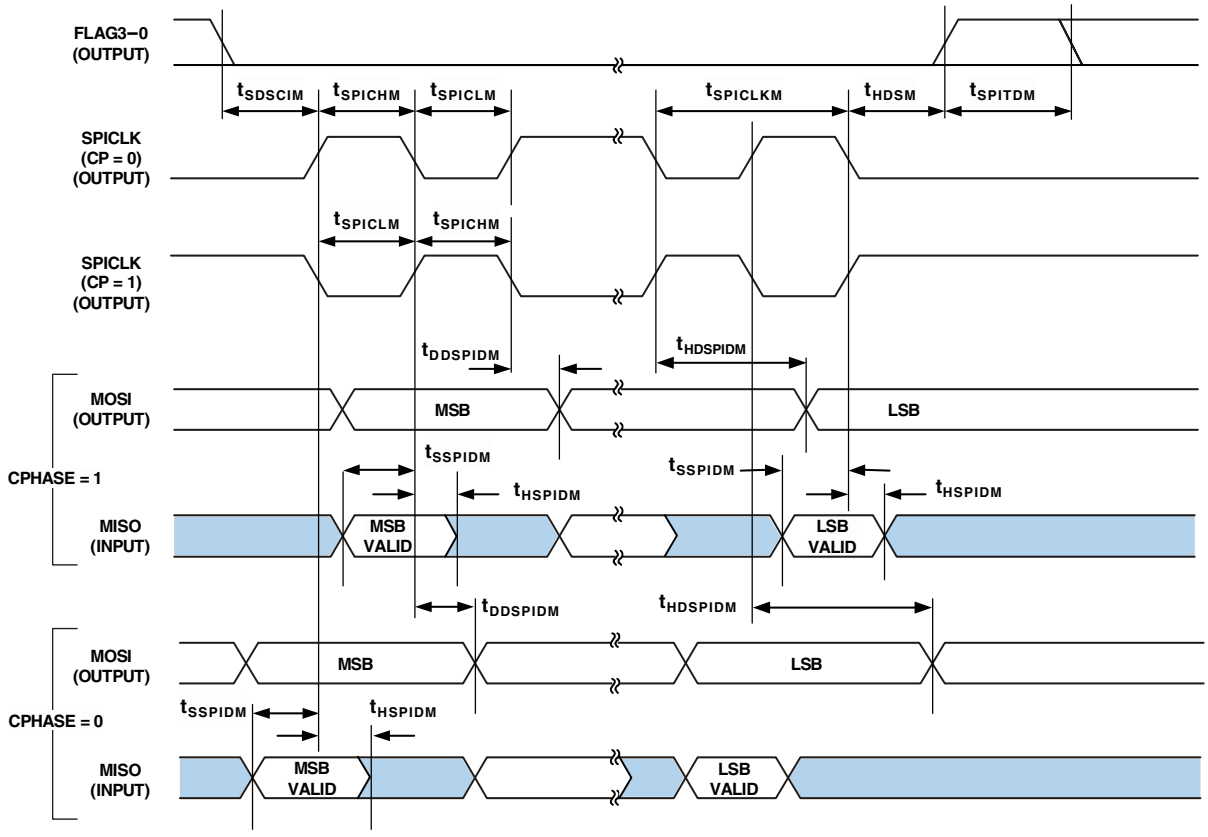

Figure 34. SPI Master Timing

SPI Interface—Slave

Table 43. SPI Interface Protocol—Slave Switching and Timing Specifications

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	TBD	TBD	ns
t_{SPICHS}	Serial Clock High Period	TBD	TBD	ns
t_{SPICLS}	Serial Clock Low Period	TBD	TBD	ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge			
	CPHASE = 0	TBD	TBD	ns
	CPHASE = 1	TBD	TBD	ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0	TBD	TBD	ns
t_{SSPIDS}	Data Input Valid to SPICLK edge (Data Input Set-up Time)	TBD	TBD	ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	TBD	TBD	ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0)	TBD	TBD	ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	TBD	TBD	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	TBD	TBD	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)	TBD	TBD	ns
$t_{HDSPIDS}$	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	TBD	TBD	ns
t_{DSOV}	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHAS E = 0)	TBD	TBD	ns

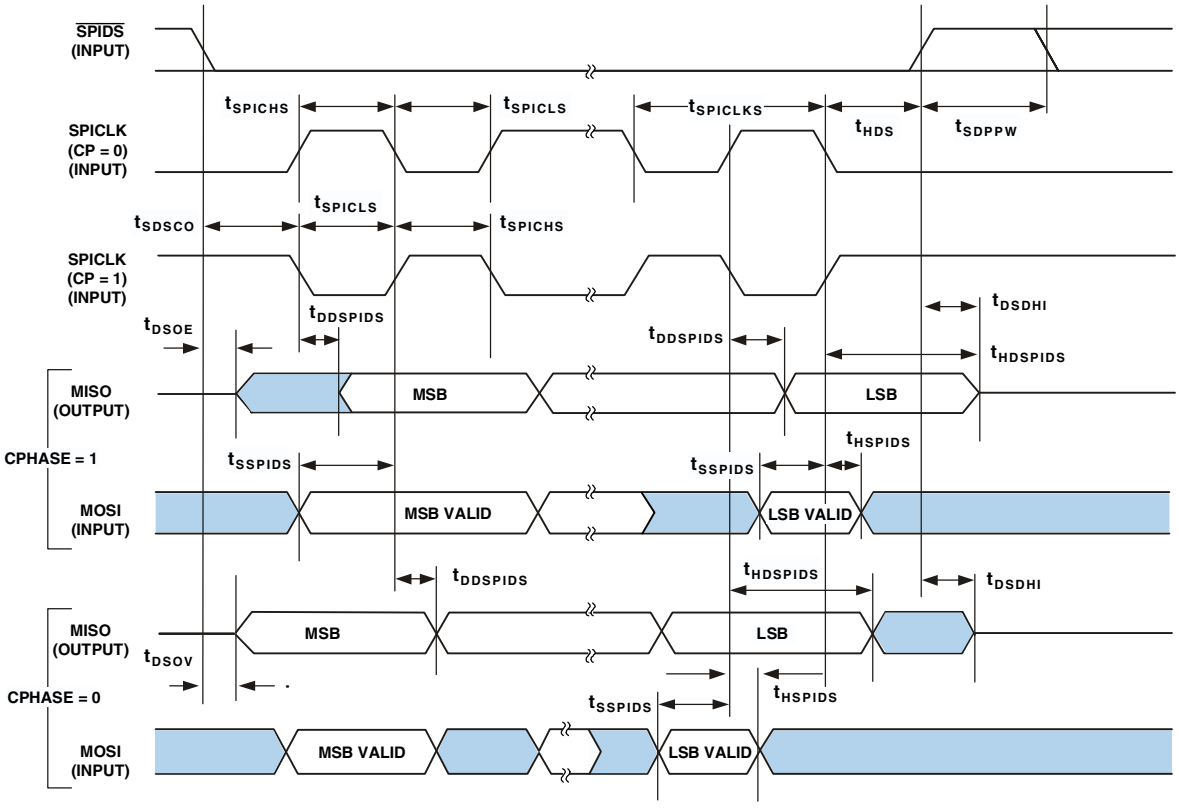

Figure 35. SPI Slave Timing

Universal Asynchronous Receiver-Transmitter (UART) Port—Receive and Transmit Timing

Figure 36 describes UART port receive and transmit operations. The maximum baud rate is PCLK/16 where PCLK = 1/tPCLK. As shown in Figure 36 there is some latency between the generation of internal UART interrupts and the external data operations. These latencies are negligible at the data transmission rates for the UART.

Table 44. UART Port

Parameter		Min	Max	Unit
Timing Requirement				
t_{RXD}[1]	Incoming Data Pulse Width	TBD	TBD	ns
Switching Characteristic		TBD	TBD	
t_{TXD}1	Outgoing Data Pulse Width	TBD	TBD	ns

[1] UART signals RXD and TXD are routed through DPI P14-1 pins using the SRU.

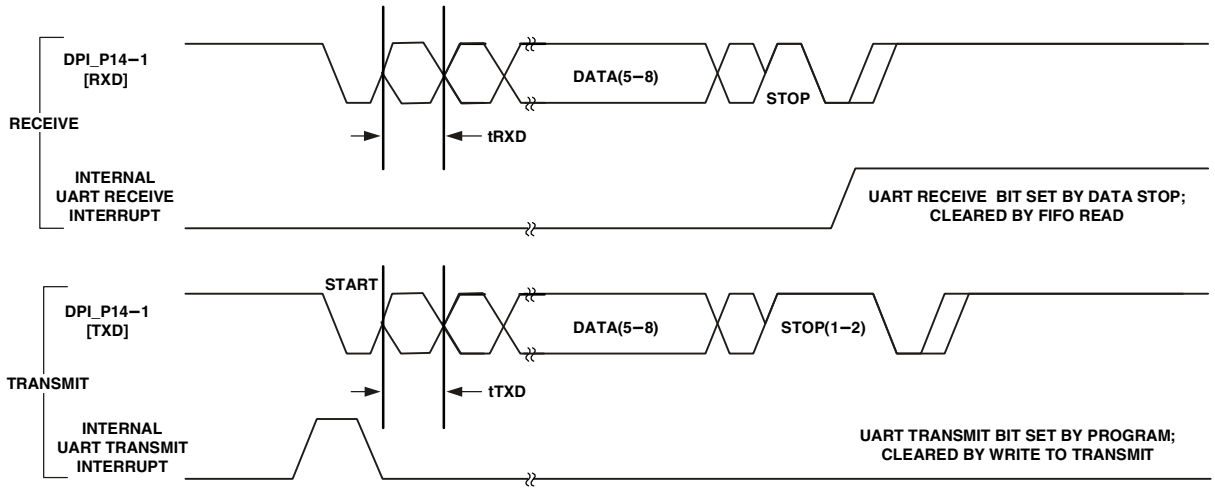

Figure 36. UART Port—Receive and Transmit Timing

TWI Controller Timing

Table 45 and Figure 37 provide timing information for the TWI interface. Input Signals (SCL, SDA) are routed to the DPI_P14–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

Table 45. Characteristics of the SDA and SCL Bus Lines for F/S-Mode TWI Bus Devices[1]

Parameter		Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency	TBD	TBD	TBD	TBD	kHz
t_{HDSTA}	Hold Time (repeated) Start Condition. After This Period, the First Clock Pulse is Generated.	TBD		TBD		µs
t_{LOW}	Low Period of the SCL Clock	TBD				µs
t_{HIGH}	High Period of the SCL Clock	TBD		TBD		µs
t_{SUSTA}	Setup Time for a Repeated Start Condition	TBD		TBD		µs
t_{HDDAT}	Data Hold Time for TWI-bus Devices	TBD		TBD		µs
t_{SUDAT}	Data Setup Time	TBD		TBD		ns
t_{SUSTO}	Setup Time for Stop Condition	TBD		TBD		µs
t_{BUF}	Bus Free Time Between a Stop and Start Condition	TBD		TBD		µs
t_{SP}	Pulse Width of Spikes Suppressed By the Input Filter	n/a	n/a	TBD	TBD	ns

[1] All values referred to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics on page 19.

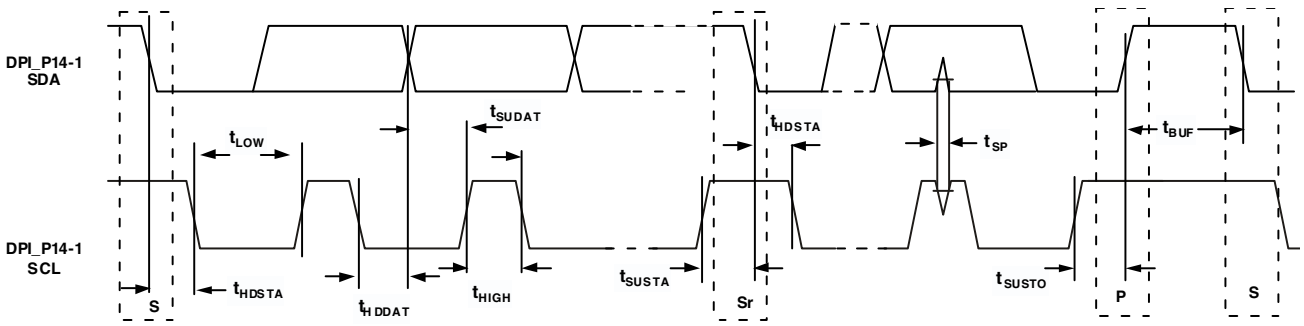

Figure 37. Fast and Standard Mode Timing on the TWI Bus

JTAG Test Access Port and Emulation

Table 46. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	TBD	TBD	ns
t_{STAP}	TDI, TMS Setup Before TCK High	TBD	TBD	ns
t_{HTAP}	TDI, TMS Hold After TCK High	TBD	TBD	ns
t_{SSYS}[1]	System Inputs Setup Before TCK High	TBD	TBD	ns
t_{HSYS}[1]	System Inputs Hold After TCK High	TBD	TBD	ns
t_{TRSTW}	$\overline{\text{TRST}}$ Pulse Width	TBD	TBD	ns
Switching Characteristics		TBD	TBD	
t_{DTDO}	TDO Delay from TCK Low	TBD	TBD	ns
t_{DSYS}[2]	System Outputs Delay After TCK Low	TBD	TBD	ns

[1] System Inputs = AD15–0, CLKCFG1–0, $\overline{\text{RESET}}$, BOOTCFG1–0, DAI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, AD15–0, $\overline{\text{AMI\_RD}}$, $\overline{\text{AMI\_WR}}$, FLAG3–0, CLKOUT, $\overline{\text{and EMU}}$.

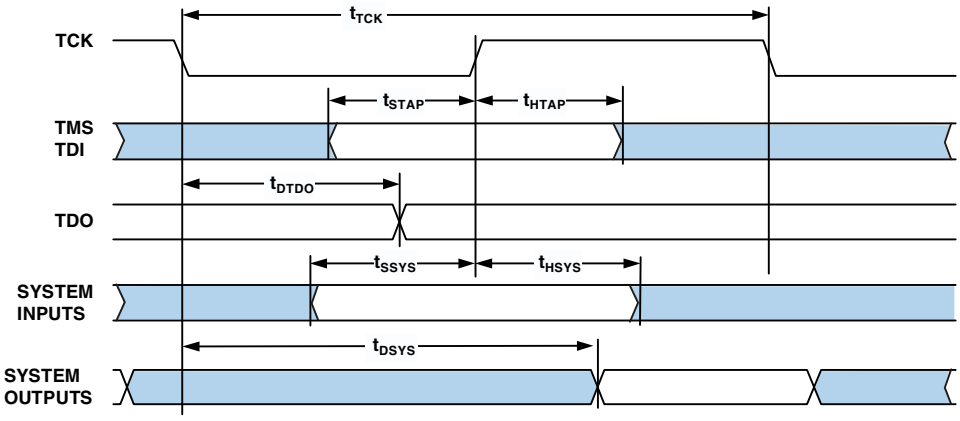

Figure 38. IEEE 1149.1 JTAG Test Access Port

Thermal Diode

TBD

Media Local Bus

TBD

OUTPUT DRIVE CURRENTS

Figure 39 shows typical I-V characteristics for the output drivers of the ADSP-21462W/ADSP-21465W/ADSP-21467. The curves represent the current drive capability of the output drivers as a function of output voltage.

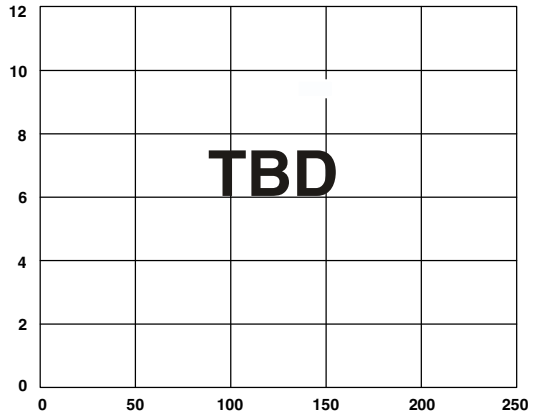

Figure 39. ADSP-21462W/ADSP-21465W/ADSP-21467 Typical Drive at Junction Temperature

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 15 on Page 25 through Table 46 on Page 51. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 40.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 41. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

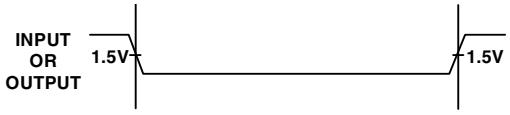

Figure 41. Voltage Reference Levels for AC Measurements

CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 40). Figure 44 shows graphically how output delays and holds vary with load capacitance. The graphs of Figure 42, Figure 43, and Figure 44 may not be linear

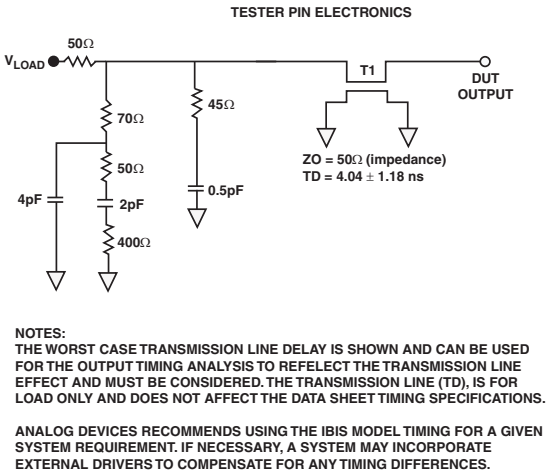

Figure 40. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

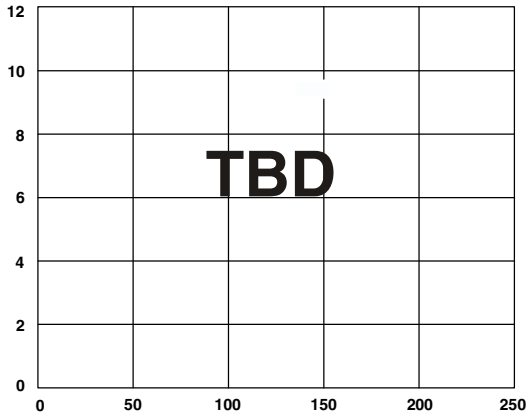

Figure 42. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Max)

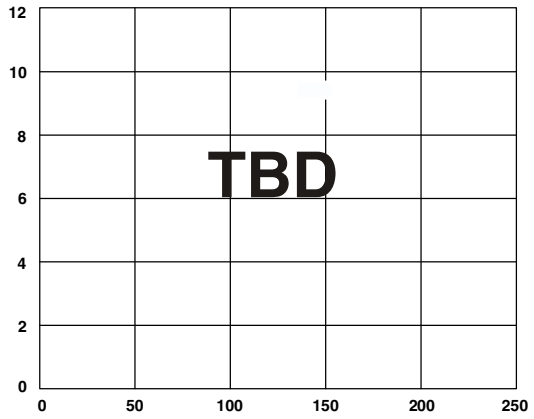

Figure 43. Typical Output Rise/Fall Time (20% to 80%, V_{DD_EXT} = Min)

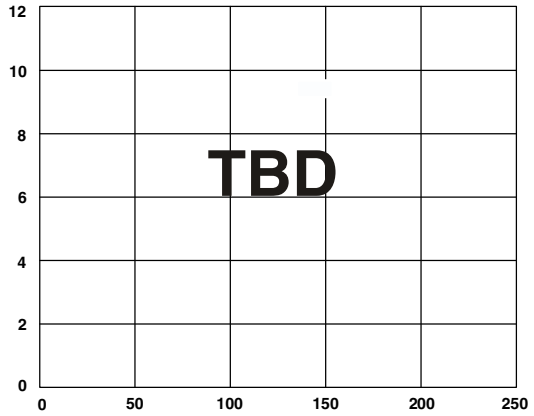

Figure 44. Typical Output Delay or Hold vs. Load Capacitance (at Ambient Temperature)

THERMAL CHARACTERISTICS

The ADSP-21462W/ADSP-21465W/ADSP-21467 processor is rated for performance over the temperature range specified in Operating Conditions on Page 18.

Table 47 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6 and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (PBGA). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature °C

T_{CASE} = case temperature (°C) measured at the top center of the package

Ψ_{JT} = junction-to-top (of package) characterization parameter is the Typical value from Table 47.

P_D = power dissipation

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = ambient temperature °C

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heatsink is required.

Values of θ_{JB} are provided for package comparison and PCB design considerations. Note that the thermal characteristics values provided in Table 47 are modeled values.

Table 47. Thermal Characteristics for 324-Lead PBGA

Parameter	Condition	Typical	Unit
θ_{JA}	Airflow = 0 m/s	TBD	°C/W
θ_{JMA}	Airflow = 1 m/s	TBD	°C/W
θ_{JMA}	Airflow = 2 m/s	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	Airflow = 0 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 1 m/s	TBD	°C/W
Ψ_{JMT}	Airflow = 2 m/s	TBD	°C/W

BALL CONFIGURATION - ADSP-2146x

Figure 45 shows the ball configuration for the ASDP-2146x.

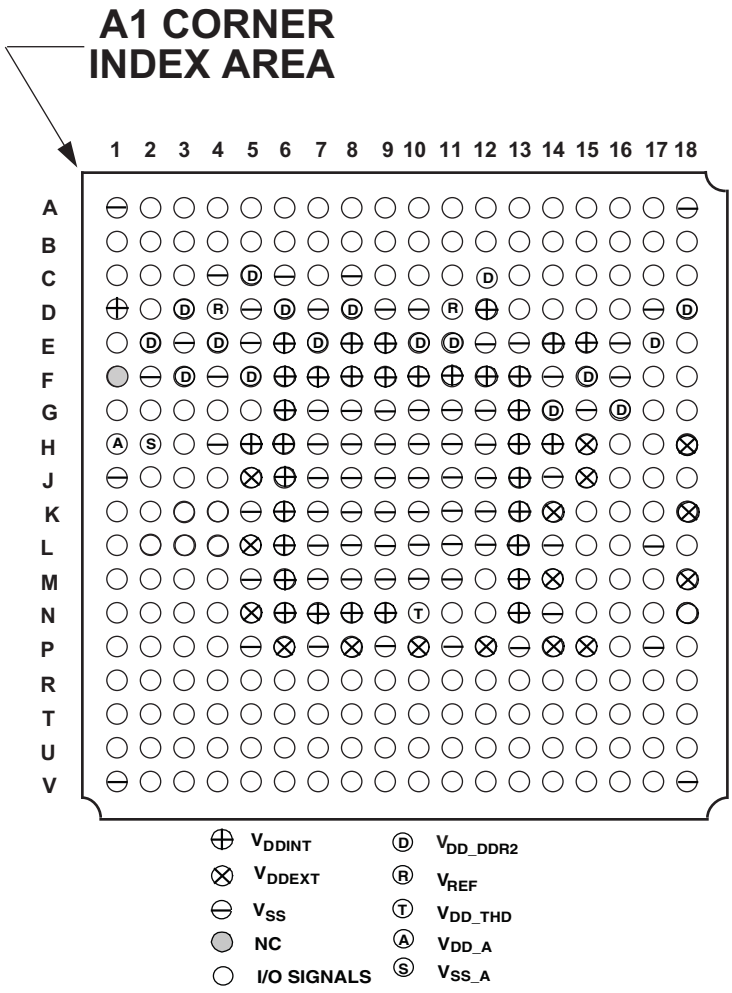

Figure 45. ADSP-21462W/ADSP-21465W/ADSP-21467 Ball Configuration - Pin Out

PBGA PINOUT

Table 48 lists the pin assignments of the SHARC processors.

Table 48. 19 mm by 19 mm PBGA Pin Assignment (Alphabetically by Signal)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
AMI_ACK	R10	$\overline{\text{BR3}}$	T8	DDR2_ADDR14	B17	DPI_P03	T1
AMI_ADDR0	V16	$\overline{\text{BR4}}$	V9	DDR2_ADDR15	A17	DPI_P04	R1
AMI_ADDR01	U16	$\overline{\text{BR5}}$	U9	DDR2_BA0	C18	DPI_P05	P1
AMI_ADDR02	T16	$\overline{\text{BR6}}$	T9	DDR2_BA1	C17	DPI_P06	P2
AMI_ADDR03	R16	CLK_CFG0	G1	DDR2_BA2	B18	DPI_P07	P3
AMI_ADDR04	V15	CLK_CFG1	G2	$\overline{\text{DDR2\_CAS}}$	C7	DPI_P08	P4
AMI_ADDR05	U15	CLKIN	L1	DDR2_CKE	E1	DPI_P09	N1
AMI_ADDR06	T15	CLKOUT/$\overline{\text{RESETOUT}}$ /$\overline{\text{RUNRSTIN}}$	M2	DDR2_CLK0	B7	DPI_P10	N2
AMI_ADDR07	R15	DAI_P01	R7	$\overline{\text{DDR2\_CLK0}}$	A7	DPI_P11	N3
AMI_ADDR08	V14	DAI_P02	V6	DDR2_CLK1	B13	DPI_P12	N4
AMI_ADDR09	U14	DAI_P03	U6	$\overline{\text{DDR2\_CLK1}}$	A13	DPI_P13	M3
AMI_ADDR10	T14	DAI_P04	T6	$\overline{\text{DDR2\_CS0}}$	C1	DPI_P14	M4
AMI_ADDR11	R14	DAI_P05	R6	$\overline{\text{DDR2\_CS1}}$	D1	$\overline{\text{EMU}}$	K2
AMI_ADDR12	V13	DAI_P06	V5	$\overline{\text{DDR2\_CS2}}$	C2	FLAG0	R8
AMI_ADDR13	U13	DAI_P07	U5	$\overline{\text{DDR2\_CS3}}$	D2	FLAG1	V7
AMI_ADDR14	T13	DAI_P08	T5	DDR2_DATA0	B2	FLAG2	U7
AMI_ADDR15	R13	DAI_P09	R5	DDR2_DATA01	A2	FLAG3	T7
AMI_ADDR16	V12	DAI_P10	V4	DDR2_DATA02	B3	ID_0	G3
AMI_ADDR17	U12	DAI_P11	U4	DDR2_DATA03	A3	ID_1	G4
AMI_ADDR18	T12	DAI_P12	T4	DDR2_DATA04	B5	ID_2	G5
AMI_ADDR19	R12	DAI_P13	R4	DDR2_DATA05	A5	LACK_0	K17
AMI_ADDR20	V11	DAI_P14	V3	DDR2_DATA06	B6	LACK_1	P17
AMI_ADDR21	U11	DAI_P15	U3	DDR2_DATA07	A6	LCLK_0	J18
AMI_ADDR22	T11	DAI_P16	T3	DDR2_DATA08	B8	LCLK_1	N18
AMI_ADDR23	R11	DAI_P17	R3	DDR2_DATA09	A8	LDAT0_0	E18
AMI_DATA0	U18	DAI_P18	V2	DDR2_DATA10	B9	LDAT0_1	F17
AMI_DATA1	T18	DAI_P19	U2	DDR2_DATA11	A9	LDAT0_2	F18
AMI_DATA2	R18	DAI_P20	T2	DDR2_DATA12	A11	LDAT0_3	G17
AMI_DATA3	P18	DDR2_ADDR0	D13	DDR2_DATA13	B11	LDAT0_4	G18
AMI_DATA4	V17	DDR2_ADDR01	C13	DDR2_DATA14	A12	LDAT0_5	H16
AMI_DATA5	U17	DDR2_ADDR02	D14	DDR2_DATA15	B12	LDAT0_6	H17
AMI_DATA6	T17	DDR2_ADDR03	C14	DDR2_DM0	C3	LDAT0_7	J16
AMI_DATA7	R17	DDR2_ADDR04	B14	DDR2_DM1	C11	LDAT1_0	K18
$\overline{\text{AMI\_MS0}}$	T10	DDR2_ADDR05	A14	$\overline{\text{DDR2\_DQS0}}$	B4	LDAT1_1	L16
$\overline{\text{AMI\_MS1}}$	U10	DDR2_ADDR06	D15	DDR2_DQS0	A4	LDAT1_2	L17
$\overline{\text{AMI\_RD}}$	J4	DDR2_ADDR07	C15	$\overline{\text{DDR2\_DQS1}}$	B10	LDAT1_3	L18
$\overline{\text{AMI\_WR}}$	V10	DDR2_ADDR08	B15	DDR2_DQS1	A10	LDAT1_4	M16
BOOT_CFG0	J2	DDR2_ADDR09	A15	DDR2_ODT	B1	LDAT1_5	M17
BOOT_CFG1	J3	DDR2_ADDR10	D16	$\overline{\text{DDR2\_RAS}}$	C9	LDAT1_6	N16
BOOT_CFG2	H3	DDR2_ADDR11	C16	$\overline{\text{DDR2\_WE}}$	C10	LDAT1_7	P16
$\overline{\text{BR1}}$	V8	DDR2_ADDR12	B16	DPI_P01	R2	MLBCLK	K3
$\overline{\text{BR2}}$	U8	DDR2_ADDR13	A16	DPI_P02	U1	MLBDO	L4

Table 48. 19 mm by 19 mm PBGA Pin Assignment (Alphabetically by Signal)

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
MLBSIG	L2	V_{DD_INT}	N9	V_{SS}	E3	V_{SS}	L12
MLBSO	L3	V_{DD_INT}	N8	V_{SS}	D10	V_{SS}	L10
MLDAT	K4	V_{DD_INT}	N7	V_{SS}	D17	V_{SS}	L11
$\overline{RESET}$	M1	V_{DD_INT}	N6	V_{SS}	D9	V_{SS}	L9
RPBA	R9	V_{DD_INT}	N13	V_{SS}	E5	V_{SS}	L14
TCK	K15	V_{DD_INT}	M6	V_{SS}	E12	V_{SS}	M5
TDI	L15	V_{DD_INT}	M13	V_{SS}	E13	V_{SS}	M7
TDO	M15	V_{DD_INT}	L6	V_{SS}	E16	V_{SS}	M8
THD_M	N12	V_{DD_INT}	L13	V_{SS}	F2	V_{SS}	M9
THD_P	N11	V_{DD_INT}	K6	V_{SS}	F4	V_{SS}	M10
TMS	K16	V_{DD_INT}	K13	V_{SS}	F14	V_{SS}	M11
$\overline{TRST}$	N15	V_{DD_INT}	J6	V_{SS}	F16	V_{SS}	M12
VDD_A	H1	V_{DD_INT}	J13	V_{SS}	G7	V_{SS}	N14
V_{DD_DDR2}	G16	V_{DD_INT}	H6	V_{SS}	G8	V_{SS}	N17
V_{DD_DDR2}	G14	V_{DD_INT}	H5	V_{SS}	G9	V_{SS}	P5
V_{DD_DDR2}	F5	V_{DD_INT}	H14	V_{SS}	G10	V_{SS}	P7
V_{DD_DDR2}	F3	V_{DD_INT}	H13	V_{SS}	G11	V_{SS}	P9
V_{DD_DDR2}	F15	V_{DD_INT}	G6	V_{SS}	G12	V_{SS}	P11
V_{DD_DDR2}	E7	V_{DD_INT}	G13	V_{SS}	G15	V_{SS}	P13
V_{DD_DDR2}	E2	V_{DD_INT}	F9	V_{SS}	H4	V_{SS}	V1
V_{DD_DDR2}	E17	V_{DD_INT}	F8	V_{SS}	H7	V_{SS}	V18
V_{DD_DDR2}	E11	V_{DD_INT}	F7	V_{SS}	H8	V_{REF}	D4
V_{DD_DDR2}	E10	V_{DD_INT}	F6	V_{SS}	H9	V_{REF}	D11
V_{DD_DDR2}	D8	V_{DD_INT}	F13	V_{SS}	H10	XTAL	K1
V_{DD_DDR2}	D6	V_{DD_INT}	F12	V_{SS}	H11		
V_{DD_DDR2}	D3	V_{DD_INT}	F11	V_{SS}	H12		
V_{DD_DDR2}	D18	V_{DD_INT}	F10	V_{SS}	J1		
V_{DD_DDR2}	C5	V_{DD_INT}	E9	V_{SS}	J7		
V_{DD_DDR2}	C12	V_{DD_INT}	E8	V_{SS}	J8		
V_{DD_DDR2}	E17	V_{DD_INT}	E6	V_{SS}	J9		
V_{DD_EXT}	P8	V_{DD_INT}	E15	V_{SS}	J10		
V_{DD_EXT}	P6	V_{DD_INT}	E14	V_{SS}	J11		
V_{DD_EXT}	P15	V_{DD_INT}	D12	V_{SS}	J12		
V_{DD_EXT}	P14	V_{DD_THD}	N10	V_{SS}	J14		
V_{DD_EXT}	P12	V_{DD_INT}	N9	V_{SS}	J17		
V_{DD_EXT}	P10	V_{DD_INT}	N8	V_{SS}	K5		
V_{DD_EXT}	N5	V_{SS_A}	H2	V_{SS}	K7		
V_{DD_EXT}	M18	V_{SS}	A1	V_{SS}	K8		
V_{DD_EXT}	M14	V_{SS}	A18	V_{SS}	K9		
V_{DD_EXT}	L5	V_{SS}	C4	V_{SS}	K10		
V_{DD_EXT}	K14	V_{SS}	C6	V_{SS}	K11		
V_{DD_EXT}	J5	V_{SS}	C8	V_{SS}	K12		
V_{DD_EXT}	J15	V_{SS}	D5	V_{SS}	L7		
V_{DD_INT}	F1	V_{SS}	D7	V_{SS}	L8		

OUTLINE DIMENSIONS

The ADSP-21462W/ADSP-21465W/ADSP-21467 processors are available in a 19 mm by 19 mm PBGA lead-free package.

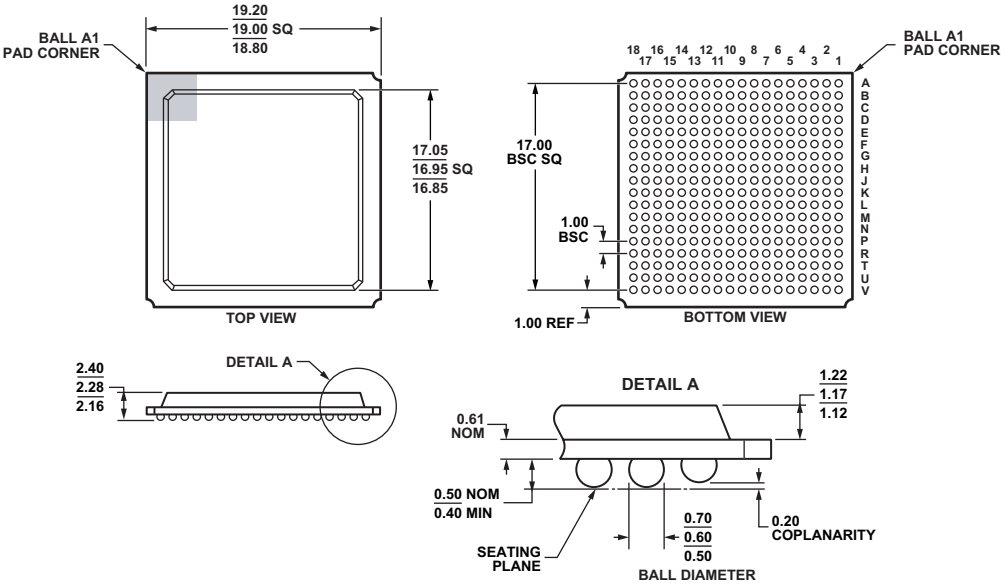

Figure 46. 324-Ball Plastic Ball Grid Array [PBGA]
(B-324)
Dimensions shown in millimeters

AUTOMOTIVE PRODUCTS

The ADSP-21462W and ADSP-21465W are available for automotive applications with controlled manufacturing. Note that these special models may have specifications that differ from the general release models.

The automotive grade products shown in Table 49 are available for use in automotive applications. Contact your local ADI account representative or authorized ADI product distributor for specific product ordering information. Note that all automotive products are RoHS compliant.

Table 49. Automotive Products

Model	Temperature Range[1]	On-Chip SRAM	ROM	Package Description	Package Option
AD21462WBBZ3xx	–40°C to +85°C	5M bit	4M bit	324-Ball Plastic Ball Grid Array (PBGA)	B-324-2
AD21465WBBZ3xx	–40°C to +85°C	5M bit	4M bit	324-Ball Plastic Ball Grid Array (PBGA)	B-324-2

[1] Referenced temperature is ambient temperature.

ORDERING GUIDE

Model	Temperature Range[1]	On-Chip SRAM	ROM	Package Description	Package Option
ADSP-21467KBZ-ENG[2, 3, 4]	0 °C to +70 °C	5 Mbit	4 Mbit	324-Ball Plastic Ball Grid Array (PBGA)	B-324-2

[1] Referenced temperature is ambient temperature.
[2] Z =Part number subject to change.
[3] Z =RoHS Compliant Part
[4] Available with a wide variety of audio algorithm combinations sold as part of a chipset and bundled with necessary software. For a complete list, visit our website at www.analog.com/SHARC

PR07900-0-11/08(PrA)