High IP3, 10 MHz to 6 GHz, Active Mixer

ADL5801

FEATURES

- Broadband upconverter/downconverter
- Power conversion gain of 1.8 dB
- Broadband RF, LO, and IF ports
- SSB noise figure (NF) of 9.75 dB
- Input IP3: 28.5 dBm
- Input P1dB: 13.3 dBm
- Typical LO drive: 0 dBm
- Single-supply operation: 5 V at 130 mA
- Adjustable bias for low power operation
- Exposed paddle, 4 mm × 4 mm, 24-lead LFCSP package

APPLICATIONS

- Cellular base station receivers
- Radio link downconverters
- Broadband block conversion
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

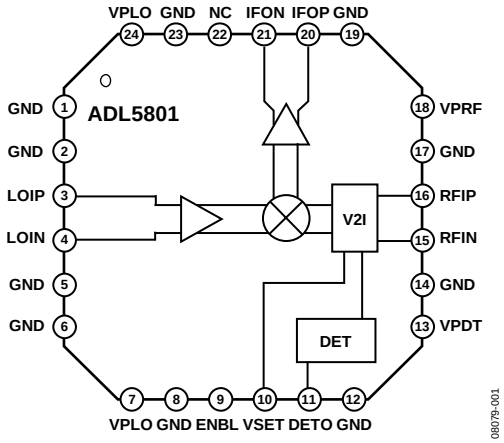

Figure 1.

GENERAL DESCRIPTION

The ADL5801 uses a high linearity, doubly balanced, active mixer core with integrated LO buffer amplifier to provide high dynamic range frequency conversion from 10 MHz to 6 GHz. The mixer benefits from a proprietary linearization architecture that provides enhanced input IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB noise figure, and dc current to be optimized using a single control pin. An optional input power detector is provided for adaptive bias control. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The adaptive bias feature allows the part to provide high input IP3 performance when presented with large blocking signals. When blockers are removed, the ADL5801 can automatically bias down to provide low noise figure and low power consumption.

The balanced active mixer arrangement provides superb LO-to-RF and LO-to-IF leakage, typically better than −40 dBm. The IF outputs are designed to provide a typical voltage conversion gain of 7.8 dB when loaded into a 200 Ω load. The broad frequency range of the open-collector IF outputs allows the ADL5801 to be applied as an upconverter for various transmit applications.

The ADL5801 is fabricated using a SiGe high performance IC process. The device is available in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

Rev. 0

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REVISION HISTORY

2/10—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 747 MHz, LO power = 0 dBm, Z_0[1] = 50 Ω, VSET = 3.8 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		12		dB
Input Impedance			50		Ω
RF Frequency Range		10		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		230		Ω
IF Frequency Range	Can be matched externally to 3000 MHz	LF		600	MHz
DC Bias Voltage[2]	Externally generated	4.75	V_S	5.25	V
LO INTERFACE					
LO Power		−10	0	+10	dBm
Return Loss			15		dB
Input Impedance			50		Ω
LO Frequency Range		10		6000	MHz
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Quiescent Current	Resistor programmable		130	200	mA
Disable Current	ENBL pin high		50		mA
Enable Time	Time from ENBL pin low to enable		182		ns
Disable Time	Time from ENBL pin high to disable		28		ns
DYNAMIC PERFORMANCE at f_{RF} = 900 MHz/1900 MHz					
Power Conversion Gain[3]	f_{RF} = 900 MHz		1.8		dB
	f_{RF} = 1900 MHz		1.8		dB
Voltage Conversion Gain[4]	f_{RF} = 900 MHz		7.8		dB
	f_{RF} = 1900 MHz		7.8		dB
SSB Noise Figure	f_{CENT} = 900 MHz, VSET = 2.0 V		9.75		dB
	f_{CENT} = 1900 MHz, VSET = 2.0 V		11.5		dB
SSB Noise Figure Under Blocking[5]	f_{CENT} = 900 MHz, VSET = 2.0 V		19.5		dB
	f_{CENT} = 1900 MHz, VSET = 2.0 V		20		dB
Input Third-Order Intercept[6]	f_{CENT} = 900 MHz		28.5		dBm
	f_{CENT} = 1900 MHz		26.4		dBm
Input Second-Order Intercept[7]	f_{CENT} = 900 MHz		63		dBm
	f_{CENT} = 1900 MHz		49.7		dBm
Input 1 dB Compression Point	f_{RF} = 900 MHz		13.3		dBm
	f_{RF} = 1900 MHz		12.7		dBm
LO-to-IF Output Leakage	Unfiltered IF output		−27		dBm
LO-to-RF Input Leakage			−30		dBm
RF-to-IF Output Isolation			−35		dBc
IF/2 Spurious[8]	0 dBm input power, f_{RF} = 900 MHz		−67.5		dBc
	0 dBm input power, f_{RF} = 1900 MHz		−53		dBc
	0 dBm input power, f_{RF} = 900 MHz		−65.5		dBc
	0 dBm input power, f_{RF} = 1900 MHz		−72.6		dBc

[1] Z_0 is the characteristic impedance assumed for all measurements and the PCB.
[2] Supply voltage must be applied from an external circuit through choke inductors.
[3] Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (TC1-1-13M+), and PCB loss.
[4] Z_{SOURCE} = 50 Ω, differential; Z_{LOAD} = 200 Ω differential; Z_{SOURCE} is the impedance of the source instrument; Z_{LOAD} is the load impedance at the output.
[5] $f_{RF} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, blocker level = 0 dBm.
[6] $f_{RF1} = (f_{CENT} - 1)$ MHz, $f_{RF2} = (f_{CENT})$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at −10 dBm.
[7] $f_{RF1} = (f_{CENT})$ MHz, $f_{RF2} = (f_{CENT} + 100)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at −10 dBm.
[8] For details, see the Spur Performance section.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
VSET, ENBL	5.5 V
IFOP, IFON	5.5 V
RFIN Power	20 dBm
Internal Power Dissipation	1.2 W
θ_{JA} (Exposed Paddle Soldered Down)[1]	26.5°C/W
θ_{JC} (at Exposed Paddle)	8.7°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] As measured on the evaluation board. For details, see the Evaluation Board section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

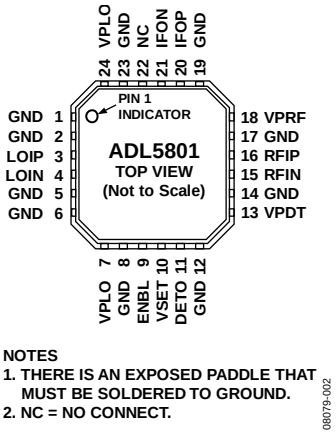

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 6, 8, 12, 14, 17, 19, 23	GND	Device Common (DC Ground).
3, 4	LOIP, LOIN	Differential LO Input Terminal. Internally matched to 50 Ω. Must be ac-coupled.
7, 24	VPLO	Positive Supply Voltage for LO System.
9	ENBL	Device Enable. Pull high to disable the device; pull low to enable.
10	VSET	Input IP3 Bias Adjustment. The voltage presented to the VSET pin sets the internal bias of the mixer core and allows for adaptive control of the input IP3 and NF characteristics of the mixer core.
11	DETO	Detector Output. The DETO pin should be loaded with a capacitor to ground. The developed voltage is proportional to the rms input level. When the DETO output voltage is connected to the VSET input pin, the part auto biases and increases input IP3 performance when presented with large signal input levels.
13	VPDT	Positive Supply Voltage for Detector.
15, 16	RFIN, RFIP	Differential RF Input Terminal. Internally matched to 50 Ω differential input impedance. Must be ac-coupled.
18	VPRF	Positive Supply Voltage for RF Input System.
20, 21	IFOP, IFON	Differential IF Output Terminal. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
22	NC	Not Connected.
	EPAD	The exposed paddle must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, VSET = 3.8 V as measured using a typical circuit schematic, unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

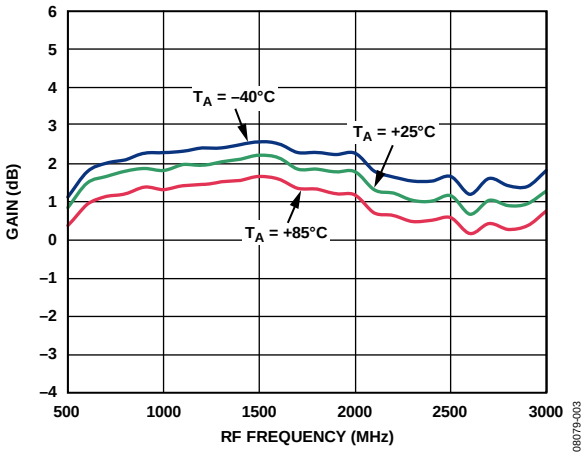

Figure 3. Power Conversion Gain vs. RF Frequency

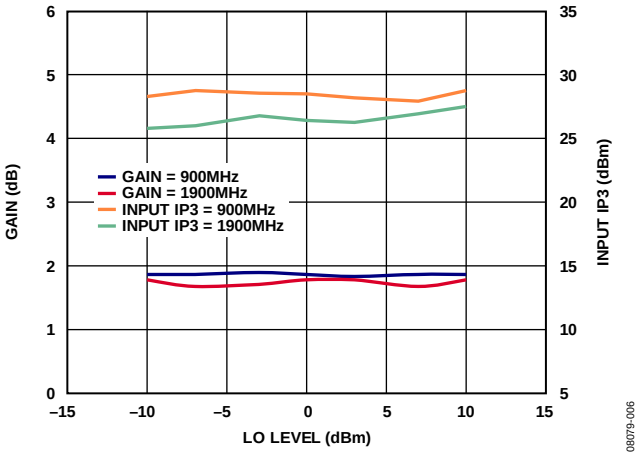

Figure 6. Power Conversion Gain and Input IP3 vs. LO Power

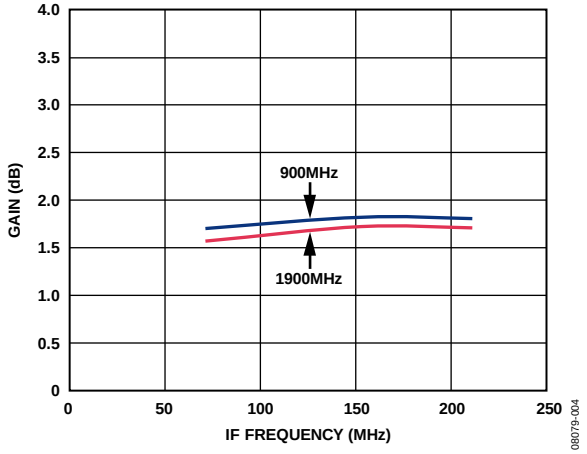

Figure 4. Power Conversion Gain vs. IF Frequency

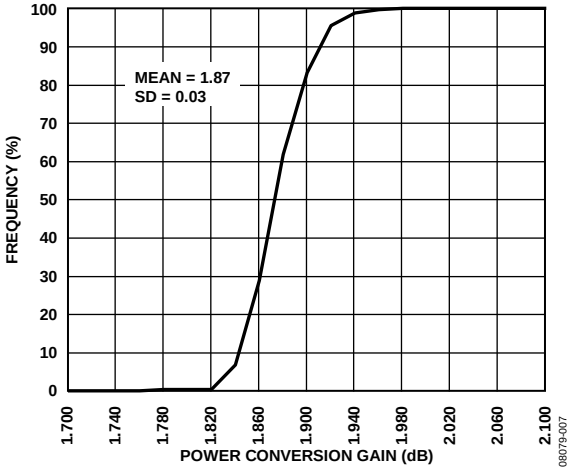

Figure 7. Power Conversion Gain Distribution

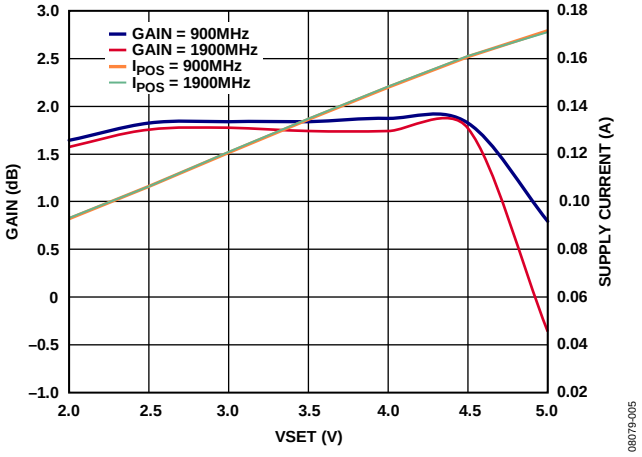

Figure 5. Power Conversion Gain and Supply Current vs. VSET

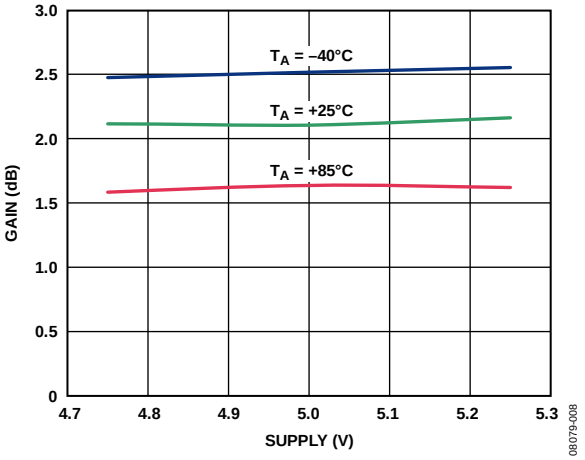

Figure 8. Power Conversion Gain vs. Supply Voltage

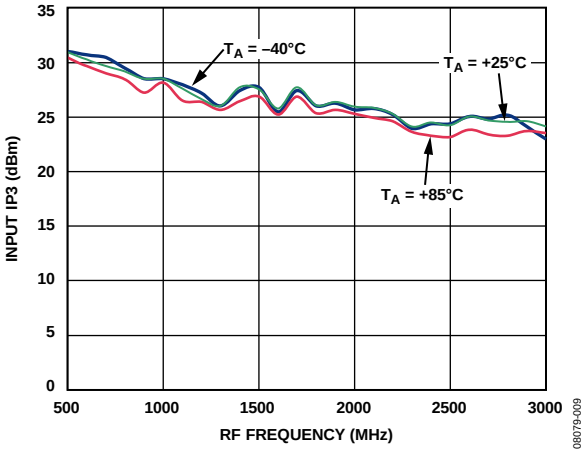

Figure 9. Input IP3 vs. RF Frequency

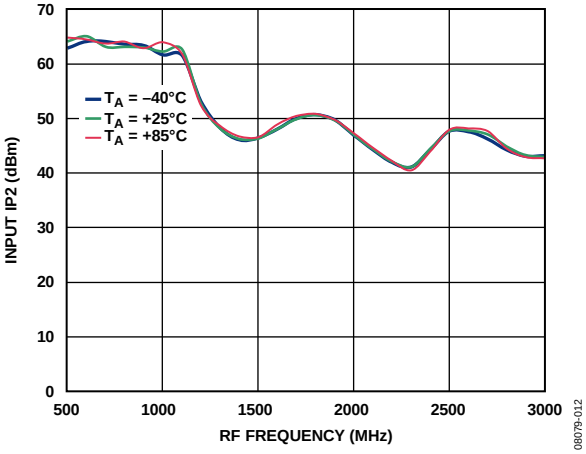

Figure 12. Input IP2 vs. RF Frequency

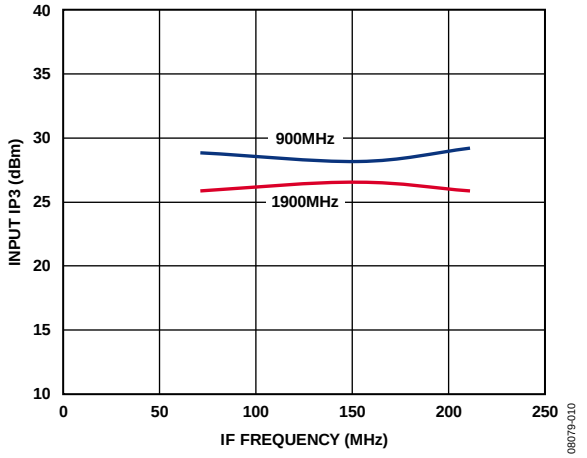

Figure 10. Input IP3 vs. IF Frequency

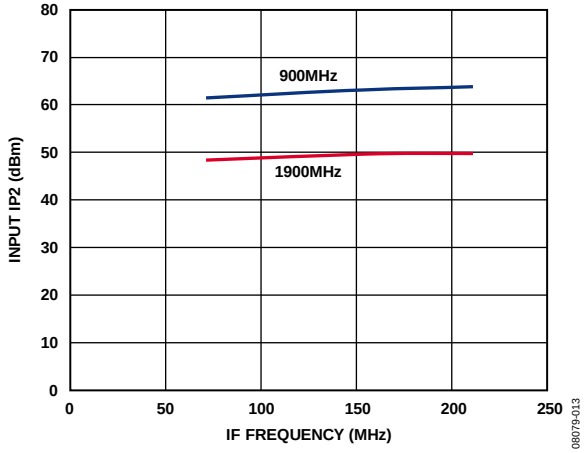

Figure 13. Input IP2 vs. IF Frequency

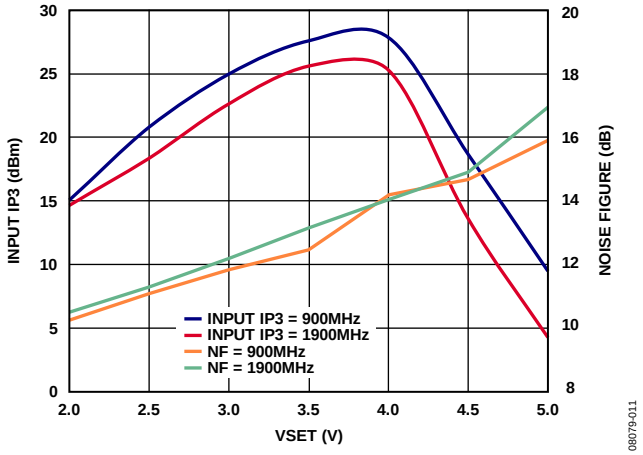

Figure 11. Input IP3 and Noise Figure vs. VSET

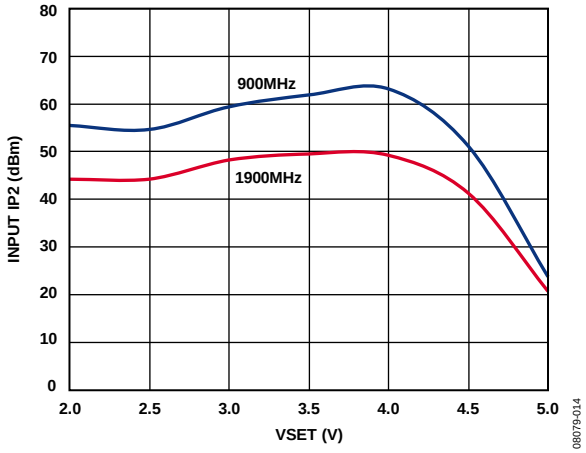

Figure 14. Input IP2 vs. VSET

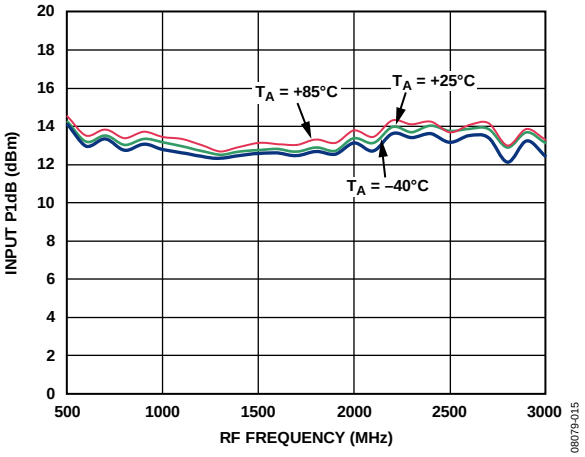

Figure 15. Input P1dB vs. RF Frequency

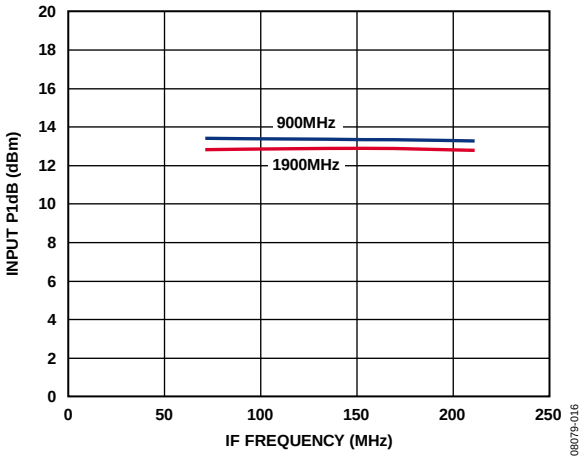

Figure 16. Input P1dB vs. IF Frequency

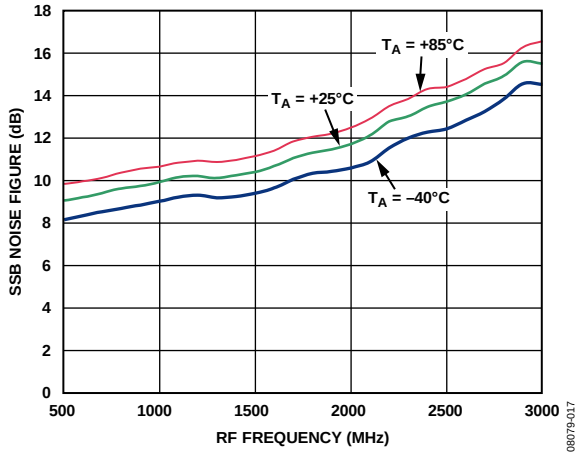

Figure 17. SSB Noise Figure vs. RF Frequency (VSET = 2.0 V)

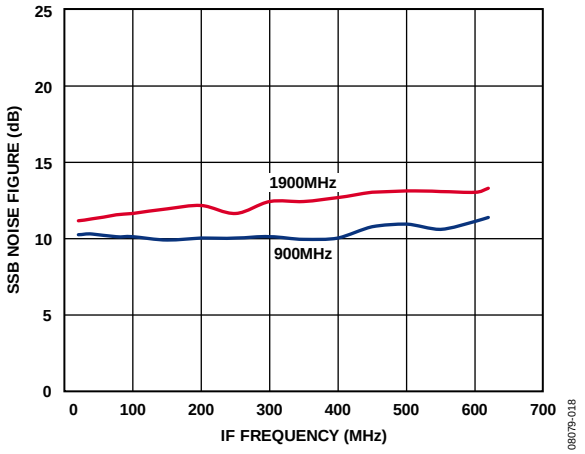

Figure 18. SSB Noise Figure vs. IF Frequency (VSET = 2.0 V)

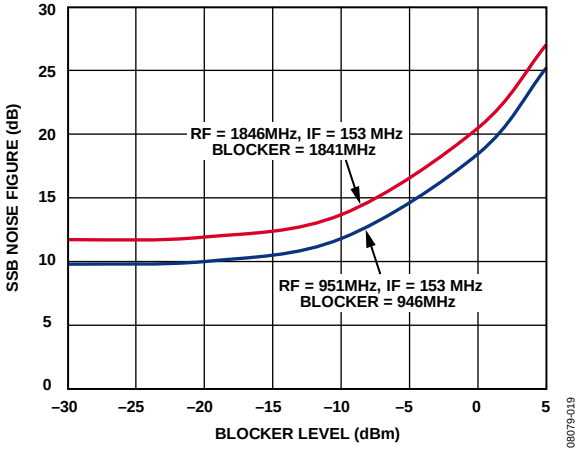

Figure 19. SSB Noise Figure vs. Blocker Level (VSET = 2.0 V)

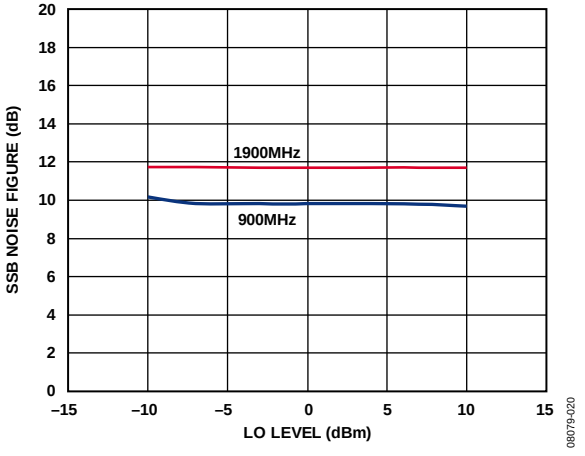

Figure 20. SSB Noise Figure vs. LO Power (VSET = 2.0 V)

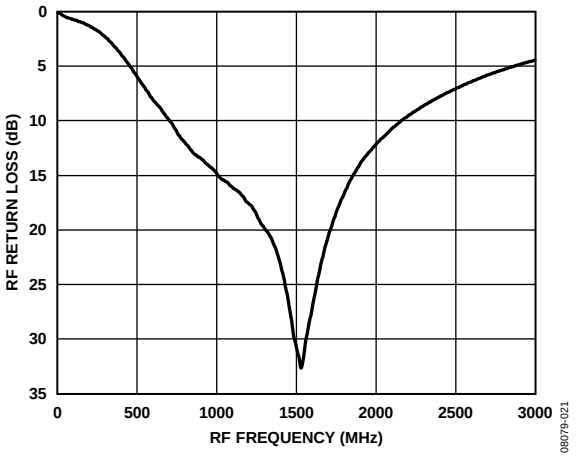

Figure 21. RF Return Loss vs. RF Frequency

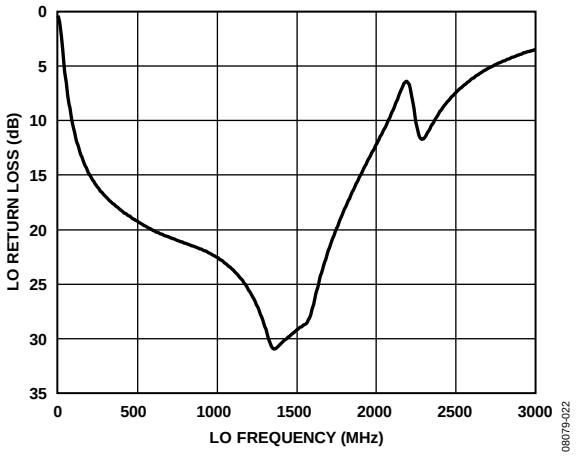

Figure 22. LO Return Loss vs. LO Frequency

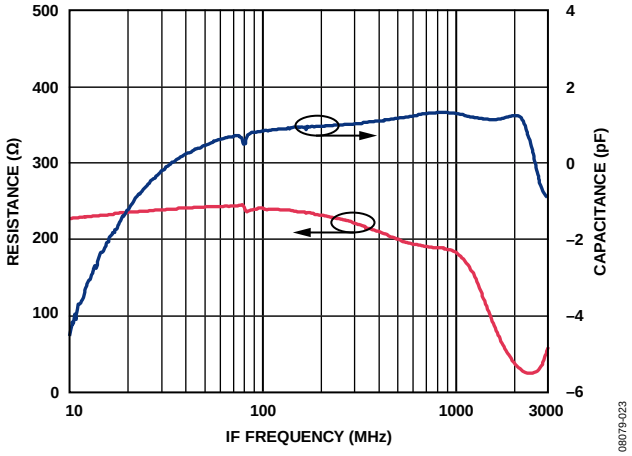

Figure 23. IF Differential Output Impedance (R Parallel C Equivalent)

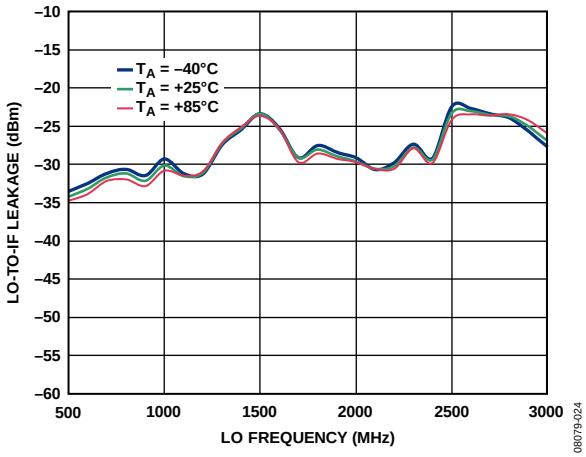

Figure 24. LO-to-IF Leakage vs. LO Frequency

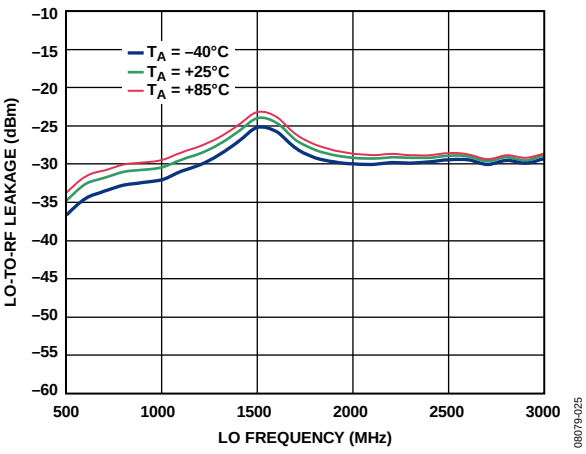

Figure 25. LO-to-RF Leakage vs. LO Frequency

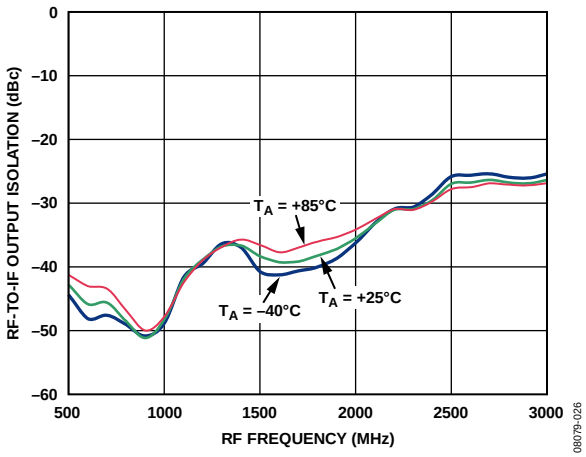

Figure 26. RF-to-IF Leakage vs. RF Frequency

SPUR PERFORMANCE

All spur tables are (N × f_{RF}) − (M × f_{LO}) and were measured using the standard evaluation board (see the Evaluation Board section). Mixer spurious products are measured in decibels relative to the carrier (dBc) from the IF output power level. Data was measured for frequencies less than 6 GHz only. The typical noise floor of the measurement system is −100 dBm.

900 MHz Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 900 MHz, f_{LO} = 703 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
	0		−33.1	−23.3	−45.8	−23.6	−45.9	−30.7	−55.4	−41.5						
	1	−48.8	0.0	−51.5	−19.0	−65.1	−29.6	−78.0	−50.3	−74.4	−57.7					
	2	−35.9	−74.9	−67.5	−66.1	−73.5	−80.5	−65.0	−89.8	−71.3	−88.5	−86.8	−98.8			
	3	−68.8	−64.8	−94.3	−65.9	−86.3	−70.2	−76.3	−70.6	−74.5	−81.4	≤−100	−99.6	≤−100		
	4	−47.5	−80.7	−78.0	−78.4	−95.1	−73.5	−89.4	−87.3	≤−100	−92.7	−99.5	−99.4	≤−100	≤−100	
	5	−95.6	−74.7	−89.8	−70.7	−84.8	−90.7	−86.7	−86.4	−83.1	−73.7	−78.7	−80.7	−91.1	≤−100	≤−100
	6	−85.7	−96.4	−83.1	−98.5	−83.3	−96.7	≤−100	−89.4	−99.6	−96.1	−96.1	−95.4	−95.5	≤−100	≤−100
N	**7**		≤−100	≤−100	−95.9	≤−100	−97.2	−83.1	−84.1	≤−100	≤−100	−99.7	−87.9	−88.8	−85.7	≤−100
	8			≤−100	≤−100	−99.0	−99.8	−86.0	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	9				≤−100	≤−100	≤−100	−90.9	−88.4	−83.5	−87.6	≤−100	≤−100	≤−100	≤−100	≤−100
	10						≤−100	≤−100	≤−100	−97.9	−95.5	−99.0	≤−100	≤−100	≤−100	≤−100
	11							≤−100	≤−100	−92.6	−87.4	−88.2	−92.3	−99.3	≤−100	≤−100
	12								≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	13										≤−100	≤−100	−95.1	−96.5	−90.4	≤−100
	14											≤−100	≤−100	≤−100	≤−100	≤−100
	15												≤−100	≤−100	≤−100	≤−100

1900 MHz Performance

V_S = 5 V, VSET = 3.8 V, T_A = 25°C, RF power = 0 dBm, LO power = 0 dBm, f_{RF} = 1900 MHz, f_{LO} = 1703 MHz, Z_0 = 50 Ω.

		M														
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
	0		−31.4	−17.1	−51.4											
	1	−40.4	0.0	−53.6	−38.5	−71.0										
	2	−38.4	−66.0	−52.9	−68.1	−64.2	−86.8									
	3	≤−100	−66.2	−73.2	−72.6	−79.9	−65.2	−92.8								
	4		≤−100	−89.4	−86.4	−94.6	−87.4	−81.5	≤−100							
	5				−83.7	−66.2	−79.3	−89.0	−75.2	≤−100	≤−100					
	6					≤−100	−86.4	≤−100	−99.0	−87.7	≤−100	≤−100				
N	**7**						≤−100	−92.4	−92.7	≤−100	−98.4	≤−100	≤−100			
	8							≤−100	≤−100	−97.5	≤−100	−95.4	≤−100	≤−100		
	9								≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	≤−100	
	10									≤−100	−97.2	−95.6	≤−100	≤−100	≤−100	≤−100
	11										≤−100	≤−100	≤−100	≤−100	≤−100	≤−100
	12											≤−100	≤−100	≤−100	≤−100	≤−100
	13												≤−100	≤−100	≤−100	≤−100
	14														≤−100	≤−100
	15															≤−100

CIRCUIT DESCRIPTION

The ADL5801 includes a double-balanced active mixer with a 50 Ω input impedance and 250 Ω output impedance. In addition, the ADL5801 integrates a local oscillator (LO) amplifier and an RF power detector that can be used to optimize the mixer dynamic range. The RF and LO are differential, providing maximum usable bandwidth at the input and output ports. The LO also operates with a 50 Ω input impedance and can, optionally, be operated differentially or single ended. The input, output, and LO ports can be operated over an exceptionally wide frequency range. The ADL5801 can be configured as a downconvert mixer or as an upconvert mixer.

The ADL5801 can be divided into the following sections: the LO amplifier and splitter, the RF voltage-to-current (V-to-I) converter, the mixer core, the output loads, the RF detector, and the bias circuit. A simplified block diagram of the device is shown in Figure 27. The LO block generates a pair of differential LO signals to drive two mixer cores. The RF input power is converted into RF currents by the V-to-I converter that then feed into the two-mixer core. The internal differential load of the mixer provides a wideband 250 Ω output impedance from the mixer. Reference currents to each section are generated by the bias circuit, which can be enabled or disabled using the ENBL pin. A detailed description of each section of the ADL5801 follows.

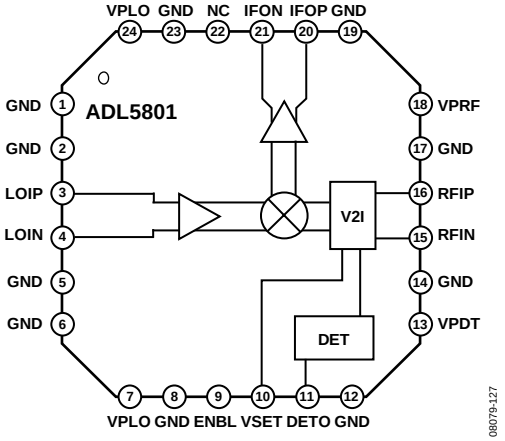

Figure 27. Block Diagram

LO AMPLIFIER AND SPLITTER

The LO input is conditioned by a series of amplifiers to provide a well controlled and limited LO swing to the mixer core, resulting in excellent input IP3. The LO input is amplified using a broadband low noise amplifier (LNA) and is then followed by LO limiting amplifiers. The LNA input impedance is nominally 50 Ω. The LO circuit exhibits low additive noise, resulting in an excellent mixer noise figure and output noise under RF blocking. For optimal performance, the LO inputs should be driven differentially but at lower frequencies; single-ended drive is acceptable.

RF VOLTAGE-TO-CURRENT (V-TO-I) CONVERTER

The differential RF input signal is applied to a V-to-I converter that converts the differential input voltage to output currents. The V-to-I converter provides a 50 Ω input impedance The V-to-I section bias current can be adjusted up or down using the VSET pin. Adjusting the current up improves IP3 and P1dB input but degrades the SSB noise figure. Adjusting the current down improves the SSB noise figure but degrades IP3 and P1dB input. Conversion gain remains nearly constant over a wide range of VSET pin settings, allowing the part to be adjusted dynamically without affecting conversion gain. The current adjustment can be made by connecting a resistor from the VSET pin to the positive supply to increase the bias current or from the VSET pin to ground to decrease the bias current. Optionally, the VSET pin can be connected to the DETO pin to provide automatic setting of the mixer core current.

MIXER CORE

The ADL5801 has a double-balanced mixer that uses high performance SiGe NPN transistors. This mixer is based on the Gilbert cell design of four cross-connected transistors.

MIXER OUTPUT LOAD

The mixer load uses a pair of 125 Ω resistors connected to the positive supply. This provides a 250 Ω differential output resistance. The mixer output should be pulled to the positive supply externally using a pair of RF chokes or using an output transformer with the center tap connected to the positive supply. It is possible to exclude these components when the mixer core current is low, but both P1dB input and IP3 input are then reduced.

The mixer load output can operate from direct current (dc) up to approximately 600 MHz into a 200 Ω load. For upconversion applications, the mixer load can be matched using off-chip matching components. Transmit operation up to 2 GHz is possible. See the Applications Information section for matching circuit details.

RF DETECTOR

An RF power detector is buffered from the V-to-I converter section. This detector has a power response range from approximately −25 dBm up to 0 dBm and provides a current output. The output current is designed to be connected to the VSET pin to boost the mixer core current when large RF signals are present at the mixer input. An external capacitor can be used to adjust the response time of this function. If not used, the DETO pin can be left open or connected to ground.

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by mixers. The bias circuit can be enabled and disabled using the ENBL pin. If the ENBL pin is grounded or left open, the part is enabled. Pulling the ENBL pin high shuts off the bias circuit and disables the part. However, the ENBL pin does not alter the current in the LO section and, therefore, does not provide a true power-down feature. In addition, if the VSET pin is connected to the positive supply through a resistor to increase the mixer core current, this continues to provide bias current to the mixer core unless the resistor supply is also removed.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5801 is designed to translate between radio frequencies (RF) and intermediate frequencies (IF). For both upconversion and downconversion applications, RFIP (Pin 16) and RFIN (Pin 15) must be configured as the input interfaces. IFOP (Pin 20) and IFON (Pin 21) must be configured as the output interfaces. Individual bypass capacitors are needed in close proximity to each supply pin (Pin 7, Pin 13, Pin 18, and Pin 24), the VSET control pin (Pin 10), and the DETO detector output pin (Pin 11). When the on-chip detector is chosen to form a closed loop, automatically controlling the VSET pin, R7 can be populated with a 0 Ω resistor. Alternatively, simply use a jumper between the VSET and DETO test points for evaluation. Figure 28 illustrates the basic connections for ADL5801 operation.

RF AND LO PORTS

The RF and LO input ports are designed for a differential input impedance of approximately 50 Ω. Figure 29 and Figure 30 illustrate the RF and LO interfaces, respectively. It is recommended that each of the RF and LO differential ports be driven through a balun for optimum performance. It is also necessary to ac couple both RF and LO ports. Using proper value capacitors may help improve the input return loss over desired frequencies. Table 4 lists the recommended components for various RF and LO frequency bands. The characterization data is available in the Typical Performance Characteristics section.

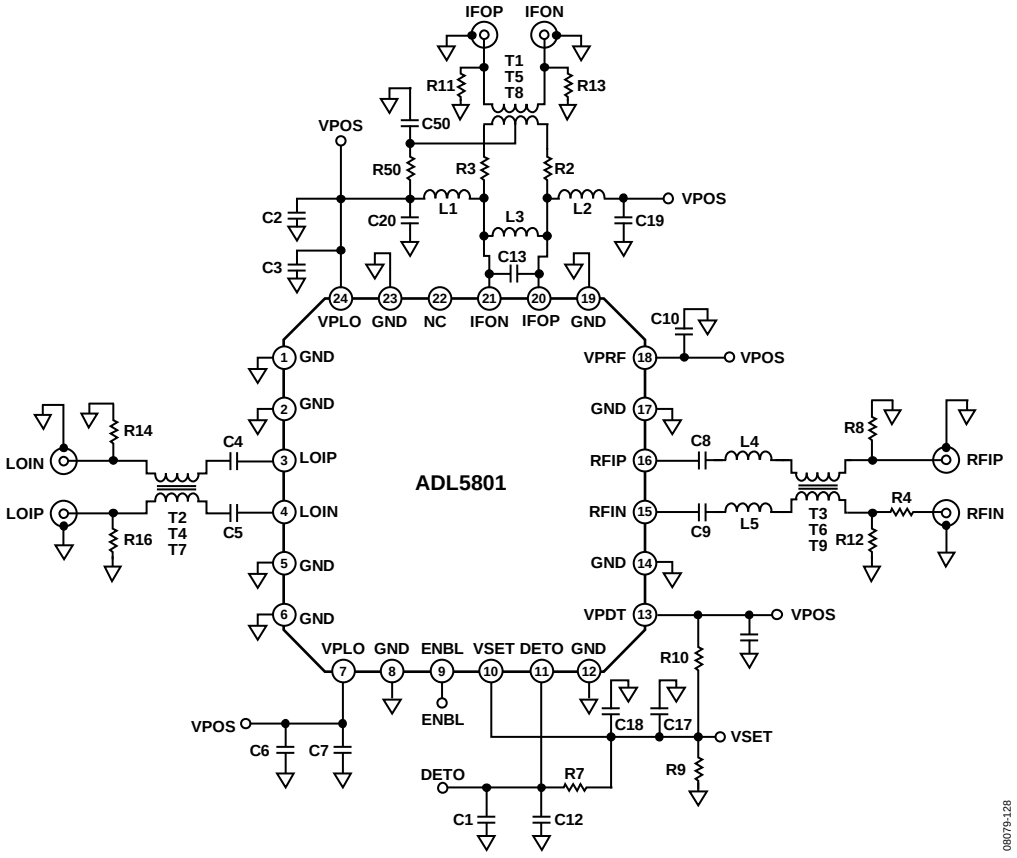

Figure 28. Basic Connections Schematic

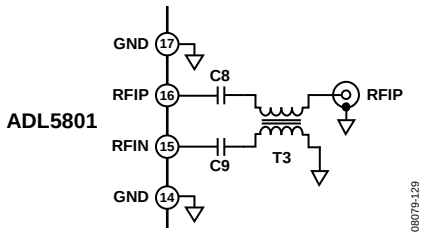

Figure 29. RF Interface

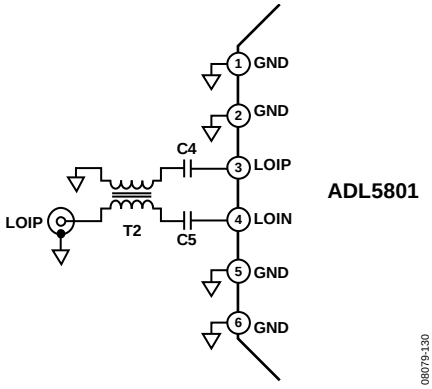

Figure 30. LO Interface

Table 4. Suggested Components for the RF and LO Interfaces

RF and LO Frequency	T1, T3, T5	C8, C9	C4, C5
900 MHz	Mini-Circuits® TC1-1-13M+	5.6 pF	100 pF
1900 MHz	Mini-Circuits TC1-1-13M+	5.6 pF	100 pF
2500 MHz	Mini-Circuits TC1-1-43+	2 pF	8 pF

IF PORT

The IF port features an open-collector, differential output interface. It is necessary to bias the open collector outputs using one of the schemes presented in Figure 31 and Figure 32.

Figure 31 shows the use of center-tapped impedance transformers. The turns ratio of the transformer should be selected to provide the desired impedance transformation. In the case of a 50 Ω load impedance, a 4:1 impedance ratio transformer should be used to transform the 50 Ω load into a 200 Ω differential load at the IF output pins.

Figure 32 shows a differential IF interface where pull-up choke inductors are used to bias the open-collector outputs. The shunting impedance of the choke inductors used to couple dc current into the mixer core should be large enough at the IF frequency of operation not to load down the output current before it reaches the intended load. Additionally, the dc current handling capability of the selected choke inductors must be at least 45 mA.

The self-resonant frequency of the selected choke inductors must be higher than the intended IF frequency. A variety of suitable choke inductors is commercially available from manufacturers such as Coilcraft® and Murata. An impedance transforming network may be required to transform the final load impedance to 200 Ω at the IF outputs.

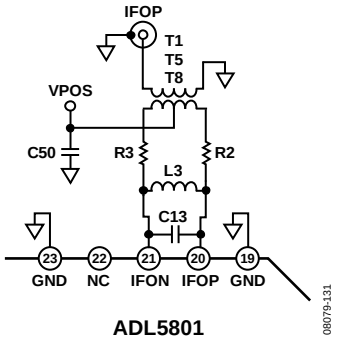

Figure 31. Biasing the IF Port Open-Collector Outputs Using a Center-Tapped Impedance Transformer

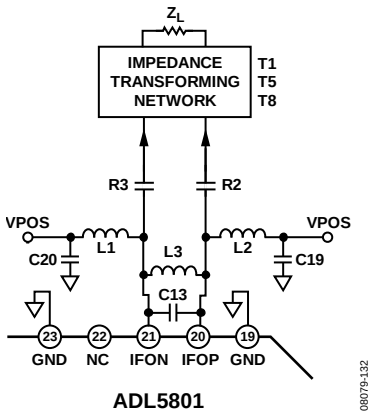

Figure 32. Biasing the IF Port Open-Collector Outputs Using Pull-Up Choke Inductors

EVALUATION BOARD

An evaluation board is available for the ADL5801. The standard evaluation board is fabricated using Rogers® RO3003 material. Each RF, LO, and IF port is configured for single-ended signaling via a balun transformer. The schematic for the evaluation board is shown in Figure 33. Table 5 describes the various configuration options for the evaluation board. Layout for the board is shown in Figure 34 and Figure 35.

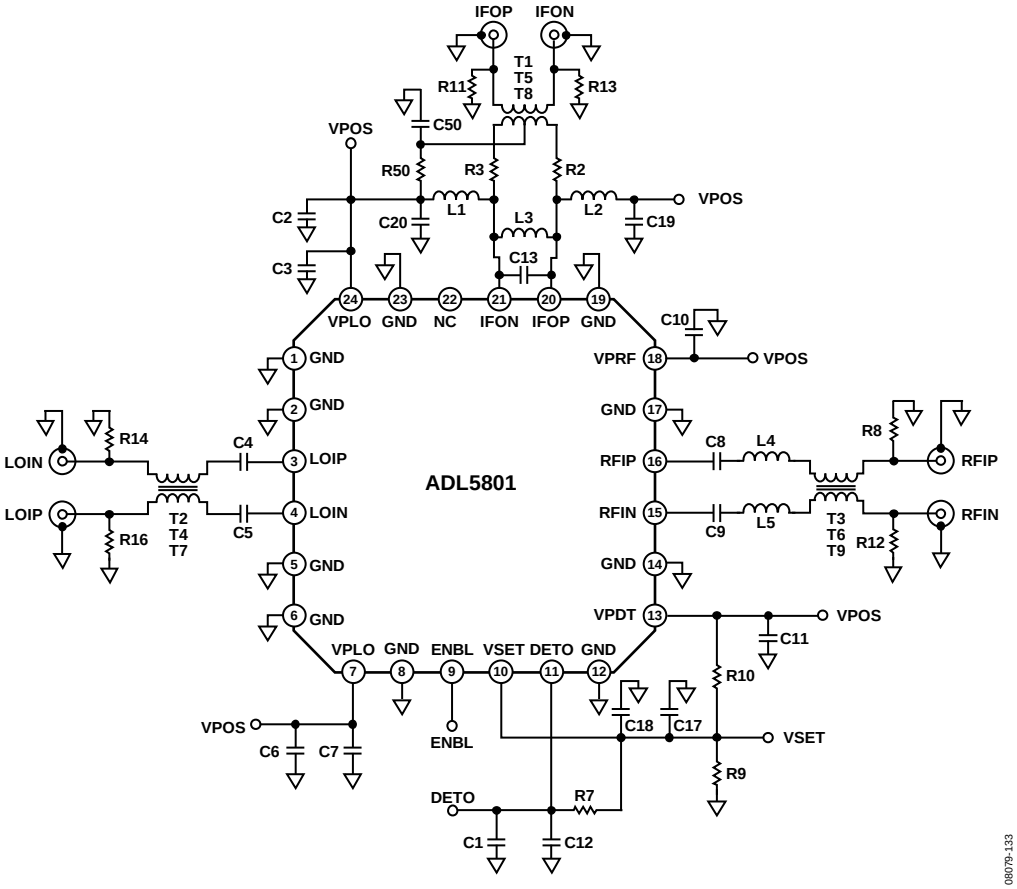

Figure 33. Evaluation Board Schematic

Table 5. Evaluation Board Configuration

Components	Function	Default Conditions
C2, C3, C6, C7, C10, C11	Power supply decoupling. Nominal supply decoupling consists of a 0.1 µF capacitor to ground in parallel with 100 pF capacitors to ground, positioned as close to the device as possible. Series resistors are provided for enhanced supply decoupling using optional ferrite chip inductors.	C2, C6, C10, C11 = 0.1 µF (size 0402) C3, C7 = 100 pF (size 0402)
C8, C9, L4, L5, R4, R8, R12, T3, T6, T9, RFIN, RFIP	RF input interfaces. Input channels are ac-coupled through C8 and C9. R8 and R12 provide options when additional matching is needed. T3 is a 1:1 balun used to interface to the 50 Ω differential inputs. T6 and T9 provide options when high frequency baluns are used and require smaller balun footprints.	C8, C9 = 5.6 pF (size 0402) L4, L5, R12 = 0 Ω (size 0402) R4, R8 = open (size 0402) T3 = TC1-1-13M+ (Mini-Circuits)
C13, C19, C20, C50, L1, L2, L3, R2, R3, R11, R13, R50, T1, T5, T8, IFON, IFOP	IF output interfaces. The 200 Ω open collector IF output interfaces are biased through the center tap of a 4:1 impedance transformer at T1. C50 provides local bypassing with R50 available for additional supply bypassing. L1 and L2 provide options when pull-up choke inductors are used to bias the open-collector outputs. C13, L3, R2, and R3 are provided for IF filtering and matching options. T5 and T8 provide options when high frequency baluns are used and require smaller balun footprints.	C13 = open (size 0402) C19, C20 = 100 pF (size 0402) C50 = 0.1 µF (size 0402) L1, L2 = open (size 0805) L3 = open (size 0402) R2, R3, R13, R50 = 0 Ω (size 0402) R11 = open (size 0402) T1 = TC4-1W+ (Mini-Circuits)
C4, C5, R14, R16, T2, T4, T7, LOIN, LOIP	LO interface. C4 and C5 provide ac coupling for the local oscillator input. T2 is a 1:1 balun that allows single-ended interfacing to the differential 50 Ω local oscillator input. T4 and T7 provide options when high frequency baluns are used and require smaller balun footprints.	C4, C5 = 100 pF (size 0402) R14 = 0 Ω (size 0402) R16 = open (size 0402) T2 = TC1-1-13M+ (Mini-Circuits)
C1, C12, R7, DETO	DETO interface. C1 and C12 provide decoupling for the DETO pin. R7 provides access to the VSET pin when automatic input IP3 control is needed.	C1 = 0.1 µF (size 0603) C12 = 100 pF (size 0402) R7 = open (size 0402)
C17, C18, R9, R10, VSET	VSET bias control. C17 and C18 provide decoupling for the VSET pin. R9 and R10 form an optional resistor divider network between VPOS and GND, allowing for a fixed bias setting. Supply 3.8 V at the VSET pin when the DETO pin is not connected for automatic input IP3 control.	C17 = 100 pF (size 0402) C18 = 0.1 µF (size 0603) R9, R10 = open (size 0402)

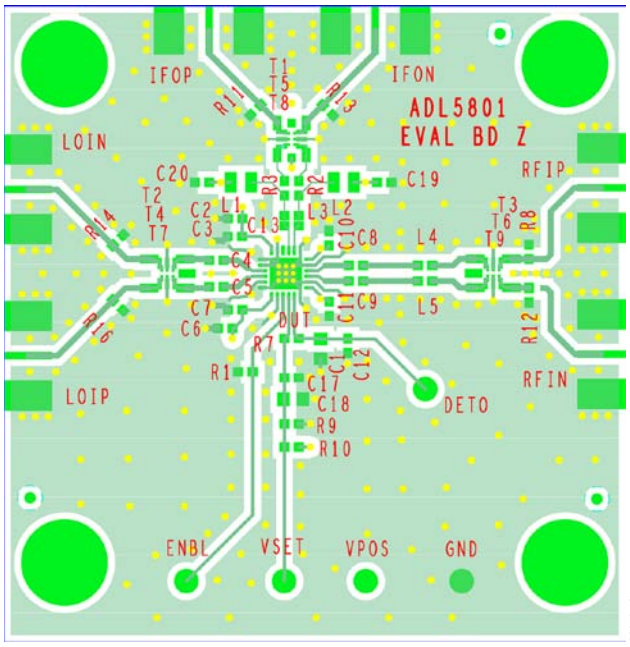

Figure 34. Evaluation Board Top Layer

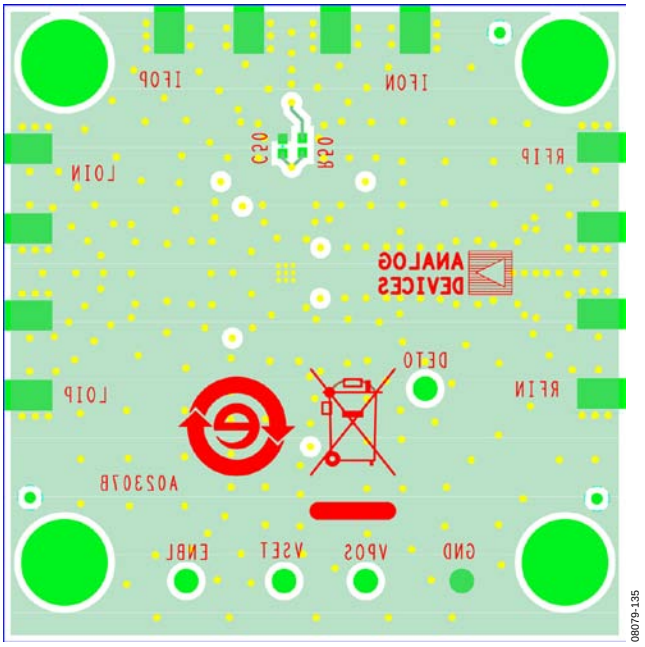

Figure 35. Evaluation Board Bottom Layer

OUTLINE DIMENSIONS

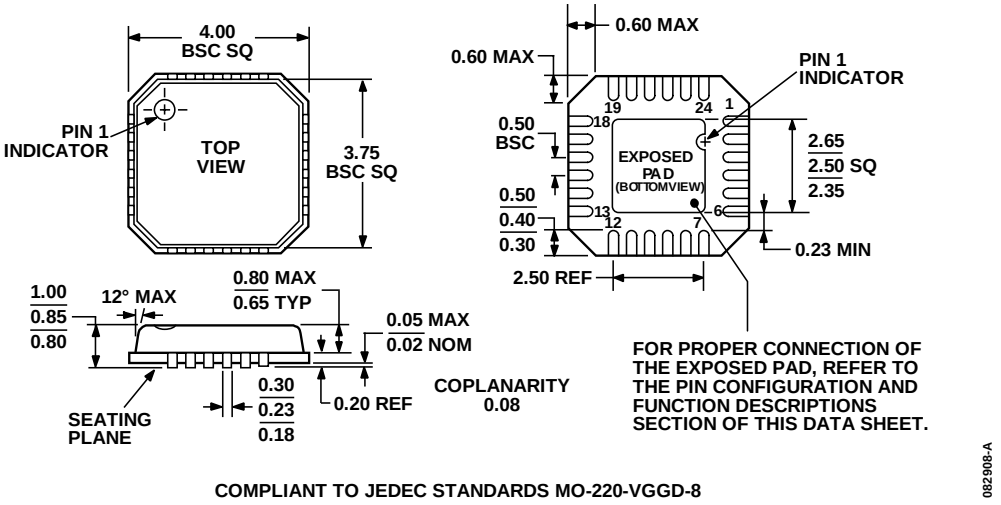

Figure 36. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5801ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-24-3	1,500 per Reel
ADL5801-EVALZ		Evaluation Board		1

[1] Z = RoHS Complaint Part.

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