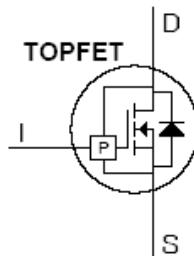
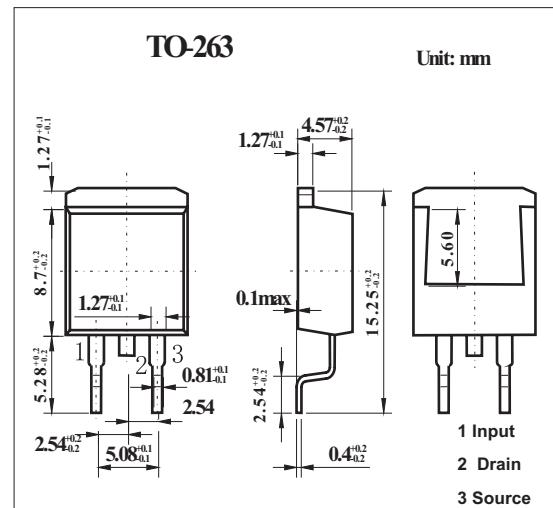


Logic level TOPFET

KUK129-50DL

■ Features

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads



■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	Rating	Unit
Continuous drain source voltage ¹	V _{DS}	50	V
Continuous drain current V _{DS} = 5 V; T _{mb} = 25°C	I _D	selflimited	A
Continuous drain current V _{DS} = 5 V; T _{mb} ≤ 125°C	I _D	16	A
Continuous input current	I _I	-5 to 5	mA
Repetitive peak input current t _p ≤ 1 ms	I _{IRRM}	-10 to 10	mA
Total power dissipation T _{mb} ≤ 25°C	P _D	65	W
Storage temperature	T _{stg}	-55 To 175	°C
Continuous junction temperature ² normal operation	T _j	150	°C
Case temperature during soldering	T _{sold}	260	°C
Electrostatic discharge capacitor voltage *2	V _C	2	kV

*1 δ ≤ 0.1, t_p = 300 μs

*2 C = 250 pF; R = 1.5 kΩ

KUK129-50DL■ Electrical Characteristics $T_a = 25^\circ\text{C}$

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit	
Non-repetitive clamping energy	E_{DSM}	$I_{DM} = 16 \text{ A}; V_{DD} \leq 20 \text{ V}; T_{mb} \leq 25^\circ\text{C}$			200	μJ	
Repetitive clamping energy	E_{DRM}	$I_{DM} = 16 \text{ A}; V_{DD} \leq 20 \text{ V}; T_{mb} \leq 95^\circ\text{C}; f = 250 \text{ Hz}$			32	μJ	
Drain source voltage	V_{DS}	$4 \text{ V} \leq V_{DS} \leq 5.5 \text{ V}$	0		35	V	
Drain-source clamping voltage	$V_{(CL)DSS}$	$V_{DS} = 0 \text{ V}; I_D = 10 \text{ mA}$	50			V	
		$V_{DS} = 0 \text{ V}; I_{DM} = 2 \text{ A}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01$	50	60	70	V	
Drain source leakage current	I_{DSS}	$V_{DS} = 40 \text{ V}$			100	μA	
		$V_{DS} = 40 \text{ V}; T_{mb} = 25^\circ\text{C}$		0.1	10	μA	
Drain-source resistance	$R_{DS(ON)}$	$V_{DS} \geq 4.4 \text{ V}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; I_{DM} = 6 \text{ A}$			95	$\text{m}\Omega$	
		$V_{DS} \geq 4.4 \text{ V}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; I_{DM} = 6 \text{ A}; T_{mb} = 25^\circ\text{C}$		36	50	$\text{m}\Omega$	
		$V_{DS} \geq 4 \text{ V}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; I_{DM} = 6 \text{ A}$			100	$\text{m}\Omega$	
		$V_{DS} \geq 4 \text{ V}; t_p \leq 300 \mu\text{s}; \delta \leq 0.01; I_{DM} = 6 \text{ A}; T_{mb} = 25^\circ\text{C}$		39	55	$\text{m}\Omega$	
Drain current limiting	I_D	$V_{DS} = 13 \text{ V}; V_{IS} = 5 \text{ V}; T_{mb} = 25^\circ\text{C}$	16	24	32	A	
		$V_{DS} = 13 \text{ V}; 4.4 \text{ V} \leq V_{IS} \leq 5.5 \text{ V}$	12		36	A	
		$V_{DS} = 13 \text{ V}; 4 \text{ V} \leq V_{IS} \leq 5.5 \text{ V}$	8		36	A	
Overload power threshold	$P_{D(TO)}$	device trips if $P_D > P_{D(TO)}$; $V_{IS} = 5 \text{ V}; T_{mb} = 25^\circ\text{C}$	40	120	160	W	
Characteristic time	T_{DSC}		200	350	600	μs	
Threshold junction temperature	$T_{J(TO)}$		150	170		$^\circ\text{C}$	
Input threshold voltage	$V_{IS(TO)}$	$V_{DS} = 5 \text{ V}; I_D = 1 \text{ mA}$	0.6		2.4	V	
		$V_{DS} = 5 \text{ V}; I_D = 1 \text{ mA}; T_{mb} = 25^\circ\text{C}$	1.1	1.6	2.1	V	
Input supply current	I_{IS}	normal operation; $V_{IS} = 5 \text{ V}$	100	220	400	μA	
		normal operation; $V_{IS} = 4 \text{ V}$	80	195	330		
Input supply current	I_{ISL}	protection latched; $V_{IS} = 5 \text{ V}$	200	400	650		
		protection latched; $V_{IS} = 3 \text{ V}$	130	250	430		
Protection reset voltage	V_{ISR}	reset time $t_r \geq 100 \mu\text{s}$	1.5	2	2.9	V	
Latch reset time	t_{lR}	$V_{IS1} = 5 \text{ V}, V_{IS2} < 1 \text{ V}$	10	40	100	μs	
Input clamping voltage	$V_{(CL)IS}$	$I_I = 1.5 \text{ mA}$	5.5		8.5	V	
Input series resistance to gate of power MOSFET	R_{IG}	$I_I = 1.5 \text{ mA}; T_{mb} = 25^\circ\text{C}$			33	$\text{k}\Omega$	
Turn-on delay time	$t_{d(on)}$	$V_{IS} = 5 \text{ V}$			15	30	
Rise time	t_r				30	60	
Turn-off delay time	$t_{d(off)}$	$V_{IS} = 0 \text{ V}$			70	140	
Fall time	t_f				35	70	
Junction to mounting base	$R_{th j-mb}$				1.75	1.92	K/W
Junction to ambient	$R_{th j-a}$	minimum footprint FR4 PCB			50		K/W