Power MOSFET -10 Amps, -20 Volts

P-Channel SOT-223

Features

- Low R_{DS(on)}
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- Pb-Free Package is Available

Typical Applications

• Power Management in Portables and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	-20	Vdc
Gate-to-Source Voltage	V _{GS}	±8.0	Vdc
Drain Current (Note 1) - Continuous @ $T_A = 25^{\circ}C$ - Continuous @ $T_A = 70^{\circ}C$ - Single Pulse ($t_p = 10 \mu s$)	I _D I _D I _{DM}	-10 -8.4 -35	Adc Apk
Total Power Dissipation @ T _A = 25°C	P _D	8.3	W
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^{\circ}\text{C}$ ($V_{DD} = -20 \text{ Vdc}, V_{GS} = -5.0 \text{ Vdc}, I_{L(pk)} = -10 \text{ A}, L = 3.0 \text{ mH}, R_G = 25\Omega$)	E _{AS}	150	mJ
Thermal Resistance - Junction to Lead (Note 1) - Junction to Ambient (Note 2) - Junction to Ambient (Note 3)	$egin{array}{c} R_{ heta JL} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	15 71.4 160	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Steady State.
- When surface mounted to an FR4 board using 1" pad size, (Cu. Area 1.127 sq in), Steady State.
- 3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu. Area 0.412 sq in), Steady State.

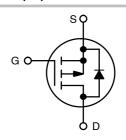


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-10 AMPERES -20 VOLTS

 $R_{DS(on)} = 44 \text{ m}\Omega \text{ (Typ.)}$

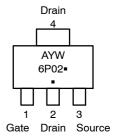


P-Channel MOSFET

MARKING DIAGRAM & PIN ASSIGNMENT



SOT-223 CASE 318E STYLE 3



A = Assembly Location

Y = Year

W = Work Week

6P02 = Specific Device Code

= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

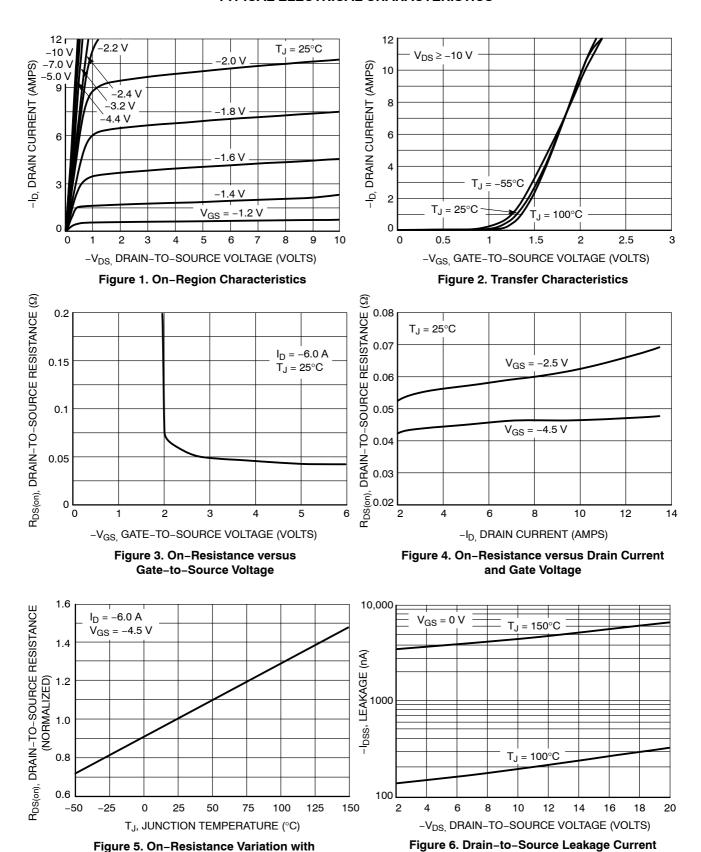
Device	Package	Shipping [†]
NTF6P02T3	SOT-223	4000/Tape & Reel
NTF6P02T3G	SOT-223 (Pb-Free)	4000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTI					I	
Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
$\begin{aligned} & \text{Drain-to-Source Breakdown Voltage} \\ & (\text{V}_{GS} = 0 \text{ Vdc, I}_D = -250 \mu\text{Adc}) \\ & \text{Temperature Coefficient (Positive)} \end{aligned}$	V _{(BR)DSS}	-20 -	-25 -11	- -	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)			_ _	_ _	-1.0 -10	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 8.0 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)			-	-	± 100	nAdc
ON CHARACTERISTICS (Note 4)					I.	I.
Gate Threshold Voltage (Note 4) $(V_{DS} = V_{GS}, I_D = -250 \mu\text{Adc})$ Threshold Temperature Coefficient (Negative)			-0.4 -	-0.7 2.6	-1.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 4) $ \begin{array}{l} (V_{GS}=-4.5~\text{Vdc},I_D=-6.0~\text{Adc})\\ (V_{GS}=-2.5~\text{Vdc},I_D=-4.0~\text{Adc})\\ (V_{GS}=-2.5~\text{Vdc},I_D=-3.0~\text{Adc}) \end{array} $			- - -	44 57 57	50 70 -	mΩ
Forward Transconductance (Note 4) $(V_{DS} = -10 \text{ Vdc}, I_D = -6.0 \text{ Adc})$	9 _{fs}	-	12	-	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	$(V_{DS} = -16 \text{ Vdc}, V_{GS} = 0 \text{ V},$	C _{iss}	-	900	1200	pF
Output Capacitance	f = 1.0 MHz)	C _{oss}	_	350	500	
Transfer Capacitance		C _{rss}	_	90	150	
Input Capacitance	$(V_{DS} = -10 \text{ Vdc}, V_{GS} = 0 \text{ V},$	C _{iss}	-	940	-	pF
Output Capacitance	f = 1.0 MHz)	C _{oss}	-	410	-	
Transfer Capacitance		C _{rss}	_	110	-	
SWITCHING CHARACTERISTIC	S (Note 5)					
Turn-On Delay Time	$(V_{DD} = -5.0 \text{ Vdc}, I_D = -1.0 \text{ Adc},$	t _{d(on)}	-	7.0	12	ns
Rise Time	$V_{GS} = -4.5 \text{ Vdc},$ $R_{G} = 6.0 \Omega)$	t _r	-	25	45	
Turn-Off Delay Time	, 	t _{d(off)}	-	75	125	
Fall Time		t _f	_	50	85	
Turn-On Delay Time	$(V_{DD} = -16 \text{ Vdc}, I_D = -6.0 \text{ Adc},$	t _{d(on)}	-	8.0	-	ns
Rise Time	$V_{GS} = -4.5 \text{ Vdc},$ $R_G = 2.5 \Omega)$	t _r	-	30	-	-
Turn-Off Delay Time		t _{d(off)}	-	60	-	
Fall Time		t _f	_	60	_	
Gate Charge	$(V_{DS} = -16 \text{ Vdc}, I_D = -6.0 \text{ Adc}, V_{GS} = -4.5 \text{ Vdc}) \text{ (Note 4)}$	Q _T	-	15	20	nC
	VGS = -4.5 Vdc) (Note 4)	Q _{gs}	-	1.7	_	
		Q_{gd}	-	6.0	_	
SOURCE-DRAIN DIODE CHARA	ACTERISTICS					
Forward On-Voltage	$ \begin{array}{c} (I_S = -3.0 \; \text{Adc, V}_{GS} = 0 \; \text{Vdc}) \; (\text{Note 4}) \\ (I_S = -2.1 \; \text{Adc, V}_{GS} = 0 \; \text{Vdc}) \\ (I_S = -3.0 \; \text{Adc, V}_{GS} = 0 \; \text{Vdc, T}_J = 125^{\circ}\text{C}) \end{array} $	V _{SD}	- - -	-0.82 -0.74 -0.68	-1.2 - -	Vdc
Reverse Recovery Time	$(I_S=-3.0$ Adc, $V_{GS}=0$ Vdc, $dI_S/dt=100$ A/ $\mu s)$ (Note 4)	t _{rr}	-	42	_	ns
		t _a	-	17	-	1
		t _b	-	25	-	
Reverse Recovery Stored Charge	Q _{RR}	-	0.036	-	μC	

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS



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versus Voltage

Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

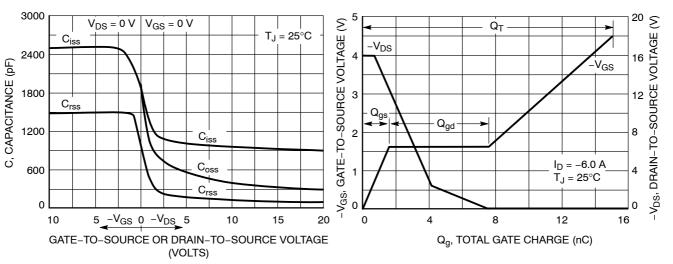


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

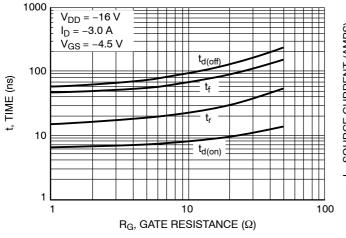


Figure 9. Resistive Switching Time Variation versus Gate Resistance

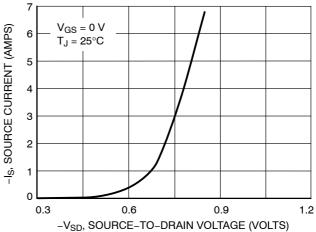


Figure 10. Diode Forward Voltage versus Current

TYPICAL ELECTRICAL CHARACTERISTICS

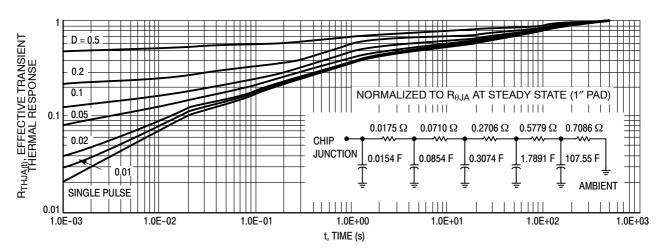
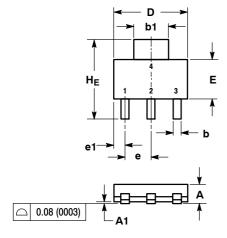
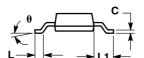


Figure 11. FET Thermal Response

PACKAGE DIMENSIONS

SOT-223 (TO-261) CASE 318E-04 ISSUE N





NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994
- CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
С	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
е	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20			0.008		
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	_	10°	0°	_	10°

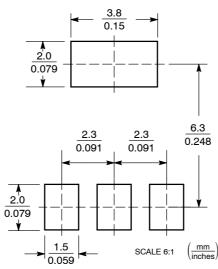
STYLE 3:

PIN 1. GATE

2. DRAIN 3. SOURCE

SOURCE 4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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