SAA7104E; SAA7105E

Digital video encoder

Rev. 02 — 23 December 2005 Product data sheet

1. General description

The SAA7104E; SAA7105E is an advanced next-generation video encoder which converts PC graphics data at maximum 1280 × 1024 resolution (optionally 1920 × 1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 1280 × 1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively this port can provide Y, P_B and P_R signals for HDTV monitors.

The device includes a sync/clock generator and on-chip DACs.

All inputs intended to interface to the host graphics controller are designed for low-voltage signals between down to 1.1 V and up to 3.6 V.

2. Features

- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- Supports Intel Digital Video Out (DVO) low voltage interfacing to graphics controller
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 85 MHz at double edged clocking, synthesized on-chip or from external source
- Programmable assignment of clock edge to bytes (in double edged mode)
- Synthesizable pixel clock (PIXCLK) with minimized output jitter, can be used as reference clock for the VGC, as well
- PIXCLK output and bi-phase PIXCLK input (VGC clock loop-through possible)
- Hot-plug detection through dedicated interrupt pin
- Supported VGA resolutions for PAL or NTSC legacy video output up to 1280 × 1024 graphics data at 60 Hz or 50 Hz frame rate
- Supported VGA resolutions for HDTV output up to 1920 × 1080 interlaced graphics data at 60 Hz or 50 Hz frame rate
- Three Digital-to-Analog Converters (DACs) at 27 MHz sample rate for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) (signals in parenthesis are optional); all at 10-bit resolution
- Non-Interlaced (NI) C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling

- Downscaling and upscaling from 50 % to 400 %
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disc (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode with maximum 85 MHz)
- 3 bytes × 256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- HDTV up to 1920 × 1080 interlaced and 1280 × 720 progressive, including 3-level sync pulses
- Programmable border color of underscan area
- Programmable 5 line anti-flicker filter
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)
- Encoder can be master or slave
- Adjustable output levels for the DACs
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Color Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion
- Macrovision Pay-per-View copy protection system rev. 7.01, rev. 6.1 and rev. 1.03 (525p) as option; this applies to the SAA7104E only
- Optional cross-color reduction for PAL and NTSC CVBS outputs
- Power-save modes
- Joint Test Action Group (JTAG) Boundary Scan Test (BST)
- Monolithic CMOS 3.3 V device, 5 V tolerant I/Os

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD}	digital supply voltage		3.15	3.3	3.45	V
I_{DDA}	analog supply current		1	110	115	mA
I_{DDD}	digital supply current		1	175	200	mA
V_i	input signal voltage levels		TTL compatible			
$V_{o(p-p)}$	analog CVBS output signal voltage for a 100/100 color bar at 75/2 Ω load (peak-to-peak value)		-	1.23	-	V
R_L	load resistance		-	37.5	-	Ω
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs		-	-	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs		-	-	±1	LSB
T_{amb}	ambient temperature		0	-	70	°C

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
SAA7104E	LBGA156	plastic low profile ball grid array package; 156 balls; body 15 × 15 × 1.05 mm	SOT700-1
SAA7105E			

5. Block diagram

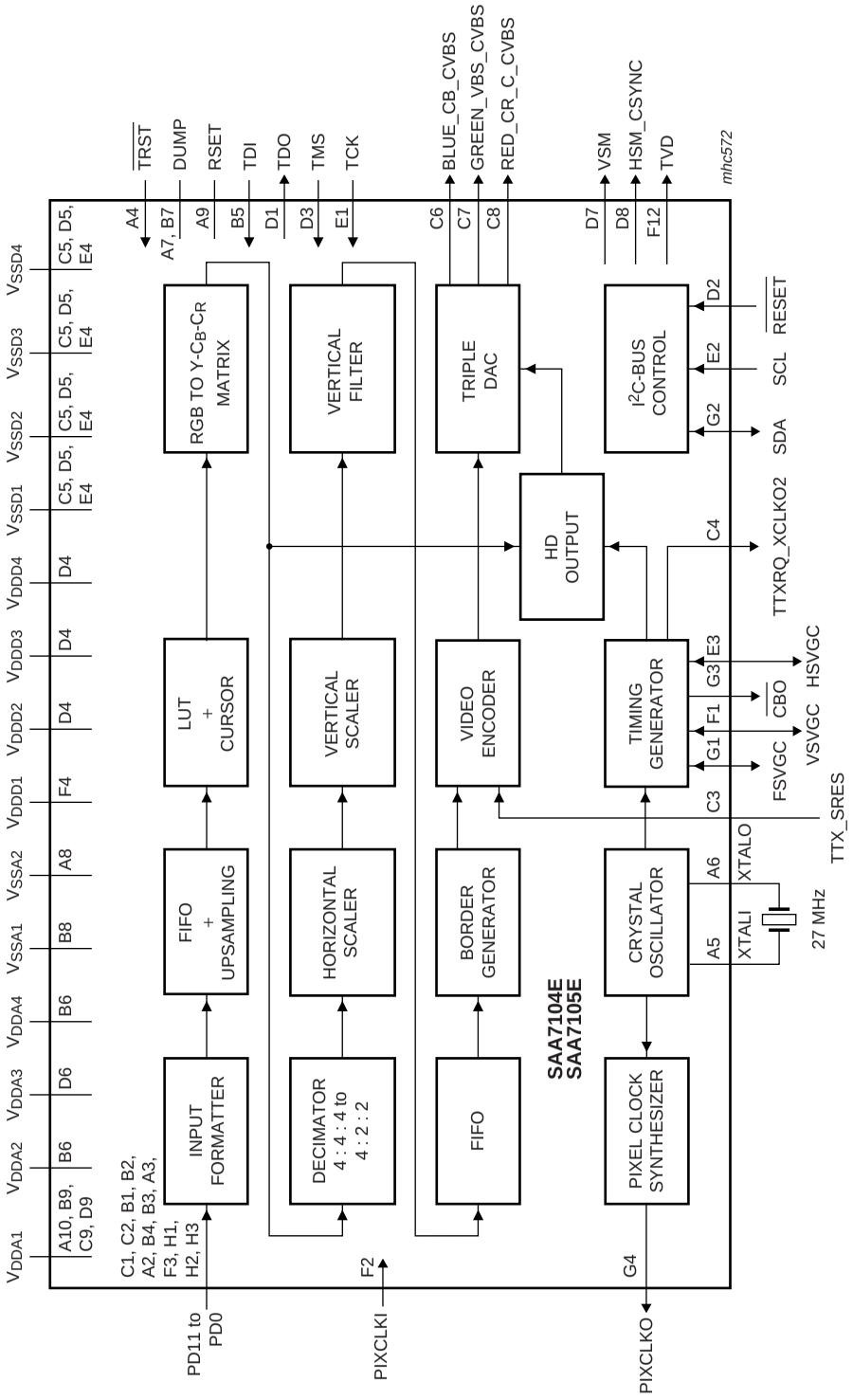


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

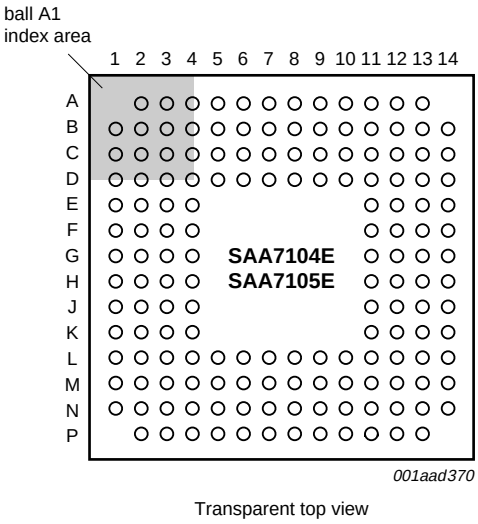


Fig 2. Pin configuration

Table 3: Pin allocation table

Pin	Symbol	Pin	Symbol
A2	PD7	A3	PD4
A4	$\overline{TRST}$	A5	XTALI
A6	XTALO	A7	DUMP
A8	V_{SSA2}	A9	RSET
A10	V_{DDA1}	B1	PD9
B2	PD8	B3	PD5
B4	PD6	B5	TDI
B6	V_{DDA2}, V_{DDA4}	B7	DUMP
B8	V_{SSA1}	B9	V_{DDA1}
C1	PD11	C2	PD10
C3	TTX_SRES	C4	TTXRQ_XCLKO2
C5	V_{SSD1}, V_{SSD2}, V_{SSD3}, V_{SSD4}	C6	BLUE_CB_CVBS
C7	GREEN_VBS_CVBS	C8	RED_CR_C_CVBS
C9	V_{DDA1}	D1	TDO
D2	$\overline{RESET}$	D3	TMS
D4	V_{DDD2}, V_{DDD3}, V_{DDD4}	D5	V_{SSD1}, V_{SSD2}, V_{SSD3}, V_{SSD4}
D6	V_{DDA3}	D7	VSM
D8	HSM_CSYNC	D9	V_{DDA1}
E1	TCK	E2	SCL
E3	HSVGC	E4	V_{SSD1}, V_{SSD2}, V_{SSD3}, V_{SSD4}

Table 3: Pin allocation table...*continued*

Pin	Symbol	Pin	Symbol
E12	reserved	F1	VSVGC
F2	PIXCLKI	F3	PD3
F4	V_{DDD1}	F12	TVD
G1	FSVGC	G2	SDA
G3	$\overline{CBO}$	G4	PIXCLKO
H1	PD2	H2	PD1
H3	PD0		

6.2 Pin description

Table 4: Pin description

Symbol	Pin	Type [1]	Description
PD7	A2	I	pixel data 7 [2]; MSB with C_B-Y-C_R 4 : 2 : 2
PD4	A3	I	pixel data 4 [2]; MSB – 3 with C_B-Y-C_R 4 : 2 : 2
$\overline{TRST}$	A4	I/pu	test reset input for BST; active LOW [3], [4] and [5]
XTALI	A5	I	crystal oscillator input
XTALO	A6	O	crystal oscillator output
DUMP	A7, B7	O	DAC reference pin; connected via 12 Ω resistor to analog ground
V_{SSA2}	A8	S	analog ground 2
RSET	A9	O	DAC reference pin; connected via 1 kΩ resistor to analog ground (do not use capacitor in parallel with 1 kΩ resistor)
V_{DDA1}	A10, B9, C9, D9	S	analog supply voltage 1 (3.3 V for DACs)
PD9	B1	I	pixel data 9 [2]
PD8	B2	I	pixel data 8 [2]
PD5	B3	I	pixel data 5 [2]; MSB – 2 with C_B-Y-C_R 4 : 2 : 2
PD6	B4	I	pixel data 6 [2]; MSB – 1 with C_B-Y-C_R 4 : 2 : 2
TDI	B5	I	test data input for BST [3]
V_{DDA2}	B6	S	analog supply voltage 2 (3.3 V for DACs)
V_{DDA4}	B6	S	analog supply voltage 4 (3.3 V)
V_{SSA1}	B8	S	analog ground 1
PD11	C1	I	pixel data 11 [2]
PD10	C2	I	pixel data 10 [2]
TTX_SRES	C3	I	teletext input or sync reset input
TTXRQ_XCLKO2	C4	O	teletext request output or 13.5 MHz clock output of the crystal oscillator [6]
V_{SSD1}	C5, D5, E4	S	digital ground 1
V_{SSD2}	C5, D5, E4	S	digital ground 2
V_{SSD3}	C5, D5, E4	S	digital ground 3
V_{SSD4}	C5, D5, E4	S	digital ground 4
BLUE_CB_CVBS	C6	O	analog output of BLUE or C_B or CVBS signal

Table 4: Pin description *…continued*

Symbol	Pin	Type [1]	Description
GREEN_VBS_CVBS	C7	O	analog output of GREEN or VBS or CVBS signal
RED_CR_C_CVBS	C8	O	analog output of RED or C_R or C or CVBS signal
TDO	D1	O	test data output for BST [3]
$\overline{\text{RESET}}$	D2	I	reset input; active LOW
TMS	D3	I/pu	test mode select input for BST [3]
V_{DDD2}	D4	S	digital supply voltage 2 (3.3 V for I/Os)
V_{DDD3}	D4	S	digital supply voltage 3 (3.3 V for core)
V_{DDD4}	D4	S	digital supply voltage 4 (3.3 V for core)
V_{DDA3}	D6	S	analog supply voltage 3 (3.3 V for oscillator)
VSM	D7	O	vertical synchronization output to monitor (non-interlaced auxiliary RGB)
HSM_CSYNC	D8	O	horizontal synchronization output to monitor (non-interlaced auxiliary RGB) or composite sync for RGB-SCART
TCK	E1	I/pu	test clock input for BST [3]
SCL	E2	I(/O)	serial clock input (I^2C-bus) with inactive output path
HSVGC	E3	I/O	horizontal synchronization output to VGC (optional input) [6]
reserved	E12	-	to be reserved for future applications
VSVGC	F1	I/O	vertical synchronization output to VGC (optional input) [6]
PIXCLKI	F2	I	pixel clock input (looped through)
PD3	F3	I	pixel data 3 [2]; MSB – 4 with C_B-Y-C_R 4 : 2 : 2
V_{DDD1}	F4	S	digital supply voltage 1 for pins PD11 to PD0, PIXCLKI, PIXCLKO, FSVGC, VSVGC, HSVGC, $\overline{\text{CBO}}$ and TVD
TVD	F12	O	interrupt if TV is detected at DAC output
FSVGC	G1	I/O	frame synchronization output to Video Graphics Controller (VGC) (optional input) [6]
SDA	G2	I/O	serial data input/output (I^2C-bus)
$\overline{\text{CBO}}$	G3	I/O	composite blanking output to VGC; active LOW [6]
PIXCLKO	G4	O	pixel clock output to VGC
PD2	H1	I	pixel data 2 [2]; MSB – 5 with C_B-Y-C_R 4 : 2 : 2
PD1	H2	I	pixel data 1 [2]; MSB – 6 with C_B-Y-C_R 4 : 2 : 2
PD0	H3	I	pixel data 0 [2]; MSB – 7 with C_B-Y-C_R 4 : 2 : 2

[1] Pin type: I = input, O = output, S = supply, pu = pull-up.

[2] See Table 12 to Table 18 for pin assignment.

[3] In accordance with the *'IEEE1149.1'* standard the pins TDI, TMS, TCK and $\overline{\text{TRST}}$ are input pins with an internal pull-up resistor and TDO is a 3-state output pin.

[4] For board design without boundary scan implementation connect $\overline{\text{TRST}}$ to ground.

[5] This pin provides easy initialization of the BST circuit. $\overline{\text{TRST}}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

[6] Pins FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTXRQ_XCLKO2 are used for bootstrapping; see Section 7.1.

7. Functional description

The digital video encoder encodes digital luminance and color difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7104E; SAA7105E can be directly connected to a PC video graphics controller with a maximum resolution of 1280×1024 (progressive) or 1920×1080 (interlaced) at a 50 Hz or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Table 12 to Table 18.

A complete 3 bytes $\times$ 256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port Pixel Data (PD) or via the I^2C-bus.

The SAA7104E; SAA7105E supports a 32-bit $\times$ 32-bit $\times$ 2-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^2C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7104E; SAA7105E can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, color modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/color difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *'RS-170-A'* and *'ITU-R BT.470-3'*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figure 6 to Figure 11. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *'ITU-R BT.656'* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in Slave mode. For assignment of the input data to the rising or falling clock edge see Table 12 to Table 18.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7104E; SAA7105E synthesizes all necessary internal signals, color subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I^2C-bus.

The IC also contains closed caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Figure 15). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Color subcarrier frequency
- Variable burst amplitude etc.

7.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset ($\overline{\text{RESET}}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I^2C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I^2C-bus access redefines the corresponding registers; see Table 5.

Table 5: Strapping pins

Pin	Tied	Preset
FSVGC	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{\text{CBO}}$	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal color bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

7.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I^{2}C-bus control bits SLOT and EDGE for correct operation.

If Y-C_B-C_R is being applied as a 27 MB/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

The horizontal upscaling is supported via the input formatter. According to the programming of the pixel clock dividers (see Section 7.10), it will sample up the data stream to 1 $\times$, 2 $\times$ or 4 $\times$ the input data rate. An optional interpolation filter is available. The clock domain transition is handled by a 4 entries wide FIFO which gets initialized every field or explicitly at request. A bypass for the FIFO is available, especially for high input data rates.

7.3 RGB LUT

The three 256 byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed color data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I^{2}C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 bytes $\times$ 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

7.4 Cursor insertion

A 32 dots $\times$ 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I^{2}C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I^{2}C-bus register as described in Table 8. Transparent means that the input pixels are passed through, the ‘cursor colors’ can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 6: Layout of a byte in the cursor bit map

7	6	5	4	3	2	1	0
pixel n + 3		pixel n + 2		pixel n + 1		pixel n	
D1	D0	D1	D0	D1	D0	D1	D0

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the 'hot spot', the other register controls the insertion position. The hot spot is the 'tip' of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 7: Cursor bit map

Byte	7	6	5	4	3	2	1	0
0	row 0 column 3		row 0 column 2		row 0 column 1		row 0 column 0	
1	row 0 column 7		row 0 column 6		row 0 column 5		row 0 column 4	
2	row 0 column 11		row 0 column 10		row 0 column 9		row 0 column 8	
...	...		...		...		...	
6	row 0 column 27		row 0 column 26		row 0 column 25		row 0 column 24	
7	row 0 column 31		row 0 column 30		row 0 column 29		row 0 column 28	
...	...		...		...		...	
254	row 31 column 27		row 31 column 26		row 31 column 25		row 31 column 24	
255	row 31 column 31		row 31 column 30		row 31 column 29		row 31 column 28	

Table 8: Cursor modes

Cursor pattern	Cursor mode	
	CMODE = 0	CMODE = 1
00	second cursor color	second cursor color
01	first cursor color	first cursor color
10	transparent	transparent
11	inverted input	auxiliary cursor color

7.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R color space in this block. The color difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

A gain adjust option corrects the level swing of the graphics world (black-to-white as 0 to 255) to the required range of 16 to 235.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

7.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the color phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7104E; SAA7105E input data is in accordance with *'ITU-R BT.656'*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

7.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 78.

An additional, programmable vertical filter supports the anti-flicker function. This filter is not available at upscaling factors of more than 2.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling by a maximum factor of 2. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 7.20.

An additional upscaling mode allows to increase the upscaling factor to maximum 4 as it is required for the old VGA modes like 320 $\times$ 240.

7.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor.

7.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true color tint.

7.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA or HDTV mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 40 MHz and 85 MHz. Two programmable dividers provide the actual clock to be used externally and internally. The dividers can be programmed to factors of 1, 2, 4 and 8. For the internal pixel clock, a divider ratio of 8 makes no sense and is thus forbidden.

The internal clock can be switched completely to the pixel clock input. In this event, the input FIFO is useless and will be bypassed.

The entire pixel clock generation can be locked to the vertical frequency. Both pixel clock dividers get re-initialized every field. Optionally, the DTO can be cleared with each V-sync. At proper programming, this will make the pixel clock frequency a precise multiple of the vertical and horizontal frequencies. This is required for some graphic controllers.

7.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

7.12 Encoder

7.12.1 Video path

The encoder generates luminance and color subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7104E only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figure 8 and Figure 9. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband color signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher color bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figure 6 and Figure 7.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, color is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

7.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Figure 15.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

7.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

7.12.4 Closed caption encoder

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

7.12.5 Anti-taping (SAA7104E only)

For more information contact your nearest Philips Semiconductors sales office.

7.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and color difference signals and 2 times oversampling for luminance and 4 times oversampling for color difference signals is performed. The transfer curves of luminance and color difference components of RGB are illustrated in Figure 10 and Figure 11.

7.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I^2C-bus status byte reflects whether a load is applied or not. In addition, an automatic sense mode can be activated which indicates a 75 Ω load at any of the three outputs at the dedicated interrupt pin TVD.

If the SAA7104E; SAA7105E is required to drive a second (auxiliary) VGA monitor or an HDTV set, the DACs receive the signal coming from the HD data path. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

7.15 HD data path

This data path allows the SAA7104E; SAA7105E to be used with VGA or HDTV monitors. It receives its data directly from the cursor generator and supports RGB and Y-P_B-P_R output formats (RGB not with Y-P_B-P_R input formats). No scaling is done in this mode.

A gain adjustment either leads the full level swing to the digital-to-analog converters or reduces the amplitude by a factor of 0.69. This enables sync pulses to be added to the signal as it is required for display units expecting signals with sync pulses, either regular or 3-level syncs.

7.16 Timing generator

The synchronization of the SAA7104E; SAA7105E is able to operate in two modes; Slave mode and Master mode.

In Slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 Hz and 60 Hz are allowed with the SAA7104E; SAA7105E. In Slave mode, it is not possible to lock the encoders color carrier to the line frequency with the PHRES bits.

In the (more common) Master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{\text{CBO}}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{\text{CBO}}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{\text{CBO}}$ goes active. This signal is programmable and it is possible to adjust the following (see Figure 13 and Figure 14):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7104E; SAA7105E will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines. The additional request pulses will be suppressed with LUTL set to logic 0; see Table 103. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

7.17 Pattern generator for HD sync pulses

The pattern generator provides appropriate synchronization patterns for the video data path in auxiliary monitor or HDTV mode. It provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced computer graphics or ATSC formats. The sync engine is capable of providing a combination of event-value pairs which can be used

to insert certain values in the outgoing data stream at specified times. It can also be used to generate digital signals associated with time events. These can be used as digital horizontal and vertical synchronization signals on pins HSM_CSYNC and VSM.

The picture position is adjustable through the programmable relationship between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined. The sequence specifies a series of line types and the number of occurrences of this specific line type. Once the sequence has been completed, it restarts from the beginning. All pulse shapes are filtered internally in order to avoid ringing after analog post filters.

The sequence of the generated pulse stream must fit precisely to the incoming data stream in terms of the total number of pixels per line and lines per frame.

The sync engines flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. Figure 3 illustrates the context between the various tables.

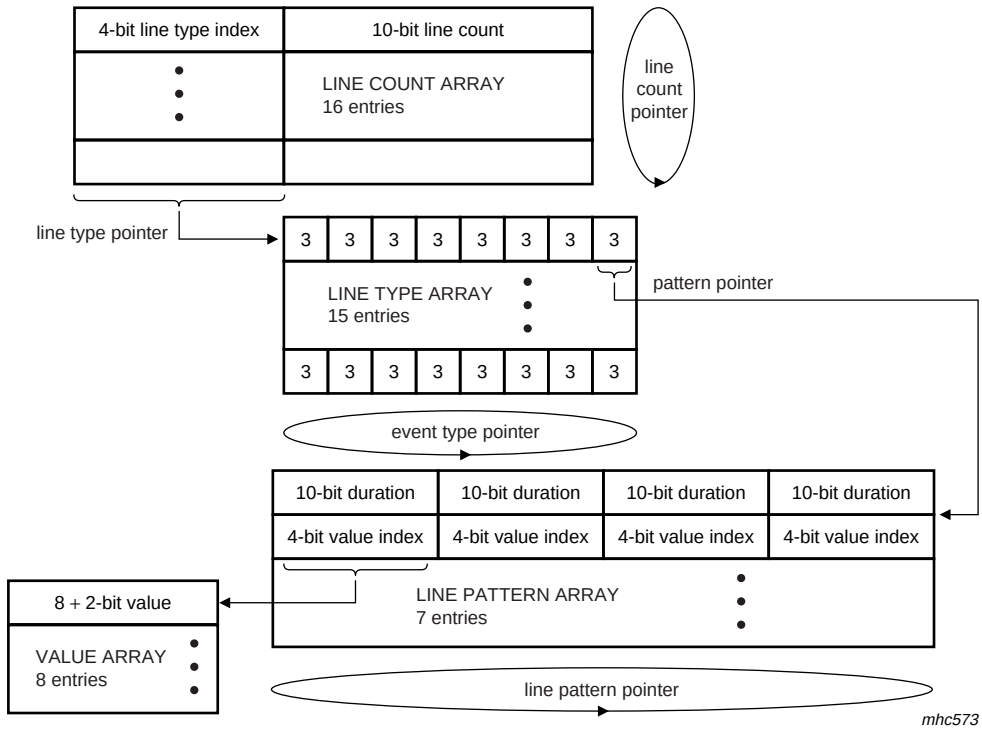


Fig 3. Context between the pattern generator tables for DH sync pulses

The first table serves as an array to hold the correct sequence of lines that compose the synchronization raster; it can contain up to 16 entries. Each entry holds a 4-bit index to the next table and a 10-bit counter value which specifies how often this particular line is invoked. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries.

The 4-bit index in the line count array points to the line type array. It holds up to 15 entries (index 0 is not used), index 1 points to the first entry, index 2 to the second entry of the line type array etc.

Each entry of the line type array can hold up to 8 index pointers to another table. These indices point to portions of a line pulse pattern: A line could be split up e.g. into a sync, a blank, and an active portion followed by another blank portion, occupying four entries in one table line.

Each index of this table points to a particular line of the next table in the linked list. This table is called the line pattern array and each of the up to seven entries stores up to four pairs of a duration in pixel clock cycles and an index to a value table. The table entries are used to define portions of a line representing a certain value for a certain number of clock cycles.

The value specified in this table is actually another 3-bit index into a value array which can hold up to eight 8-bit values. If bit 4 (MSB) of the index is logic 1, the value is inserted into the G or Y signal, only; if bit 4 = 0, the associated value is inserted into all three signals.

Two additional bits of the entries in the value array (LSBs of the second byte) determine if the associated events appear as a digital pulse on the HSM_CSYNC and/or VSM outputs.

To ease the trigger set-up for the sync generation module, a set of registers is provided to set up the screen raster which is defined as width and height. A trigger position can be specified as an x, y co-ordinate within the overall dimensions of the screen raster. If the x, y counter matches the specified co-ordinates, a trigger pulse is generated which pre-loads the tables with their initial values.

The listing in Table 9 outlines an example on how to set up the sync tables for a 1080i HD raster.

Important note:

Due to a problem in the programming interface, writing to the line pattern array (address D2) might destroy the data of the line type array (address D1). A work around is to write the line pattern array data before writing the line type array. Reading of the arrays is possible but all address pointers must be initialized before the next write operation.

Table 9: Example for set-up of the sync tables

Sequence	Comment
Write to subaddress D0h	
00	points to first entry of line count array (index 0)
05 20	generate 5 lines of line type index 2 (this is the second entry of the line type array); will be the first vertical raster pulse
01 40	generate 1 line of line type index 4; will be sync-black-sync-black sequence after the first vertical pulse
0E 60	generate 14 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence
01 50	generate 1 line of line type index 5; will be the following line (line 563) with sync-black-sync-black-null sequence (null is equivalent to sync tip)
04 20	generate 4 lines of line type index 2; will be the second vertical raster pulse
01 30	generate 1 line of line type index 3; will be the following line with sync-null-sync-black sequence
0F 60	generate 15 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence; now, 1125 lines are defined
Write to subaddress D2h (insertion is done into all three analog output signals)	
00	points to first entry of line pattern array (index 1)
6F 33 2B 30 00 00 00 00	880 × value(3) + 44 × value(3); (subtract 1 from real duration)
6F 43 2B 30 00 00 00 00	880 × value(4) + 44 × value(3)
3B 30 BF 03 BF 03 2B 30	60 × value(3) + 960 × value(0) + 960 × value(0) + 44 × value(3)
2B 10 2B 20 57 30 00 00	44 × value(1) + 44 × value(2) + 88 × value(3)
3B 30 BF 33 BF 33 2B 30	60 × value(3) + 960 × value(3) + 960 × value(3) + 44 × value(3)
Write to subaddress D1h	
00	points to first entry of line type array (index 1)
34 00 00 00	use pattern entries 4 and 3 in this sequence (for sync and active video)
24 24 00 00	use pattern entries 4, 2, 4 and 2 in this sequence (for 2 × sync-black-null-black)
24 14 00 00	use pattern entries 4, 2, 4 and 1 in this sequence (for sync-black-null-black-null)
14 14 00 00	use pattern entries 4, 1, 4 and 1 in this sequence (for sync-black-sync-black)
14 24 00 00	use pattern entries 4, 1, 4 and 2 in this sequence (for sync-black-sync-black-null)
54 00 00 00	use pattern entries 4 and 5 in this sequence (for sync-black)
Write to subaddress D3h (no signals are directed to pins HSM_CSYNC and VSM)	
00	points to first entry of value array (index 0)
CC 00	black level, to be added during active video
80 00	sync level LOW (minimum output voltage)
0A 00	sync level HIGH (3-level sync)
CC 00	black level (needed elsewhere)
80 00	null (identical to sync level LOW)
Write to subaddress DCh	
0B	insertion is active, gain for signal is adapted accordingly

7.18 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbit/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFh. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I²C-bus slave address is defined as 88h.

7.19 Power-down modes

In order to reduce the power consumption, the SAA7104E; SAA7105E supports 2 Power-down modes, accessible via the I²C-bus. The analog Power-down mode (DOWNA = 1) turns off the digital-to-analog converters and the pixel clock synthesizer. The digital Power-down mode (DOWND = 1) turns off all internal clocks and sets the digital outputs to LOW except the I²C-bus interface. The IC keeps its programming and can still be accessed in this mode, however not all registers can be read or written to. Reading or writing to the look-up tables, the cursor and the HD sync generator require a valid pixel clock. The typical supply current in full power-down is approximately 5 mA.

Because the analog Power-down mode turns off the pixel clock synthesizer, there are limitations in some applications. If there is no pixel clock, the IC is not able to set its outputs to LOW. So, in most cases, DOWNA and DOWND should be set to logic 1 simultaneously. If the EIDIV bit is logic 1, it should be set to logic 0 before power-down.

7.20 Programming the SAA7104E; SAA7105E

The SAA7104E; SAA7105E needs to provide a continuous data stream at its analog outputs as well as receive a continuous stream of data from its data source. Because there is no frame memory isolating the data streams, restrictions apply to the input frame timings.

Input and output processing of the SAA7104E; SAA7105E are only coupled through the vertical frequencies. In Master mode, the encoder provides a vertical sync and an odd/even pulse to the input processing. In Slave mode, the encoder receives them.

The parameters of the input field are mainly given by the memory capacity of the SAA7104E; SAA7105E. The rule is that the scaler and thus the input processing needs to provide the video data in the same time frames as the encoder reads them. Therefore, the vertical active video times (and the vertical frequencies) need to be the same.

The second rule is that there has to be data in the buffer FIFO when the encoder enters the active video area. Therefore, the vertical offset in the input path needs to be a bit shorter than the offset of the encoder.

The following Sections give the set of equations required to program the IC for the most common application: A post processor in Master mode with non-interlaced video input data.

Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- RiePclk: the ratio of internal to external pixel clock
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns)

7.20.1 TV display window

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible.

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 47.

ADWHS = 256 + 710 – OutPix (60 Hz); ADWHS = 284 + 702 – OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287; see Table 55 to Table 57.

$$\mathrm{FAL} = 19 + \frac{240 - \mathrm{OutLin}}{2}\ (60\ \mathrm{Hz});\quad \mathrm{FAL} = 23 + \frac{287 - \mathrm{OutLin}}{2}\ (50\ \mathrm{Hz});$$

LAL = FAL + OutLin (all frequencies)

Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10 %, giving approximately 640 output pixels per line.

7.20.2 Input frame and pixel clock

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

$$\mathrm{TPclk} = \frac{262.5 \times 1716 \times \mathrm{TXclk}}{\mathrm{InPpl} \times \mathrm{integer}\left(\frac{\mathrm{InLin} + 2}{\mathrm{OutLin}} \times 262.5\right)}\ (60\ \mathrm{Hz})$$

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)}$$ (50 Hz) and for the pixel clock generator

$$PCL = \frac{TXclk}{TPclk} \times 2^{20 + PCLE}$$ (all frequencies); see Table 59 and Table 60. The divider PCLE should be set according to Table 60. PCLI may be set to a lower or the same value. Setting a lower value means that the internal pixel clock is higher and the data get sampled up. The difference may be 1 at 640 × 480 pixels resolution and 2 at resolutions with 320 pixels per line as a rule of thumb. This allows horizontal upscaling by a maximum factor of 2 respectively 4 (this is the parameter RiePclk).

$$PCLI = PCLE - \frac{log\,RiePclk}{log\,2}$$ (all frequencies)

The equations ensure that the last line of the field has the full number of clock cycles. Many graphic controllers require this. Note that the bit PCLSY needs to be set to ensure that there is not even a fraction of a clock left at the end of the field.

7.20.3 Horizontal scaler

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN = InPpl × RiePclk − 1

$$XPIX = \frac{InPix}{2} \times RiePclk$$

$$XINC = \frac{OutPix}{InPix} \times \frac{4096}{RiePclk}$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

7.20.4 Vertical scaler

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2.5$$ (60 Hz) $$YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2.5$$ (50 Hz)

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth. Note that the maximum value for YINC is 4095. It might be necessary to reduce the value of YSKIP to fulfil this requirement.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

It should be noted that these equations assume that the input is non-interlaced but the output is interlaced. If the input is interlaced, the initial weighting factors need to be adapted to obtain the proper phase offsets in the output frame.

If vertical upscaling beyond the upper capabilities is required, the parameter YUPSC may be set to logic 1. This extends the maximum vertical scaling factor by a factor of 2. Only the parameter YINC is affected, it needs to be divided by two to get the same effect.

There are restrictions in this mode:

- The vertical filter YFILT is not available in this mode; the circuit will ignore this value
- The horizontal blanking needs to be long enough to transfer an output line between 2 memory locations. This is 710 internal pixel clocks.

  Or the upscaling factor needs to be limited to 1.5 and the horizontal upscaling factor is also limited to less than ~1.5. In this case a normal blanking length is sufficient.

7.21 Input levels and formats

The SAA7104E; SAA7105E accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *'ITU-R BT.601'*. An optional gain adjustment also allows to accept data with the full level swing of 0 to 255.

For C and CVBS outputs, deviating amplitudes of the color difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and color difference signals (GCD). Reference levels are measured with a color bar, 100 % white, 100 % amplitude and 100 % saturation.

The SAA7104E; SAA7105E has special input cells for the VGC port. They operate at a wider supply voltage range and have a strict input threshold at $\frac{1}{2}V_{DDD}$. To achieve full speed of these cells, the EIDIV bit needs to be set to logic 1. Note that the impedance of these cells is approximately 6 kΩ. This may cause trouble with the bootstrapping pins of some graphic chips. So the power-on reset forces the bit to logic 0, the input impedance is regular in this mode.

Table 10: *'ITU-R BT.601'* signal component levels

Color	Signals [1]					
	Y	C_B	C_R	R	G	B
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

[1] Transformation:

$R = Y + 1.3707 \times (C_R - 128)$

$G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$

$B = Y + 1.7324 \times (C_B - 128)$.

Table 11: Usage of bits SLOT and EDGE

Data slot control (example for format 0)			
SLOT	EDGE	1st data	2nd data
0	0	at rising edge G3/Y3	at falling edge R7/C_R7
0	1	at falling edge G3/Y3	at rising edge R7/C_R7
1	0	at rising edge R7/C_R7	at falling edge G3/Y3
1	1	at falling edge R7/C_R7	at rising edge G3/Y3

Table 12: Pin assignment for input format 0

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	Falling clock edge	Rising clock edge
PD11	G3/Y3	R7/C_R7
PD10	G2/Y2	R6/C_R6
PD9	G1/Y1	R5/C_R5
PD8	G0/Y0	R4/C_R4
PD7	B7/C_B7	R3/C_R3
PD6	B6/C_B6	R2/C_R2
PD5	B5/C_B5	R1/C_R1
PD4	B4/C_B4	R0/C_R0
PD3	B3/C_B3	G7/Y7
PD2	B2/C_B2	G6/Y6
PD1	B1/C_B1	G5/Y5
PD0	B0/C_B0	G4/Y4

Table 13: Pin assignment for input format 1

5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	X
PD6	G1	R4
PD5	G0	R3
PD4	B4	R2
PD3	B3	R1
PD2	B2	R0
PD1	B1	G4
PD0	B0	G3

Table 14: Pin assignment for input format 2

5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB		
Pin	**Falling clock edge**	**Rising clock edge**
PD7	G2	R4
PD6	G1	R3
PD5	G0	R2
PD4	B4	R1
PD3	B3	R0
PD2	B2	G5
PD1	B1	G4
PD0	B0	G3

Table 15: Pin assignment for input format 3

8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R				
Pin	**Falling clock edge n**	**Rising clock edge n**	**Falling clock edge n + 1**	**Rising clock edge n + 1**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)
PD4	$C_B4(0)$	Y4(0)	$C_R4(0)$	Y4(1)
PD3	$C_B3(0)$	Y3(0)	$C_R3(0)$	Y3(1)
PD2	$C_B2(0)$	Y2(0)	$C_R2(0)$	Y2(1)
PD1	$C_B1(0)$	Y1(0)	$C_R1(0)$	Y1(1)
PD0	$C_B0(0)$	Y0(0)	$C_R0(0)$	Y0(1)

Table 16: Pin assignment for input format 4

8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock)				
Pin	**Rising clock edge n**	**Rising clock edge n + 1**	**Rising clock edge n + 2**	**Rising clock edge n + 3**
PD7	$C_B7(0)$	Y7(0)	$C_R7(0)$	Y7(1)
PD6	$C_B6(0)$	Y6(0)	$C_R6(0)$	Y6(1)
PD5	$C_B5(0)$	Y5(0)	$C_R5(0)$	Y5(1)

Table 16: Pin assignment for input format 4 *...continued*

8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock)				
Pin	**Rising clock edge n**	**Rising clock edge n + 1**	**Rising clock edge n + 2**	**Rising clock edge n + 3**
PD4	$C_B4(0)$	Y4(0)	$C_R4(0)$	Y4(1)
PD3	$C_B3(0)$	Y3(0)	$C_R3(0)$	Y3(1)
PD2	$C_B2(0)$	Y2(0)	$C_R2(0)$	Y2(1)
PD1	$C_B1(0)$	Y1(0)	$C_R1(0)$	Y1(1)
PD0	$C_B0(0)$	Y0(0)	$C_R0(0)$	Y0(1)

Table 17: Pin assignment for input format 5 [1]

8-bit non-interlaced index color		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	X	X
PD10	X	X
PD9	X	X
PD8	X	X
PD7	INDEX7	X
PD6	INDEX6	X
PD5	INDEX5	X
PD4	INDEX4	X
PD3	INDEX3	X
PD2	INDEX2	X
PD1	INDEX1	X
PD0	INDEX0	X

[1] X = don't care.

Table 18: Pin assignment for input format 6

8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB/C_B-Y-C_R		
Pin	**Falling clock edge**	**Rising clock edge**
PD11	G4/Y4	R7/C_R7
PD10	G3/Y3	R6/C_R6
PD9	G2/Y2	R5/C_R5
PD8	B7/C_B7	R4/C_R4
PD7	B6/C_B6	R3/C_R3
PD6	B5/C_B5	G7/Y7
PD5	B4/C_B4	G6/Y6
PD4	B3/C_B3	G5/Y5
PD3	G0/Y0	R2/C_R2
PD2	B2/C_B2	R1/C_R1
PD1	B1/C_B1	R0/C_R0
PD0	B0/C_B0	G1/Y1

8.1 Bit allocation map

Table 19: Slave receiver (slave address 88h)

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Status byte (read only)	00	VER2	VER1	VER0	CCRDO	CCRDE	-	FSEQ	O_E
Null	01 to 15	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Common DAC adjust fine	16	[1]	[1]	[1]	[1]	DACF3	DACF2	DACF1	DACF0
R DAC adjust coarse	17	[1]	[1]	[1]	RDACC4	RDACC3	RDACC2	RDACC1	RDACC0
G DAC adjust coarse	18	[1]	[1]	[1]	GDACC4	GDACC3	GDACC2	GDACC1	GDACC0
B DAC adjust coarse	19	[1]	[1]	[1]	BDACC4	BDACC3	BDACC2	BDACC1	BDACC0
MSM threshold	1A	MSMT7	MSMT6	MSMT5	MSMT4	MSMT3	MSMT2	MSMT1	MSMT0
Monitor sense mode	1B	MSM	MSA	MSOE	[1]	[1]	RCOMP	GCOMP	BCOMP
Chip ID (04h or 05h, read only)	1C	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	[1]	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28	[1]	[1]	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29	SRES	[1]	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2A	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2B	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2C	CGEN	[1]	[1]	[1]	CG19	CG18	CG17	CG16
Output port control	2D	VBSEN	CVBSEN1	CVBSEN0	CEN	ENCOFF	CLK2EN	CVBSEN2	[1]
Null	2E to 36	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Input path control	37	[1]	YUPSC	YFIL1	YFIL0	[1]	CZOOM	IGAIN	XINT
Gain luminance for RGB	38	[1]	[1]	[1]	GY4	GY3	GY2	GY1	GY0
Gain color difference for RGB	39	[1]	[1]	[1]	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3A	CBENB	[1]	SYNTV	SYMP	DEMOFF	CSYNC	Y2C	UV2C
VPS enable, input control 2	54	VPSEN	[1]	GPVAL	GPEN	[1]	[1]	EDGE	SLOT
VPS byte 5	55	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0

Table 19: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	[1]	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	[1]	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Standard control	61	DOWND	DOWNA	INPI	YGS	[1]	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Null	6B	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	NVTRIG	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed caption, teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
Active display window horizontal start	70	ADWHS7	ADWHS6	ADWHS5	ADWHS4	ADWHS3	ADWHS2	ADWHS1	ADWHS0
Active display window horizontal end	71	ADWHE7	ADWHE6	ADWHE5	ADWHE4	ADWHE3	ADWHE2	ADWHE1	ADWHE0
MSBs ADWH	72	[1]	ADWHE10	ADWHE9	ADWHE8	[1]	ADWHS10	ADWHS9	ADWHS8
TTX request horizontal start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request horizontal delay	74	[1]	[1]	[1]	[1]	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance	75	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	[1]	[1]	[1]
TTX odd request vertical start	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0

Table 19: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
TTX even request vertical start	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request vertical end	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7C	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13
FIFO status (read only)	80	-	-	-	-	IFERR	BFERR	OVFL	UDFL
Pixel clock 0	81	PCL07	PCL06	PCL05	PCL04	PCL03	PCL02	PCL01	PCL00
Pixel clock 1	82	PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL09	PCL08
Pixel clock 2	83	PCL23	PCL22	PCL21	PCL20	PCL19	PCL18	PCL17	PCL16
Pixel clock control	84	DCLK	PCLSY	IFRA	IFBP	PCLE1	PCLE0	PCLI1	PCLI0
FIFO control	85	EIDIV	[1]	[1]	[1]	FILI3	FILI2	FILI1	FILI0
Null	86 to 8F	[1]	[1]	[1]	[1]	[1]	[1]	[1]	[1]
Horizontal offset	90	XOFS7	XOFS6	XOFS5	XOFS4	XOFS3	XOFS2	XOFS1	XOFS0
Pixel number	91	XPIX7	XPIX6	XPIX5	XPIX4	XPIX3	XPIX2	XPIX1	XPIX0
Vertical offset odd	92	YOFSO7	YOFSO6	YOFSO5	YOFSO4	YOFSO3	YOFSO2	YOFSO1	YOFSO0
Vertical offset even	93	YOFSE7	YOFSE6	YOFSE5	YOFSE4	YOFSE3	YOFSE2	YOFSE1	YOFSE0
MSBs	94	YOFSE9	YOFSE8	YOFSO9	YOFSO8	XPIX9	XPIX8	XOFS9	XOFS8
Line number	95	YPIX7	YPIX6	YPIX5	YPIX4	YPIX3	YPIX2	YPIX1	YPIX0
Scaler CTRL, MCB YPIX	96	EFS	PCBN	SLAVE	ILC	YFIL	[1]	YPIX9	YPIX8
Sync control	97	HFS	VFS	OFS	PFS	OVS	PVS	OHS	PHS
Line length	98	HLEN7	HLEN6	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
Input delay, MSB line length	99	IDEL3	IDEL2	IDEL1	IDEL0	HLEN11	HLEN10	HLEN9	HLEN8
Horizontal increment	9A	XINC7	XINC6	XINC5	XINC4	XINC3	XINC2	XINC1	XINC0
Vertical increment	9B	YINC7	YINC6	YINC5	YINC4	YINC3	YINC2	YINC1	YINC0
MSBs vertical and horizontal increment	9C	YINC11	YINC10	YINC9	YINC8	XINC11	XINC10	XINC9	XINC8
Weighting factor odd	9D	YIWGTO7	YIWGTO6	YIWGTO5	YIWGTO4	YIWGTO3	YIWGTO2	YIWGTO1	YIWGTO0

Table 19: Slave receiver (slave address 88h) *...continued*

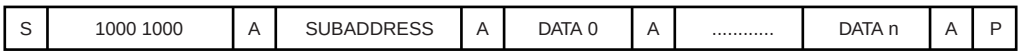
Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Weighting factor even	9E	YIWGTE7	YIWGTE6	YIWGTE5	YIWGTE4	YIWGTE3	YIWGTE2	YIWGTE1	YIWGTE0
Weighting factor MSB	9F	YIWGTE11	YIWGTE10	YIWGTE9	YIWGTE8	YIWGTO11	YIWGTO10	YIWGTO9	YIWGTO8
Vertical line skip	A0	YSKIP7	YSKIP6	YSKIP5	YSKIP4	YSKIP3	YSKIP2	YSKIP1	YSKIP0
Blank enable for NI-bypass, vertical line skip MSB	A1	BLEN	[1]	[1]	[1]	YSKIP11	YSKIP10	YSKIP9	YSKIP8
Border color Y	A2	BCY7	BCY6	BCY5	BCY4	BCY3	BCY2	BCY1	BCY0
Border color U	A3	BCU7	BCU6	BCU5	BCU4	BCU3	BCU2	BCU1	BCU0
Border color V	A4	BCV7	BCV6	BCV5	BCV4	BCV3	BCV2	BCV1	BCV0
HD sync line count array	D0	RAM address (see Table 83)							
HD sync line type array	D1	RAM address (see Table 85)							
HD sync line pattern array	D2	RAM address (see Table 87)							
HD sync value array	D3	RAM address (see Table 89)							
HD sync trigger state 1	D4	HLCT7	HLCT6	HLCT5	HLCT4	HLCT3	HLCT2	HLCT1	HLCT0
HD sync trigger state 2	D5	HLCPT3	HLCPT2	HLCPT1	HLCPT0	HLPPT1	HLPPT0	HLCT9	HLCT8
HD sync trigger state 3	D6	HDCT7	HDCT6	HDCT5	HDCT4	HDCT3	HDCT2	HDCT1	HDCT0
HD sync trigger state 4	D7	[1]	HEPT2	HEPT1	HEPT0	[1]	[1]	HDCT9	HDCT8
HD sync trigger phase x	D8	HTX7	HTX6	HTX5	HTX4	HTX3	HTX2	HTX1	HTX0
	D9	[1]	[1]	[1]	[1]	HTX11	HTX10	HTX9	HTX8
HD sync trigger phase y	DA	HTY7	HTY6	HTY5	HTY4	HTY3	HTY2	HTY1	HTY0
	DB	[1]	[1]	[1]	[1]	[1]	[1]	HTY9	HTY8
HD output control	DC	[1]	[1]	[1]	[1]	HDSYE	HDTC	HDGY	HDIP
Cursor color 1 R	F0	CC1R7	CC1R6	CC1R5	CC1R4	CC1R3	CC1R2	CC1R1	CC1R0
Cursor color 1 G	F1	CC1G7	CC1G6	CC1G5	CC1G4	CC1G3	CC1G2	CC1G1	CC1G0
Cursor color 1 B	F2	CC1B7	CC1B6	CC1B5	CC1B4	CC1B3	CC1B2	CC1B1	CC1B0
Cursor color 2 R	F3	CC2R7	CC2R6	CC2R5	CC2R4	CC2R3	CC2R2	CC2R1	CC2R0
Cursor color 2 G	F4	CC2G7	CC2G6	CC2G5	CC2G4	CC2G3	CC2G2	CC2G1	CC2G0
Cursor color 2 B	F5	CC2B7	CC2B6	CC2B5	CC2B4	CC2B3	CC2B2	CC2B1	CC2B0
Auxiliary cursor color R	F6	AUXR7	AUXR6	AUXR5	AUXR4	AUXR3	AUXR2	AUXR1	AUXR0
Auxiliary cursor color G	F7	AUXG7	AUXG6	AUXG5	AUXG4	AUXG3	AUXG2	AUXG1	AUXG0
Auxiliary cursor color B	F8	AUXB7	AUXB6	AUXB5	AUXB4	AUXB3	AUXB2	AUXB1	AUXB0

Table 19: Slave receiver (slave address 88h) *...continued*

Register function	Subaddress (hexadecimal)	7	6	5	4	3	2	1	0
Horizontal cursor position	F9	XCP7	XCP6	XCP5	XCP4	XCP3	XCP2	XCP1	XCP0
Horizontal hot spot, MSB XCP	FA	XHS4	XHS3	XHS2	XHS1	XHS0	XCP10	XCP9	XCP8
Vertical cursor position	FB	YCP7	YCP6	YCP5	YCP4	YCP3	YCP2	YCP1	YCP0
Vertical hot spot, MSB YCP	FC	YHS4	YHS3	YHS2	YHS1	YHS0	[1]	YCP9	YCP8
Input path control	FD	LUTOFF	CMODE	LUTL	IF2	IF1	IF0	MATOFF	DFOFF
Cursor bit map	FE	RAM address (see Table 104)							
Color look-up table	FF	RAM address (see Table 105)							

[1] All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

8.2 I²C-bus format

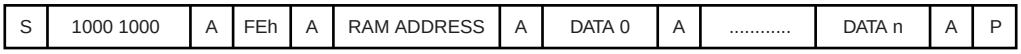


001aad411

a. to control registers

001aad412

b. to the HD line count array (subaddress D0h)



001aad413

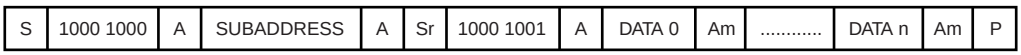
c. to cursor bit map (subaddress FEh)

001aad414

d. to color look-up table (subaddress FFh)

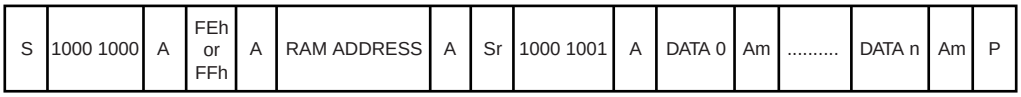
See Table 20 for explanations.

Fig 4. I²C-bus write access



001aad415

a. to control registers



001aad416

b. to cursor bit map or color LUT

See Table 20 for explanations.

Fig 5. I²C-bus read access

Table 20: Explanations of Figure 4 and Figure 5

Code	Description
S	START condition
Sr	repeated START condition
1000 100X [1]	slave address
A	acknowledge generated by the slave
Am	acknowledge generated by the master
SUBADDRESS [2]	subaddress byte
DATA	data byte
--------	continued data bytes and acknowledges
P	STOP condition
RAM ADDRESS	start address for RAM access

[1] X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.

[2] If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

8.3 Slave receiver

Table 21: Common DAC adjust fine register, subaddress 16h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	DACF[3:0]	R/W		DAC fine output voltage adjustment, 1 % steps for all DACs
			0111	7 %
			0110	6 %
			0101	5 %
			0100	4 %
			0011	3 %
			0010	2 %
			0001	1 %
			0000*	0 %
			1000	0 %
			1001	−1 %
			1010	−2 %
			1011	−3 %
			1100	−4 %
			1101	−5 %
			1110	−6 %
			1111	−7 %

Table 22: RGB DAC adjust coarse registers, subaddresses 17h to 19h, bit description

Subaddress	Bit	Symbol	Description
17h to 19h	7 to 5	-	must be programmed with logic 0 to ensure compatibility to future enhancements
17h	4 to 0	RDACC[4:0]	output level coarse adjustment for RED DAC; default after reset is 1Bh for output of C signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
18h	4 to 0	GDACC[4:0]	output level coarse adjustment for GREEN DAC; default after reset is 1Bh for output of VBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
19h	4 to 0	BDACC[4:0]	output level coarse adjustment for BLUE DAC; default after reset is 1Fh for output of CVBS signal 0 0000b ≡ 0.585 V to 1 1111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion

Table 23: MSM threshold, subaddress 1Ah, bit description

Bit	Symbol	Description
7 to 0	MSMT[7:0]	monitor sense mode threshold for DAC output voltage, should be set to 70h

Table 24: Monitor sense mode register, subaddress 1Bh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	MSM	R/W		monitor sense mode
			0*	off; RCOMP, GCOMP and BCOMP bits are not valid
			1	on
6	MSA	R/W		automatic monitor sense mode
			0*	off; RCOMP, GCOMP and BCOMP bits are not valid
			1	on if MSM = 0
5	MSOE	R/W	0	pin TVD is active
			1*	pin TVD is 3-state
4 and 3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	RCOMP	R		check comparator at DAC on pin RED_CR_C_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded
1	GCOMP	R		check comparator at DAC on pin GREEN_VBS_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded
0	BCOMP	R		check comparator at DAC on pin BLUE_CB_CVBS
			0	active, output is loaded
			1	inactive, output is not loaded

Table 25: Wide screen signal registers, subaddresses 26h and 27h, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
27h	7	WSSON	R/W	0*	wide screen signalling output is disabled
				1	wide screen signalling output is enabled
	6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	5 to 3	WSS[13:11]	R/W	-	wide screen signalling bits, reserved
	2 to 0	WSS[10:8]	R/W	-	wide screen signalling bits, subtitles
26h	7 to 4	WSS[7:4]	R/W	-	wide screen signalling bits, enhanced services
	3 to 0	WSS[3:0]	R/W	-	wide screen signalling bits, aspect ratio

Table 26: Real-time control and burst start register, subaddress 28h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BS[5:0]	R/W		starting point of burst in clock cycles
			21h*	PAL: BS = 33; strapping pin FSVGC tied to HIGH
			19h*	NTSC: BS = 25; strapping pin FSVGC tied to LOW

Table 27: Sync reset enable and burst end register, subaddress 29h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	SRES	R/W	0*	pin TTX_SRES accepts a teletext bit stream (TTX)
			1	pin TTX_SRES accepts a sync reset input (SRES); a HIGH impulse resets synchronization of the encoder (first field, first line)
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5 to 0	BE[5:0]	R/W		ending point of burst in clock cycles
			1Dh*	PAL: BE = 29; strapping pin FSVGC tied to HIGH
			1Dh*	NTSC: BE = 29; strapping pin FSVGC tied to LOW

Table 28: Copy generation 0, 1, 2 and CG enable registers, subaddresses 2Ah to 2Ch, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
2Ch	7	CGEN	R/W		copy generation data output
				0*	disabled
				1	enabled
	6 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	3 to 0	CG[19:16]	R/W	-	LSBs of the respective bytes are encoded immediately after run-in, the MSBs of the respective bytes have to carry the CRCC bits, in accordance with the definition of copy generation management system encoding format.
2Bh	7 to 0	CG[15:8]			
2Ah	7 to 0	CG[7:0]			

Table 29: Output port control register, subaddress 2Dh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VBSEN	R/W		pin GREEN_VBS_CVBS provides a
			0	component GREEN signal (CVBSEN1 = 0) or CVBS signal (CVBSEN1 = 1)
			1*	luminance (VBS) signal
6	CVBSEN1	R/W		pin GREEN_VBS_CVBS provides a
			0*	component GREEN (G) or luminance (VBS) signal
			1	CVBS signal
5	CVBSEN0	R/W		pin BLUE_CB_CVBS provides a
			0	component BLUE (B) or color difference BLUE (C_B) signal
			1*	CVBS signal
4	CEN	R/W		pin RED_CR_C_CVBS provides a
			0	component RED (R) or color difference RED (C_R) signal
			1*	chrominance signal (C) as modulated subcarrier for S-video
3	ENCOFF	R/W		encoder
			0*	active
			1	bypass, DACs are provided with RGB signal after cursor insertion block
2	CLK2EN	R/W		pin TTXRQ_XCLKO2 provides
			0	teletext request signal (TTXRQ)
			1*	buffered crystal clock divided by two (13.5 MHz)
1	CVBSEN2	R/W		pin RED_CR_C_CVBS provides a
			0*	signal according to CEN
			1	CVBS signal
0	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 30: Input path control register, subaddress 37h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
6	YUPSC	R/W		vertical scaler
			0*	normal operation
			1	upscaling is enabled
5 and 4	YFIL[1:0]	R/W		vertical interpolation filter control; the filter is not available if YUPSC = 1
			00*	no filter active
			01	filter is inserted before vertical scaling
			10	filter is inserted after vertical scaling; YSKIP should be logic 0
			11	reserved
3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	CZOOM	R/W		cursor generator
			0*	normal operation
			1	cursor will be zoomed by a factor of 2 in both directions
1	IGAIN	R/W		expected input level swing is
			0*	16 to 235 (8-bit RGB)
			1	0 to 255 (8-bit RGB)
0	XINT	R/W		interpolation filter for horizontal upscaling
			0*	not active
			1	active

Table 31: Gain luminance for RGB register, subaddress 38h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GY[4:0]	R/W	-	Gain luminance of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 32: Gain color difference for RGB register, subaddress 39h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 5	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
4 to 0	GCD[4:0]	R/W	-	Gain color difference of RGB (C_R, Y and C_B) output, ranging from $(1 - {}^{16}/_{32})$ to $(1 + {}^{15}/_{32})$. Suggested nominal value = 0, depending on external application.

Table 33: Input port control 1 register, subaddress 3Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	CBENB	R/W	0	data from input ports is encoded
			1	color bar with fixed colors is encoded
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5	SYNTV	R/W		in Slave mode
			0*	the encoder is only synchronized at the beginning of an odd field
			1	the encoder receives a vertical sync signal
4	SYMP	R/W		horizontal and vertical trigger
			0*	taken from FSVGC or both VSVGC and HSVGC
			1	decoded out of *'ITU-R BT.656'* compatible data at PD port
3	DEMOFF	R/W		Y-C_B-C_R to RGB dematrix
			0*	active
			1	bypassed
2	CSYNC	R/W		pin HSM_CSYNC provides
			0	horizontal sync for non-interlaced VGA components output (at PIXCLK)
			1	composite sync for interlaced components output (at XTAL clock)
1	Y2C	R/W		input luminance data
			0	twos complement from PD input port
			1*	straight binary from PD input port
0	UV2C	R/W		input color difference data
			0	twos complement from PD input port
			1*	straight binary from PD input port

Table 34: VPS enable, input control 2, subaddress 54h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	VPSEN	R/W		video programming system data insertion
			0*	is disabled
			1	in line 16 is enabled
6	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
5	GPVAL	R/W		if GPEN = 1, pin VSM provides
			0	LOW level
			1	HIGH level
4	GPEN	R/W		pin VSM provides
			0*	vertical sync for a monitor
			1	constant signal according to GPVAL
3 and 2	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 34: VPS enable, input control 2, subaddress 54h, bit description *...continued*

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
1	EDGE	R/W		input data is sampled with
			0	inverse clock edges
			1*	the clock edges specified in Table 12 to Table 18
0	SLOT	R/W	0*	normal assignment of the input data to the clock edge
			1	correct time misalignment due to inverted assignment of input data to the clock edge

Table 35: VPS byte 5, 11, 12, 13 and 14 registers, subaddresses 55h to 59h, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
55h	7 to 0	VPS5[7:0]	R/W	-	fifth byte of video programming system data
56h	7 to 0	VPS11[7:0]	R/W	-	eleventh byte of video programming system data
57h	7 to 0	VPS12[7:0]	R/W	-	twelfth byte of video programming system data
58h	7 to 0	VPS13[7:0]	R/W	-	thirteenth byte of video programming system data
59h	7 to 0	VPS14[7:0]	R/W	-	fourteenth byte of video programming system data

[1] In line 16; LSB first; all other bytes are not relevant for VPS.

Table 36: Chrominance phase register, subaddress 5Ah, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	CHPS[7:0]	R/W	00h*	phase of encoded color subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees
			6Bh	PAL B/G and data from input ports in Master mode
			16h	PAL B/G and data from look-up table
			25h	NTSC M and data from input ports in Master mode
			46h	NTSC M and data from look-up table

Table 37: Gain U and gain U MSB, black level registers, subaddresses 5Bh and 5Dh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Bh	7 to 0	GAINU[8:0] [1]	white-to-black = 92.5 IRE	GAINU = –2.17 × nominal to +2.16 × nominal
5Dh	7		GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 118 (76h)	output subcarrier of U contribution = nominal
			white-to-black = 100 IRE	GAINU = –2.05 × nominal to +2.04 × nominal
			GAINU = 0	output subcarrier of U contribution = 0
			GAINU = 125 (7Dh)	output subcarrier of U contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLCKL[5:0] [2]	white-to-sync = 140 IRE [3]	recommended value: BLCKL = 58 (3Ah)
			BLCKL = 0 [3]	output black level = 29 IRE
			BLCKL = 63 (3Fh) [3]	output black level = 49 IRE
			white-to-sync = 143 IRE [4]	recommended value: BLCKL = 51 (33h)
			BLCKL = 0 [4]	output black level = 27 IRE
			BLCKL = 63 (3Fh) [4]	output black level = 47 IRE

[1] Variable gain for C_B signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable black level; input representation in accordance with *'ITU-R BT.601'*.

[3] Output black level/IRE = BLCKL × 2/6.29 + 28.9.

[4] Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 38: Gain V and gain V MSB, blanking level registers, subaddresses 5Ch and 5Eh, bit description

Subaddress	Bit	Symbol	Conditions	Remarks
5Ch	7 to 0	GAINV[8:0] [1]	white-to-black = 92.5 IRE	GAINV = –1.55 × nominal to +1.55 × nominal
5Eh	7		GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 165 (A5h)	output subcarrier of V contribution = nominal
			white-to-black = 100 IRE	GAINV = –1.46 × nominal to +1.46 × nominal
			GAINV = 0	output subcarrier of V contribution = 0
			GAINV = 175 (AFh)	output subcarrier of V contribution = nominal
	6	-	must be programmed with logic 0 to ensure compatibility to future enhancements	
	5 to 0	BLNNL[5:0] [2]	white-to-sync = 140 IRE [3]	recommended value: BLNNL = 46 (2Eh)
			BLNNL = 0 [3]	output blanking level = 25 IRE
			BLNNL = 63 (3Fh) [3]	output blanking level = 45 IRE
			white-to-sync = 143 IRE [4]	recommended value: BLNNL = 53 (35h)
			BLNNL = 0 [4]	output blanking level = 26 IRE
			BLNNL = 63 (3Fh) [4]	output blanking level = 46 IRE

[1] Variable gain for C_R signal; input representation in accordance with *'ITU-R BT.601'*.

[2] Variable blanking level.

[3] Output black level/IRE = BLNNL × 2/6.29 + 25.4.

[4] Output black level/IRE = BLNNL × 2/6.18 + 25.9; default after reset: 35h.

Table 39: CCR and blanking level VBI register, subaddress 5Fh, bit description

Bit	Symbol	Access	Value	Description
7 and 6	CCRS[1:0]	R/W		select cross-color reduction filter in luminance; for overall transfer characteristic of luminance see Figure 8
			00	no cross-color reduction
			01	cross-color reduction #1 active
			10	cross-color reduction #2 active
			11	cross-color reduction #3 active
5 to 0	BLNVB[5:0]	R/W	-	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 40: Standard control register, subaddress 61h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	DOWND	R/W		digital core
			0*	in normal operational mode
			1	in Sleep mode and is reactivated with an I^2C-bus address
6	DOWNA	R/W		DACs
			0*	in normal operational mode
			1	in Power-down mode
5	INPI	R/W		PAL switch
			0*	phase is nominal
			1	is inverted compared to nominal if RTCE = 1
4	YGS	R/W		luminance gain for white – black
			0	100 IRE
			1	92.5 IRE including 7.5 IRE set-up of black
3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
2	SCBW	R/W		bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figure 6 and Figure 7)
			0	enlarged
			1*	standard
1	PAL	R/W		encoding
			0	NTSC (non-alternating V component)
			1	PAL (alternating V component)
0	FISE	R/W		total pixel clocks per line
			0	864
			1	858

Table 41: Burst amplitude register, subaddress 62h, bit description

*Legend: * = default value after reset, ^ = recommended value.*

Bit	Symbol	Access	Value	Description
7	RTCE	R/W		real-time control
			0*	no real-time control of generated subcarrier frequency
			1	real-time control of generated subcarrier frequency through a Philips video decoder; for a specification of the RTC protocol see document *'RTC Functional Description'*, available on request
6 to 0	BSTA[6:0]	R/W		amplitude of color burst; input representation in accordance with *'ITU-R BT.601'*
			3Fh (63)^	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding; BSTA = 0 to 2.02 × nominal
			2Dh (45)^	white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding; BSTA = 0 to 2.82 × nominal
			43h (67)^	white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding; BSTA = 0 to 1.90 × nominal
			2Fh (47)*^	white-to-black = 100 IRE; burst = 43 IRE; PAL encoding; BSTA = 0 to 3.02 × nominal

Table 42: Subcarrier 0, 1, 2 and 3 registers, subaddresses 63h to 66h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
66h	7 to 0	FSC[31:24]	R/W	-	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency); FSC[31:24] = most significant byte; FSC[07:00] = least significant byte [1]
65h	7 to 0	FSC[23:16]	R/W	-	
64h	7 to 0	FSC[15:08]	R/W	-	
63h	7 to 0	FSC[07:00]	R/W	-	

[1] $$FSC = \text{round}\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$$

Examples:

a) NTSC M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F0 7C1Fh).

b) PAL B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A09 8ACBh).

Table 43: Line 21 odd 0, 1 and even 0, 1 registers, subaddresses 67h to 6Ah, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
67h	7 to 0	L21O[07:00]	R/W	-	first byte of captioning data, odd field
68h	7 to 0	L21O[17:10]	R/W	-	second byte of captioning data, odd field
69h	7 to 0	L21E[07:00]	R/W	-	first byte of extended data, even field
6Ah	7 to 0	L21E[17:10]	R/W	-	second byte of extended data, even field

[1] LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.

Table 44: Trigger control registers, subaddresses 6Ch and 6Dh, bit description

*Legend: * = default value after reset.*

Subaddress	Bit	Symbol	Access	Value	Description
6Ch	7 to 0	HTRIG[7:0]	R/W	00h*	sets the horizontal trigger phase related to chip-internal horizontal input [1]
6Dh	7 to 5	HTRIG[10:8]	R/W	0h*	
	4 to 0	VTRIG[4:0]	R/W	00h*	sets the vertical trigger phase related to chip-internal vertical input [2]

[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals.

[2] Increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1Fh).

Table 45: Multi control register, subaddress 6Eh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	NVTRIG	R/W		values of the VTRIG register are
			0	positive
			1	negative
6	BLCKON	R/W	0*	encoder in normal operation mode
			1	output signal is forced to blanking level
5 and 4	PHRES[1:0]	R/W		selects the phase reset mode of the color subcarrier generator
			00	no subcarrier reset
			01	subcarrier reset every two lines
			10	subcarrier reset every eight fields
			11	subcarrier reset every four fields
3 and 2	LDEL[1:0]	R/W		selects the delay on luminance path with reference to chrominance path
			00*	no luminance delay
			01	1 LLC luminance delay
			10	2 LLC luminance delay
			11	3 LLC luminance delay
1 and 0	FLC[1:0]	R/W		field length control
			00*	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz
			01	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
			10	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
			11	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 46: Closed caption, teletext enable register, subaddress 6Fh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 and 6	CCEN[1:0]	R/W		enables individual line 21 encoding
			00*	line 21 encoding off
			01	enables encoding in field 1 (odd)
			10	enables encoding in field 2 (even)
			11	enables encoding in both fields
5	TTXEN	R/W		teletext insertion
			0*	disabled
			1	enabled
4 to 0	SCCLN[4:0]	R/W	-	selects the actual line, where closed caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 47: Active Display Window Horizontal (ADWH) start and end registers, subaddresses 70h to 72h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
70h	7 to 0	ADWHS[7:0]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color [1]
71h	7 to 0	ADWHE[7:0]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color [1]
72h	7	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	6 to 4	ADWHE[10:8]	R/W	-	active display window horizontal end; defines the end of the active TV display portion before the border color [1]
	3	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
	2 to 0	ADWHS[10:8]	R/W	-	active display window horizontal start; defines the start of the active TV display portion after the border color [1]

[1] Values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed.

Table 48: TTX request horizontal start register, subaddress 73h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXHS[7:0]	R/W		start of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0); see Figure 15
			42h*	if strapped to PAL
			54h*	if strapped to NTSC

Table 49: TTX request horizontal delay register, subaddress 74h, bit description

*Legend: * = default value after reset and minimum value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0h	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	TTXHD[3:0]	R/W	2h*	indicates the delay in clock cycles between rising edge of TTXRQ output signal on pin TTXRQ_XCLKO2 (CLK2EN = 0) and valid data at pin TTX_SRES

Table 50: CSYNC advance register, subaddress 75h, bit description

Bit	Symbol	Access	Value	Description
7 to 3	CSYNCA[4:0]	R/W	-	advanced composite sync against RGB output from 0 XTAL clocks to 31 XTAL clocks
2 to 0	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements

Table 51: TTX odd request vertical start register, subaddress 76h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVS[7:0]	R/W		with TTXOVS8 (see Table 57) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVS + 4) for M-systems and line = (TTXOVS + 1) for other systems
			05h*	if strapped to PAL
			06h*	if strapped to NTSC

Table 52: TTX odd request vertical end register, subaddress 77h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXOVE[7:0]	R/W		with TTXOVE8 (see Table 57) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field, line = (TTXOVE + 3) for M-systems and line = TTXOVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

Table 53: TTX even request vertical start register, subaddress 78h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVS[7:0]	R/W		with TTXEVS8 (see Table 57) first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVS + 4) for M-systems and line = (TTXEVS + 1) for other systems
			04h*	if strapped to PAL
			05h*	if strapped to NTSC

Table 54: TTX even request vertical end register, subaddress 79h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 0	TTXEVE[7:0]	R/W		with TTXEVE8 (see Table 57) last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field, line = (TTXEVE + 3) for M-systems and line = TTXEVE for other systems
			16h*	if strapped to PAL
			10h*	if strapped to NTSC

Table 55: First active line register, subaddress 7Ah, bit description

Bit	Symbol	Access	Value	Description
7 to 0	FAL[7:0]	R/W		with FAL8 (see Table 57) first active line = (FAL + 4) for M-systems and (FAL + 1) for other systems, measured in lines
			00h	coincides with the first field synchronization pulse

Table 56: Last active line register, subaddress 7Bh, bit description

Bit	Symbol	Access	Value	Description
7 to 0	LAL[7:0]	R/W		with LAL8 (see Table 57) last active line = (LAL + 3) for M-systems and LAL for other system, measured in lines
			00h	coincides with the first field synchronization pulse

Table 57: TTX mode, MSB vertical register, subaddress 7Ch, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	TTX60	R/W	0*	enables NABTS (FISE = 1) or European TTX (FISE = 0)
			1	enables world standard teletext 60 Hz (FISE = 1)
6	LAL8	R/W		see Table 56
5	TTXO	R/W		teletext protocol selected (see Figure 15)
			0*	new teletext protocol selected; at each rising edge of TTXRQ a single teletext bit is requested
			1	old teletext protocol selected; the encoder provides a window of TTXRQ going HIGH; the length of the window depends on the chosen teletext standard
4	FAL8	R/W		see Table 55
3	TTXEVE8	R/W		see Table 54
2	TTXOVE8	R/W		see Table 52
1	TTXEVS8	R/W		see Table 53
0	TTXOVS8	R/W		see Table 51

Table 58: Disable TTX line registers, subaddresses 7Eh and 7Fh, bit description [1]

Subaddress	Bit	Symbol	Access	Value	Description
7Eh	7 to 0	LINE[12:5]	R/W	-	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate)
7Fh	7 to 0	LINE[20:13]	R/W	-	

[1] This bit mask is effective only if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE.

Table 59: Pixel clock 0, 1 and 2 registers, subaddresses 81h to 83h, bit description

Subaddress	Bit	Symbol	Access	Value	Description
81h	7 to 0	PCL[07:00]	R/W		defines the frequency of the synthesized pixel clock PIXCLKO; $f_{PIXCLK} = \left(\frac{PCL}{2^{24}} \times f_{XTAL}\right) \times 8$; f_{XTAL} = 27 MHz nominal
82h	7 to 0	PCL[15:08]			
83h	7 to 0	PCL[23:16]			
				20 F63Bh	640 × 480 to NTSC M
				1B 5A73h	640 × 480 to PAL B/G (as by strapping pins)

Table 60: Pixel clock control register, subaddress 84h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	DCLK	R/W	0*	set to logic 1
			1	set to logic 1
6	PCLSY	R/W		pixel clock generator
			0*	runs free
			1	gets synchronized with the vertical sync
5	IFRA	R/W		input FIFO gets reset
			0	explicitly at falling edge
			1*	every field
4	IFBP	R/W		input FIFO
			0	active
			1*	bypassed
3 and 2	PCLE[1:0]	R/W		controls the divider for the external pixel clock
			00	divider ratio for PIXCLK output is 1
			01*	divider ratio for PIXCLK output is 2
			10	divider ratio for PIXCLK output is 4
			11	divider ratio for PIXCLK output is 8
1 and 0	PCLI[1:0]	R/W		controls the divider for the internal pixel clock
			00	divider ratio for internal PIXCLK is 1
			01*	divider ratio for internal PIXCLK is 2
			10	divider ratio for internal PIXCLK is 4
			11	not allowed

Table 61: FIFO control register, subaddress 85h, bit description

*Legend: * = default value after reset, ^ = nominal value.*

Bit	Symbol	Access	Value	Description
7	EIDIV	R/W	0*	DVO compliant signals are applied
			1	non-DVO compliant signals are applied
6 to 4	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	FILI[3:0]	R/W	8h*^	threshold for FIFO internal transfers

Table 62: Horizontal offset register, subaddress 90h, bit description

Bit	Symbol	Description
7 to 0	XOFS[7:0]	with XOFS[9:8] (see Table 66) horizontal offset; defines the number of PIXCLKs from horizontal sync (HSVGC) output to composite blanking ($\overline{CBO}$) output

Table 63: Pixel number register, subaddress 91h, bit description

Bit	Symbol	Description
7 to 0	XPIX[7:0]	with XPIX[9:8] (see Table 66) pixel in X direction; defines half the number of active pixels per input line (identical to the length of $\overline{CBO}$ pulses)

Table 64: Vertical offset odd register, subaddress 92h, bit description

Bit	Symbol	Description
7 to 0	YOFSO[7:0]	with YOFSO[9:8] (see Table 66) vertical offset in odd field; defines (in the odd field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSO + 2; usually, YOFSO = YOFSE with the exception of extreme vertical downscaling and interlacing

Table 65: Vertical offset even register, subaddress 93h, bit description

Bit	Symbol	Description
7 to 0	YOFSE[7:0]	with YOFSE[9:8] (see Table 66) vertical offset in even field; defines (in the even field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSE + 2; usually, YOFSE = YOFSO with the exception of extreme vertical downscaling and interlacing

Table 66: MSBs register, subaddress 94h, bit description

Bit	Symbol	Description
7 and 6	YOFSE[9:8]	see Table 65
5 and 4	YOFSO[9:8]	see Table 64
3 and 2	XPIX[9:8]	see Table 63
1 and 0	XOFS[9:8]	see Table 62

Table 67: Line number register, subaddress 95h, bit description

Bit	Symbol	Description
7 to 0	YPIX[7:0]	with YPIX[9:8] (see Table 68) defines the number of requested input lines from the feeding device; number of requested lines = YPIX + YOFSE – YOFSO

Table 68: Scaler CTRL, MCB and YPIX register, subaddress 96h, bit description

Bit	Symbol	Access	Value	Description
7	EFS	R/W		in Slave mode frame sync signal at pin FSVGC
			0	ignored
			1	accepted
6	PCBN	R/W		polarity of $\overline{CBO}$ signal
			0	normal (HIGH during active video)
			1	inverted (LOW during active video)
5	SLAVE	R/W		from the SAA7104E; SAA7105E the timing to the graphics controller is
			0	master
			1	slave
4	ILC	R/W		if hardware cursor insertion is active
			0	set LOW for non-interlaced input signals
			1	set HIGH for interlaced input signals
3	YFIL	R/W		luminance sharpness booster
			0	disabled
			1	enabled
2	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
1 and 0	YPIX[9:8]			see Table 67

Table 69: Sync control register, subaddress 97h, bit description

Bit	Symbol	Access	Value	Description
7	HFS	R/W		horizontal sync is derived from
			0	input signal (Save mode) at pin HSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
6	VFS	R/W		vertical sync (field sync) is derived from
			0	input signal (Slave mode) at pin VSVGC
			1	a frame sync signal (Slave mode) at pin FSVGC (only if EFS is set HIGH)
5	OFS	R/W		pin FSVGC is
			0	input
			1	active output
4	PFS	R/W		polarity of signal at pin FSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode
3	OVS	R/W		pin VSVGC is
			0	input
			1	active output

Table 69: Sync control register, subaddress 97h, bit description *...continued*

Bit	Symbol	Access	Value	Description
2	PVS	R/W		polarity of signal at pin VSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode
1	OHS	R/W		pin HSVGC is
			0	input
			1	active output
0	PHS	R/W		polarity of signal at pin HSVGC in output mode (Master mode) is
			0	active HIGH; rising edge of the input signal is used in Slave mode
			1	active LOW; falling edge of the input signal is used in Slave mode

Table 70: Line length register, subaddress 98h, bit description

Bit	Symbol	Description
7 to 0	HLEN[7:0]	with HLEN[11:8] (see Table 71) horizontal length; $\mathrm{HLEN} = \frac{\text{number of PIXCLKs}}{\text{line}} - 1$

Table 71: Input delay, MSB line length register, subaddress 99h, bit description

Bit	Symbol	Description
7 to 4	IDEL[3:0]	input delay; defines the distance in PIXCLKs between the active edge of $\overline{\text{CBO}}$ and the first received valid pixel
3 to 0	HLEN[11:8]	see Table 70

Table 72: Horizontal increment register, subaddress 9Ah, bit description

Bit	Symbol	Description
7 to 0	XINC[7:0]	with XINC[11:8] (see Table 74) incremental fraction of the horizontal scaling engine; $\mathrm{XINC} = \frac{\frac{\text{number of output pixels}}{\text{line}}}{\frac{\text{number of input pixels}}{\text{line}}} \times 4096$

Table 73: Vertical increment register, subaddress 9Bh, bit description

Bit	Symbol	Description
7 to 0	YINC[7:0]	with YINC[11:8] (see Table 74) incremental fraction of the vertical scaling engine; $\mathrm{YINC} = \frac{\text{number of active output lines}}{\text{number of active input lines}} \times 4096$

Table 74: MSBs vertical and horizontal increment register, subaddress 9Ch, bit description

Bit	Symbol	Description
7 to 4	YINC[11:8]	see Table 73
3 to 0	XINC[11:8]	see Table 72

Table 75: Weighting factor odd register, subaddress 9Dh, bit description

Bit	Symbol	Description
7 to 0	YIWGTO[7:0]	with YIWGTO[11:8] (see Table 77) weighting factor for the first line of the odd field; $YIWGTO = \frac{YINC}{2} + 2048$

Table 76: Weighting factor even, subaddress 9Eh, bit description

Bit	Symbol	Description
7 to 0	YIWGTE[7:0]	with YIWGTE[11:8] (see Table 77) weighting factor for the first line of the even field; $YIWGTE = \frac{YINC - YSKIP}{2}$

Table 77: Weighting factor MSB register, subaddress 9Fh, bit description

Bit	Symbol	Description
7 to 4	YIWGTE[11:8]	see Table 76
3 to 0	YIWGTO[11:8]	see Table 75

Table 78: Vertical line skip register, subaddress A0h, bit description

Bit	Symbol	Access	Value	Description
7 to 0	YSKIP[7:0]	R/W		with YSKIP[11:8] (see Table 79) vertical line skip; defines the effectiveness of the anti-flicker filter
			000h	most effective
			FFFh	anti-flicker filter switched off

Table 79: Blank enable for NI-bypass, vertical line skip MSB register, subaddress A1h, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7	BLEN	R/W		for non-interlaced graphics in bypass mode
			0*	no internal blanking
			1	forced internal blanking
6 to 4	-	R/W	000	must be programmed with logic 0 to ensure compatibility to future enhancements
3 to 0	YSKIP[11:8]	R/W		see Table 78

Table 80: Border color Y register, subaddress A2h, bit description

Bit	Symbol	Description
7 to 0	BCY[7:0]	luminance portion of border color in underscan area

Table 81: Border color U register, subaddress A3h, bit description

Bit	Symbol	Description
7 to 0	BCU[7:0]	color difference portion of border color in underscan area

Table 82: Border color V register, subaddress A4h, bit description

Bit	Symbol	Description
7 to 0	BCV[7:0]	color difference portion of border color in underscan area

Table 83: Subaddress D0h

Data byte	Description
HLCA	RAM start address for the HD sync line count array; the byte following subaddress D0 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line count array entry consists of 2 bytes; see Table 84. The array has 15 entries.
HLC	HD line counter. The system will repeat the pattern described in 'HLT' HLC times and then start with the next entry in line count array.
HLT	HD line type pointer. If not 0, the value points into the line type array, index HLT – 1 with the description of the current line. 0 means the entry is not used.

Table 84: Layout of the data bytes in the line count array

Byte	Description							
0	HLC7	HLC6	HLC5	HLC4	HLC3	HLC2	HLC1	HLC0
1	HLT3	HLT2	HLT1	HLT0	0	0	HLC9	HLC8

Table 85: Subaddress D1h

Data byte	Description
HLTA	RAM start address for the HD sync line type array; the byte following subaddress D1 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line type array entry consists of 4 bytes; see Table 86. The array has 15 entries.
HLP	HD line type; if not 0, the value points into the line pattern array. The index used is HLP – 1. It consists of value-duration pairs. Each entry consists of 8 pointers, used from index 0 to 7. The value 0 means that the entry is not used.

Table 86: Layout of the data bytes in the line type array

Byte	Description							
0	0	HLP12	HLP11	HLP10	0	HLP02	HLP01	HLP00
1	0	HLP32	HLP31	HLP30	0	HLP22	HLP21	HLP20
2	0	HLP52	HLP51	HLP50	0	HLP42	HLP41	HLP40
3	0	HLP72	HLP71	HLP70	0	HLP62	HLP61	HLP60

Table 87: Subaddress D2h

Data byte	Description
HLPA	RAM start address for the HD sync line pattern array; the byte following subaddress D2 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 4 value-duration pairs occupying 2 bytes; see Table 88. The array has 7 entries.
HPD	HD pattern duration. The value defines the time in pixel clocks (HPD + 1) the corresponding value HPV is added to the HD output signal. If 0, this entry will be skipped.
HPV	HD pattern value pointer. This gives the index in the HD value array containing the level to be inserted into the HD output path. If the MSB of HPV is logic 1, the value will only be inserted into the Y/GREEN channel of the HD data path, the other channels remain unchanged.

Table 88: Layout of the data bytes in the line pattern array

Byte	Description							
0	HPD07	HPD06	HPD05	HPD04	HPD03	HPD02	HPD01	HPD00
1	HPV03	HPV02	HPV01	HPV00	0	0	HPD09	HPD08
2	HPD17	HPD16	HPD14	HPD14	HPD13	HPD12	HPD11	HPD10
3	HPV13	HPV12	HPV11	HPV10	0	0	HPD19	HPD18
4	HPD27	HPD26	HPD25	HPD24	HPD23	HPD22	HPD21	HPD20
5	HPV23	HPV22	HPV21	HPV20	0	0	HPD29	HPD28
6	HPD37	HPD36	HPD35	HPD34	HPD33	HPD32	HPD31	HPD30
7	HPV33	HPV32	HPV31	HPV30	0	0	HPD39	HPD38

Table 89: Subaddress D3h

Data byte	Description
HPVA	RAM start address for the HD sync value array; the byte following subaddress D3 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 2 bytes. The array has 8 entries.
HPVE	HD pattern value entry. The HD path will insert a level of (HPV + 52) $\times$ 0.66 IRE into the data path. The value is signed 8-bits wide; see Table 90.
HHS	HD horizontal sync. If the HD engine is active, this value will be provided at pin HSM_CSYNC; see Table 90.
HVS	HD vertical sync. If the HD engine is active, this value will be provided at pin VSM; see Table 90.

Table 90: Layout of the data bytes in the value array

Byte	Description							
0	HPVE7	HPVE6	HPVE5	HPVE4	HPVE3	HPVE2	HPVE1	HPVE0
1	0	0	0	0	0	0	HVS	HHS

Table 91: HD sync trigger state 1 register, subaddress D4h, bit description

Bit	Symbol	Description
7 to 0	HLCT[7:0]	with HLCT[9:8] (see Table 92) state of the HD line counter after trigger (counts backwards)

Table 92: HD sync trigger state 2 register, subaddress D5h, bit description

Bit	Symbol	Description
7 to 4	HLCPT[3:0]	state of the HD line type pointer after trigger
3 and 2	HLPPT[1:0]	state of the HD pattern pointer after trigger
1 and 0	HLCT[9:8]	see Table 91

Table 93: HD sync trigger state 3 register, subaddress D6h, bit description

Bit	Symbol	Description
7 to 0	HDCT[7:0]	with HDCT[9:8] (see Table 94) state of the HD duration counter after trigger (counts backwards)

Table 94: HD sync trigger state 4 register, subaddress D7h, bit description

Bit	Symbol	Description
7	-	must be programmed with logic 0 to ensure compatibility to future enhancements
6 to 4	HEPT[2:0]	state of the HD event type pointer in the line type array after trigger
3 and 2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
1 and 0	HDCT[9:8]	see Table 93

Table 95: HD sync trigger phase x registers, subaddresses D8h and D9h, bit description

Subaddress	Bit	Symbol	Description
D9h	7 to 4	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	3 to 0	HTX[11:8]	horizontal trigger phase for the HD sync engine in pixel clocks
D8h	7 to 0	HTX[7:0]	

Table 96: HD sync trigger phase y registers, subaddresses DAh and DBh, bit description

Subaddress	Bit	Symbol	Description
DBh	7 to 2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	1 and 0	HTY[9:8]	vertical trigger phase for the HD sync engine in input lines
DAh	7 to 0	HTY[7:0]	

Table 97: HD output control register, subaddress DCh, bit description

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	0	must be programmed with logic 0 to ensure compatibility to future enhancements
3	HDSYE	R/W		HD sync engine
			0*	off
			1	active
2	HDTC	R/W		HD output path processes
			0*	RGB
			1	YUV

Table 97: HD output control register, subaddress DCh, bit description *...continued*

*Legend: * = default value after reset.*

Bit	Symbol	Access	Value	Description
1	HDGY	R/W	0*	gain in the HD output path is reduced, insertion of sync pulses is possible
			1	full level swing at the input causes full level swing at the DACs in HD mode
0	HDIP	R/W		interpolator for the color difference signal in the HD output path
			0*	active
			1	off

Table 98: Cursor color 1 R, G and B registers, subaddresses F0h to F2h, bit description

Subaddress	Bit	Symbol	Description
F0h	7 to 0	CC1R[7:0]	RED portion of first cursor color
F1h	7 to 0	CC1G[7:0]	GREEN portion of first cursor color
F2h	7 to 0	CC1B[7:0]	BLUE portion of first cursor color

Table 99: Cursor color 2 R, G and B registers, subaddresses F3h to F5h, bit description

Subaddress	Bit	Symbol	Description
F3h	7 to 0	CC2R[7:0]	RED portion of second cursor color
F4h	7 to 0	CC2G[7:0]	GREEN portion of second cursor color
F5h	7 to 0	CC2B[7:0]	BLUE portion of second cursor color

Table 100: Auxiliary cursor color R, G and B registers, subaddresses F6h to F8h, bit description

Subaddress	Bit	Symbol	Description
F6h	7 to 0	AUXR[7:0]	RED portion of auxiliary cursor color
F7h	7 to 0	AUXG[7:0]	GREEN portion of auxiliary cursor color
F8h	7 to 0	AUXB[7:0]	BLUE portion of auxiliary cursor color

Table 101: Horizontal cursor position and horizontal hot spot, MSB XCP registers, subaddresses F9h and FAh, bit description

Subaddress	Bit	Symbol	Description
FAh	7 to 3	XHS[4:0]	horizontal hot spot of cursor
	2 to 0	XCP[10:8]	horizontal cursor position
F9h	7 to 0	XCP[7:0]	

Table 102: Vertical cursor position and vertical hot spot, MSB YCP registers, subaddresses FBh and FCh, bit description

Subaddress	Bit	Symbol	Description
FCh	7 to 3	YHS[4:0]	vertical hot spot of cursor
	2	-	must be programmed with logic 0 to ensure compatibility to future enhancements
	1 and 0	YCP[9:8]	vertical cursor position
FBh	7 to 0	YCP[7:0]	

Table 103: Input path control register, subaddress FDh, bit description

Bit	Symbol	Access	Value	Description
7	LUTOFF	R/W		color look-up table
			0	active
			1	bypassed
6	CMODE	R/W		cursor mode
			0	cursor mode; input color will be inverted
			1	auxiliary cursor color will be inserted
5	LUTL	R/W		LUT loading via input data stream
			0	inactive
			1	color and cursor LUTs are loaded
4 to 2	IF[2:0]	R/W		input format
			000	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R
			001	5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB
			010	5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB
			011	8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R
			100	8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock) (in subaddresses 91h and 94h set XPIX = number of active pixels/line)
			101	8-bit non-interlaced index color
			110	8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R (special bit ordering)
1	MATOFF	R/W		RGB to C_R-Y-C_B matrix
			0	active
			1	bypassed
0	DFOFF	R/W		down formatter
			0	(4 : 4 : 4 to 4 : 2 : 2) in input path is active
			1	bypassed

Table 104: Cursor bit map register, subaddress FEh, bit description

Data byte	Description
CURSA	RAM start address for cursor bit map; the byte following subaddress FEh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

Table 105: Color look-up table register, subaddress FFh, bit description

Data byte	Description
COLSA	RAM start address for color LUT; the byte following subaddress FFh points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

In subaddresses 5Bh, 5Ch, 5Dh, 5Eh, 62h and D3h all IRE values are rounded up.

8.4 Slave transmitter

Table 106: Status byte register, subaddress 00h, bit description

Bit	Symbol	Access	Value	Description
7 to 5	VER[2:0]	R	101	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 101 binary
4	CCRDO	R	1	set immediately after the closed caption bytes of the odd field have been encoded
			0	reset after information has been written to the subaddresses 67h and 68h
3	CCRDE	R	1	set immediately after the closed caption bytes of the even field have been encoded
			0	reset after information has been written to the subaddresses 69h and 6Ah
2	-	R	0	-
1	FSEQ	R	1	during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields)
			0	not first field of a sequence
0	O_E	R	1	during even field
			0	during odd field

Table 107: Slave transmitter (slave address 89h)

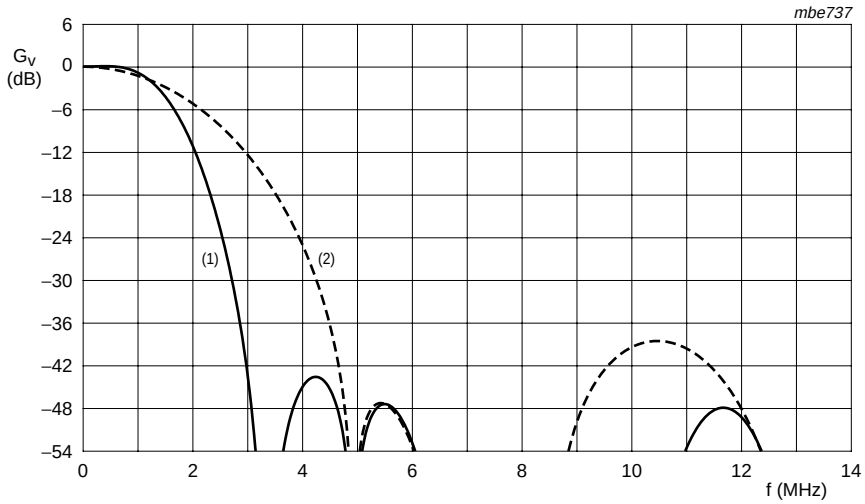
Register function	Subaddress	Data byte							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	00h	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Chip ID	1Ch	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
FIFO status	80h	0	0	0	0	0	0	OVFL	UDFL

Table 108: Chip ID register, subaddress 1Ch, bit description

Bit	Symbol	Access	Value	Description
7 to 0	CID[7:0]	R		chip ID
			04h	SAA7104E
			05h	SAA7105E

Table 109: FIFO status register, subaddress 80h, bit description

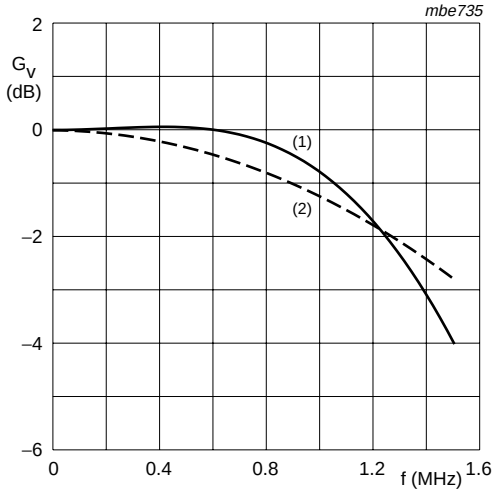
Bit	Symbol	Access	Value	Description
7 to 4	-	R	0h	-
3	IFERR	R	0	normal FIFO state
			1	input FIFO overflow/underflow has occurred
2	BFERR	R	0	normal FIFO state
			1	buffer FIFO overflow, only if YUPSC = 1
1	OVFL	R	0	no FIFO overflow
			1	FIFO overflow has occurred; this bit is reset after this subaddress has been read
0	UDFL	R	0	no FIFO underflow
			1	FIFO underflow has occurred; this bit is reset after this subaddress has been read



(1) SCBW = 1.

(2) SCBW = 0.

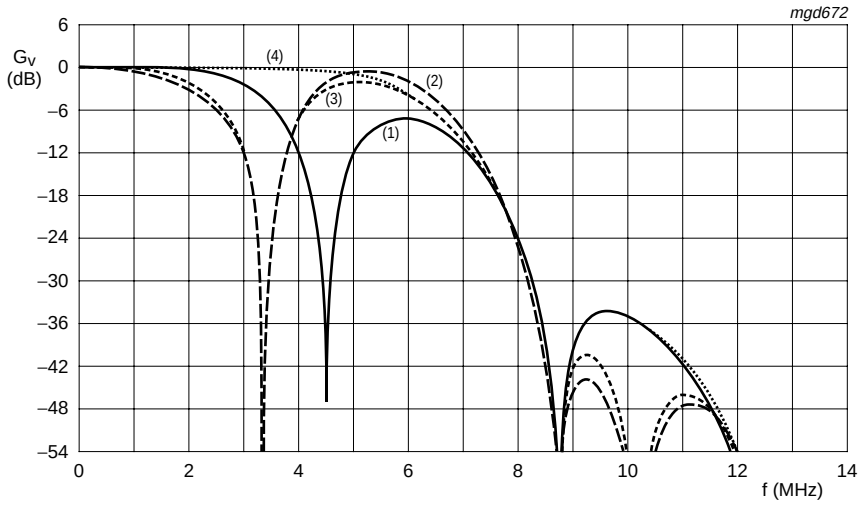
Fig 6. Chrominance transfer characteristic 1



(1) SCBW = 1.

(2) SCBW = 0.

Fig 7. Chrominance transfer characteristic 2



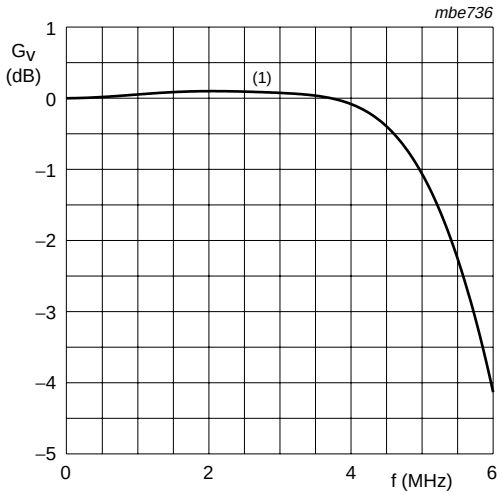
(1) CCRS[1:0] = 01.

(2) CCRS[1:0] = 10.

(3) CCRS[1:0] = 11.

(4) CCRS[1:0] = 00.

Fig 8. Luminance transfer characteristic 1 (excluding scaler)



(1) CCRS[1:0] = 00

Fig 9. Luminance transfer characteristic 2 (excluding scaler)

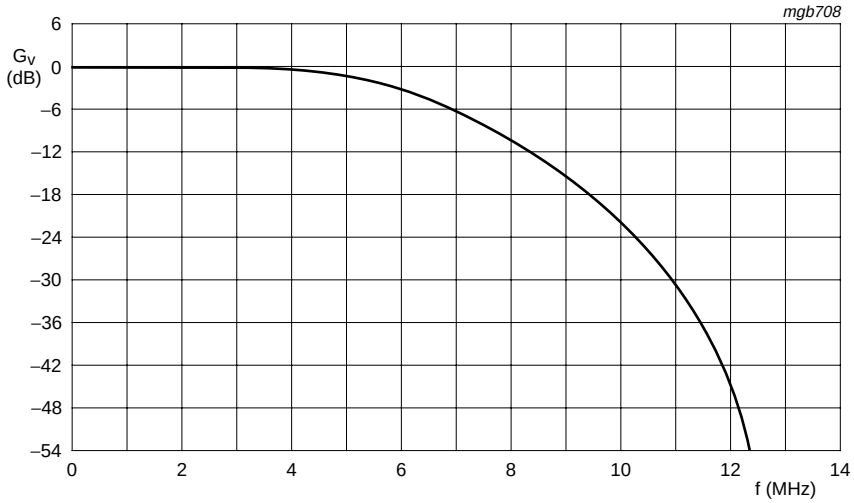


Fig 10. Luminance transfer characteristic in RGB (excluding scaler)

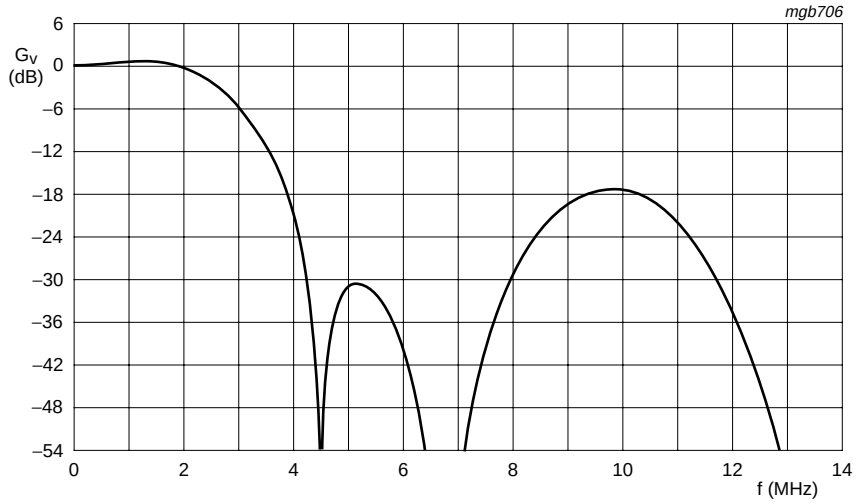


Fig 11. Color difference transfer characteristic in RGB (excluding scaler)

9. Limiting values

Table 110: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All ground pins connected together and grounded (0 V); all supply pins connected together.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDD}	digital supply voltage			–0.5	+4.6	V
V_{DDA}	analog supply voltage			–0.5	+4.6	V
$V_{i(A)}$	input voltage at analog inputs			–0.5	+4.6	V
$V_{i(n)}$	input voltage at pins XTALI, SDA and SCL			–0.5	V_{DDD} + 0.5	V
$V_{i(D)}$	input voltage at digital inputs or I/O pins	outputs in 3-state		–0.5	+4.6	V
		outputs in 3-state	[1]	–0.5	+5.5	V
ΔV_{SS}	voltage difference between $V_{SSA(n)}$ and $V_{SSD(n)}$			-	100	mV
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			0	70	°C
V_{esd}	electrostatic discharge voltage	human body model	[2]	-	±2000	V
		machine model	[3]	-	±200	V

[1] Condition for maximum voltage at digital inputs or I/O pins: 3.0 V < V_{DDD} < 3.6 V.

[2] Class 2 according to JESD22-A114-B.

[3] Class B according to EIA/JESD22-A115-A.

10. Thermal characteristics

Table 111: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	38 [1]	K/W

[1] The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area directly under the SAA7104E; SAA7105E with a number of through-hole plating, connected to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

11. Characteristics

Table 112: Characteristics

T_{amb} = 0 °C to 70 °C (typical values excluded); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DDA}	analog supply voltage			3.15	3.3	3.45	V
V_{DDD2}	digital supply voltage			3.15	3.3	3.45	V
V_{DDD3}	digital supply voltage			3.15	3.3	3.45	V
V_{DDD4}	digital supply voltage			3.15	3.3	3.45	V
V_{DDD1}	digital supply voltage (DVO)			1.045	1.1	1.155	V
				1.425	1.5	1.575	V
				1.71	1.8	1.89	V
				2.375	2.5	2.625	V
				3.135	3.3	3.465	V
I_{DDA}	analog supply current		[1]	1	110	115	mA
I_{DDD}	digital supply current		[2]	1	175	200	mA
Inputs							
V_{IL}	LOW-level input voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	−0.1	-	+0.2	V
		V_{DDD1} = 3.3 V	[3]	−0.5	-	+0.8	V
		pins $\overline{\text{RESET}}$, TMS, TCK, $\overline{\text{TRST}}$ and TDI		−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	V_{DDD1} − 0.2	-	V_{DDD1} + 0.1	V
		V_{DDD1} = 3.3 V	[3]	2	-	V_{DDD1} + 0.3	V
		pins $\overline{\text{RESET}}$, TMS, TCK, $\overline{\text{TRST}}$ and TDI		2	-	V_{DDD2} + 0.3	V
I_{LI}	input leakage current			-	-	10	µA
C_i	input capacitance	clocks		-	-	10	pF
		data		-	-	10	pF
		I/Os at high-impedance		-	-	10	pF

Table 112: Characteristics…*continued*

T_{amb} = 0 °C to 70 °C (typical values excluded); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Outputs							
V_{OL}	LOW-level output voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	0	-	0.1	V
		V_{DDD1} = 3.3 V	[3]	0	-	0.4	V
		pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC		0	-	0.4	V
V_{OH}	HIGH-level output voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V	[3]	V_{DDD1} – 0.1	-	V_{DDD1}	V
		V_{DDD1} = 3.3 V	[3]	2.4	-	V_{DDD1}	V
		pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC		2.4	-	V_{DDD2}	V
I^2C-bus; pins SDA and SCL							
V_{IL}	LOW-level input voltage			–0.5	-	$0.3V_{DDD2}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DDD2}$	-	V_{DDD2} + 0.3	V
I_i	input current	V_i = LOW or HIGH		–10	-	+10	µA
V_{OL}	LOW-level output voltage (pin SDA)	I_{OL} = 3 mA		-	-	0.4	V
I_o	output current	during acknowledge		3	-	-	mA
Clock timing; pins PIXCLKI and PIXCLKO							
T_{PIXCLK}	cycle time		[4]	12	-	-	ns
$t_{d(CLKD)}$	delay from PIXCLKO to PIXCLKI		[5]	-	-	-	ns
δ	duty factor	t_{HIGH}/T_{PIXCLK}	[4]	40	50	60	%
		t_{HIGH}/T_{CLKO2}; output		40	50	60	%
t_r	rise time		[4]	-	-	1.5	ns
t_f	fall time		[4]	-	-	1.5	ns
Input timing							
$t_{SU;DAT}$	input data set-up time	pins PD11 to PD0		2	-	-	ns
		pins HSVGC, VSVGC and FSVGC	[6]	2	-	-	ns
$t_{HD;DAT}$	input data hold time	pins PD11 to PD0		0.9	-	-	ns
		pins HSVGC, VSVGC and FSVGC	[6]	1.5	-	-	ns
Crystal oscillator							
f_{nom}	nominal frequency			-	27	-	MHz
$\Delta f/f_{nom}$	permissible deviation of nominal frequency		[7]	-50×10^{-6}	-	$+50 \times 10^{-6}$	
Crystal specification							
T_{amb}	ambient temperature			0	-	70	°C
C_L	load capacitance			8	-	-	pF
R_S	series resistance			-	-	80	Ω
C_1	motional capacitance (typical)			1.2	1.5	1.8	fF
C_0	parallel capacitance (typical)			2.8	3.5	4.2	pF

Table 112: Characteristics…*continued*

T_{amb} = 0 °C to 70 °C (typical values excluded); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Data and reference signal output timing						
$C_{o(L)}$	output load capacitance		8	-	40	pF
$t_{o(h)(gfx)}$	output hold time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$	1.5	-	-	ns
$t_{o(d)(gfx)}$	output delay time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$	-	-	10	ns
$t_{o(h)}$	output hold time	pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	3	-	-	ns
$t_{o(d)}$	output delay time	pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	-	-	25	ns
CVBS and RGB outputs						
$V_{o(CVBS)(p-p)}$	output voltage CVBS (peak-to-peak value)	see Table 113	-	1.23	-	V
$V_{o(VBS)(p-p)}$	output voltage VBS (S-video) (peak-to-peak value)	see Table 113	-	1	-	V
$V_{o(C)(p-p)}$	output voltage C (S-video) (peak-to-peak value)	see Table 113	-	0.89	-	V
$V_{o(RGB)(p-p)}$	output voltage R, G, B (peak-to-peak value)	see Table 113	-	0.7	-	V
ΔV_o	inequality of output signal voltages		-	2	-	%
$R_{o(L)}$	output load resistance		-	37.5	-	Ω
B_{DAC}	output signal bandwidth of DACs	–3 dB [8]	-	170	-	MHz
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs		-	-	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs		-	-	±1	LSB

[1] Minimum value for I^2C-bus bit DOWNA = 1.

[2] Minimum value for I^2C-bus bit DOWND = 1.

[3] Levels refer to pins PD11 to PD0, FSVGC, PIXCLKI, VSVGC, PIXCLKO, $\overline{CBO}$, TVD, and HSVGC, being inputs or outputs directly connected to a graphics controller. Input sensitivity is $\frac{1}{2}V_{DDD2}$ + 100 mV for HIGH and $\frac{1}{2}V_{DDD2}$ – 100 mV for LOW. The reference voltage $\frac{1}{2}V_{DDD2}$ is generated on chip.

[4] The data is for both input and output direction.

[5] This parameter is arbitrary, if PIXCLKI is looped through the VGC.

[6] Tested with programming IFBP = 1.

[7] If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.

[8] $B_{-3\,dB} = \frac{1}{2\pi R_L (C_{ext} + 5\,pF)}$ with R_L = 37.5 Ω and C_{ext} = 20 pF (typical).

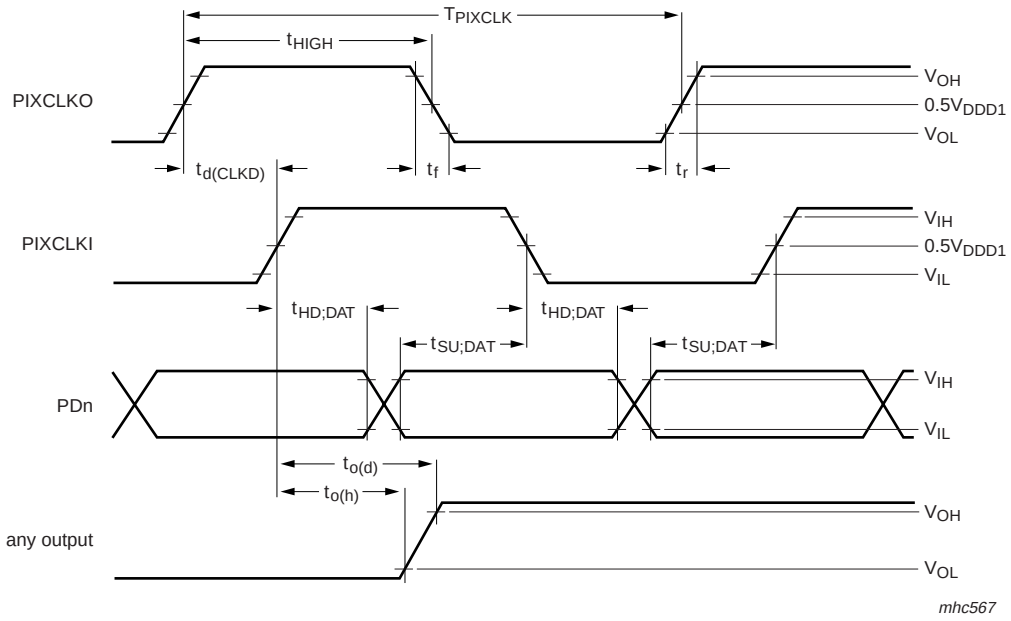


Fig 12. Input/output timing specification

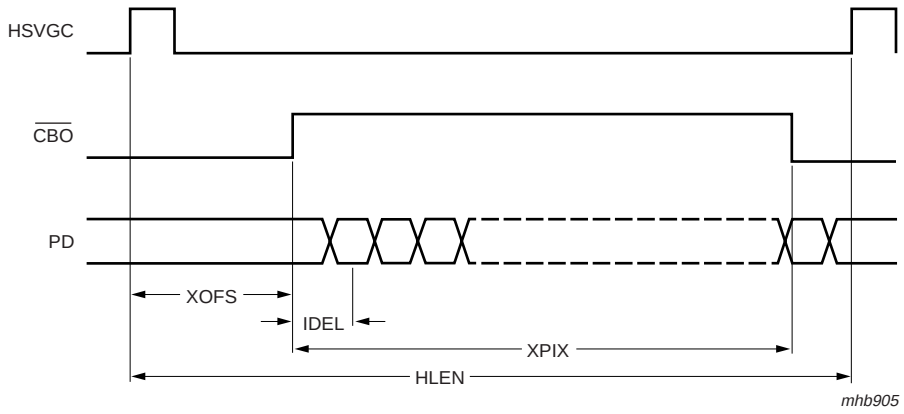


Fig 13. Horizontal input timing

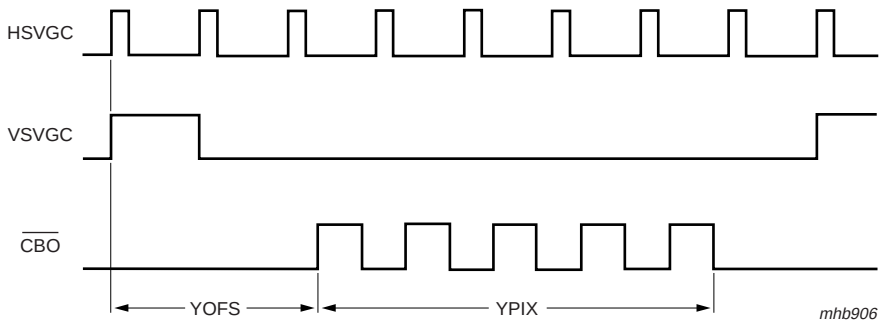


Fig 14. Vertical input timing

11.1 Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ_XCLKO2 in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ_XCLKO2, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of the outgoing horizontal synchronization pulse.

Time $t_{i(TTXW)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbit/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbit/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbit/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

It is essential to note that the two pins used for teletext insertion must be configured for this purpose by the correct I²C-bus register settings.

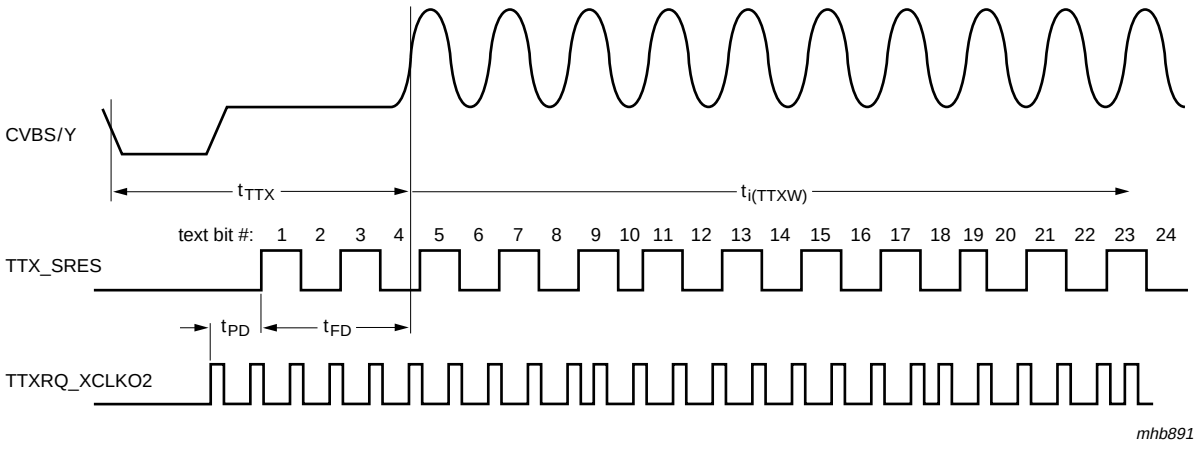


Fig 15. Teletext timing

12. Application information

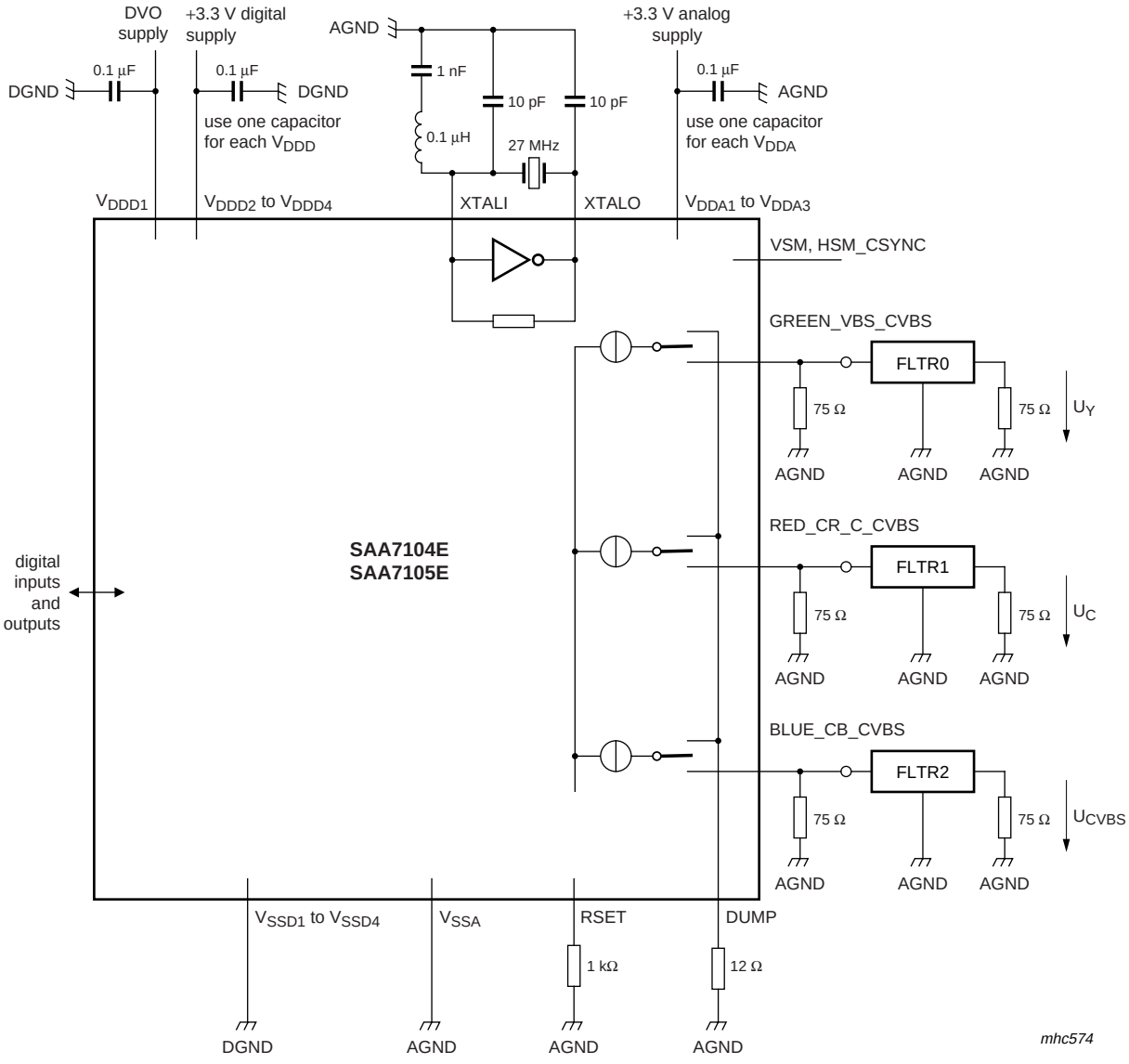


Fig 16. Application circuit

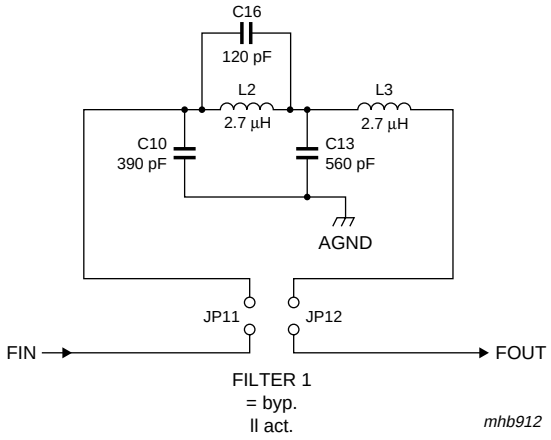
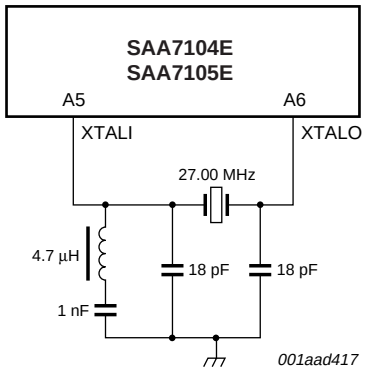
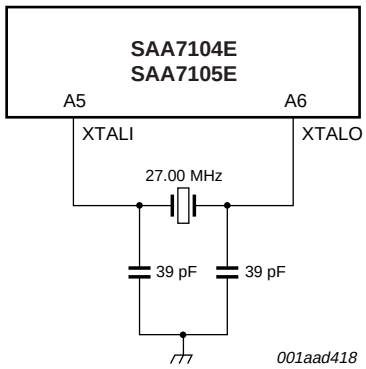


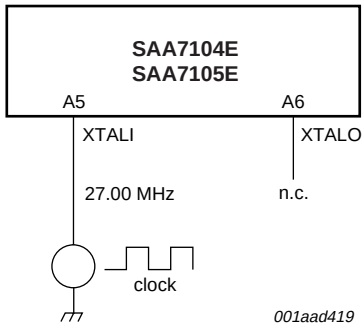
Fig 17. FLTR0, FLTR1 and FLTR2 of Figure 16



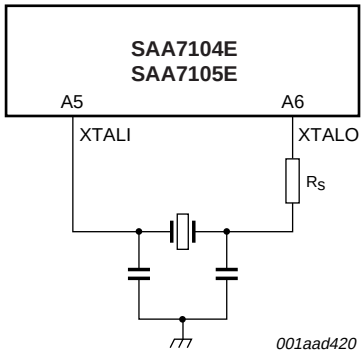
a. With 3rd harmonic quartz. Crystal load = 8 pF.



b. With fundamental quartz. Crystal load = 20 pF.



c. With direct clock.



d. With fundamental quartz and restricted drive level. When P_{drive} of the internal oscillator is too high, a resistance R_s can be placed in series with the oscillator output XTALO.

Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig 18. Oscillator application

12.1 Reconstruction filter

Figure 17 shows a possible reconstruction filter for the digital-to-analog converters. Due to its cut-off frequency of ~6 MHz, it is not suitable for HDTV applications.

12.2 Analog output voltages

The analog output voltages are dependent on the total load (typical value 37.5 Ω), the digital gain parameters and the I²C-bus settings of the DAC reference currents (analog settings).

The digital output signals in front of the DACs under nominal (nominal here stands for the settings given in Table 37 to Table 41 for example a standard PAL or NTSC signal) conditions occupy different conversion ranges, as indicated in Table 113 for a $^{100}/_{100}$ color bar signal.

By setting the reference currents of the DACs as shown in Table 113, standard compliant amplitudes can be achieved for all signal combinations; it is assumed that in subaddress 16h, parameter DACF = 0000b, that means the fine adjustment for all DACs in common is set to 0 %.

If S-video output is desired, the adjustment for the C (chrominance subcarrier) output should be identical to the one for VBS (luminance plus sync) output.

Table 113: Digital output signals conversion range

Set/out	CVBS, sync tip-to-white	VBS, sync tip-to-white	RGB, black-to-white
Digital settings	see Table 37 to Table 41	see Table 37 to Table 41	see Table 31 and Table 32
Digital output	1014	881	876
Analog settings	e.g. B DAC = 1Fh	e.g. G DAC = 1Bh	e.g. R DAC = G DAC = B DAC = 0Bh
Analog output	1.23 V (p-p)	1.00 V (p-p)	0.70 V (p-p)

12.3 Suggestions for a board layout

Use separate ground planes for analog and digital ground. Connect these planes only at one point directly under the device, by using a 0 Ω resistor directly at the supply stage. Use separate supply lines for the analog and digital supply. Place the supply decoupling capacitors close to the supply pins.

Use L_{bead} (ferrite coil) in each digital supply line close to the decoupling capacitors to minimize radiation energy (EMC).

Place the analog coupling (clamp) capacitors close to the analog input pins. Place the analog termination resistors close to the coupling capacitors.

Be careful of hidden layout capacitors around the crystal application.

Use serial resistors in clock, sync and data lines, to avoid clock or data reflection effects and to soften data energy.

13. Test information

13.1 Boundary scan test

The SAA7104E; SAA7105E has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7104E; SAA7105E follows the *'IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture'* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset ($\overline{\text{TRST}}$), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 114. Details about the JTAG BST-TEST can be found in the specification *'IEEE Std. 1149.1'*. A file containing the detailed Boundary Scan Description Language (BSDL) of the SAA7104E; SAA7105E is available on request.

Table 114: BST instructions supported by the SAA7104E; SAA7105E

Instruction	Description
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.

13.1.1 Initialization of boundary scan circuit

The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

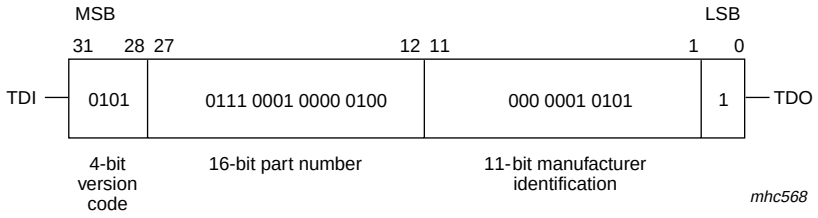
To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the $\overline{\text{TRST}}$ pin LOW.

13.1.2 Device identification codes

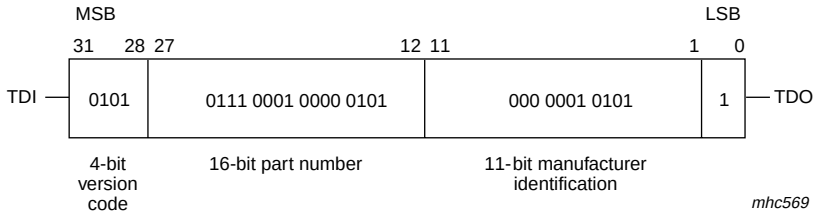
A device identification register is specified in *'IEEE Std. 1149.1b-1994'*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and to determine the version number of the ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between pins TDI and TDO of the IC. The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller, this code can subsequently be shifted out. At board level this code can be

used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Figure 19.



a. SAA7104E.

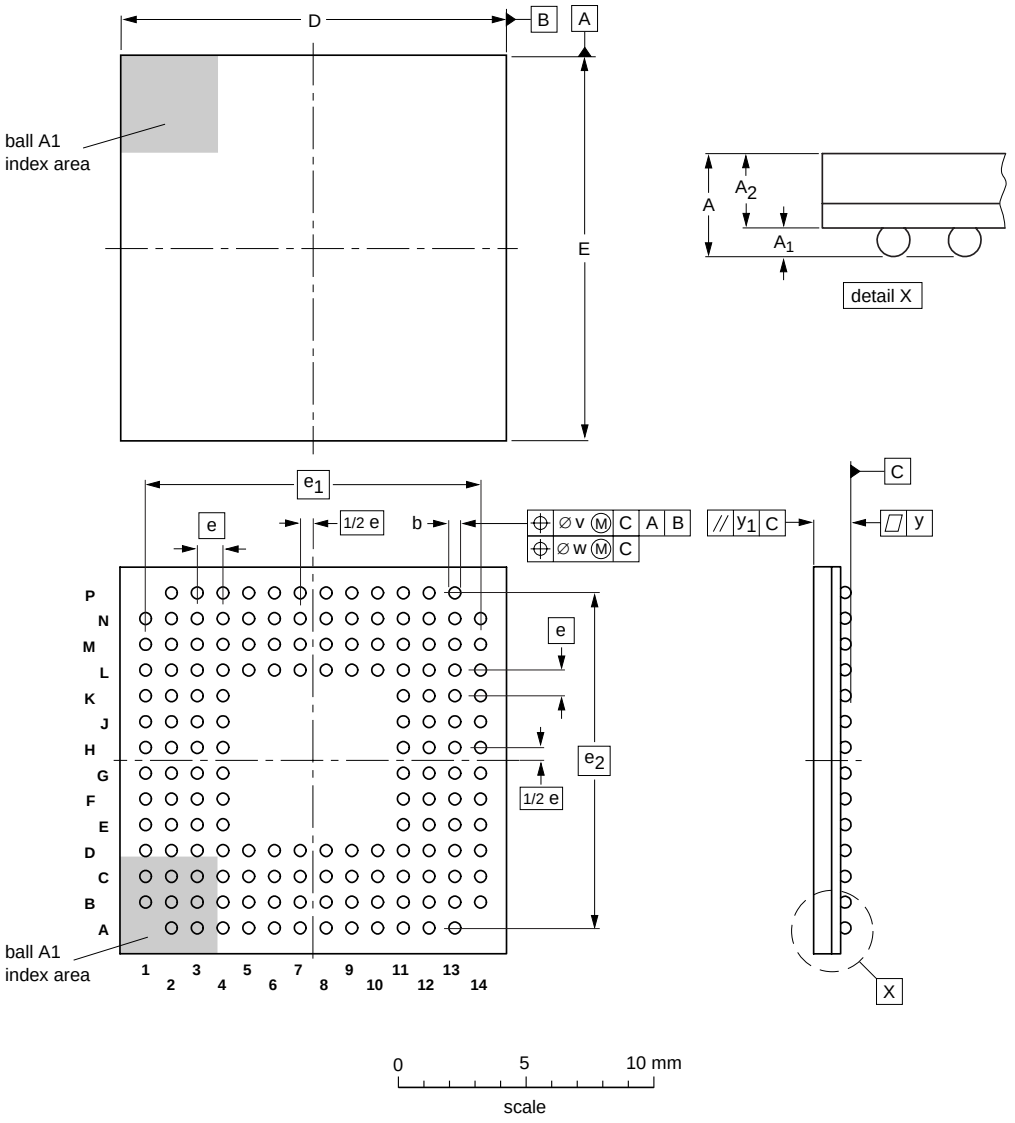


b. SAA7105E.

Fig 19. 32 bits of identification code

14. Package outline

LBGA156: plastic low profile ball grid array package; 156 balls; body 15 x 15 x 1.05 mm **SOT700-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.65	0.45 0.35	1.20 0.95	0.55 0.45	15.2 14.8	15.2 14.8	1	13	13	0.25	0.1	0.12	0.35

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT700-1	- - -	MO-192	- - -			~~01-05-11~~ 01-11-06

Fig 20. Package outline SOT700-1 (LBGA156)

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 115: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Revision history

Table 116: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
SAA7104E_SAA7105E_2	20051223	Product data sheet	CPCN 200505019	-	SAA7104E_SAA7105E_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 4: updated description for pin E2 • Package outline changed from SOT472-1 to SOT700-1				
SAA7104E_SAA7105E_1	20040304	Product specification	-	9397 750 11436	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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