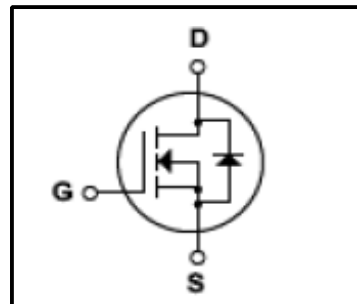
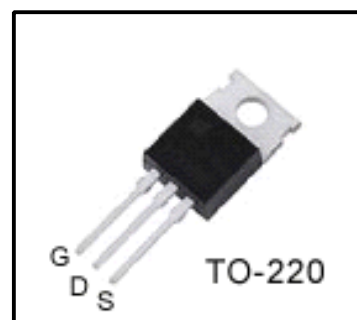


Silicon N-Channel MOSFET
Features

- 9A,500V, $R_{DS(on)}$ (Max0.85 Ω)@ $V_{GS}=10V$
- Ultra-low Gate charge(Typical 30nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 $^{\circ}C$)


General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe,DMOS technology.This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics .This devices is specially well suited for high efficiency switch model power supplies, power factor correction and half bridge and full bridge resonant topology line a electronic lamp ballast.


Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	500	V
I_D	Continuous Drain Current(@ $T_c=25^{\circ}C$)	9	A
	Continuous Drain Current(@ $T_c=100^{\circ}C$)	5.1	A
I_{DM}	Drain Current Pulsed (Note1)	32	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	510	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	13	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	3.5	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^{\circ}C$)	125	W
	Derating Factor above 25 $^{\circ}C$	1.0	W/ $^{\circ}C$
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^{\circ}C$
T_L	Channel Temperature	300	$^{\circ}C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	1	$^{\circ}C/W$
R_{QCS}	Thermal Resistance , Case-to-Sink	-	0.5	-	$^{\circ}C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	62	$^{\circ}C/W$

Electrical Characteristics(Tc=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±30V,V _{DS} =0V	-	-	±100	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G =±10 μA,V _{DS} =0V	±30	-	-	V	
Drain cut -off current	I _{DSS}	V _{DS} =400V,V _{GS} =0V	-	-	1	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =250 μA,V _{GS} =0V	500	-	-	V	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V,I _D =250 μA	2	-	4	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V,I _D =4.8A	-		0.85	Ω	
Forward Transconductance	g _{fs}	V _{DS} =50V,I _D =4.8A	3.7			S	
Input capacitance	C _{iss}	V _{DS} =25V,	-	1018	-	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} =0V,	-	155	-		
Output capacitance	C _{oss}	f=1MHz	-	8	-		
Switching time	Rise time	t _r	V _{DD} =250V,	-	11	-	ns
	Turn-on time	t _{on}	I _D =9A	-	23	-	
	Fall time	t _f	R _G =9.1Ω	-	26	-	
	Turn-off time	t _{off}	R _D =31Ω (Note4,5)	-	19	-	
Total gate charge(gate-source plus gate-drain)	Q _g	V _{DD} =400V, V _{GS} =10V,	-	30	38	nC	
Gate-source charge	Q _{gs}	I _D =9A	-	7	9		
Gate-drain("miller") Charge	Q _{gd}	(Note4,5)	-	15	18		

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	9	A
Pulse drain reverse current	I _{DRP}	-	-	-	32	A
Forward voltage(diode)	V _{DSF}	I _{DR} =9A,V _{GS} =0V	-	1.4	2.0	V
Reverse recovery time	t _{rr}	I _{DR} =9A,V _{GS} =0V,	-	442	633	ns
Reverse recovery charge	Q _{rr}	dI _{DR} / dt =100 A / μs	-	2.16	3.24	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=18.5mH I_{AS}=9A,V_{DD}=50V,R_G=0Ω,Starting T_J=25°C

3.I_{SD}≤9A,di/dt≤300A/us,V_{DD}<BV_{DSS},STARTING T_J=25°C

4.Pulse Test:Pulse Widths≤300us,Duty Cycle≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

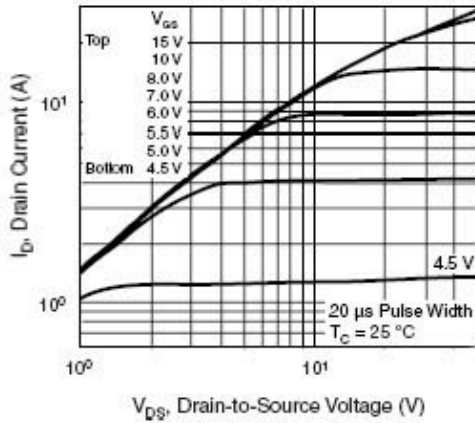


Fig.1 On State Characteristics

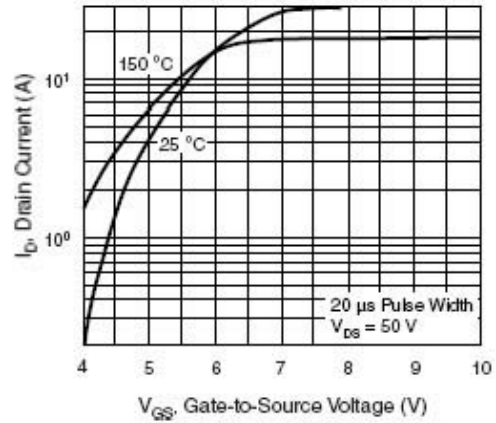


Fig.2 Transfer Characteristics

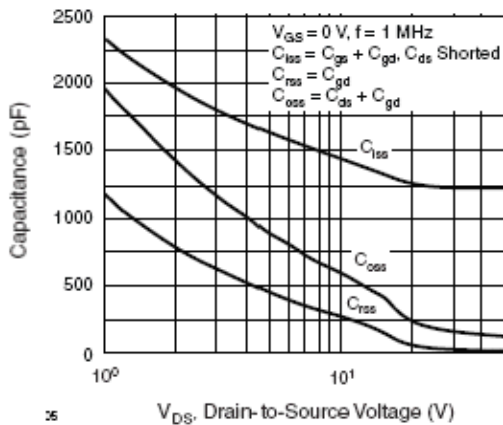


Fig.3 Capacitance Variation vs Drain Voltage

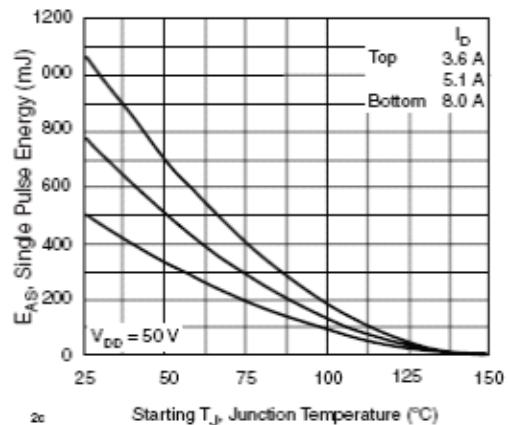


Fig.4 Maximum Avalanche Energy vs On-State Current

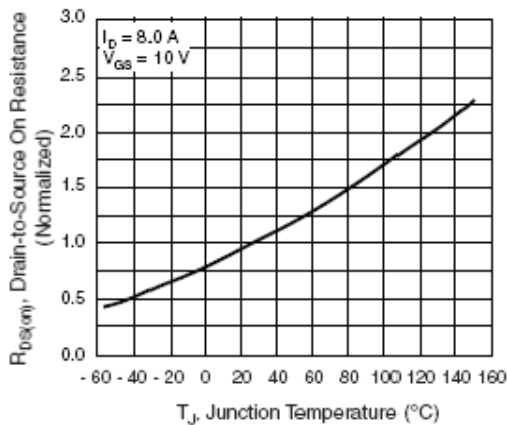


Fig.5 On-Resistance Variation vs Junction temperature

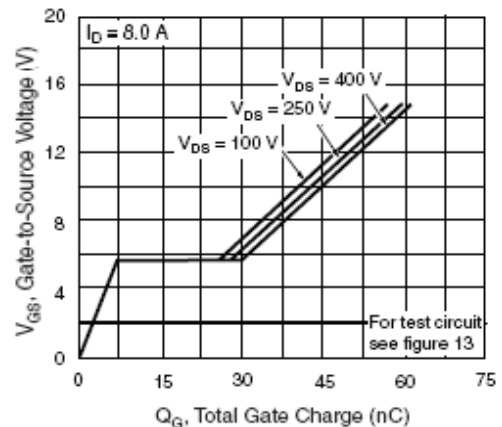


Fig.6 Gate Charge Characteristics

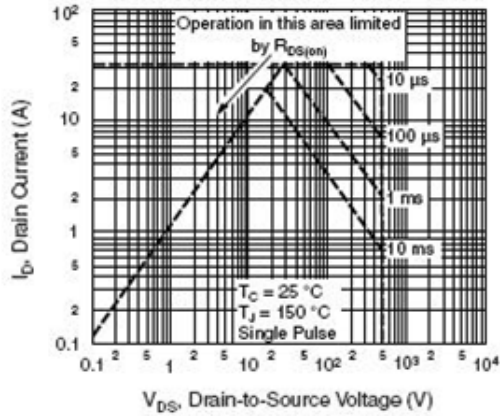


Fig.7 Maximum Safe Operation Area

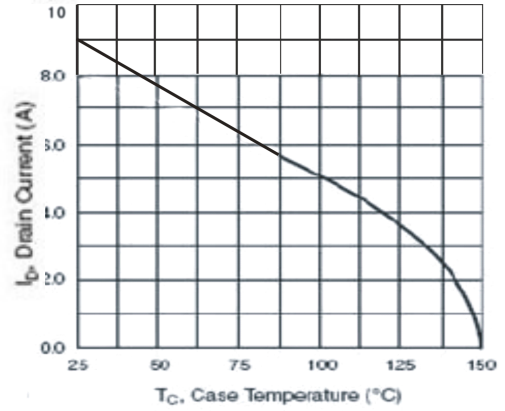


Fig.8 Maximum Drain Current vs Case temperature

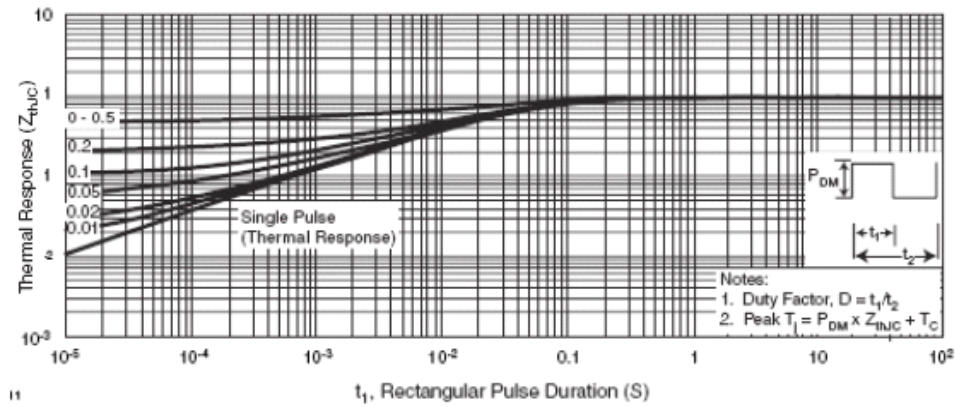


Fig.9 Transient thermal Response Curve

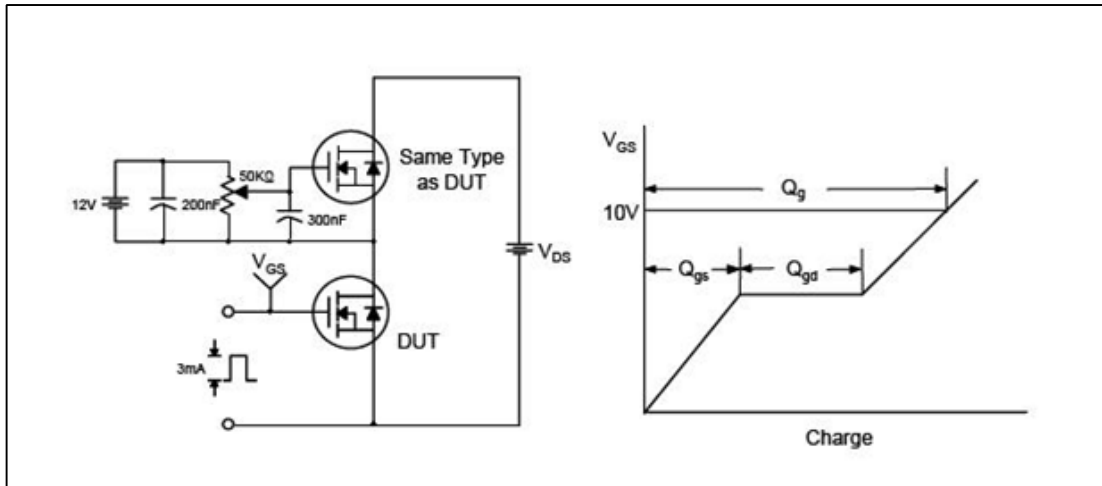


Fig.10 Gate Test circuit & Waveform

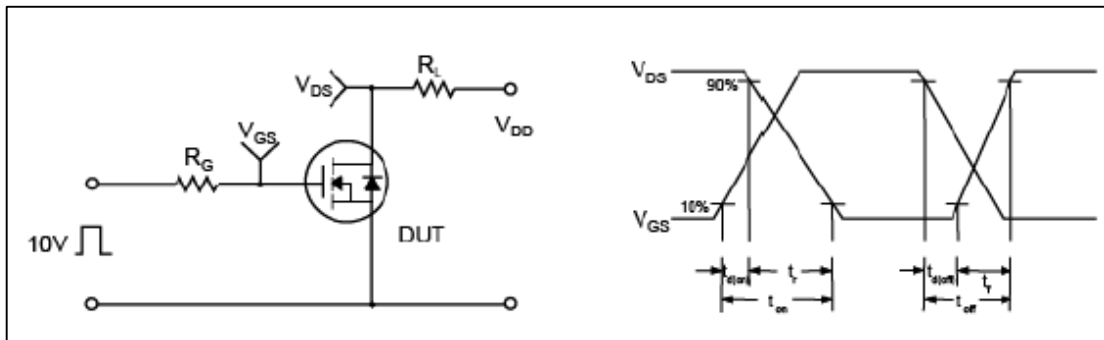


Fig.11 Resistive Switching Test Circuit & Waveform

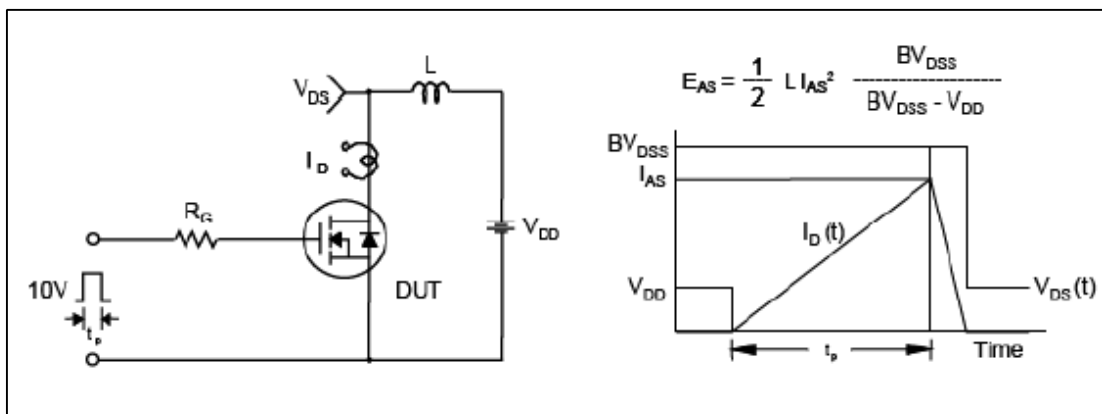


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

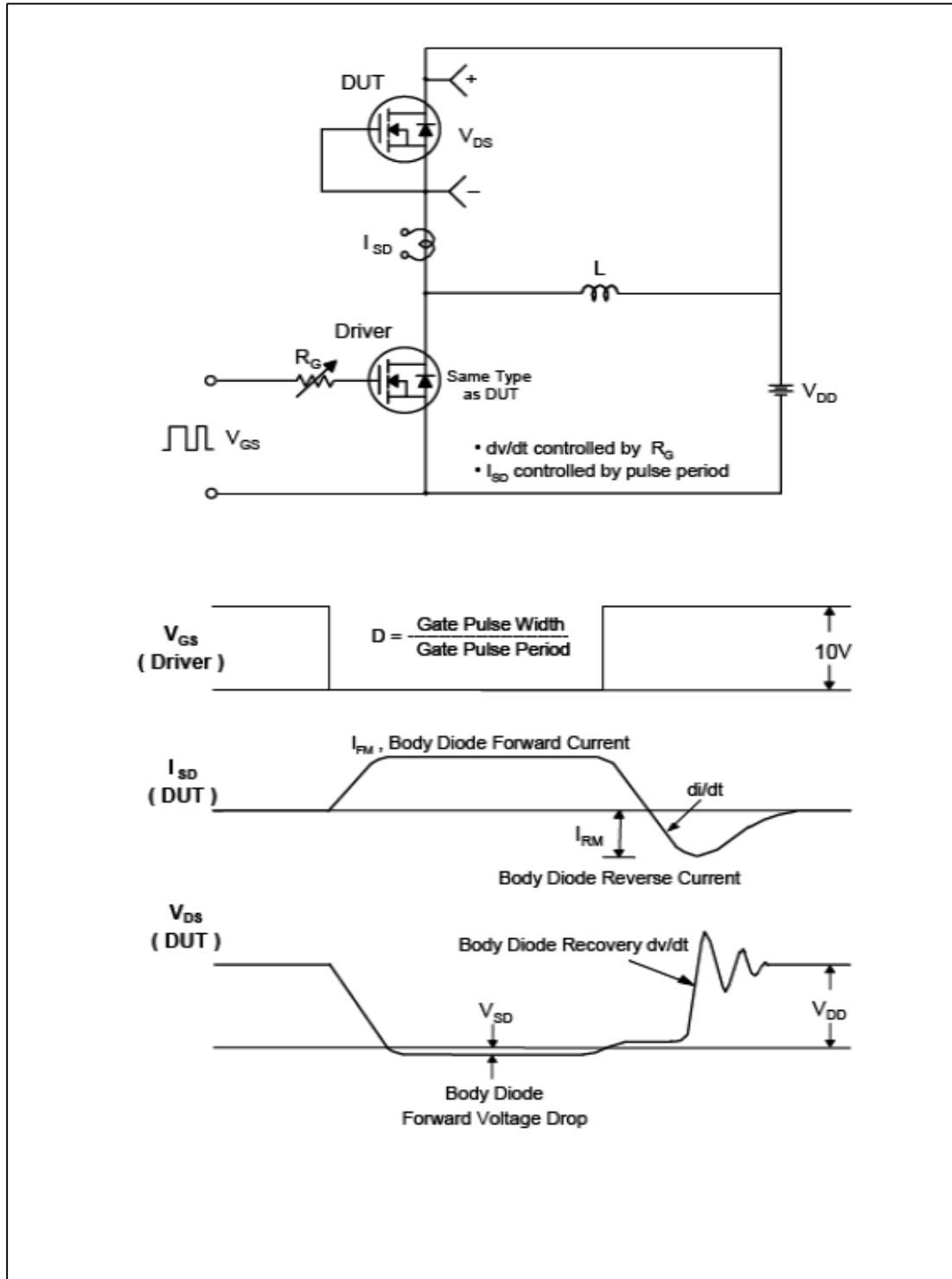


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

