

# TLE7279-2

Low Dropout Voltage Regulator

Automotive Power



Never stop thinking



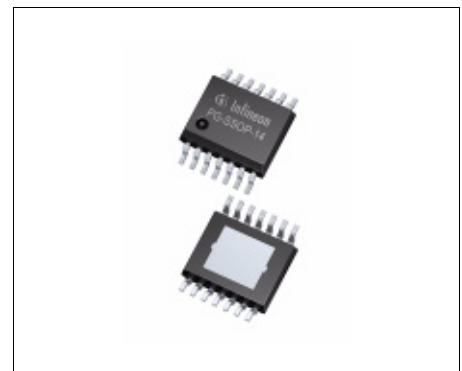
## 1 Overview

### Features

- Output voltage 5 V, 3.3 V or 2.6 V
- Output voltage tolerance  $\pm 2\%$
- Output current up to 180 mA
- Ultra low quiescent current consumption  $< 36 \mu\text{A}$
- Enable function
- Very low dropout voltage
- Reset with adjustable power-on delay
- Input Voltage Sense (Early Warning)
- Output protected against short circuit
- Wide operation range: up to 45 V
- Wide temperature range:  $-40 \text{ }^\circ\text{C}$  to  $150 \text{ }^\circ\text{C}$
- Overtemperature protection
- Overload protection
- Green Product (RoHS compliant)
- AEC Qualified



PG-DSO-14



PG-SSOP-14 Exposed Pad

### Description

The TLE7279-2 is a monolithic integrated voltage regulator with early warning and reset dedicated for microcontroller supplies under harsh automotive environment conditions.

Due to its ultra low quiescent current the TLE7279-2 is perfectly suited for applications permanently connected to battery. In addition the regulator can be shut down via the Enable input causing the current consumption to drop below  $3 \mu\text{A}$ . The TLE7279-2 is equipped with an output current limitation and an overtemperature shutdown protecting the device against overload, short circuit and overtemperature. It operates in the wide junction temperature range from  $-40 \text{ }^\circ\text{C}$  to  $150 \text{ }^\circ\text{C}$ .

| Type          | Package                | Marking       |
|---------------|------------------------|---------------|
| TLE7279-2GV50 | PG-DSO-14              | TLE7279-2GV50 |
| TLE7279-2GV33 | PG-DSO-14              | TLE7279-2GV33 |
| TLE7279-2GV26 | PG-DSO-14              | TLE7279-2GV26 |
| TLE7279-2EV50 | PG-SSOP-14 Exposed Pad | 7279 V50      |

## 2 Pin Configuration

### 2.1 Pin Assignment (PG-DSO-14)

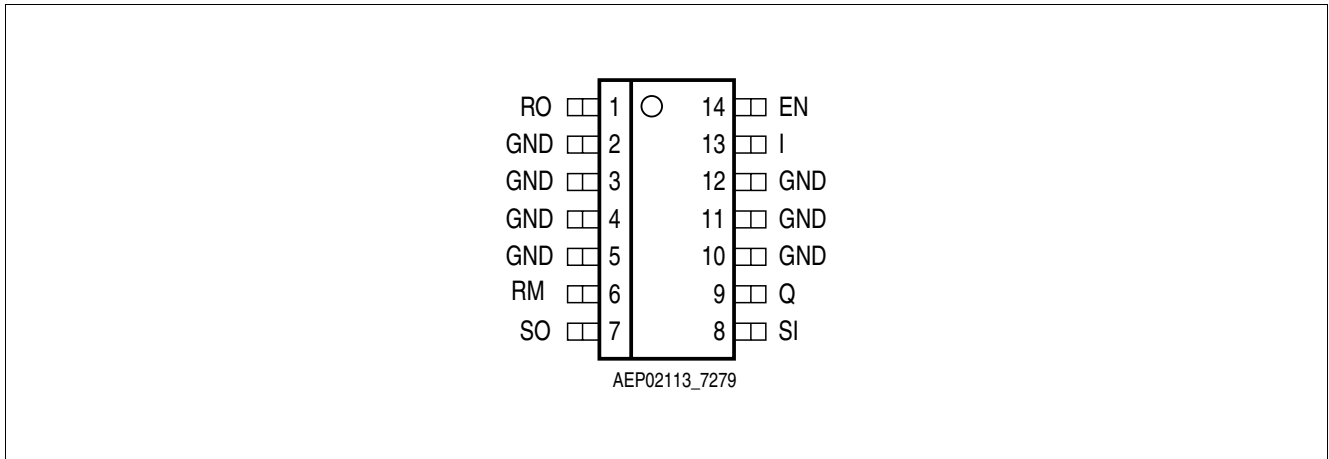


Figure 1 Pin Configuration

### 2.2 Pin Definitions and Functions (PG-DSO-14)

| Pin           | Symbol | Function  |
|---------------|--------|---|
| 1             | RO     | <b>Reset Output</b><br>TLE7279-2GV33, TLE7279-2GV26: open drain output;<br>TLE7279-2GV50: integrated 20 kΩ pull-up resistor;<br>leave open if Reset is not needed   |
| 2-5,<br>10-12 | GND    | <b>Ground</b><br>connect pin 2 and 3 to GND;<br>connect pin 4-5, 10-12 to PCB heat sink area with GND potential   |
| 8             | SI     | <b>Sense Input</b><br>connect to Q if not needed  |
| 6             | RM     | <b>Reset Mode</b><br>power-on reset delay time selection: set to LOW for fast timing, to HIGH for slow timing;<br>see reset timing definitions in <b>“Electrical Characteristics” on Page 10</b> ;<br>connect to Q or GND |
| 7             | SO     | <b>Sense Output</b><br>TLE7279-2GV33, TLE7279-2GV26: open-drain output;<br>TLE7279-2GV50: integrated 20 kΩ pull-up resistor;<br>keep open, if sense comparator not needed   |
| 9             | Q      | <b>Output Voltage</b><br>block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <b>“Functional Range” on Page 7</b>                                  |
| 13            | I      | <b>Input Voltage</b><br>block to ground directly at the IC with a 100 nF ceramic capacitor  |
| 14            | EN     | <b>Enable Input</b><br>low level disables the IC;<br>integrated pull-down resistor to GND   |

### 2.3 Pin Assignment (PG-SSOP-14 Exposed Pad)

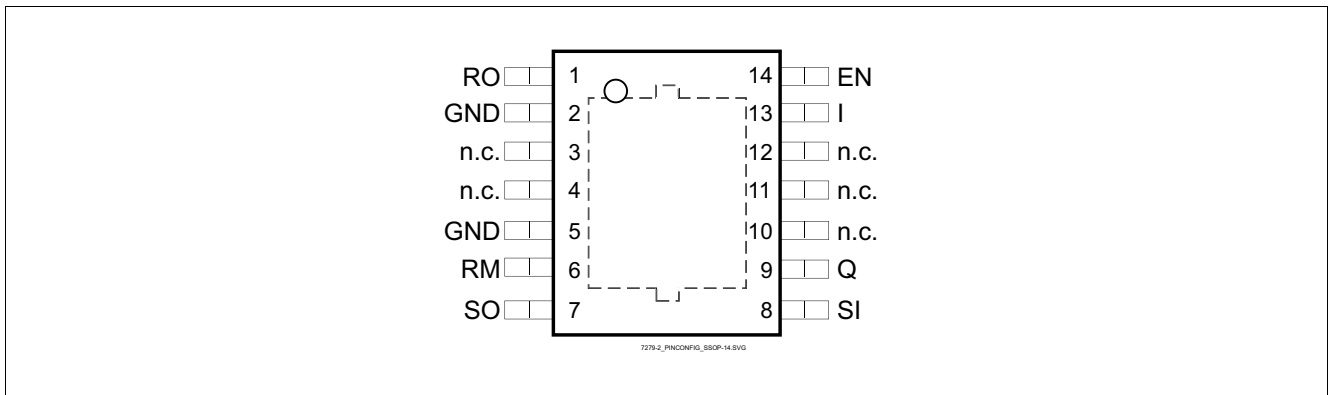


Figure 2 Pin Configuration

### 2.4 Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)

| Pin              | Symbol | Function   |
|------------------|--------|--|
| 1                | RO     | <b>Reset Output</b><br>integrated 20 kΩ pull-up resistor;<br>leave open if Reset is not needed   |
| 2, 5             | GND    | <b>Ground</b><br>connect pin 2 and 5 to GND  |
| 3, 4, 10, 11, 12 | n.c.   | <b>not connected</b><br>leave open or connect to GND   |
| 6                | RM     | <b>Reset Mode</b><br>power-on reset delay time selection: set to LOW for fast timing, to HIGH for slow timing;<br>see reset timing definitions in <a href="#">“Electrical Characteristics” on Page 10</a> ;<br>connect to Q or GND |
| 7                | SO     | <b>Sense Output</b><br>integrated 20 kΩ pull-up resistor;<br>keep open, if sense comparator not needed   |
| 8                | SI     | <b>Sense Input</b><br>connect to Q if not needed   |
| 9                | Q      | <b>Output Voltage</b><br>block to GND with a ceramic capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <a href="#">“Functional Range” on Page 7</a>                                  |
| 13               | I      | <b>Input Voltage</b><br>block to ground directly at the IC with a 100 nF ceramic capacitor   |
| 14               | EN     | <b>Enable Input</b><br>low level disables the IC;<br>integrated pull-down resistor to GND  |
| Pad              | –      | <b>Exposed Pad</b><br>connect to heatsink area;<br>connect to GND on PCB   |

### 3 Block Diagram

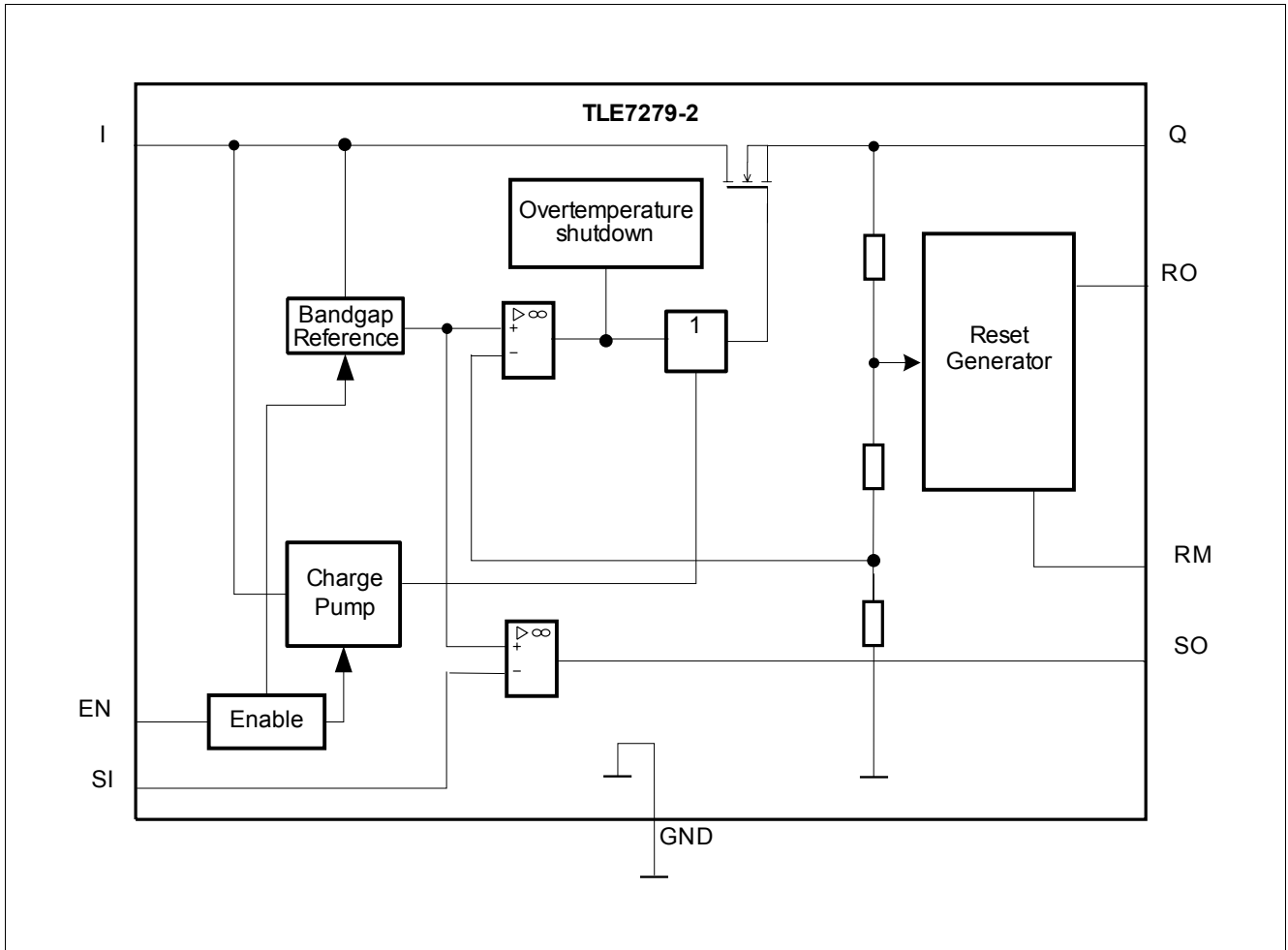


Figure 3 Block Diagram

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.   | Parameter                               | Symbol                | Limit Values |      | Unit | Conditions           |
|--|---|-----------------------|--------------|------|------|----------------------|
|  |   |                       | Min.         | Max. |      |                      |
| <b>Input I, Sense Input SI</b>                 |   |                       |              |      |      |                      |
| 4.1.1  | Voltage                                 | $V_I, V_{SI}$         | -0.3         | 45   | V    | –                    |
| <b>Output Q, Reset Output RO, Sense Out SO</b> |   |                       |              |      |      |                      |
| 4.1.2  | Voltage                                 | $V_Q, V_{RO}, V_{SO}$ | -0.3         | 5.5  | V    | permanent            |
| 4.1.3  | Voltage                                 | $V_Q, V_{RO}, V_{SO}$ | -0.3         | 6.2  | V    | $t < 10\text{ s}^2)$ |
| <b>Enable Input EN</b>                         |   |                       |              |      |      |                      |
| 4.1.4  | Voltage                                 | $V_{EN}$              | -1           | 45   | V    | –                    |
| 4.1.5  | Current                                 | $I_{EN}$              | -1           | 1    | mA   | –                    |
| <b>Reset Mode RM</b>                           |   |                       |              |      |      |                      |
| 4.1.6  | Voltage                                 | $V_{RM}$              | -0.3         | 5.5  | V    | permanent            |
| 4.1.7  | Voltage                                 | $V_{RM}$              | -0.3         | 6.2  | V    | $t < 10\text{ s}^2)$ |
| 4.1.8  | Current                                 | $I_{RM}$              | -5           | 5    | mA   | –                    |
| <b>ESD Susceptibility</b>                      |   |                       |              |      |      |                      |
| 4.1.9  | Human Body Model (HBM) <sup>3)</sup>    | Voltage               | –            | 3    | kV   | –                    |
| 4.1.10   | Charge Device Model (CDM) <sup>4)</sup> | Voltage               | –            | 1.5  | kV   | –                    |
| <b>Temperatures</b>                            |   |                       |              |      |      |                      |
| 4.1.11   | Junction temperature                    | $T_j$                 | -40          | 150  | °C   | –                    |
| 4.1.12   | Storage temperature                     | $T_{stg}$             | -50          | 150  | °C   | –                    |

1) not subject to production test, specified by design

2) exposure to these absolute maximum ratings for extended periods ( $t > 10\text{ s}$ ) may affect device reliability

3) ESD HBM Test according to JEDEC JESD22-A114

4) ESD CDM Test according to AEC/ESDA ESD-STM5.3.1-1999

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

| Pos.  | Parameter                                     | Symbol     | Limit Values |      | Unit     | Conditions                      |
|-------|---|------------|--------------|------|----------|---------------------------------|
|       |   |            | Min.         | Max. |          |                                 |
| 4.2.1 | Input voltage                                 | $V_I$      | 5.5          | 45   | V        | TLE7279-2GV50,<br>TLE7279-2EV50 |
| 4.2.2 |   |            | 4.2          | 45   | V        | TLE7279-2GV33                   |
| 4.2.3 |   |            | 4.5          | 45   | V        | TLE7279-2GV26                   |
| 4.2.4 | Output capacitor's requirements for Stability | $C_Q$      | 470          | –    | nF       | – <sup>1)</sup>                 |
|       |   | $ESR(C_Q)$ | –            | 3    | $\Omega$ | – <sup>2)</sup>                 |
| 4.2.5 | Junction temperature                          | $T_j$      | -40          | 150  | °C       | –                               |

- 1) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%  
 2) relevant ESR value at  $f = 10$  kHz

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

| Pos.                                  | Parameter                                 | Symbol      | Limit Values |      |      | Unit | Conditions   |
|---------------------------------------|---|-------------|--------------|------|------|------|--|
|                                       |   |             | Min.         | Typ. | Max. |      |  |
| <b>Package PG-DSO-14</b>              |   |             |              |      |      |      |  |
| 4.3.1                                 | Junction to Soldering Point <sup>1)</sup> | $R_{thJSP}$ | –            | 30   | –    | K/W  | measured to group of pins 3, 4, 5, 10, 11, 12          |
| 4.3.2                                 | Junction to Ambient <sup>1)</sup>         | $R_{thJA}$  | –            | 53   | –    | K/W  | <sup>2)</sup>  |
| 4.3.3                                 |   |             | –            | 105  | –    | K/W  | footprint only <sup>3)</sup>                           |
| 4.3.4                                 |   |             | –            | 74   | –    | K/W  | 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |
| 4.3.5                                 |   |             | –            | 65   | –    | K/W  | 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |
| <b>Package PG-SSOP-14 Exposed Pad</b> |   |             |              |      |      |      |  |
| 4.3.6                                 | Junction to Case <sup>1)</sup>            | $R_{thJC}$  | –            | 14   | –    | K/W  | measured to exposed pad                                |
| 4.3.7                                 | Junction to Ambient <sup>1)</sup>         | $R_{thJA}$  | –            | 47   | –    | K/W  |  |
| 4.3.8                                 |   |             | –            | 141  | –    | K/W  | footprint only <sup>3)</sup>                           |
| 4.3.9                                 |   |             | –            | 66   | –    | K/W  | 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |
| 4.3.10                                |   |             | –            | 56   | –    | K/W  | 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |

- 1) not subject to production test, specified by design  
 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.  
 3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70 $\mu$ m Cu).

## 5 Block Description and Electrical Characteristics

### 5.1 Circuit Description

#### 5.1.1 Power On Reset and Reset Output

For an output voltage level  $V_Q \geq 1$  V the reset output is hold low. When the level of  $V_Q$  reaches the reset threshold  $V_{RT}$ , the signal at RO remains low for the power-up reset delay time  $t_{RD}$ . The reset function and timing is illustrated in **Figure 4**. The reset reaction time  $t_{RR}$  avoids wrong triggering caused by short “glitches” on the  $V_Q$ -line. In case of  $V_Q$  power down ( $V_Q < V_{RT}$  for  $t > t_{RR}$ ) a logic low signal is generated at the pin RO to reset an external microcontroller.

The TLE7279-2GV50 and TLE7279-2EV50 feature an integrated pull-up resistor on the reset output while the TLE7279-2GV33 and TLE7279-2GV26 have an open drain output requiring an external pull-up resistor. When connected to a voltage level of  $V_{ext} = 5$  V, a recommended value for this external resistor is  $\geq 5.6$  k $\Omega$ .

But it's also possible calculating its value by using the following formula, based on the reset sink current (Example: external pull-up resistor connected to  $V_{ext} = 5$  V):

$$R_{extmin} = \Delta V / I_{RO} = (V_{ext} - V_{ROmin}) / I_{RO} = (5 \text{ V} - 0.25 \text{ V}) / 1.0 \text{ mA} = 4.75 \text{ k}\Omega$$

At low output voltage levels  $V_Q < 1$  V the integrated pull-up resistor of the TLE7279-2GV50 is switched off setting the reset output high ohmic.

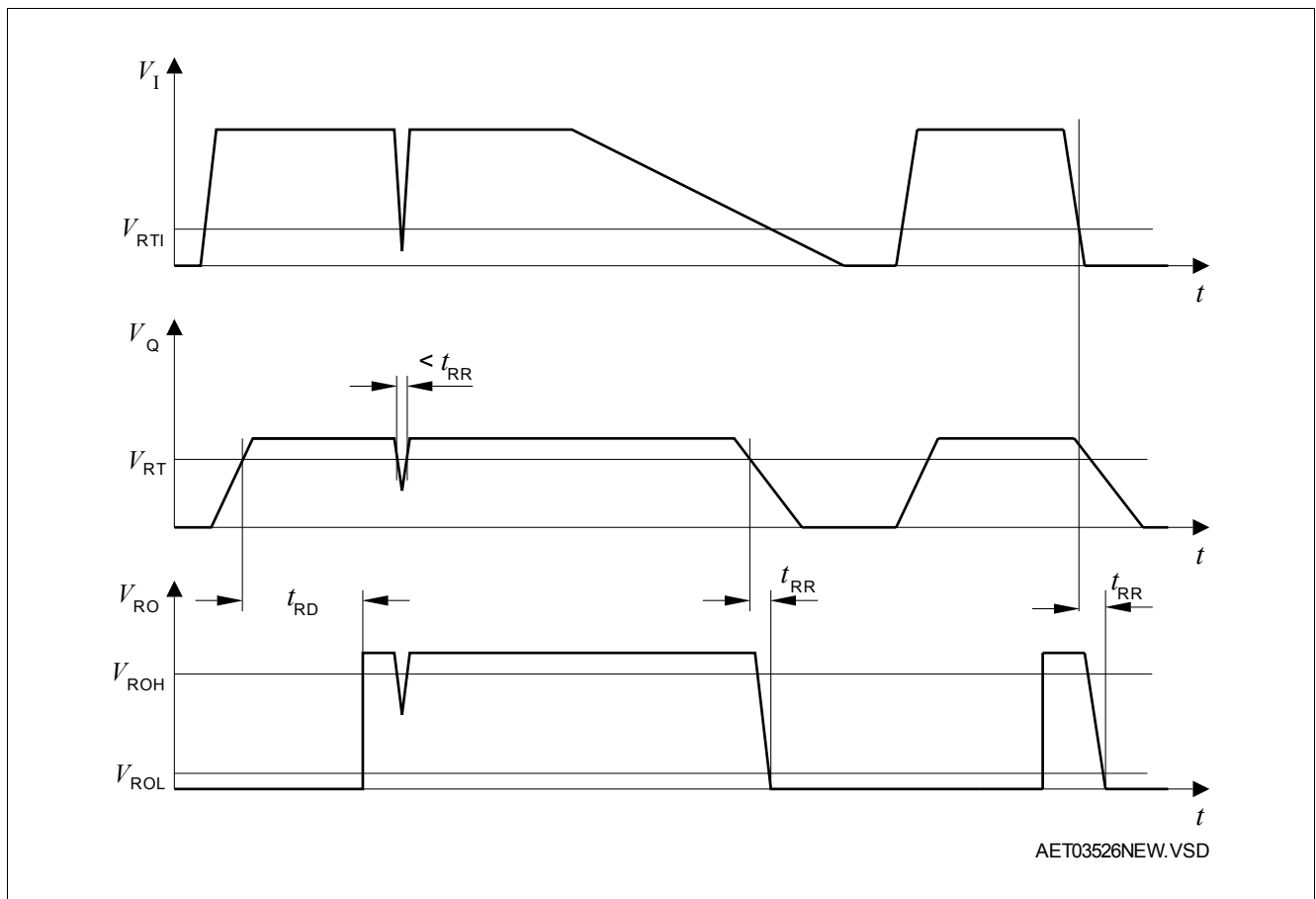
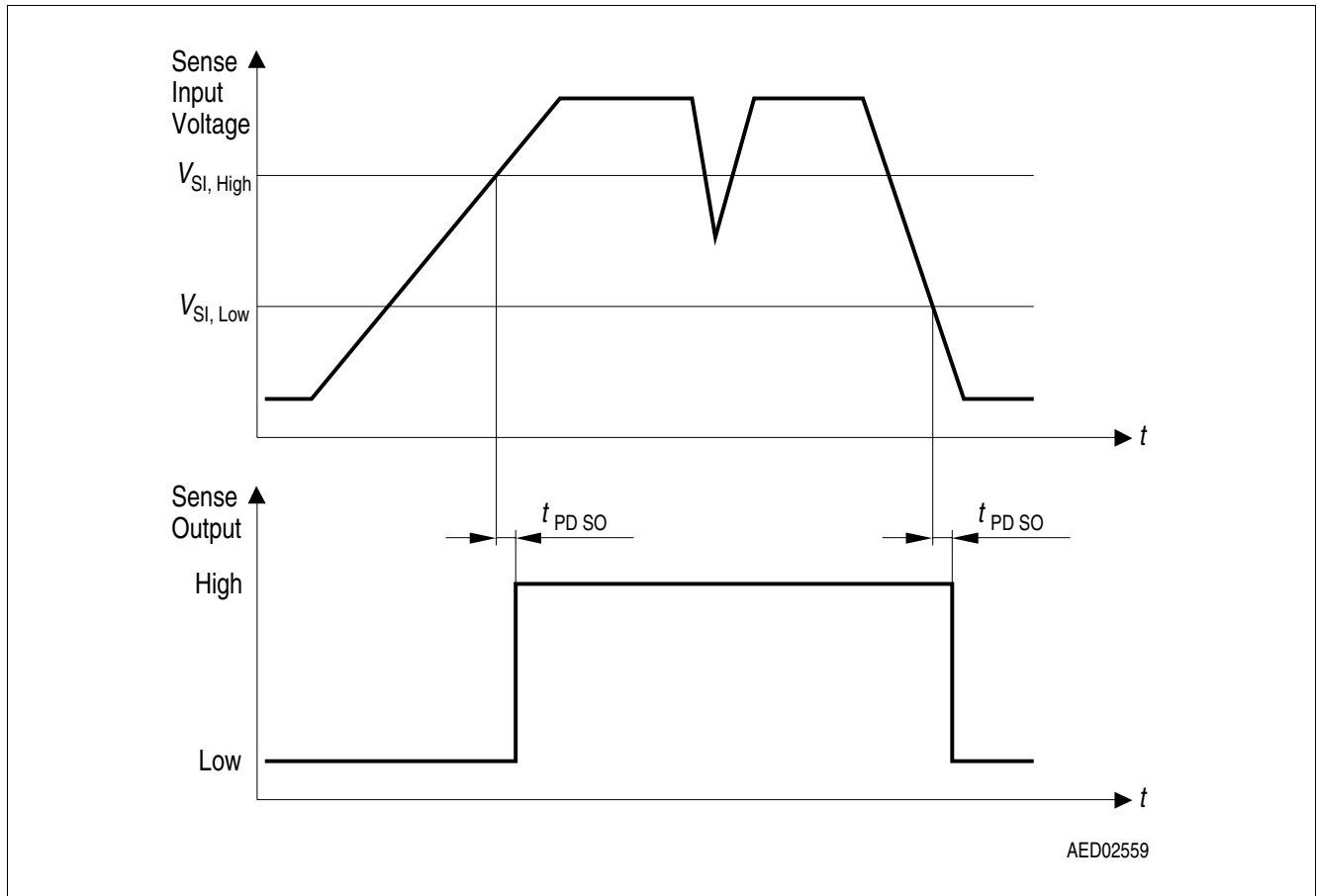


Figure 4 Reset Function and Timing Diagram



### 5.1.2 Early Warning

The additional sense comparator provides an early warning function: Any voltage (e.g. the input voltage) can be monitored, an undervoltage condition is indicated by setting the comparator's output to low. See [Figure 5](#).



**Figure 5 Early Warning Timing**

The calculation of the voltage divider is easily done since the sense input current can be neglected.

$$V_{thHL} = (R_{S11} + R_{S12})/R_{S12}, V_{Si} \text{ low} \tag{1}$$

$$V_{thLH} = (R_{S11} + R_{S12})/R_{S12}, V_{Si} \text{ high} \tag{2}$$

The sense comparator has a hysteresis of typical 100 mV. This hysteresis of the supervised threshold is multiplied by the resistor dividers amplification  $(R_{S11} + R_{S12})/R_{S11}$ .

The sense in comparator can also be used for receiving data with a threshold of typical 1.35 V and a hysteresis of 100 mV. Of course also the data signal can be scaled down with a resistive divider as shown above. With a typical delay time of 4  $\mu$ s receiving data of up to 100 kBaud are possible.

## 5.2 Electrical Characteristics

### Electrical Characteristics

$V_I = 13.5\text{ V}$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.                       | Parameter                                | Symbol            | Limit Values |      |       | Unit          | Conditions   |
|----------------------------|--|-------------------|--------------|------|-------|---------------|--|
|                            |  |                   | Min.         | Typ. | Max.  |               |  |
| <b>Output Q</b>            |  |                   |              |      |       |               |  |
| 5.2.1                      | Output voltage                           | $V_Q$             | 4.90         | 5.00 | 5.10  | V             | TLE7279-2GV50,<br>TLE7279-2EV50<br>$1\text{ mA} < I_Q < 180\text{ mA}$<br>$6\text{ V} < V_I < 16\text{ V}$ |
| 5.2.2                      | Output voltage                           | $V_Q$             | 4.90         | 5.00 | 5.10  | V             | TLE7279-2GV50,<br>TLE7279-2EV50<br>$I_Q = 10\text{ mA}$<br>$6\text{ V} < V_I < 45\text{ V}$                |
| 5.2.3                      | Output voltage                           | $V_Q$             | 3.234        | 3.30 | 3.366 | V             | TLE7279-2GV33<br>$1\text{ mA} < I_Q < 180\text{ mA}$<br>$4.5\text{ V} < V_I < 16\text{ V}$                 |
| 5.2.4                      | Output voltage                           | $V_Q$             | 3.234        | 3.30 | 3.366 | V             | TLE7279-2GV33<br>$I_Q = 10\text{ mA}$<br>$4.5\text{ V} < V_I < 45\text{ V}$                                |
| 5.2.5                      | Output voltage                           | $V_Q$             | 2.548        | 2.60 | 2.652 | V             | TLE7279-2GV26<br>$1\text{ mA} < I_Q < 180\text{ mA}$<br>$4.5\text{ V} < V_I < 16\text{ V}$                 |
| 5.2.6                      | Output voltage                           | $V_Q$             | 2.548        | 2.60 | 2.652 | V             | TLE7279-2GV26<br>$I_Q = 10\text{ mA}$<br>$4.5\text{ V} < V_I < 45\text{ V}$                                |
| 5.2.7                      | Output current limitation                | $I_Q$             | 200          | –    | 500   | mA            | $V_Q = 2.0\text{ V}$   |
|                            |  |                   | 200          | –    | 600   | mA            | $V_Q = 0\text{ V}$   |
| 5.2.8                      | Dropout voltage;<br>$V_{DR} = V_I - V_Q$ | $V_{DR}$          | –            | 250  | 500   | mV            | $I_Q = 180\text{ mA}^1$<br>TLE7279-2GV50,<br>TLE7279-2EV50   |
| 5.2.9                      | Load regulation                          | $\Delta V_{Q,Lo}$ | –            | 50   | 90    | mV            | $1\text{ mA} < I_Q < 180\text{ mA}$  |
| 5.2.10                     | Line regulation                          | $\Delta V_{Q,Li}$ | –            | 10   | 50    | mV            | $I_Q = 1\text{ mA}$ ;<br>$10\text{ V} < V_I < 32\text{ V}$   |
| 5.2.11                     | Power-Supply-Ripple-Rejection            | $PSRR$            | –            | 60   | –     | dB            | $f_r = 100\text{ Hz}$ ;<br>$V_r = 0.5\text{ Vpp}$  |
| 5.2.12                     | Reverse Output Current Clamping          | $V_{Q,REV}$       | –            | –    | 5.5   | V             | $I_{Q,REV} = -1\text{ mA}$ ;<br>$V_{EN} = 0\text{ V}$  |
| <b>Current Consumption</b> |  |                   |              |      |       |               |  |
| 5.2.13                     | Quiescent current;<br>$I_q = I_I - I_Q$  | $I_q$             | –            | 28   | 36    | $\mu\text{A}$ | $I_Q = 100\text{ }\mu\text{A}$ ;<br>$T_j < 80\text{ °C}$   |
| 5.2.14                     | Quiescent current;<br>Disabled           | $I_q$             | –            | 1    | 3     | $\mu\text{A}$ | $V_{EN} = 0\text{ V}$ ;<br>$T_j < 80\text{ °C}$  |
| <b>Enable Input EN</b>     |  |                   |              |      |       |               |  |
| 5.2.15                     | High Level Input Voltage                 | $V_{EN,H}$        | 3.0          | –    | –     | V             | $V_Q$ on   |

**Block Description and Electrical Characteristics**
**Electrical Characteristics (cont'd)**

$V_I = 13.5\text{ V}$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.   | Parameter                | Symbol     | Limit Values |      |      | Unit          | Conditions  |
|--------|--------------------------|------------|--------------|------|------|---------------|---|
|        |                          |            | Min.         | Typ. | Max. |               |   |
| 5.2.16 | Low Level Input Voltage  | $V_{EN,L}$ | –            | –    | 0.5  | V             | $V_Q = 0.02\text{ V}$<br>$I_Q = 5\text{ mA}$<br>$T_j < 125\text{ °C}$ |
| 5.2.17 |                          |            | –            | –    | 0.3  | V             | $V_Q = 0.02\text{ V}$<br>$I_Q = 5\text{ mA}$                          |
| 5.2.18 | High Level Input current | $I_{EN,H}$ | –            | 3    | 4    | $\mu\text{A}$ | $V_{EN} = 5\text{ V}$   |

**Reset Mode Bit RM**

|        |                          |            |      |   |      |   |                                 |
|--------|--------------------------|------------|------|---|------|---|---------------------------------|
| 5.2.19 | High Level Input Voltage | $V_{RM,H}$ | 4.00 | – | –    | V | TLE7279-2GV50,<br>TLE7279-2EV50 |
| 5.2.20 |                          |            | 2.65 | – | –    | V | TLE7279-2GV33                   |
| 5.2.21 |                          |            | 2.30 | – | –    | V | TLE7279-2GV26                   |
| 5.2.22 | Low Level Input Voltage  | $V_{RM,L}$ | –    | – | 0.80 | V | –                               |

**Input Voltage Sense**

|        |                                   |                      |      |      |      |               |  |
|--------|-----------------------------------|----------------------|------|------|------|---------------|--|
| 5.2.23 | Sense threshold high              | $V_{SIH}$            | 1.10 | 1.16 | 1.22 | V             | $V_{SI}$ increasing (see <a href="#">Figure 4</a> )  |
| 5.2.24 | Sense threshold low               | $V_{SIL}$            | 1.06 | 1.12 | 1.18 | V             | $V_{SI}$ decreasing (see <a href="#">Figure 4</a> )  |
| 5.2.25 | Sense input switching hysteresis  | $V_{SI\text{ HYST}}$ | 25   | –    | 75   | mV            | $V_{SI\text{ HYST}} = V_{SIH} - V_{SIL}$   |
| 5.2.26 | Sense output low current          | $I_{SOL}$            | –    | –    | 1.1  | mA            | $V_{SI} < 1.01\text{ V}$ ;<br>$V_I > 4.5\text{ V}$ ; EN = High;<br>$V_{SOL} < 0.4\text{ V}$          |
| 5.2.27 | Sense output low voltage          | $V_{SO}$             | –    | 0.15 | 0.25 | V             | $V_{SI} < 1.01\text{ V}$ ;<br>$V_I > 4.5\text{ V}$ ; EN = High;<br>$I_{SO} < 200\text{ }\mu\text{A}$ |
| 5.2.28 | Sense high voltage                | $V_{SOH}$            | 4.5  | –    | –    | V             | TLE7279-2GV50,<br>TLE7279-2EV50  |
| 5.2.29 | Sense high leakage current        | $I_{SOLK}$           | –    | –    | 1    | $\mu\text{A}$ | TLE7279-2GV33<br>TLE7279-2GV26   |
| 5.2.30 | Integrated sense pull-up resistor | $R_{SO}$             | 10   | 20   | 40   | k $\Omega$    | TLE7279-2GV50,<br>TLE7279-2EV50<br>internally connected<br>to $V_Q$                                  |
| 5.2.31 | Sense input current               | $I_{SI}$             | -1   | 0.1  | 1    | $\mu\text{A}$ | $V_{SI} = 5\text{ V}$  |
| 5.2.32 | Sense reaction time               | $t_{pd\text{ SO}}$   | –    | 4.0  | –    | $\mu\text{s}$ | –  |

**Block Description and Electrical Characteristics**
**Electrical Characteristics (cont'd)**

$V_I = 13.5\text{ V}$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.                   | Parameter                                     | Symbol       | Limit Values |      |      | Unit          | Conditions   |
|------------------------|---|--------------|--------------|------|------|---------------|--|
|                        |   |              | Min.         | Typ. | Max. |               |  |
| <b>Reset Output RO</b> |   |              |              |      |      |               |  |
| 5.2.33                 | Output Undervoltage Reset Switching Threshold | $V_{RT}$     | 4.50         | 4.60 | 4.70 | V             | TLE7279-2GV50,<br>TLE7279-2EV50<br>$V_Q$ decreasing  |
| 5.2.34                 |   |              | 3.00         | 3.07 | 3.13 | V             | TLE7279-2GV33 <sup>2)</sup><br>$V_Q$ decreasing  |
| 5.2.35                 |   |              | 2.35         | 2.38 | 2.45 | V             | TLE7279-2GV26 <sup>2)</sup><br>$V_Q$ decreasing  |
| 5.2.36                 | Input Voltage Reset Switching Threshold       | $V_{RT\_VI}$ | –            | 3.9  | 4.0  | V             | TLE7279-2GV26 <sup>2)</sup><br>TLE7279-2GV33 <sup>2)</sup><br><br>$V_Q > V_{RT}$ ,<br>$V_I$ decreasing |
| 5.2.37                 | Reset Hysteresis                              | $V_{RH}$     | –            | 45   | –    | mV            | TLE7279-2GV26  |
| 5.2.38                 |   |              | –            | 60   | –    | mV            | TLE7279-2GV33  |
| 5.2.39                 |   |              | –            | 90   | –    | mV            | TLE7279-2GV50,<br>TLE7279-2EV50  |
| 5.2.40                 | Maximum Reset Sink Current                    | $I_{RO,max}$ | 1.75         | –    | –    | mA            | TLE7279-2GV50,<br>TLE7279-2EV50<br><br>$V_Q = 4.5\text{ V}$ ,<br>$V_{RO} = 0.25\text{ V}$              |
| 5.2.41                 |   |              | 1.3          | –    | –    | mA            | TLE7279-2GV33<br>$V_Q = 3.0\text{ V}$ ,<br>$V_{RO} = 0.25\text{ V}$                                    |
| 5.2.42                 |   |              | 1.0          | –    | –    | mA            | TLE7279-2GV26<br>$V_Q = 2.35\text{ V}$ ,<br>$V_{RO} = 0.25\text{ V}$                                   |
| 5.2.43                 | Reset output low voltage                      | $V_{ROL}$    | –            | 0.15 | 0.25 | V             | $V_Q \geq 1\text{ V}$ ;<br>$I_{RO} < 200\text{ }\mu\text{A}$   |
| 5.2.44                 | Reset high voltage                            | $V_{ROH}$    | 4.5          | –    | –    | V             | TLE7279-2GV50,<br>TLE7279-2EV50  |
| 5.2.45                 | Reset high leakage current                    | $I_{ROLK}$   | –            | –    | 1    | $\mu\text{A}$ | TLE7279-2GV33<br>TLE7279-2GV26   |
| 5.2.46                 | Integrated reset pull-up resistor             | $R_{RO}$     | 10           | 20   | 40   | k $\Omega$    | TLE7279-2GV50,<br>TLE7279-2EV50<br><br>internally connected<br>to $V_Q$                                |

Block Description and Electrical Characteristics

Electrical Characteristics (cont'd)

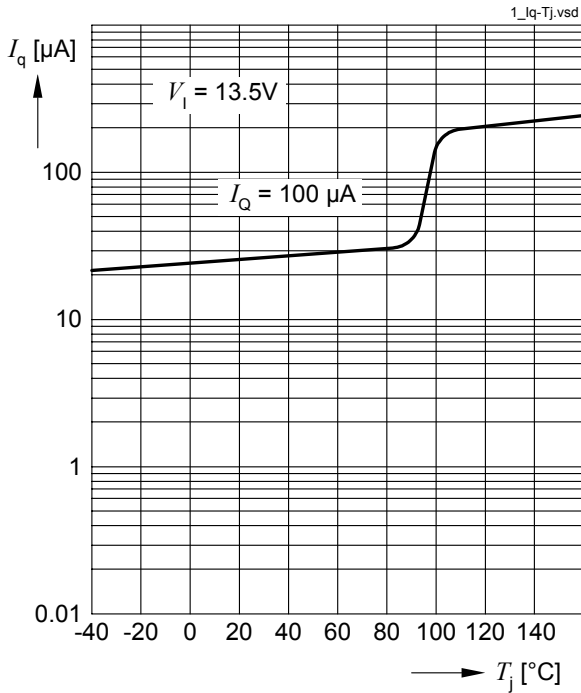
$V_I = 13.5\text{ V}$ ,  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Pos.   | Parameter                 | Symbol   | Limit Values |      |      | Unit          | Conditions                     |
|--------|---------------------------|----------|--------------|------|------|---------------|--------------------------------|
|        |                           |          | Min.         | Typ. | Max. |               |                                |
| 5.2.47 | Power-on reset delay time | $T_{RD}$ | 12.8         | 16.0 | 19.2 | ms            | fast reset timing<br>RM = Low  |
|        |                           |          | 25.6         | 32.0 | 38.4 | ms            | slow reset timing<br>RM = High |
| 5.2.48 | Reset Reaction Time       | $T_{RR}$ | –            | 4    | 12   | $\mu\text{s}$ | – <sup>3)</sup>                |

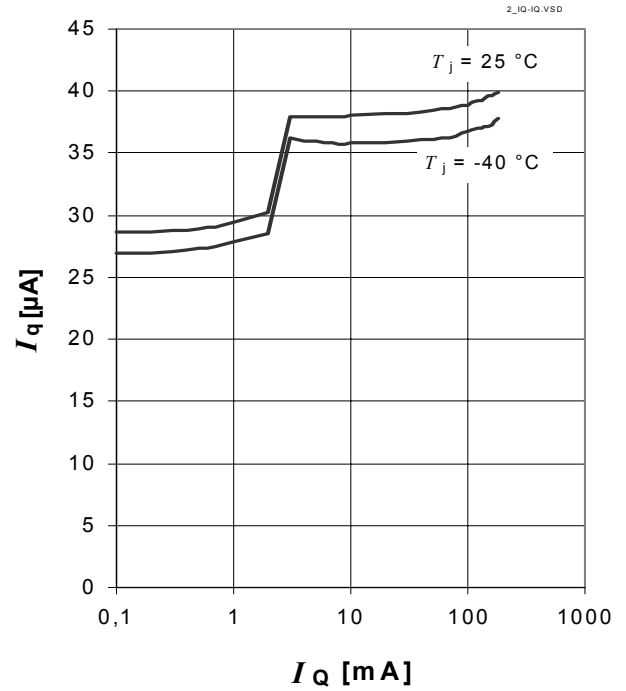
- 1) measured when the output voltage has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{ V}$
- 2) reset output triggered when output voltage  $V_Q$  is lower than output voltage reset switching threshold  $V_{RT}$  or is also triggered, when Input Voltage is decreasing to  $V_I < 4.0\text{ V}$  and  $V_Q > V_{RT}$
- 3) not subject to production test, specified by design

Typical Performance Characteristics

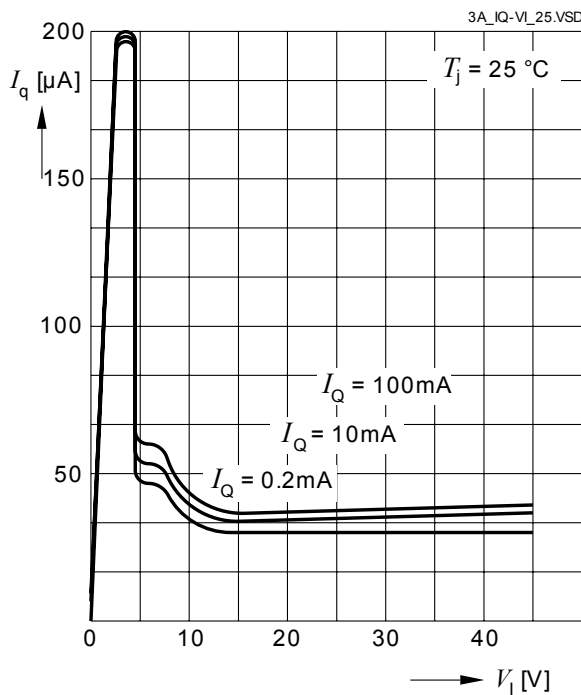
Current Consumption  $I_q$  versus Junction Temperature  $T_j$  (EN=ON)



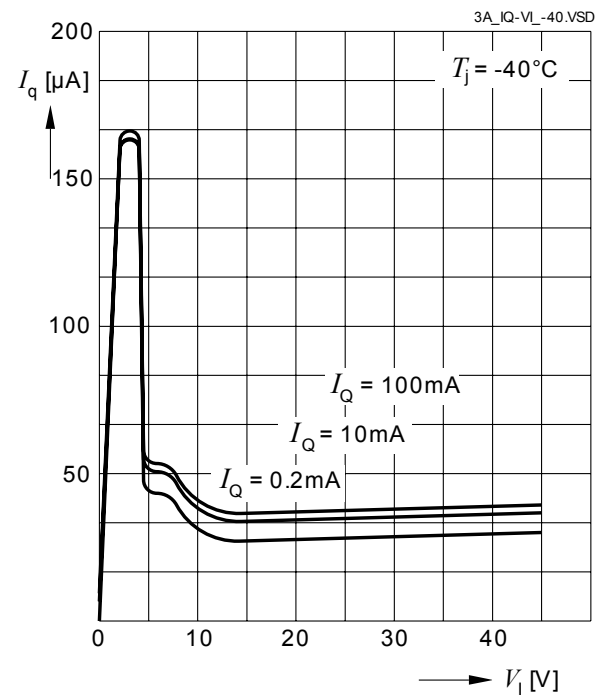
Current Consumption  $I_q$  versus Output Current  $I_Q$  (EN=ON)



Current Consumption  $I_q$  versus Input Voltage  $V_i$  at  $T_j=25^\circ\text{C}$  (EN=ON)

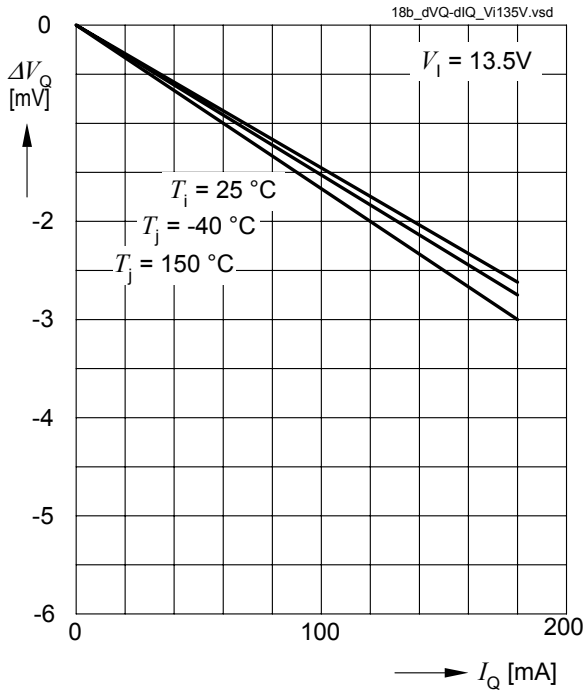


Current Consumption  $I_q$  versus Input Voltage  $V_i$  at  $T_j=-40^\circ\text{C}$  (EN=ON)

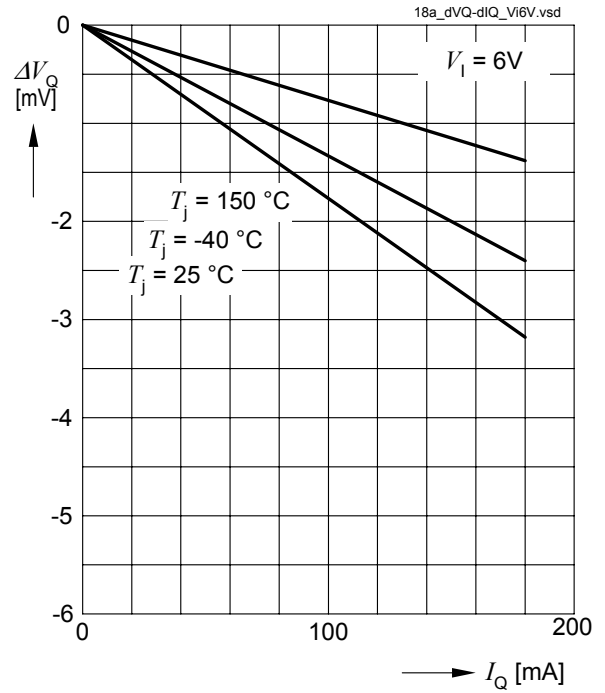


Typical Performance Characteristics (cont'd)

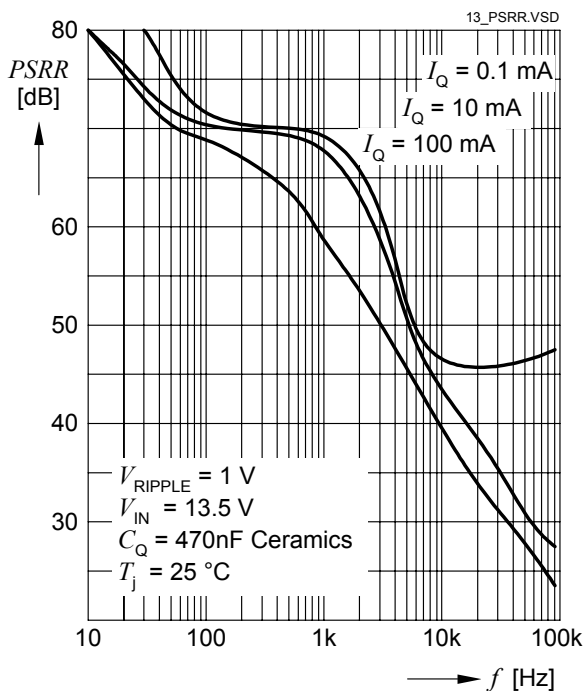
Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$



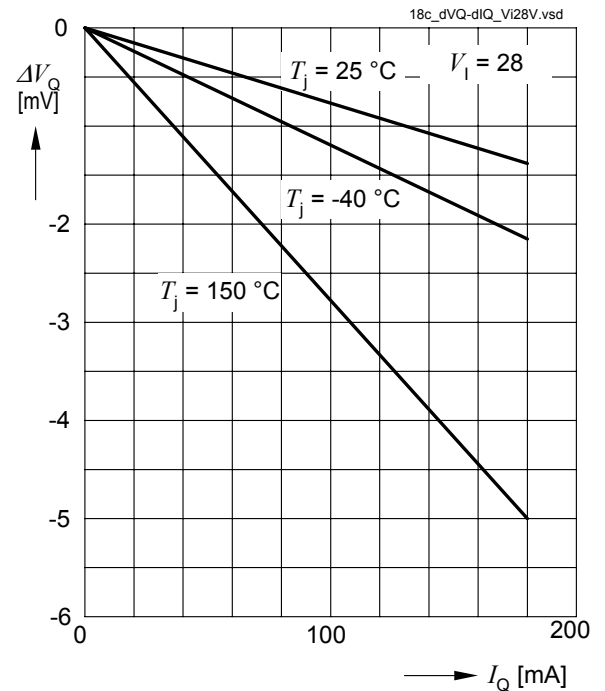
Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$



Power Supply Ripple Rejection *PSRR*

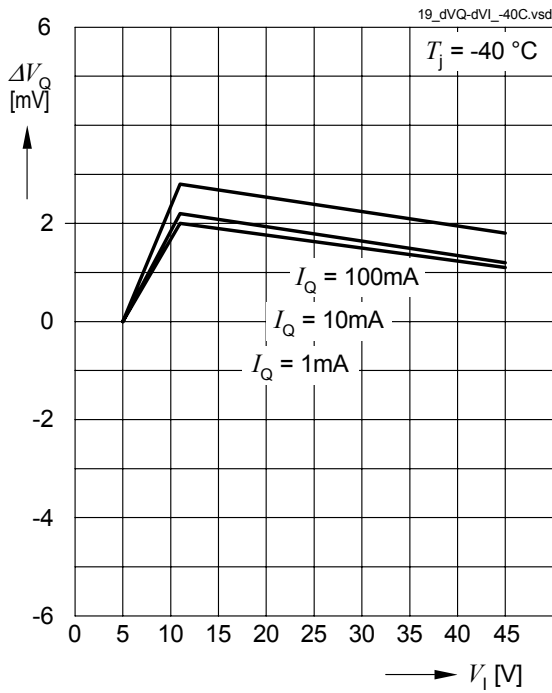


Load Regulation  $dV_Q$  versus Output Current Change  $dI_Q$

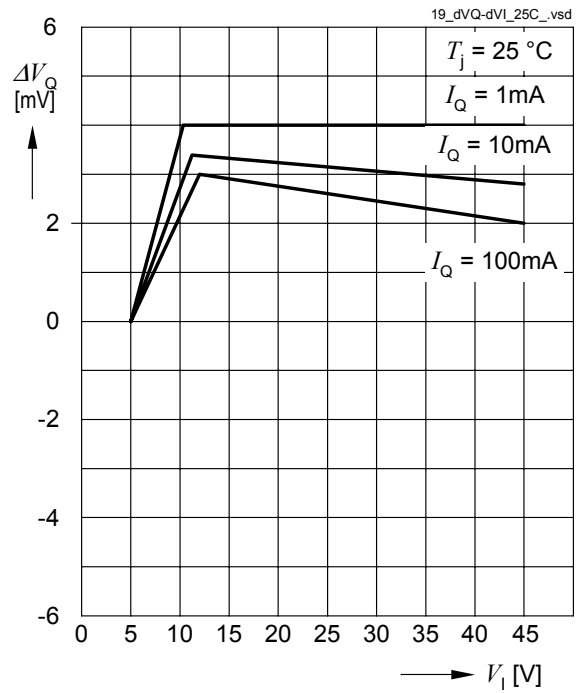


Typical Performance Characteristics (cont'd)

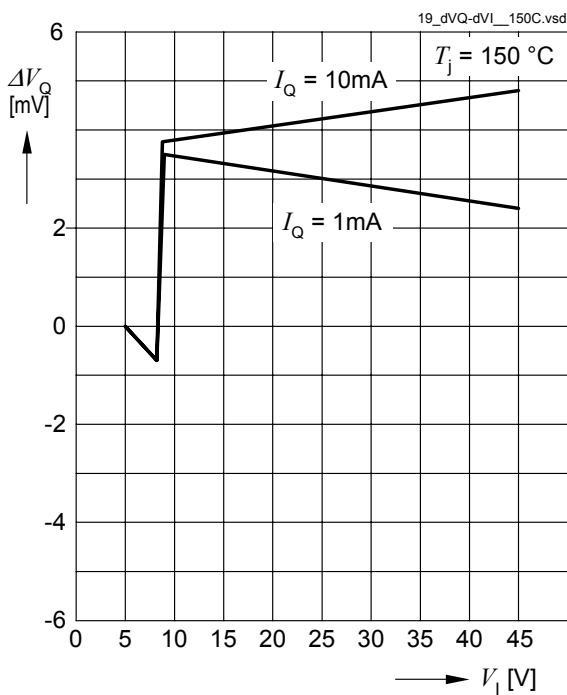
Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$



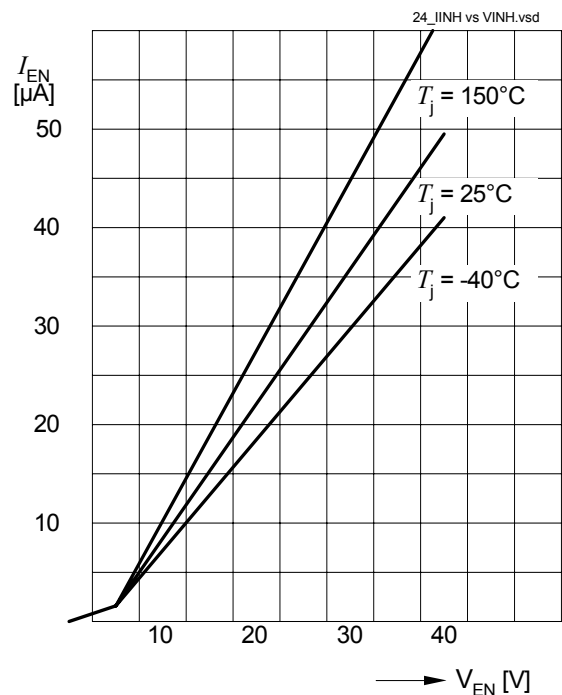
Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$



Line Regulation  $dV_Q$  versus Input Voltage Change  $dV_I$



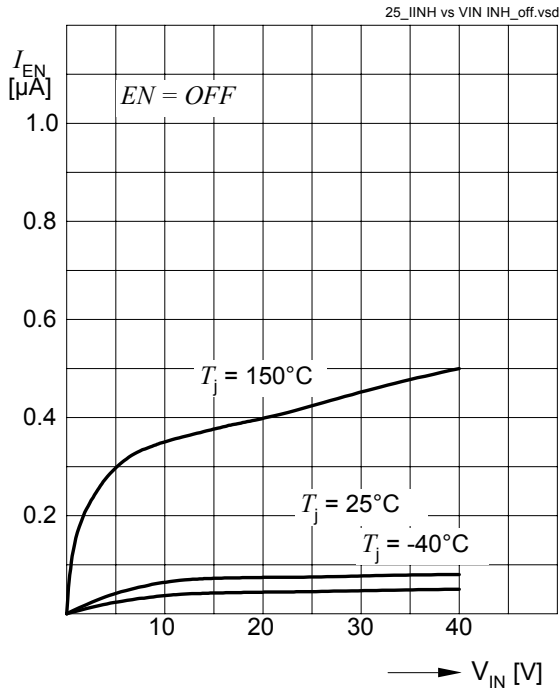
Enable Input Current  $I_{EN}$  versus Enable Input Voltage  $V_{EN}$



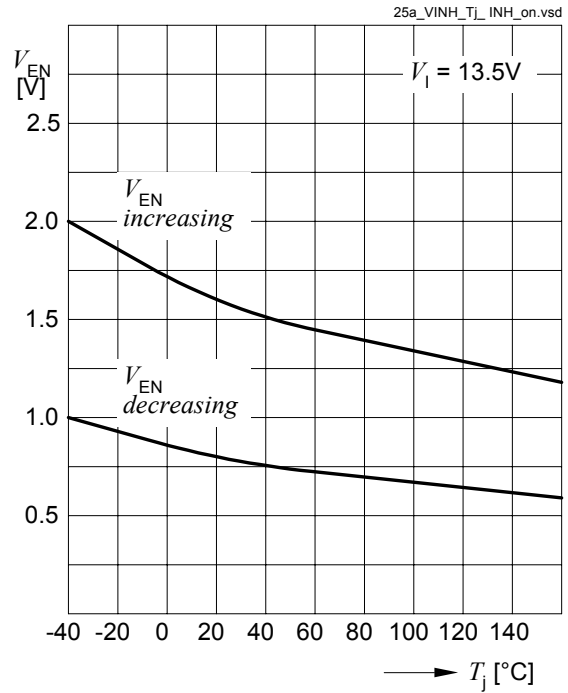


Typical Performance Characteristics (cont'd)

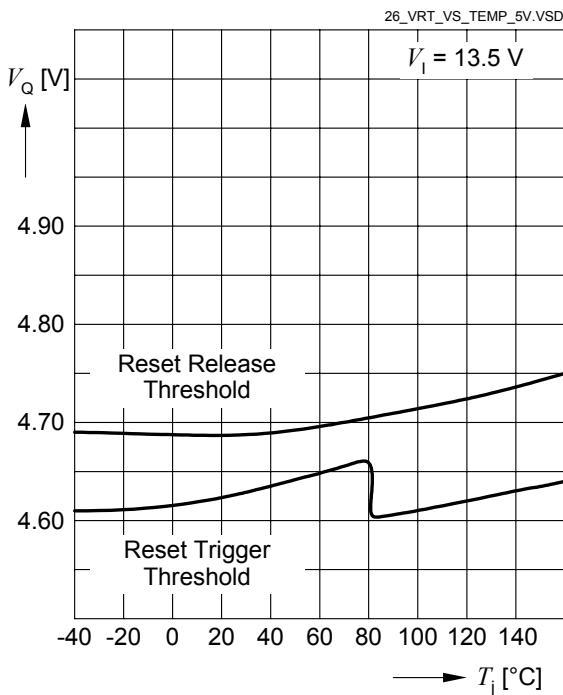
Enable Input Current  $I_{EN}$  versus Input Voltage  $V_I$ , EN=Off



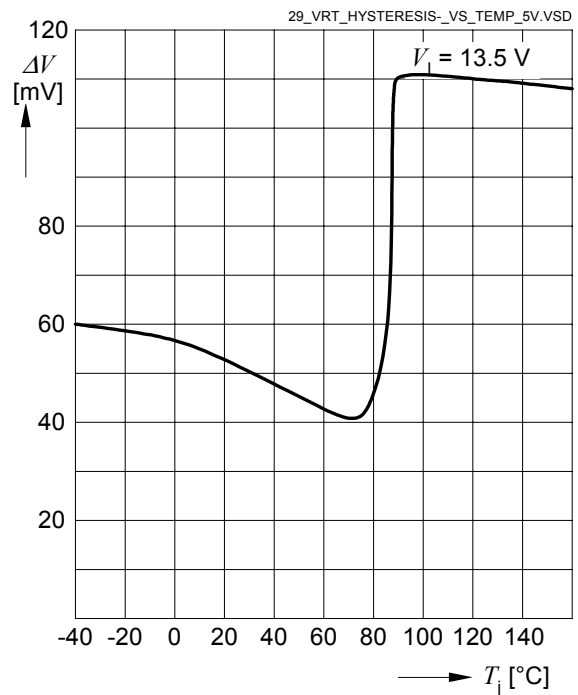
Enable High Level / Low Level Input Voltage  $V_{EN,H} / V_{EN,L}$  versus Junction Temperature  $T_j$



Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (5V-Version)

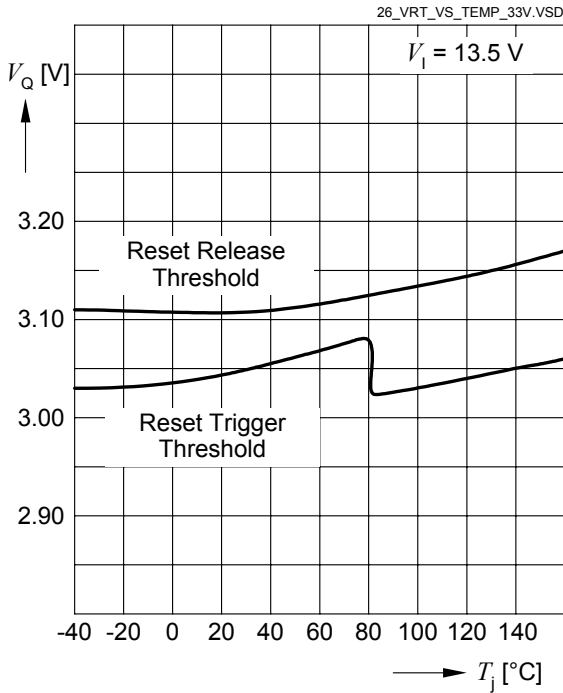


Reset Hysteresis versus Junction Temperature  $T_j$  (5V-Version)

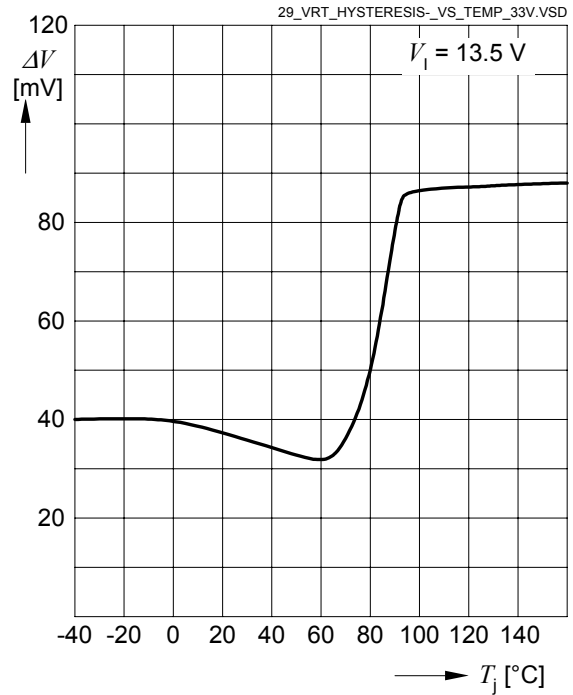


Typical Performance Characteristics (cont'd)

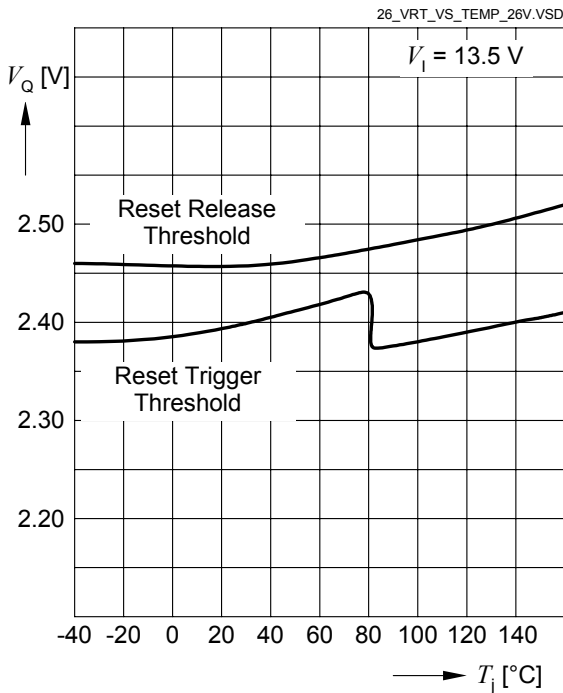
Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (3.3V-Version)



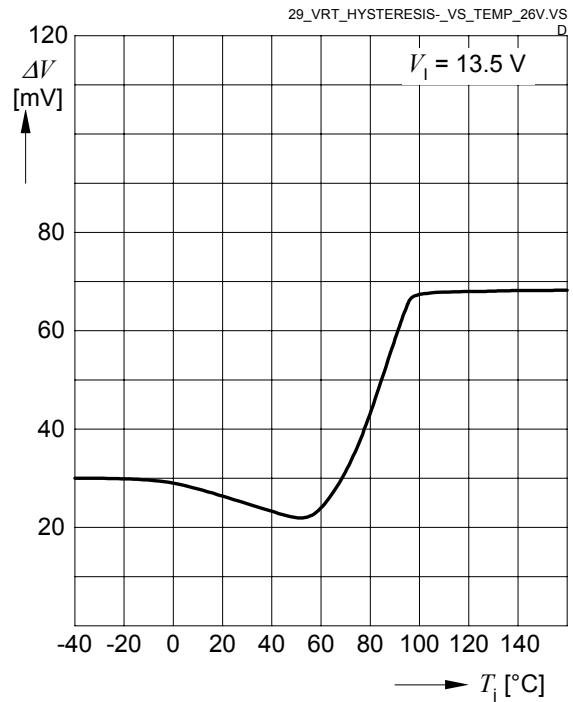
Reset Hysteresis versus Junction Temperature  $T_j$  (3.3V-Version)



Reset Threshold  $V_{RT}$  versus Junction Temperature  $T_j$  (2.6V-Version)

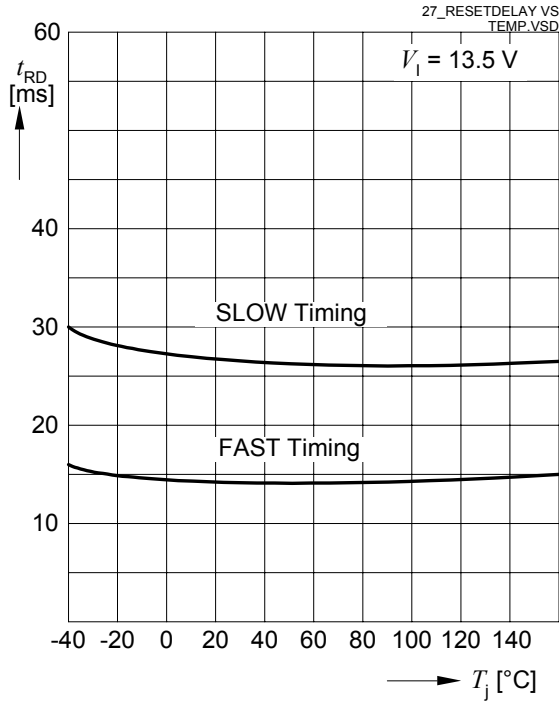


Reset Hysteresis versus Junction Temperature  $T_j$  (2.6V-Version)

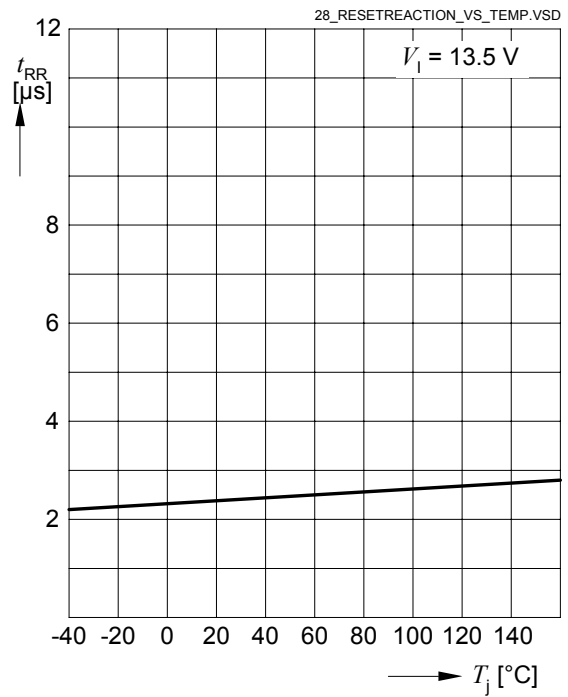


Typical Performance Characteristics (cont'd)

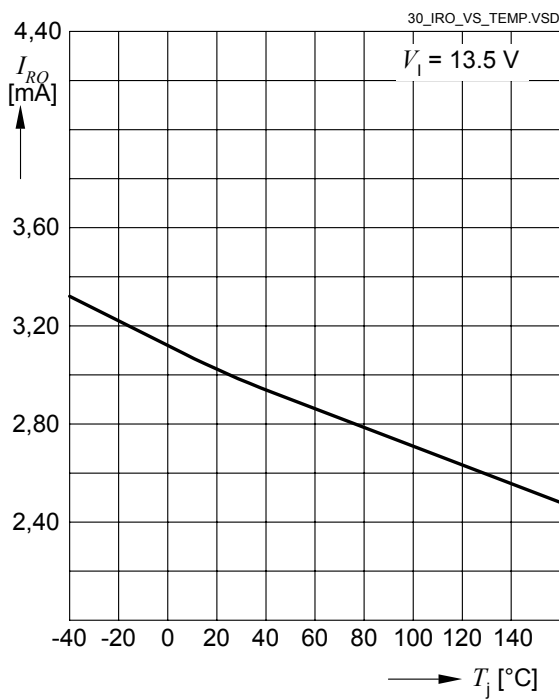
Reset Delay  $t_{RD}$  Time versus Junction Temperature  $T_j$



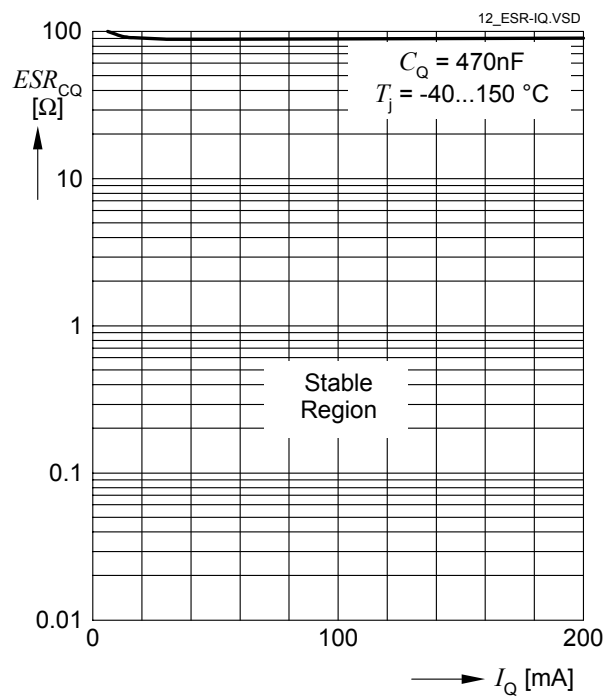
Reset Reaction Time  $t_{RR}$  versus Junction Temperature  $T_j$



Reset Output Sink Current  $I_{RO}$  versus Junction Temperature  $T_j$



Region of Stability  $ESR(C_Q)$  versus Output Current  $I_Q$



## 6 Package Outlines

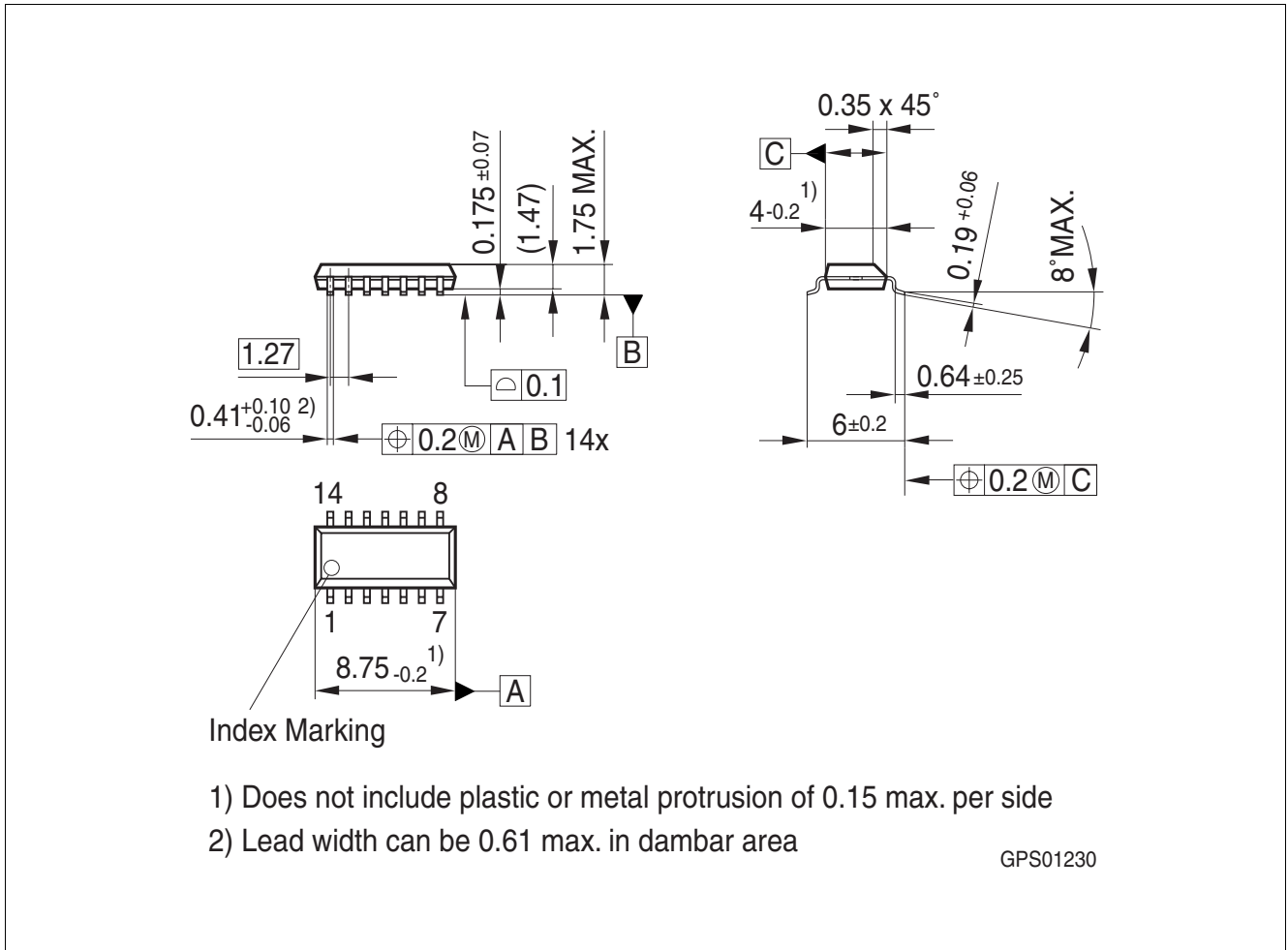


Figure 6 PG-DSO-14 (Plastic/Plastic Green - Dual Small Outline Package)

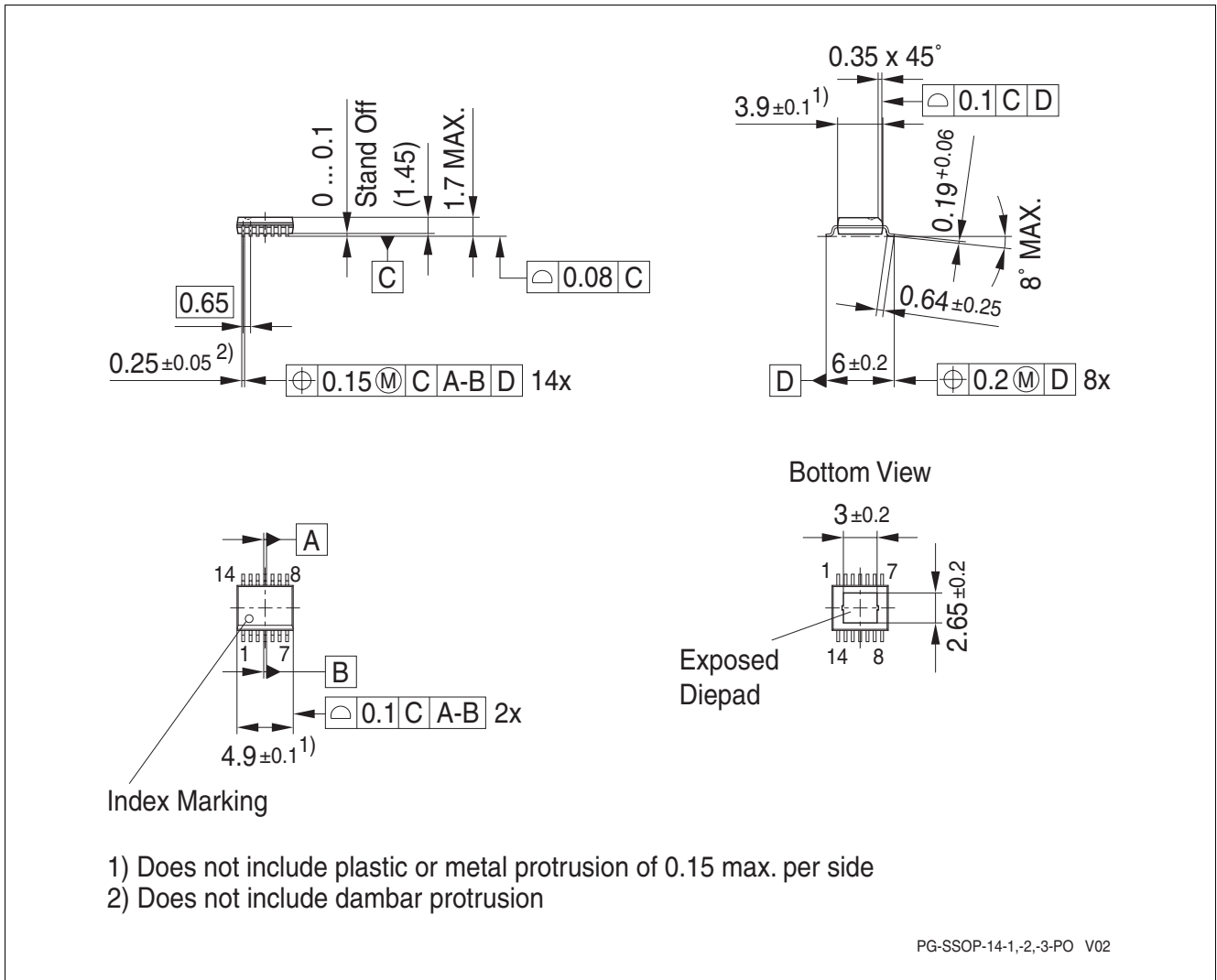


Figure 7 PG-SSOP-14 Exposed Pad

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm

## 7 Revision History

| Revision  | Date       | Changes  |
|---|------------|--|
| 1.2   | 2009-05-08 | 2.6V version, 5V version in PG-SSOP-14 package and all related description added:  |
|   |            | In <b>“Features” on Page 2</b> “or 2.6V” added   |
|   |            | In <b>“Features” on Page 2</b> package drawing for PG-DSO-14 updated, package drawing for PG-SSOP-14 added   |
|   |            | In <b>“Overview” on Page 2</b> in table at the bottom types “TLE7278-2GV26” and TLE7279-2EV50” added   |
|   |            | In <b>Table 2.2 “Pin Definitions and Functions (PG-DSO-14)” on Page 3</b> in description for Pin 1 and Pin 7 “, TLE7273-2GV26” added   |
|   |            | In <b>“Pin Assignment (PG-DSO-14)” on Page 3</b> “(PG-DSO-14)” added; In <b>“Pin Definitions and Functions (PG-DSO-14)” on Page 3</b> “(PG-DSO-14)” added;   |
|   |            | In <b>Table 2.2 “Pin Definitions and Functions (PG-DSO-14)” on Page 3</b> in description for pin 1 “; leave open if Reset is not needed” added   |
|   |            | <b>“Pin Assignment (PG-SSOP-14 Exposed Pad)” on Page 4</b> and <b>“Pin Definitions and Functions (PG-SSOP-14 Exposed Pad)” on Page 4</b> added   |
|   |            | In <b>“Functional Range” on Page 7 Item 4.2.3</b> added, in <b>Item 4.2.1</b> “, TLE7279-2EV50” added  |
|   |            | In <b>Table 4.3 “Thermal Resistance” on Page 7</b> above <b>Item 4.3.1</b> line with “Package PG-DSO-14” and values for PG-SSOP-14 package added: <b>Item 4.3.6</b> , <b>Item 4.3.7</b> , <b>Item 4.3.8</b> , <b>Item 4.3.9</b> , and <b>Item 4.3.10</b> added |
|   |            | In <b>“Power On Reset and Reset Output” on Page 8</b> “and TLE7279-2EV50” in description added   |
|   |            | 1.1  |
| In <b>“Typical Performance Characteristics” on Page 14</b> Graphs <b>“Reset Threshold VRT versus Junction Temperature Tj (3.3V-Version)” on Page 18</b> , <b>“Reset Hysteresis versus Junction Temperature Tj (3.3V-Version)” on Page 18</b> , <b>“Reset Threshold VRT versus Junction Temperature Tj (2.6V-Version)” on Page 18</b> and <b>“Reset Hysteresis versus Junction Temperature Tj (2.6V-Version)” on Page 18</b> added |            |  |
| In <b>“Package Outlines” on Page 20</b> Outlines for PG-SSOP-14 package added: <b>Figure 7</b>  |            |  |
| 3.3V version and all related description added:   |            |  |
| In <b>“Features” on Page 2</b> “3.3V” added   |            |  |
| In <b>“Overview” on Page 2</b> in table at the bottom type “TLE7273-2GV33” added  |            |  |
| In <b>“Pin Definitions and Functions (PG-DSO-14)” on Page 3</b> in description for Pin 1 and Pin 7 “TLE7273-2GV33: open drain output;” added  |            |  |
| In <b>“Functional Range” on Page 7 Item 4.2.2</b> added   |            |  |

## Revision History

| Revision | Date       | Changes   |
|----------|------------|---|
|          |            | In <b>“Power On Reset and Reset Output” on Page 8</b> description for dimensioning external pull-up resistor at RO added  |
|          |            | In <b>“Electrical Characteristics” on Page 10</b> all specific Items for 3.3V version added: <b>Item 5.2.3, Item 5.2.4, Item 5.2.20, Item 5.2.29, Item 5.2.34, Item 5.2.36, Item 5.2.38, Item 5.2.41</b> and <b>Item 5.2.45</b> added |
| 1.0      | 2008-04-10 | final version data sheet  |

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