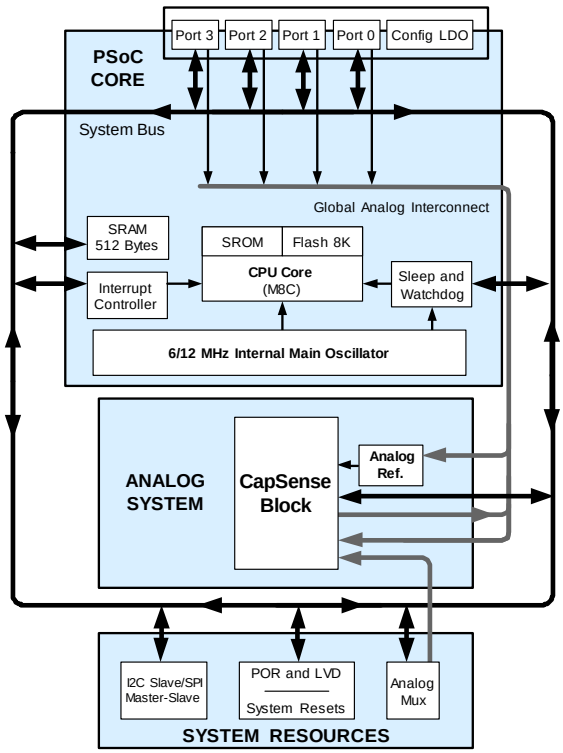
CY8C20234

Automotive PSoC® Programmable System-on-Chip

Features

- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports combination of CapSense buttons, sliders, touch-pads, and proximity sensors
- AEC qualified
- Powerful Harvard architecture processor
  - M8C processor speeds up to 12 MHz
  - Low power at high speed
  - 3.0V to 5.25V operating voltage
  - Automotive temperature range: -40°C to +85°C
- Flexible on-chip memory
  - 8 KB of Flash program storage, 1000 erase/write cycles
  - 512 bytes of SRAM data storage
  - Partial Flash updates
  - Flexible protection modes
  - In-System Serial Programming (ISSP)
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full featured, In-Circuit Emulator (ICE) and Programmer
  - Full speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Precision, programmable clocking
  - Internal ±5% 6/12 MHz oscillator
  - Internal low speed, low power oscillator for Watchdog and Sleep functionality
- Programmable pin configurations
  - 20 mA Sink on all General Purpose I/O (GPIO)
  - Pull up, High Z, open drain, and strong drive modes on all GPIO
  - Up to 13 analog inputs on GPIO
  - Configurable inputs on all GPIO
  - Selectable, Regulated Digital I/O on Port 1
    - 3.0V, 2.4V, and 1.8V Regulation Available
    - Up to 5 mA Source on Port 1 GPIO
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Comparator noise immunity
- Additional system resources
  - Configurable communication speeds
    - I^2C™: Selectable to 50 kHz, 100 kHz, or 400 kHz
    - SPI: Configurable between 46.9 kHz and 12 MHz
  - I^2C slave
  - SPI master and SPI slave
  - Watchdog and Sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit

Logic Block Diagram



Contents

PSoC® Functional Overview

The PSoC family consists of many Programmable System-on-Chip with on-chip controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in Figure 1, consists of three main areas: the Core, the System Resources, and the CapSense Analog System. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 13 GPIO are also included. The GPIO provide access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, Internal Main Oscillator (IMO), and Internal Low speed Oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS, 8-bit Harvard architecture microprocessor.

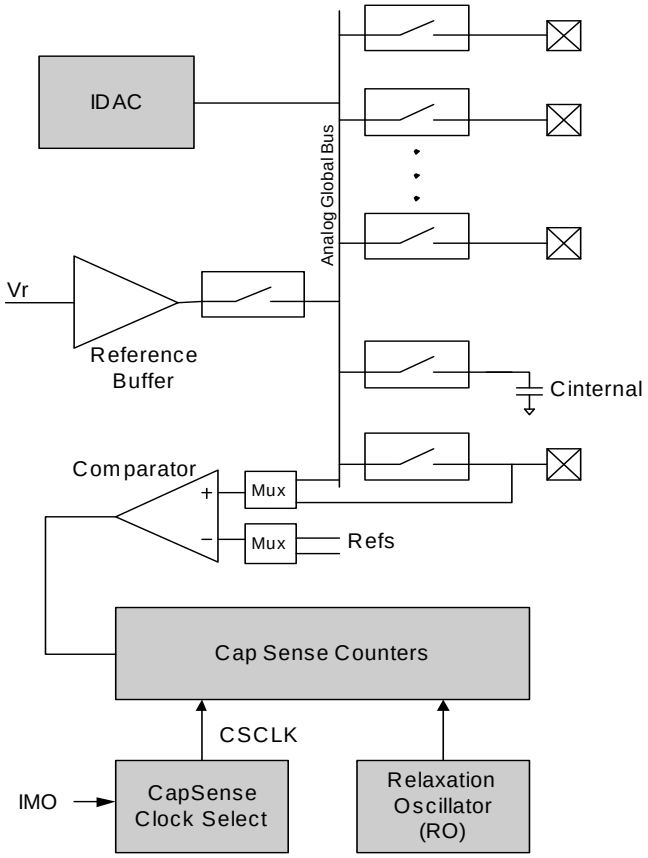
System Resources provide additional capability such as a configurable I^2C slave, SPI slave, or SPI master communication interface and various system resets supported by the M8C.

The Analog System consists of the CapSense® PSoC block and an internal analog reference. Together they support capacitive sensing of up to 13 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combination

Additional System Resources

System Resources provide additional capability useful for complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource are presented below.

- There is a digital module in CY8C20x34 devices that implements an I^2C slave, SPI slave, or SPI master interface.The I^2C slave mode provides 0 to 400 kHz communication over two wires. The SPI master and slave modes provide communication over three or four wires at frequencies of 46.9 kHz to 12 MHz (lower for a slower system clock).
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced Power On Reset (POR) circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for capacitive sensing.
- The 3.0V/2.4V/1.8V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the *Technical Reference Manual* for this PSoC device.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs and are available at http://www.cypress.com.

Development Kits

PSoC Development Kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

Cypros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to http://www.cypress.com and refer to CYPros Consultants.

Solutions Library

Visit our growing library of solution focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE). Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Table 1 lists the acronyms that are used in this document.

Table 1. Acronyms Used

Acronym	Description
AC	Alternating Current
API	Application Programming Interface
CPU	Central Processing Unit
DC	Direct Current
GPIO	General Purpose I/O
GUI	Graphical User Interface
ICE	In-Circuit Emulator
ILO	Internal Low Speed Oscillator
IMO	Internal Main Oscillator
I/O	Input Or Output
LSb	Least Significant Bit
LVD	Low Voltage Detect
MSb	Most Significant Bit
POR	Power On Reset
PPOR	Precision Power On Reset
PSoC	Programmable System-on-Chip
SLIMO	Slow IMO
SRAM	Static Random Access Memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3 on page 9 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are in decimal format.

Pinouts

This section describes, lists, and illustrates the CY8C20x34 PSoC device pins and pinout configurations.

The automotive CY8C20x34 PSoC device is available in the packages listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and can connect to the common analog bus. However, Vss, Vdd, and XRES are not capable of digital I/O.

16-Pin Part Pinout

Figure 2. CY8C20234 16-Pin PSoC Device

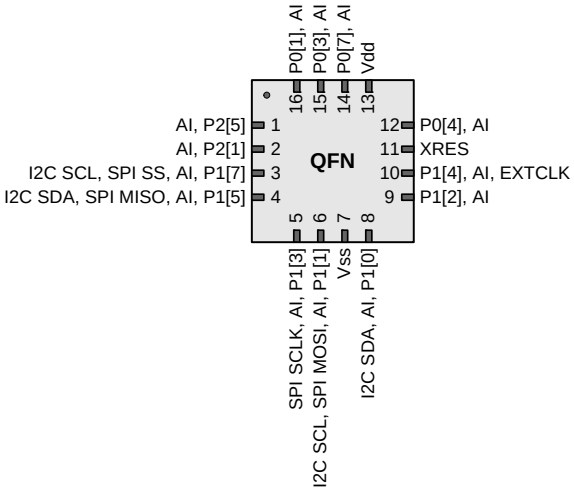


Table 2. Pin Definitions - CY8C20234 16-Pin (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I/OH	I	P1[7]	I^2C Serial Clock (SCL), SPI Slave Select (SS)
4	I/OH	I	P1[5]	I^2C Serial Data (SDA), SPI Master-In-Slave-Out (MISO)
5	I/OH	I	P1[3]	SPI Serial Clock (SCLK)
6	I/OH	I	P1[1]	ISSP-SCLK[1], I^2C Serial Clock (SCL), SPI Master-Out-Slave-In (MOSI)
7	Power		Vss	Ground Connection
8	I/OH	I	P1[0]	ISSP-SDATA[1], I^2C Serial Data (SDA)
9	I/OH	I	P1[2]	
10	I/OH	I	P1[4]	Optional External Clock Input (EXTCLK)
11	Input		XRES	Active High External Reset with Internal Pull Down
12	I/O	I	P0[4]	
13	Power		Vdd	Supply Voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating Input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
1. These are the ISSP pins, that are not High Z after exiting a reset state. See the *PSoC Technical Reference Manual* for CY8C20x34 devices for details.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C20x34 PSoC device. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C as specified, except where mentioned.

Refer to Table 12 on page 14 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 3. Voltage versus CPU Frequency

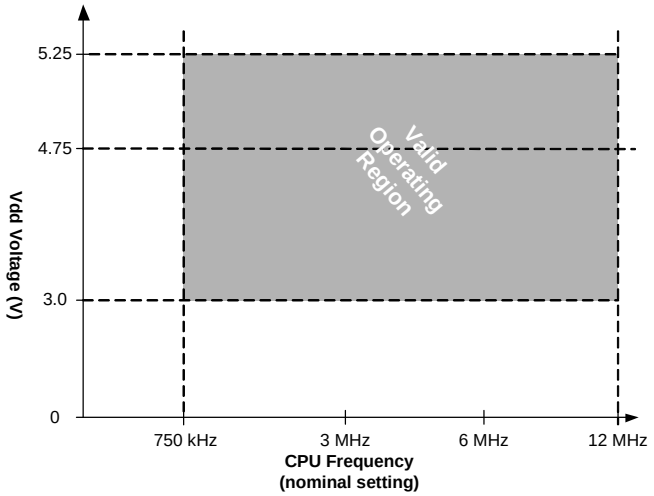


Figure 4. IMO Frequency Trim Options

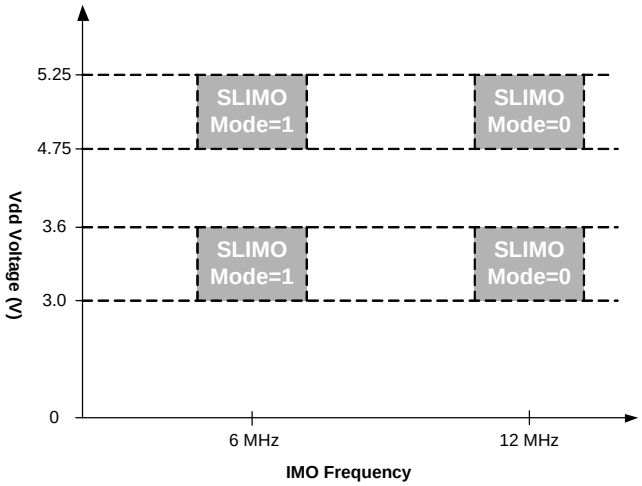


Table 3 lists the units of measure that are used in this section.

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milliampere
fF	femto farad	ms	millisecond
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
$T_{BAKETEMP}$	Bake Temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	–	72	Hours	
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 20 on page 18. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 6 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 6. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See Table 9 on page 12.
I_{DD12}	Supply Current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 12 MHz.
I_{DD6}	Supply Current, IMO = 6 MHz	–	1	1.5	mA	Conditions are Vdd = 3.0V, T_A = 25°C, CPU = 6 MHz
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and ILO Active.	–	2.8	5	µA	Vdd = 3.3V, -40°C ≤ T_A ≤ 85°C

DC General Purpose I/O Specifications

Table 7 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 7. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
V_{OH1}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.2	–	–	V	I_{OH} ≤ 10 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High Output Voltage Port 0, 2, or 3 Pins	Vdd - 0.9	–	–	V	I_{OH} ≤ 1 mA, Vdd ≥ 3.0V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.2	–	–	V	I_{OH} ≤ 10 µA, Vdd ≥ 3.0V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High Output Voltage Port 1 Pins with LDO Regulator Disabled	Vdd - 0.9	–	–	V	I_{OH} ≤ 5 mA, Vdd ≥ 3.0V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High Output Voltage Port 1 Pins with 3.0V LDO Regulator Enabled	2.7	3.0	3.3	V	I_{OH} ≤ 10 µA, Vdd ≥ 3.1V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High Output Voltage Port 1 Pins with 3.0V LDO Regulator Enabled	2.2	–	–	V	I_{OH} ≤ 5 mA, Vdd ≥ 3.1V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High Output Voltage Port 1 Pins with 2.4V LDO Regulator Enabled	2.1	2.4	2.7	V	I_{OH} ≤ 10 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High Output Voltage Port 1 Pins with 2.4V LDO Regulator Enabled	2.0	–	–	V	I_{OH} ≤ 200 µA, Vdd ≥ 3.0V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.6	1.8	2.0	V	I_{OH} ≤ 10 µA 3.0V ≤ Vdd ≤ 3.6V 0°C ≤ T_A ≤ 85°C Maximum of 20 mA source current in all I/Os.

Table 7. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OH10}	High Output Voltage Port 1 Pins with 1.8V LDO Regulator Enabled	1.5	–	–	V	$I_{OH} \le 100$ µA. 3.0V ≤ Vdd ≤ 3.6V. 0°C ≤ T_A ≤ 85°C. Maximum of 20 mA source current in all I/Os.
V_{OL}	Low Output Voltage	–	–	0.75	V	$I_{OL} \le 20$ mA, Vdd ≥ 3.0V, maximum of 60 mA sink current on even port pins (for example, P0[4] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{IL}	Input Low Voltage	–	–	0.8	V	
V_{IH}	Input High Voltage	2.0	–		V	
V_H	Input Hysteresis Voltage	–	140	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive Load on Pins as Input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C
C_{OUT}	Capacitive Load on Pins as Output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25°C

DC Analog Mux Bus Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 8. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch Resistance to Common Analog Bus	–	–	450	Ω	

DC POR and LVD Specifications

Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 9. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip					Vdd is greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.34	2.45	2.51[3]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[4]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[5]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.44	4.73	4.93	V	

DC Analog Reference Specifications

Table 10 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 10. DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap Reference Voltage	1.274	1.30	1.326	V	

DC Programming Specifications

Table 11 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only. Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25°C ± 20°C during the Flash Write operation. Refer to the EEPROM User Module data sheet instructions for EEPROM Flash Write requirements outside of the 25°C ± 20°C temperature window.

Table 11. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	3.0	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ILP} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull down resistor.
I_{IHP}	Input Current when Applying V_{IHP} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd -1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)[6]	1,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[7]	128,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Notes
3. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
4. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
5. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.
6. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0V to 3.6V and 4.75V to 5.25V.
7. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 12. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency	0.71	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	Internal Low Speed Oscillator (ILO) Frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO Untrimmed Frequency	5	–	–	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{IMO12}	Internal Main Oscillator (IMO) Stability for 12 MHz	11.4	12	12.6	MHz	Trimmed using factory trim values. See Figure 4 on page 9, SLIMO Mode = 0.
F_{IMO6}	IMO Stability for 6 MHz	5.5	6.0	6.5	MHz	Trimmed using factory trim values. See Figure 4 on page 9, SLIMO Mode = 1.
DC_{IMO}	Duty Cycle of IMO	40	50	60	%	
DC_{ILO}	ILO Duty Cycle	20	50	80	%	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
$SR_{POWERUP}$	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power up from 0V.

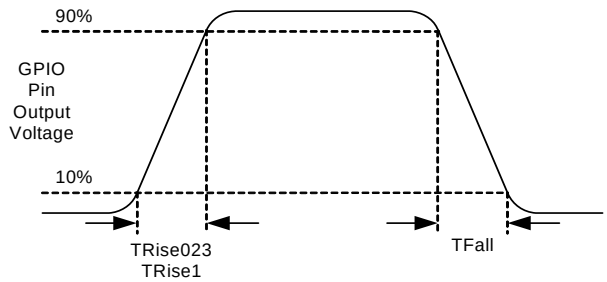
AC General Purpose I/O Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 13. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	6.30	MHz	Normal Strong Mode, Port 1.
TRise023	Rise Time, Strong Mode, Cload = 50 pF Ports 0, 2, 3	15	–	80	ns	Vdd = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%
TRise1	Rise Time, Strong Mode, Cload = 50 pF Port 1	10	–	50	ns	Vdd = 3.0V to 3.6V, 10% - 90%
TFall	Fall Time, Strong Mode, Cload = 50 pF All Ports	10	–	50	ns	Vdd = 3.0V to 3.6V and 4.75V to 5.25V, 10% - 90%

Figure 5. GPIO Timing Diagram



AC Comparator Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 14. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Response Time, 50 mV Overdrive	– –	– –	100 200	ns ns	Vdd > 3.6V 3.0V ≤ Vdd ≤ 3.6V

AC External Clock Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and –40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 15. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High Period	38	–	5300	ns	
–	Low Period	38	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and –40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 16. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	40	ms	
T_{WRITE}	Flash Block Write Time	–	40	160	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6V
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0V ≤ Vdd ≤ 3.6V
T_{PRGH}	Total Flash Block Program Time (T_{ERASEB} + T_{WRITE}), Hot	–	–	100	ms	T_J ≥ 0°C
T_{PRGC}	Total Flash Block Program Time (T_{ERASEB} + T_{WRITE}), Cold	–	–	200	ms	T_J < 0°C

AC SPI Specifications

Table 17 and Table 18 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 17. SPI Master AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{SCLK}	SCLK clock frequency	–	–	12.6	MHz	
DC_{SCLK}	SCLK duty cycle	–	50	–	%	
T_{SETUP}	MISO to SCLK setup time	40	–	–	ns	
T_{HOLD}	SCLK to MISO hold time	40	–	–	ns	
T_{OUT_VAL}	SCLK to MOSI valid time	–	–	40	ns	
T_{OUT_HIGH}	MOSI high time	40	–	–	ns	

Table 18. SPI Slave AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{SCLK}	SCLK clock frequency	–	–	12.6	MHz	
T_{LOW}	SCLK low time	39.6	–	–	ns	
T_{HIGH}	SCLK high time	39.6	–	–	ns	
T_{SETUP}	MOSI to SCLK setup time	30	–	–	ns	
T_{HOLD}	SCLK to MOSI hold time	50	–	–	ns	
T_{SS_MISO}	SS low to MISO valid	–	–	153	ns	
T_{SCLK_MISO}	SCLK to MISO valid	–	–	125	ns	
T_{SS_HIGH}	SS high time	50	–	–	ns	
T_{SS_SCLK}	Time from SS low to first SCLK	$2/F_{SCLK}$	–	–	ns	
T_{SCLK_SS}	Time from last SCLK to SS high	$2/F_{SCLK}$	–	–	ns	

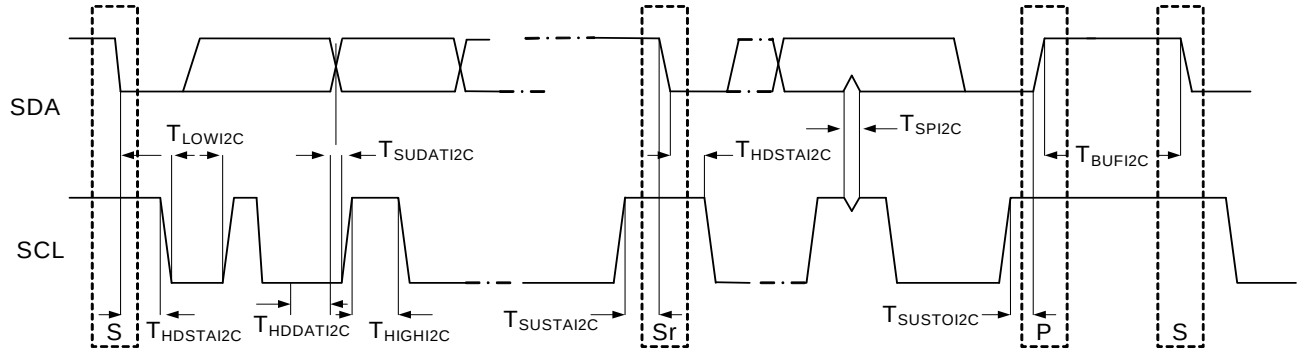
AC I²C Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Table 19. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL Clock Frequency	0	100[8]	0	400[8]	kHz
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs
$T_{SUDATI2C}$	Data Setup Time	250	–	100[9]	–	ns
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 6. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

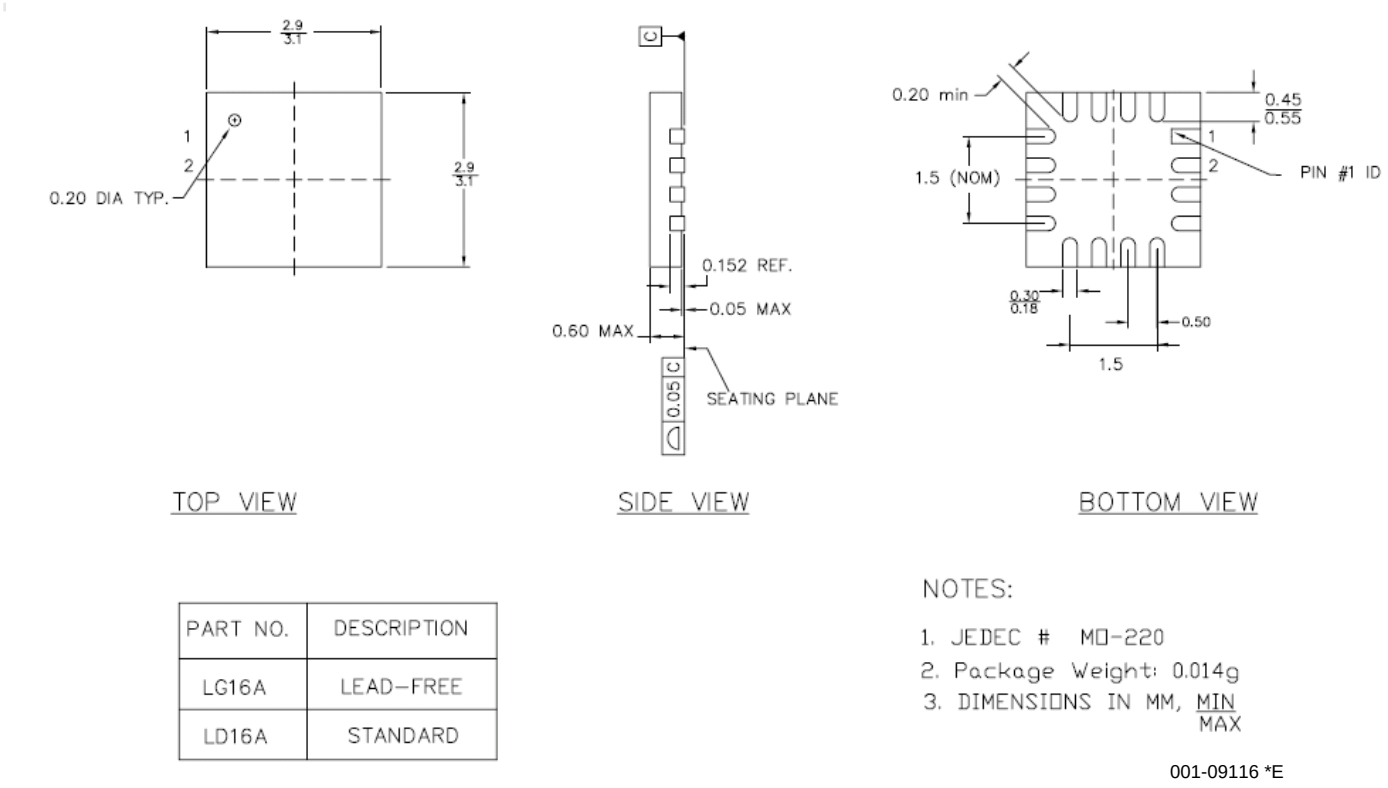
8. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 12 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
9. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Packaging Information

This section illustrates the packaging specifications for the automotive CY8C20x34 PSoC device along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 7. 16-Pin Chip On Lead 3 x 3 mm Package Outline (Sawn)



Important Note For information on the preferred dimensions for mounting QFN packages, see the application note “Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.

Thermal Impedances

Table 20 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 20. Thermal Impedances Per Package

Package	Typical θ_{JA} [9]
16 QFN	46 °C/W

Solder Reflow Peak Temperature

Table 21 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 21. Solder Reflow Peak Temperature

Package	Min Peak Temperature [10]	Max Peak Temperature
16 QFN	240 °C	260 °C

Notes
9. $T_J = T_A + \text{Power} \times \theta_{JA}$.
10. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for the CY8C20x34 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer also supports the advance emulation features. The kit includes:

- ICE-Cube Unit
- 28-Pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

CY3280-BK1

The Universal CapSense Control Kit is designed for easy prototyping and debug of CapSense designs with pre defined control circuitry and plug-in hardware. The kit comes with a control boards for CY8C20x34 and CY8C21x34 devices as well as a breadboard module and a button(5)/slider module.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-20X34 Evaluation Pod (EvalPod)

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-20X34 provides evaluation of the CY8C20x34 PSoC device family.

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 22. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [12]	Foot Kit [13]	Prototyping Module	Adapter [14]
CY8C20234-12LKXA	16 QFN	-	-	CY3210-20X34	-

Notes
12. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
13. Foot kit includes surface mount feet that is soldered to the target PCB.
14. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is found at http://www.emulation.com.

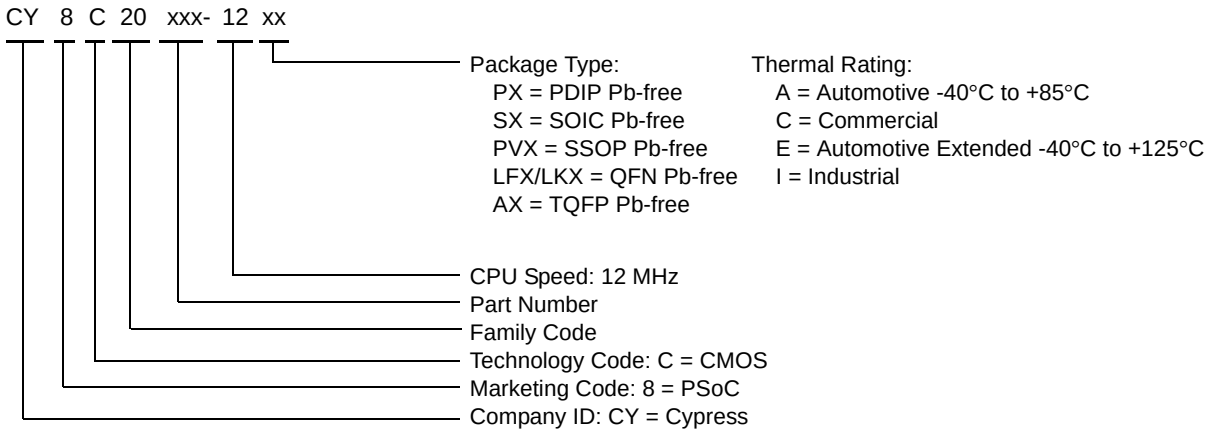
Ordering Information

Table 23 lists the automotive CY8C20x34 PSoC device key package features and ordering codes.

Table 23. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20234-12LKXA	16-Pin (3 x 3 x 0.60 mm) Sawn QFN	8K	512	0	1	13	13[15]	0	Yes
CY8C20234-12LKXAT	16-Pin (3 x 3 x 0.60 mm) Sawn QFN (Tape and Reel)	8K	512	0	1	13	13[15]	0	Yes

Ordering Code Definitions



Note
15. Digital I/O pins also connect to the common analog mux.

Document History Page

Document Title: CY8C20234 Automotive PSoC® Programmable System-on-Chip Document Number: 001-54650				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2743436	MASJ/AESA	07/24/09	New data sheet.
*A	2799448	BTK	11/05/09	Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections to improve consistency. Added clarifying comments to some electrical specifications. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Improved and edited content in Development Tool Selection section. Improved the bookmark structure. Changed $Flash_{ENT}$, F_{OSCEXT}, T_{ERASEB}, and T_{WRITE} electrical specifications according to MASJ input. Added and slightly modified the expanded SPI AC specifications from 001-05356 Rev *I. Added a table of contents.This revision fixes CDT 61474.
*B	2822792	BTK/AESA	12/07/2009	Added T_{PRGH}, T_{PRGC}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the footnotes for Table 11, “DC Programming Specifications,” on page 13. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Changed F_{IMO6} electrical specification to have an 8.33% accuracy instead of 5%. Added “Contents” on page 2. This revision fixes CDT 63984.
*C	2888007	NJF	03/30/2010	Updated Cypress website links. Updated CapSense Analog System. Removed PSoC Designer 4.4 reference in PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Removed DC Low Power Comparator Specifications, AC Analog Mux Bus Specifications, and AC Low Power Comparator Specifications. Updated Packaging Information. Added Solder Reflow Peak Temperature. Removed Third Party Tools and Build a PSoC Emulator into Your Board. Updated links in Sales, Solutions, and Legal Information.
*D	3043236	ARVM	09/30/10	Under section "AC Comparator Amplifier Specifications", the caption for spec table changed from "AC Operational Amplifier Specifications" to “AC Comparator Specifications”. Also the section heading changed to AC Comparator specifications.

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