MIK2152 Video Decoder Preliminary Specification

(Rev. 1.4)

February 2007

MIKTAM Technologies, Inc.

REVISION HISTORY: (last updated on February 27, 2007)

1. Rev 1.0 with the updated registers details – Tom 01/09/06

Date	Revision	Description	In-charger
9/3/05	1.0	Published spec	Tom
3/16/06	1.1	Revise Pin 3 & pin 7	Tom
8/21/06	1.2	Revise supported video formats; document built-in color bars	Tom
2/26/07	1.4	Add chip level block diagram	Tom

1. Introduction

The MIK2152 device is an ultra-low power NTSC/PAL video decoder. Available in a popular space saving 32-pin TQFP package, the MIK2152 decoder converts NTSC, PAL video signals to 8-bit CCIR 656 format. Discrete syncs are also available. The MIK2152 decoder has an ultra-low power consumption, around 150 mW of power in typical operation and consumes less than 1 mW in power down mode, which increasing battery life in hand-held application. The decoder uses just one crystal for all supported standards. The MIK2152 decoder can be programmed using an I^2C serial interface. The decoder uses a 1.8 v power supply for its digital and analog circuits and 3.3 v power supply for its I/O.

The MIK2152 decoder converts base band analog video into digital YCbCr 4:2:2 component video. Composite and S-video inputs are supported. The MIK2152 decoder includes one 10-bit analog-to-digital converter (ADC) with 2x sampling rate. Sampling is CCIR 601 (27.0 MHz, generated from the 27.0 MHz or other common used crystals). The output format can be 8-bit 4:2:2 or 8-bit CCIR 656 with embedded synchronization.

Complementary 5 line adaptive comb filtering is available for both the luma and chroma data paths to reduce both cross-luma and cross-chroma artifacts.

Video characteristics including hue, contrast, brightness, saturation, and sharpness may be programmed using the industry standard I^2C serial interface. The MIK2152 decoder generates synchronization, blanking, lock, and clock signals in addition to digital video outputs.

The MIK2152 decoder detects copy-protected input signals according to the Macrovision™ standard.

The main blocks of the MIK2152 decoder include:

- Sync detector
- ADC with clamping and Automatic Gain Control (AGC)
- Y/C separation using 5-line adaptive comb filter
- Chroma processor
- Luma processor
- Video clock/timing processor and power-down control
- I^2C interface
- Macrovision™ detection for composite and S-video

1.1 Features

- Accepts NTSC (M), PAL (B, D, G, H, I, M, Nc)
- Support CCIR 601 standard sampling
- High-speed 10-bit ADC
- Two composite inputs or one S-video input
- Fully differential CMOS analog pre-processing channel with clamping and automatic gain control (AGC) for the best signal-to-noise performance.
- Ultra-low power consumption: around 150 mW typical
- Power-down mode: <1 mW

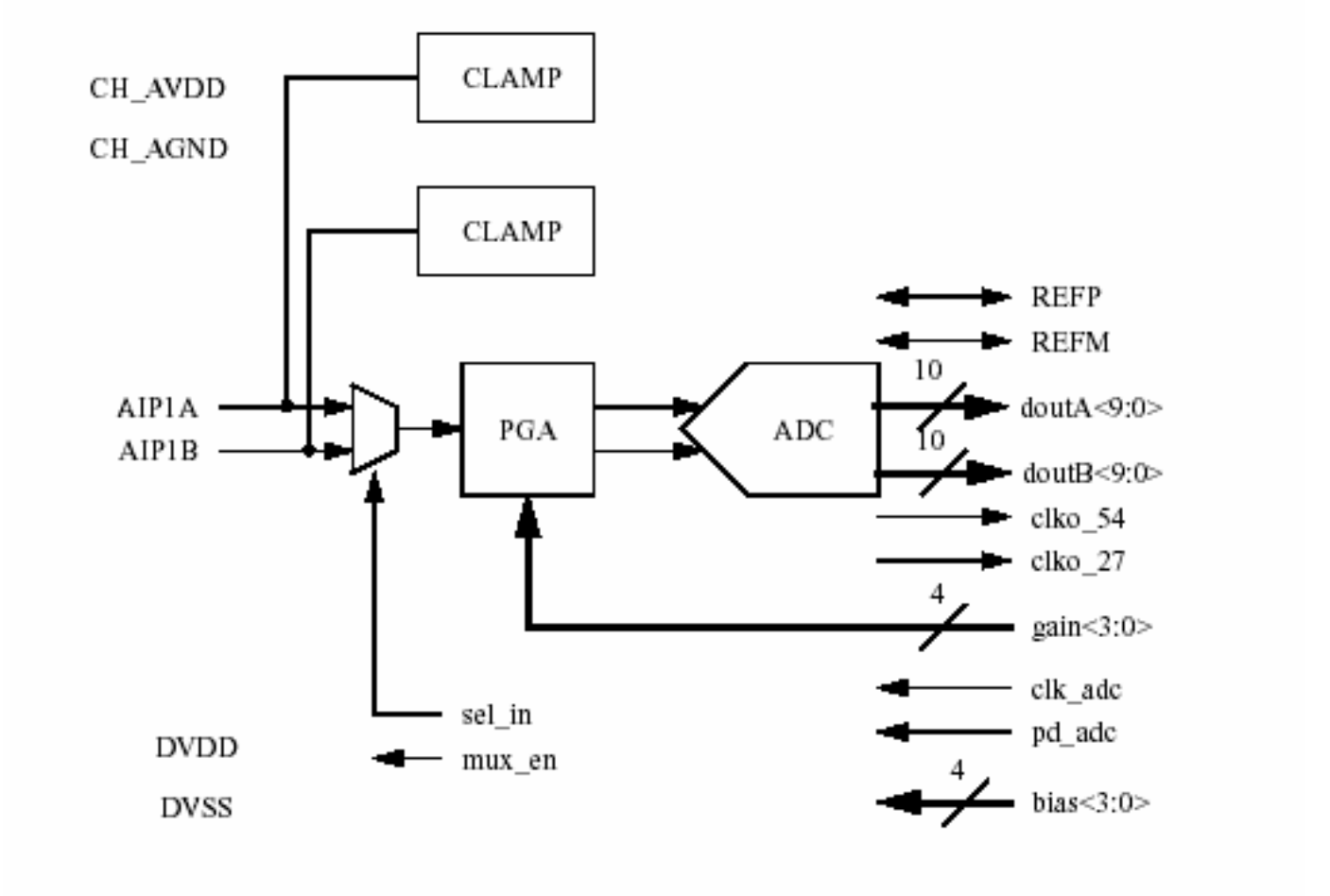
- Popular 32-pin TQFP
- Using I^2C for brightness, contrast, saturation, hue, and sharpness control
- Complementary 5-line adaptive comb filters for both cross-luma and cross-chroma noise reduction
- Special architecture for locking to weak, noisy, or unstable signals
- Single 27.0 MHz or other common used crystal for all standards
- Internal phase-locked loop (PLL) for signal clock and sampling
- Subcarrier Genlock output for synchronizing color subcarrier of external encoder
- Standard programmable video output format:
  - CCIR 656 8-bit 4:2:2 with embedded syncs
  - 8-bit 4:2:2 with discrete syncs (CCIR 601)
- Macrovision^{TM} copy protection detection
- Power-on reset

1.2 Application

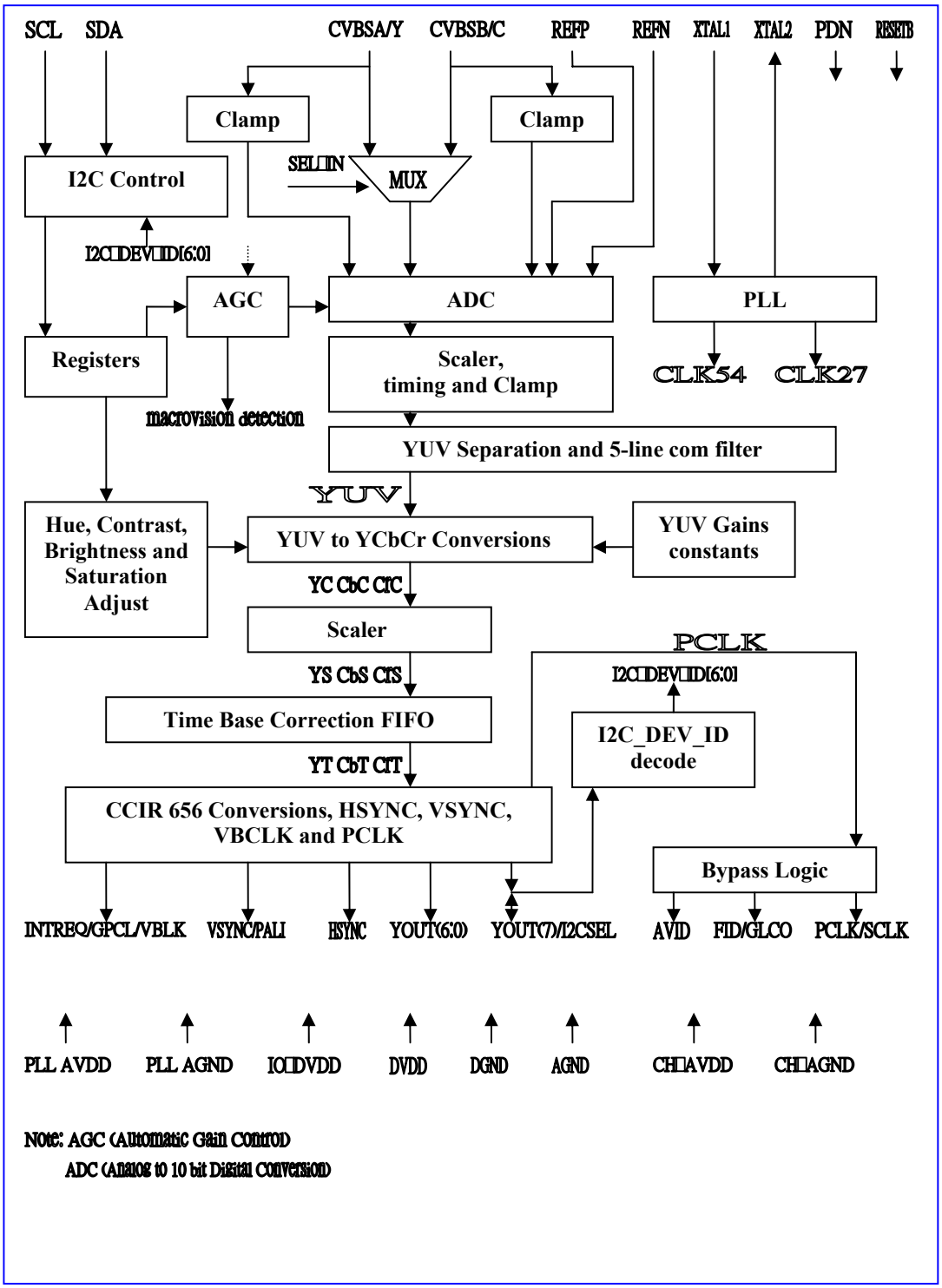
Following is a partial list of suggested application:

- Digital TV
- PDA
- Notebook PC
- Cellular phone
- Video recoder/player
- Internet/web appliances
- Handheld games
- Surveillance system
- Personal media player
- Video capture

1.2 Analog Front-end Functional Block Diagram

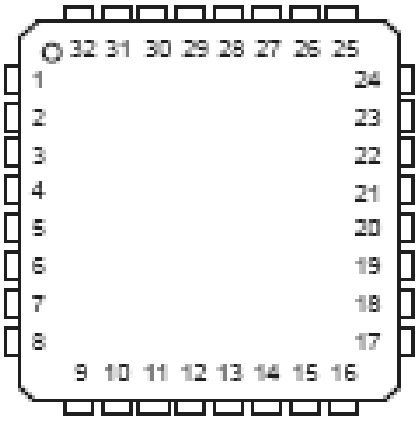


1.3 Chip Level Functional Block Diagram



1.4 Terminal Assignment

Pin #1: CVBSA/Y
Pin #2: CVBSB/C
Pin #3: AGND
Pin #4: PLL_AVDD
Pin #5: XTAL1
Pin #6: XTAL2
Pin #7: PLL_AGND
Pin #8: RESETB
Pin #9: PCLK/SCLK
Pin #10: IO_DVDD
Pin #11: YOUT(7)/I2CSEL
Pin #12: YOUT(6)
Pin #13: YOUT(5)
Pin #14: YOUT(4)
Pin #15: YOUT(3)
Pin #16: YOUT(2)



Pin #17: YOUT(1)
Pin #18: YOUT(0)
Pin #19: DGND
Pin #20: DVDD
Pin #21: SCL
Pin #22: SDA
Pin #23: FID/GLCO
Pin #24: VSYNC/PAL1
Pin #25: HSYNC
Pin #26: AVID
Pin #27: INTREQ/GPCL/ VBLK
Pin #28: PDN
Pin #29: REFP
Pin #30: REFM
Pin #31: CH_AGND
Pin #32: CH_AVDD

1.5 Terminal Functions

TERMINAL NAME	NUMBER	TYPE		DESCRIPTION
CVBSA/Y	1	Analog	Input	Analog input. Connect to the video analog input via 0.1-µF capacitor. The maximum input range is 0-1.2 V_{PP}, and may require an attenuator to reduce the input amplitude to the desire level. If not used, connect to AGND via 0.1- µF capacitor.
CVBSB/C	2	Analog	Input	Analog input. Connect to the video analog input via 0.1-µF capacitor. The maximum input range is 0-1.2 V_{PP}, and may require an attenuator to reduce the input amplitude to the desire level. If not used, connect to AGND via 0.1- µF

TERMINAL NAME	NUMBER	TYPE		DESCRIPTION
				capacitor.
AGND	3	Analog	Input	Substrate. Connect to analog ground
PLL_AVDD	4	Analog	Input	PLL power supply. Conncet to 1.8-V analog power supply
XTAL1	5		Input	External clock reference. XTAL1 can be connected to an oscillator or to one terminal of a crystal oscillator. XTAL2 may be connected to the other terminal of the crystal or not connected at all. One signal 27.0 MHz or other common used crystal is needed for CCIR 601 sampling, for all supported standards.
XTAL2	6		Output	
PLL_AGND	7	Analog	Input	PLL ground. Connect to analog ground
RESETB	8	Digital	Input	Active-low reset. RESETB can be used only when PDN=1. When RESETB is pulled low, it resets all the registers.
PCLK/SCLK	9	Digital	Output	System Clock
IO_DVDD	10	Digital	Input	Digital power supply. Connect to 3.3 V
YOUT(7)/I2CSEL	11	Digital	I/O	I2CSEL: Determines the address for I^2C (sampled during reset). 1 = Address is 0xBA 0 = Address is 0xB8 YOUT7: MSB of output decoded CCIR 656 output/YCbCr 4:2:2 output.
YOUT(6:0)	12-18	Digital	I/O	Output decoded CCIR-656 output/YCbCr 4:2:2 output with discrete sync.
DGND	19	Digital	Input	Digital ground
DVDD	20	Digital	Input	Digital power supply. Connect to 1.8-V digital power supply.
SCL	21	Digital	I/O	I^2C serial clock (open drain)
SDA	22	Digital	I/O	I^2C serial data (open drain)
FID/GLCO	23	Digital	Output	FID: Odd/even field indicator or vertical lock indicator. For the odd/even indicator, a 1 indicates the odd field. GLCO: This serial output carries color PLL information. A slave device can decode the information to allow chroma frequency control from the MIK2152 decoder.
VSYNC/PALI	24	Digital	Output	VSYNC: Vertical synchronization signal PALI: PAL line indicator or horizotal lock indicator For the PAL line indicator, a 1 indicates noninverted line, and a 0 indicates an inverted line.
HSYNC	25	Digial	Output	Horizotal synchronization signal
AVID	26	Digital	Output	Activate video indicator. The signal is high during the horizontal active time of the video output.
INTREQ/GPCL/ VBLK	27	Digital	I/O	INTREQ: Interrupt request output. GPCL: General-purpose control logic. This terminal has two functions: 1. General-purpose output. In this mode, the state of GPCL is dirrectly programmed vis I^2C.

TERMINAL NAME	NUMBER	TYPE		DESCRIPTION
				2. Vertical blank output. In this mode, the GPCL terminal is used to indicate the vertical blanking interval of the output video. The beginning and end times of this signal are programmed via I^2C.
PDN	28	Digital	Inputs	Power-down signal (active low). Put the decoder in standby mode
REFP	29		Input	ADC reference power supply. Connect to analog ground through 1-μF capacitor.
REFM	30		Input	ADC reference ground. Connect to analog ground through 1-μF capacitor.
CH_AGND	31	Analog	Input	Analog ground
CH_AVDD	32	Analog	Input	Analog power supply. Connect to 1.8-V analog power supply

2. Internal Control Registers

ADDRESS	DEFAULT	R/W	REGISTER FUNCTION
00h	01h	R/W	Video input format control
01h	F8h	R/W	Brightness control
02h	A0h	R/W	Contrast control
03h	A2h	R/W	Saturation control
04h	80h	R/W	Hue control
05h	00h	R/W	Decoder operation I
06h	00h	R/W	Decoder operation II
07h	00h	R/W	AGC Adjustment and Clock Mode
08h	B8h	R/W	AGC control
09h	0Ah	R/W	Color processing
0Ah	20h	R/W	Clamp delay control
0Bh	00h	R/W	Clamp position adjustment
0Ch	88h	R/W	Reference settings
0Dh	00h	R/W	U and V swap control
0Eh	00h	R/W	Subcarrier phase adjustment
0Fh	00h	R/W	System test mode
10h	00h	R/W	Debug mode
11h	03h	R/W	Digital clamp
12h	---	---	Reserved
13h	---	---	Reserved
14h	00h	R/W	ADC gain and bias

2.1 Register Definition

2.1.1 Reg_00 Video Input Format Control Register

Address	00h
Default	8'b00000001

7	6	5	4	3	2	1	0
Bars[1:0]		PED	SVID[1:0]		MMode[1:0]		StdV

StdV=Reg_00[0]
1 : standard video input, (NTSC or PAL)
0 : for PAL(M) & PAL(Nc)

MMode[1:0]=Reg_00[2:1];
MMode[1]=0 : auto-detected
MMode[1]=1 :
MMode[0]=0, PAL(Nc) or PAL, 625 lines depending on StdV
MMode[0]=1, PAL(M) or NTSC, 525 lines depending on StdV

Case of SVID[1:0]=
2'b11 : S-Video
2'b10 : Composite
2'b0x : Auto-detect

PED=1
If PAL, black=64d
If NTSC, black=72d
PED=0
If PAL, black=64d
If NTSC, black=61d

Case of Bars[1:0]=Reg_00[7:6];
2'b10 : display built-in 75% color bar
2'b11 : display built-in 100% color bar

2.1.2 Reg_01 Brightness Control Register

Address	01h
Default	8'b11111000

Brit = Reg_01[7:0]; signed; default = F8h

2.1.3 Reg_02 Contrast Control Register

Address	02h
Default	8'b10100000

Cont = Reg_02[7:0]; unsigned; default = A0h

2.1.4 Reg_03 Saturation Control Register

Address	03h
Default	8'hA2

Satur = Reg_03[7:0]; unsigned; default = A2h

2.1.5 Reg_04 Hue Control Register

Address	04h
Default	8'h80

Hue = Reg_04[7:0]; unsigned; default = 80h

2.1.6 Reg_05 Decoder Operation Control Register I

Address	05h
Default	8'd0

7	6	5	4	3	2	1	0
VFM[5:0] manual fader control for upper line/lower line fader						DMode[1:0]	

Case DMode[1:0]=
0x : 5 line;
10 : 3 line;
11 : 1 line (bandpass)

Case VFM[5]=
0 : Fade Value is automatic;
1 : Fade Value = VFM[4:0]

2.1.7 Reg_06 Decoder Operation Control Register II

Address	06h
Default	8'd0

7	6	5	4	3	2	1	0
SLM[5:0] manual fader control for single line/comb fader						FM[1:0]	

Case of FM[1:0]=
2'b0x : auto-detect
2'b10 : wide
2'b11 : narrow

Case SLM[5]=
0 : Fade Value is automatic;
1 : Fade Value = SLM[4:0]

2.1.8 Reg_07 AGC Adjustment and Clock Mode Register

Address	07h
Default	8'd0

7	6	5	4	3	2	1	0
CMode		InvClamp	soft_rst	NoBlue	XCAGC	XSAGC	XAGC

XAGC=Reg_07[0]: set to disable automatic gain adjustment (AGC);

XSAGC=Reg_07[1]: set to disable automatic adjustment of Sync Error (SAGC);

XCAGC=Reg_07[2]: set to disable automatic adjustment of Chroma (CAGC);

NoBlue=Reg_07[3]: set to disable insertion of blue screen;

soft_rst=Reg_07[4]: Software reset, active high; after program to 1, then must program to 0

InvClamp=Reg_07[5]: Invert Clamp signal;

CMode[1:0]=Reg_07[7:6] Clock mode
Case of 00 : 54 MHz clock and data
01 : 54 MHz clock and 27 MHz data
1x : 27 MHz clock and data

2.1.9 Reg_08 AGC Control Register

Address	08h
Default	8'hB8

7	6	5	4	3	2	1	0
AGC0[7:0]							

AGC0 = Reg_08[7:0]; default AGC gain;

2.1.10 Reg_09 Color Processing Register

Address	09h
Default	8'h0A

7	6	5	4	3	2	1	0
CCor[1:0]		SbcAdj0[1:0]		CDly[3:0]			

CDly[3:0] = Reg_09[3:0] adjust chroma to luma delay; default = 10d

SbcAdj0[1:0] = Reg_09[5:4] adjust phase of subcarrier for NTSC; default = 0

CCor[1:0] = Reg_09[7:6] control color correction
00: PAL
01: always
1x: never

2.1.11 Reg_0A Clamp delay Control Register

Address	0Ah
Default	8'h20

CDelay = Reg_0A[7:0]; adjust delay of falling edge of Clamp; default =32d

2.1.12 Reg_0B Clamp Position Adjustment Register

Address	0Bh
Default	8'd0

CDstart = Reg_0B[7:0]; value to adjust clamp position

2.1.13 Reg_0C Reference Settings Register

Address	0Ch
Default	8'h88

7	6	5	4	3	2	1	0
BLimit[3:0]				SSlice[3:0]			

SSlice[3:0] = Reg_0C[3:0] slicing level of sync for FPGA control; default = 8

BLimit[3:0] = Reg_0C[7:4] used in identifying unstable burst for FPGA control; default = 8

2.1.14 Reg_0D U and V Swap Control Register

Address	0Dh
Default	8'd0

7	6	5	4	3	2	1	0
---	---	---	---	---	SwpUV[2:0]		

Case of SwpUV[2:0]=

3'b000 : No swap
3'b001 : swap UV when composite and PAL;
3'b010 : swap UV when composite and NTSC;
3'b011 : swap UV when composite;
3'b100 : swap UV;
3'b101 : swap UV when S-Video and PAL;
3'b110 : swap UV when S-Video and NTSC;
3'b111 : swap UV when S-Video;

2.1.15 Reg_0E Subcarrier Phase Adjustment Register

Address	0Eh
Default	8'd0

when Composite and NTSC
    SbcAdj taken from reg_OE[1:0]
when Composite and PAL
    SbcAdj taken from reg_OE[3:2]
when S-Video and NTSC
    SbcAdj taken from reg_OE[5:4]
when S-Video and PAL
    SbcAdj taken from reg_OE[7:6]

2.1.16 Reg_0F System Test Mode Register

Address	0Fh
Default	8'h0

7	6	5	4	3	2	1	0

TSel[3:0]	TOSel[3:0]

TSel[3:0] = Reg_0F[7:4] Used to select test

TOSel[3:0] = Reg_0F[3:0] Used to select outputs in Test Mode

2.1.17 Reg_10 Debug Mode Control Register

Address	10h
Default	8'h00

7	6	5	4	3	2	1	0
		Channel_B	adc_sv_B	digital_debug	pd_pll	pd_xtal	adc_debug

adc_debug = Reg_10 [0]; adc debug mode
pd_xtal = Reg_10 [1]; set to power-down the crystal oscillator for IDDQ test
pd_pll = Reg_10 [2]; set to power-down and bypasses the PLL. In this mode the crystal input goes directly to the ADC clock, so an external 54 MHz clock can be used to drive the ADC and bypass the PLL. This is also for IDDQ test
digital_debug = Reg_10 [3]; by-pass adc; input to digital section directly
adc_sv_B = Reg_10 [4]; set to output S-video portB(C) signal
ChannelB = Reg_10 [5]; set to select port B

2.1.18 Reg_11 Digital Clamp Control Register

Address	11h
Default	8'h03

7	6	5	4	3	2	1	0
					DClamp [2:0]		

DClamp [0]: set, disable analog clamp;
DClamp [1]: set, enable digital clamp on composite or Y of S-video
DClamp [2]: set, enable digital clamp on chroma, C of S-video

2.1.20 Reg_14 ADC Gain and Bias Control Register

Address	14h
Default	8'h00

7	6	5	4	3	2	1	0
ADC_GAIN[3:0]				ADC_BIAS[3:0]			

ADC_GAIN[3:0] = Reg_14[7:4] ADC_GAIN for ADC

ADC_BIAS[3:0] = Reg_14[3:0] ADC_BIAS for ADC

3. Electrical Specifications

3.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range

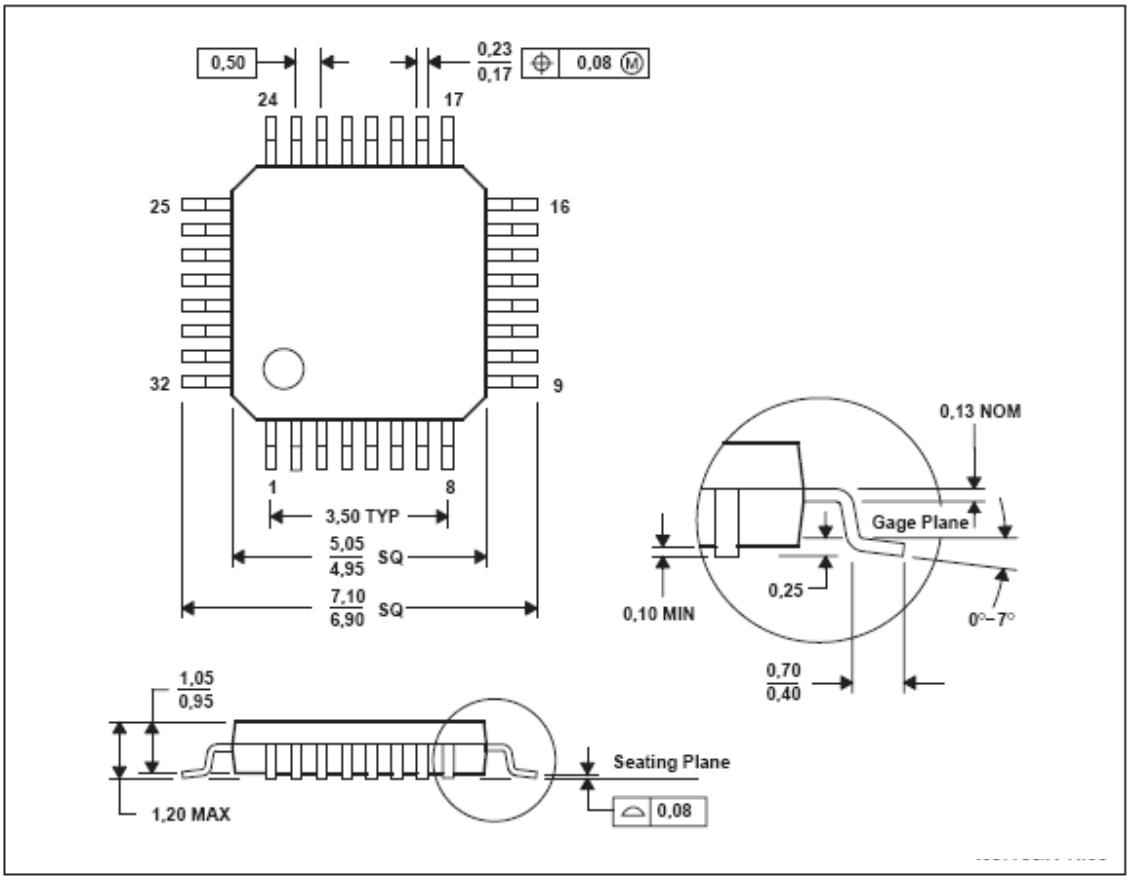
Supply voltage range: IOV_{DD} to DGND . . . . . -0.5 V to 4.5 V
DV_{DD} to DGND . . . . . -0.5 V to 2.3 V
PLL_AV_{DD} to PLL_AGND . . . . . -0.5 V to 2.3 V
$CH1\_AV_{DD}$ to CH1_AGND . . . . . -0.5 V to 2.3 V
Digital input voltage range, V_I to DGND . . . . . -0.5 V to 4.5 V
Input voltage range, XTAL1 to PLL_GND . . . . . -0.5 V to 2.3 V
Analog input voltage range A_I to CH1_AGND . . . . . -0.5 V to 2.0 V
Digital Output voltage range, V_O to DGND . . . . . -0.5 V to 4.5 V
Operating free-air temperature, TA . . . . . 0^oC to 70^oC

3.2 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
$IODV_{DD}$	Digital I/O supply voltage	3.0	3.3	3.6	V
DV_{DD}	Digital supply voltage	1.65	1.8	2.0	V
PLL_AV_{DD}	Analog PLL supply voltage	1.65	1.8	2.0	V
$CH1\_AV_{DD}$	Analog core supply voltage	1.65	1.8	2.0	V
$V_{I(P-P)}$	Analog input voltage (ac-coupling necessary)	0		1.0	V
V_{IH}	Digital input voltage high	0.7 IOV_{DD}			V
V_{IL}	Digital input voltage low			0.3 IOV_{DD}	V
V_{IH_XTAL}	XTAL input voltage high	0.7 PLL_AV_{DD}			V
V_{IL_XTAL}	XTAL input voltage low			0.3 PLL_AV_{DD}	V
I_{OH}	High-level output current			2	mA
I_{OL}	Low-level output current			-2	mA
I_{OH_SCLK}	SCLK high-level output current			4	mA
I_{OL_SCLK}	SCLK low-level output current			-4	mA
T_A	Operating free-air temperature	0		70	^oC

4. Packaging

32-pin TQFP



Unit: All linear dimensions are in millimeters.