Product Brief
December 2006
Revision 1.0

87541V
Embedded Controller for Mobile Systems

General Description

The Winbond 87541V is an embedded controller (EC) for mainstream notebook applications. It contains a highly optimized set of functions, providing a hardware/firmware partition that enables the implementation of flexible solutions; and it incorporates the National Semiconductor® CompactRISC™ CR16B core (a high-performance 16-bit RISC processor), which enables the EC functionality to be extended via the firmware.

In addition, the 87541V contains internal ROM and RAM memories, system support functions and a Bus Interface Unit (BIU) that directly interfaces with both external memory (such as flash) and I/O devices.

System support functions include: watchdog, PWM, timers, interrupt control, General-Purpose I/O (GPIO) with internal keyboard matrix scanning, PS/2® Interface, SMBus® interface, and analog-to-digital (ADC) and digital-to-analog (DAC) converters for battery charging, system monitoring and analog controls.

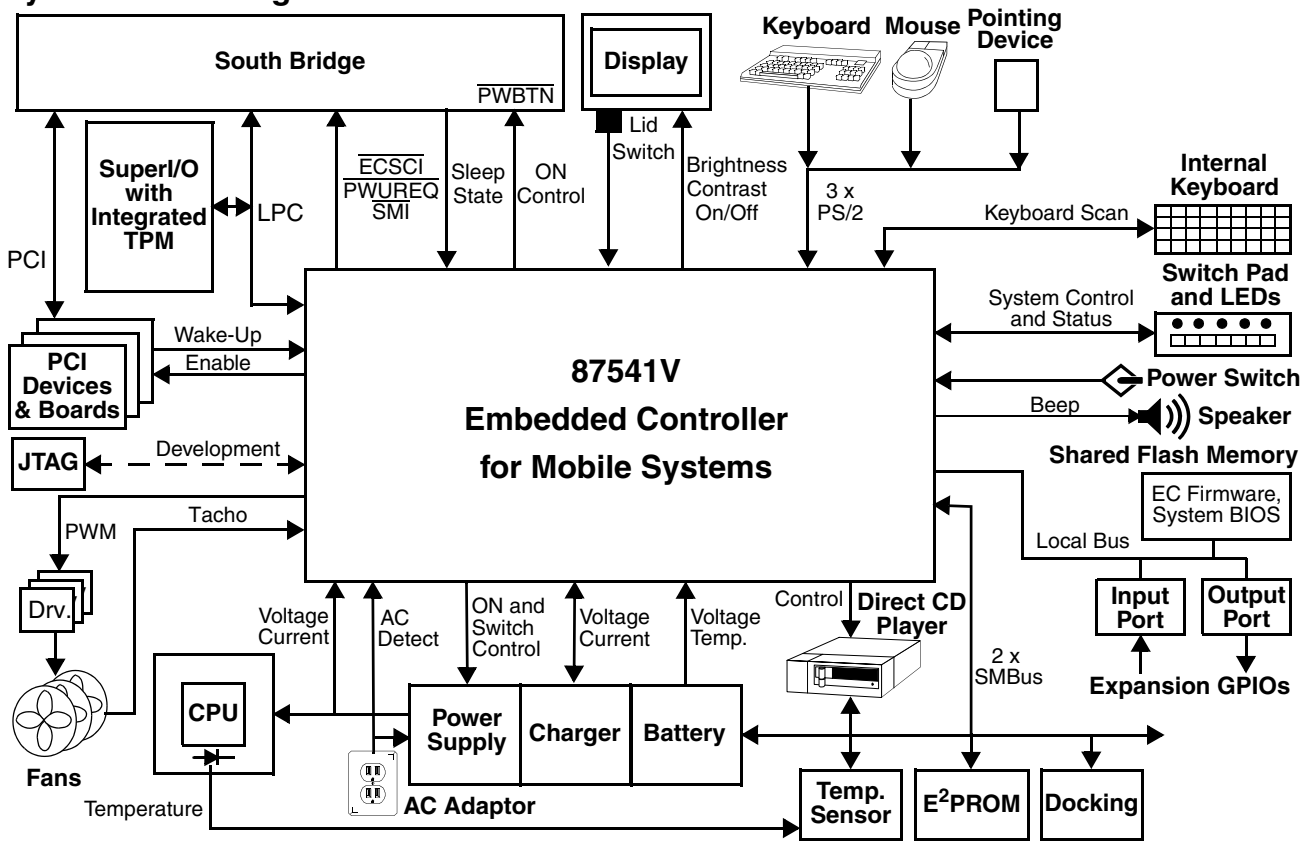
The 87541V interfaces with the host via an LPC interface, which provides the host with access to the Keyboard and embedded controller interface channels and to the BIOS flash.

Like other members of Winbond's Advanced I/O family, the 87541V is PC01 and ACPI compliant.

Outstanding Features

- Host interface, based on Intel's *LPC Interface Specification Revision 1.1*, August 2002
- PC01 Rev 1.0, and ACPI 2.0 compliant
- 16-bit RISC core, with 2 Mbytes address space, running at up to 20 MHz
- Shared BIOS flash memory (external)
- 88 GPIO ports (including keyboard scanning) with a variety of wake-up events
- JTAG-based debugger interface
- Software and hardware controlled clock throttling and extremely low current consumption in Idle mode
- 176-pin LQFP package

System Block Diagram



Features

Embedded Controller

- CompactRISC CR16B Processing Unit - a 16-bit embedded RISC processor core (the “core”)
- Internal Memory
  - Boot block for core code in 4 Kbytes of ROM
  - 2 Kbytes of on-chip RAM with contents protection
  - ROM and RAM both can hold code and data
- Bus Interface Unit (BIU) supporting:
  - Up to 1 Mbyte for code and data
  - Provides one chip-select for a flash/ROM device; one additional chip-select is available in Development mode for flash/ROM and SRAM devices
  - Provides one chip-select for I/O devices
  - 8- or 16-bit wide bus
  - Configurable wait states
  - Enhanced performance using fast read cycles
    - Single-cycle, fast-read (word-aligned)
    - Two-byte, burst-read (byte-aligned)
  - BIOS sharing with PC host
  - Host-core shared memory access protection
    - Host-controlled with core override
    - 64-Kbyte and 8-Kbyte blocks with independent protection
    - Hardware-protected boot zone for host code
  - Download for on-board code updating
    - Host-controlled via LPC
    - Core-controlled via JTAG or serial port
  - External memory “power-down” mode
- Operation Modes
  - IRE - Normal operation mode
  - OBD - On-Board Development mode
    - Used for development in the final system
    - Communicates with debugger via JTAG interface
    - Supports hardware breakpoint
  - DEV - Development mode
    - Used in In-System Emulators (ISE) and Application Development Boards (ADB)
    - Communicates with debugger via JTAG interface
    - On-chip ROM is replaced with off-chip SRAM
    - Cycle-by-cycle compatible with IRE mode
- LPC System Interface
  - 8-bit I/O and 8-bit memory read and write cycles
  - 8-bit Firmware Memory read and write with wait-sync cycles
  - Bootable memory support
  - Base Address (BADDR) strap to determine the base address of the Index-Data register pair
  - Serial IRQ (SERIRQ) support
  - $\overline{\text{LPCPD}}$ and $\overline{\text{CLKRUN}}$ support

Core-Controlled Functions

- Interrupt Control Unit (ICU)
  - Non-maskable interrupt input ($\overline{\text{PFAIL}}$)
  - 31 maskable vectored interrupts
  - Enable and pending indication for each interrupt
  - General-purpose external interrupt inputs through MIWU
  - Provides interrupt on system events (via MSWC)
    - External modem ring on $\overline{\text{RI}}$
    - IRQ from Keyboard, Mouse and PM channels
    - Software-triggered event
    - System ACPI sleep-state change
    - Power Button mode change
    - Legacy software “Off” command
- Multi-Input Wake-Up (MIWU)
  - Supports up to 20 wake-up inputs
  - Provides user-selectable trigger conditions
  - Provides wake-up on activity of external pins
    - General-purpose wake-up inputs
    - Power switch input
    - Keyboard scan inputs
  - Generates wake-up event to Power Management Controller (PMC)
  - Generates interrupts to ICU
- General-Purpose I/O (GPIO)
  - 88 port pins (including keyboard scanning)
  - I/O pins individually configured as input or output
  - Optional internal pull-up resistors on inputs
  - Special ports for internal keyboard matrix scanning
    - 16 open-collector outputs
    - Eight Schmitt inputs with internal pull-ups
  - Dedicated input for system On/Off switch
  - External GPIO expansion through the BIU I/O Expansion protocol
- Three PS/2 Interfaces
  - Supports external ports for: external keyboard, mouse and an additional pointing device
  - Supports byte-level handling via hardware accelerator
- Two ACB Interface modules. Each module:
  - Is Intel SMBus and Philips I^2C® compatible
  - Is SMBus master and slave
  - Detects four simultaneous slave addresses (two user-defined, broadcast and ARP)
  - Supports polling and interrupt controlled operation
  - Generates a wake-up event on detection of a Start Condition (while in Idle mode)
  - Has an optional internal pull-up on SDA and SCL pins

Features (Continued)

- Universal Synchronous/Asynchronous Receiver-Transmitter (USART)
  - — Supports full-duplex USART communication
  - — Has programmable baud rate
  - — Supports polling and interrupt controlled data transfer
  - — Supports synchronous mode with either internal or external clock
  - — Supports 9-bit Attention mode
- Two 16-bit Multi-Function Timer (MFT16) modules; each module:
  - — Contains two 16-bit timers
  - — Supports Pulse Width Modulation (PWM), Capture and Counter
- Timer and Watchdog (TWM)
  - — 16-bit periodic interrupt timer with 30 μs resolution and 5-bit prescaler for system tick and periodic wake-up tasks
  - — 8-bit watchdog timer
- Pulse Width Modulation (PWM) Module
  - — Eight outputs
  - — 8-bit duty cycle resolution
  - — 8-bit common input clock prescaler
- Analog to Digital Converter (ADC)
  - — Five voltage channels (four external and one internal), with 8-bit resolution
  - — Sigma-delta technology for high noise rejection
  - — Internal voltage reference
  - — Every 100 ms, three of the five channels are measured
- Digital to Analog Converter (DAC)
  - — Four channels with 8-bit resolution
  - — Rail-to-Rail output range, from AGND to AVCC
  - — 1 μs conversion time

Host-Core Interface Functions

- Host Bus Interface (HBI)
  - — Comprises three host interface ports, typically used for KBC and ACPI EC channels:
    - ❑ One 8042 KBC-standard, interface (legacy 60_{16}, 64_{16}).
    - ❑ Two PM interface ports (legacy 62_{16}, 66_{16} and 68_{16}, $6C_{16}$).

      These provide ACPI Embedded Controller support with either “Shared” or “Private” interface (regarding SCI/SMI generation).
  - — Generates IRQ (with Legacy support), SMI and SCI
  - — Provides Fast Gate A20 and Fast Keyboard Reset via firmware
- Core Access to Host-Controlled Functions
  - — Host-Core arbitration of function control
  - — Host access blocked by the core via lock bits

Host-Controlled Functions

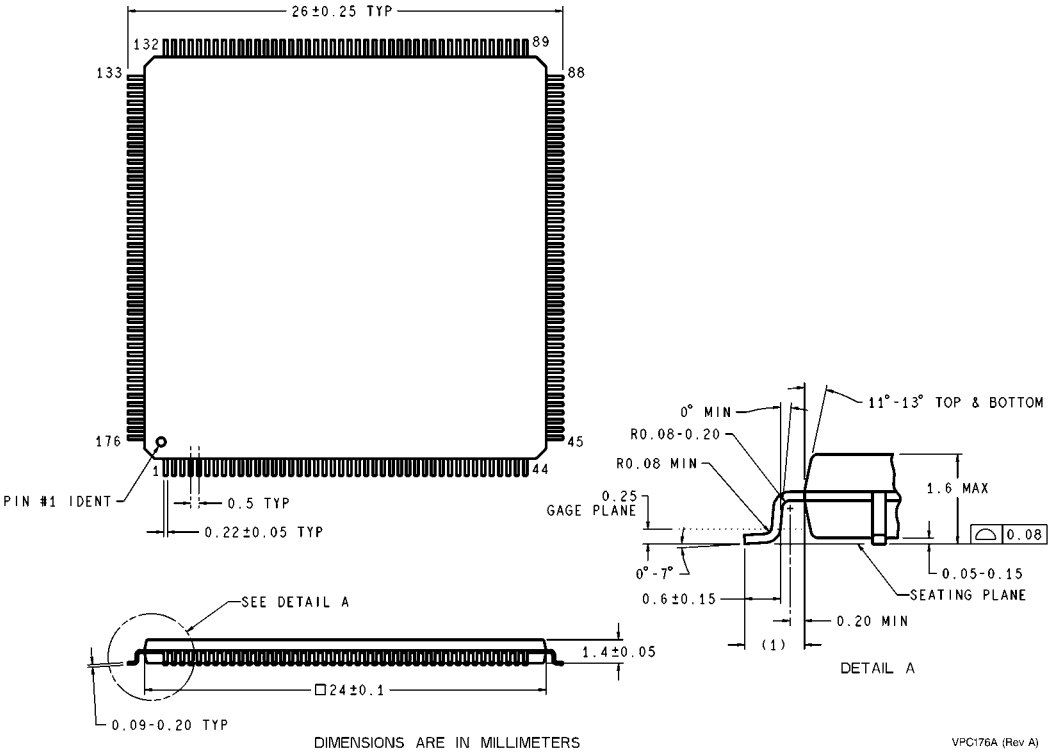
- Supports *Microsoft® Advanced Power Management (APM) Specifications Revision 1.2*, February 1996
  - — Generates the System Management Interrupt (SMI)
- Supports *ACPI Specification Revision 2.0b,* July 27, 2000
  - — Generates Power Management Interrupt ($\overline{\text{ECSCI}}$)
  - — Generates Power-Up Request ($\overline{\text{PWUREQ}}$)
- Host-controlled functions configuration PC01
  - — PnP Configuration Register structure
  - — Flexible resource allocation for all logical devices
    - ❑ Relocatable base address
    - ❑ 15 IRQ routing options
- Mobile System Wake-Up Control (MSWC)
  - — Wake-up on detection of:
    - ❑ External modem ring on $\overline{\text{RI}}$
    - ❑ IRQ from Keyboard, Mouse and PM channels
    - ❑ Software-triggered event
  - — Routing of wake-up to IRQ, SMI and $\overline{\text{PWUREQ}}$

Miscellaneous Features

- Clocks
  - — Single 32.768 KHz crystal oscillator with buffered output
  - — LPC clock, 0 to 33 MHz
  - — On-chip high frequency clock generator
    - ❑ Provides core clock, 4-20 MHz
    - ❑ Software-controlled frequency generation
    - ❑ Generation is based on the 32.768 KHz clock
  - — Buffered core clock output
- Strap Inputs for operation control
  - — ENV1-0 for IRE/OBD/DEV operating mode selection
  - — SHBM for shared BIOS control
  - — TRI-STATE® for ISE/ADB support
- Testability
  - — TRI-STATE device pins, selected at power-up by strap input
- Power Supply
  - — 3.3V supply operation
  - — 5V tolerance and back-drive protection on all pins (except LPC bus pins, keyboard scan inputs and analog pins)
  - — Separate supplies for Host-controlled functions (V_{DD}) and Core-controlled functions (V_{CC})
  - — Pin for filtering the on-chip voltage regulator (V_{CORF})
  - — Backup battery input for wake-up configuration
  - — Four power modes, switched by software or hardware with graduated current consumption
- Package
  - — 176-pin LQFP package

Physical Dimensions

All dimensions are in millimeters



176-Pin Low-Profile Plastic Quad Flatpack (LQFP)
Order Number 87541VDG/K2

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

For Advanced PC Product Line information contact: APC.Support@winbond.com