

Ordering Information

EM 48 8M 32 4 4 V B A – 8 F

EOREX
Logo

EDO/FPM : 40
D-RAMBUS : 41
DDRSDRAM : 42
DDRSGRAM : 43
SGRAM : 46
SDRAM : 48

Density
16M : 16 Mega Bits
8M : 8 Mega Bits
4M : 4 Mega Bits
2M : 2 Mega Bits
1M : 1 Mega Bit

Organization
8 : x8
9 : x9
16 : x16
18 : x18
32 : x32

Refresh
1 : 1K, **8** : 8K
2 : 2K, **6** : 16K
4 : 4K

Bank
2 : 2Bank **6** : 16Bank
4 : 4Bank **3** : 32Bank
8 : 8Bank

Interface
V : 3.3V
R : 2.5V

F: PB free package
Power
 Blank : Standard
L : Low power
I : Industrial

Min Cycle Time (Max Freq.)
-5 : 5ns (200MHz)
-6 : 5ns (167MHz)
-7 : 7ns (143MHz)
-75 : 7.5ns (133MHz)
-8 : 8ns (125MHz)
-10 : 10ns (100MHz)

Revision
A : 1st **B** : 2nd
C : 3rd **D** : 4th
G : for VGA version only

Package
C : CSP **B** : FBGA
T : TSOP **Q** : TQFP
P : PQFP (QFP)
L : LQFP

256Mb(4Banks) Synchronous DRAM

EM488M3244VBA (8Mx32)

Description

The EM488M3244VBA is Synchronous Dynamic Random Access Memory (SDRAM) organized as 2Meg words x 4 banks x 32 bits. All inputs and outputs are synchronized with the positive edge of the clock . The 256Mb SDRAM uses synchronized pipelined architecture to achieve high speed data transfer rates and is designed to operate in 3.3V low power memory system. It also provides auto refresh with power saving / down mode. All inputs and outputs voltage levels are compatible with LVTTL.

Features

- Fully synchronous to positive clock edge
- Clock frequency :125MHz(max)
- Single 3.3V +/- 0.3V power supply
- LVTTL compatible with multiplexed address
- Programmable Burst Length (B/ L) - 1,2,4,8 or full page
- Programmable CAS Latency (C/ L) - 2 or 3
- Data Mask (DQM) for Read/Write masking
- Programmable wrap sequential - Sequential (B/ L = 1/2/4/8/full page)
- Interleave (B/ L = 1/2/4/8)
- Burst read with single-bit write operation
- All inputs are sampled at the positive rising edge of the system clock.
- Auto refresh and self refresh
- 4,096 refresh cycles / 64ms (15.6us/row)
- FBGA package is lead free solder (Sn-Ag-Cu)

** EOREX reserves the right to change products or specification without notice.*

Pin Assignment (Top View)

90-ball FBGA

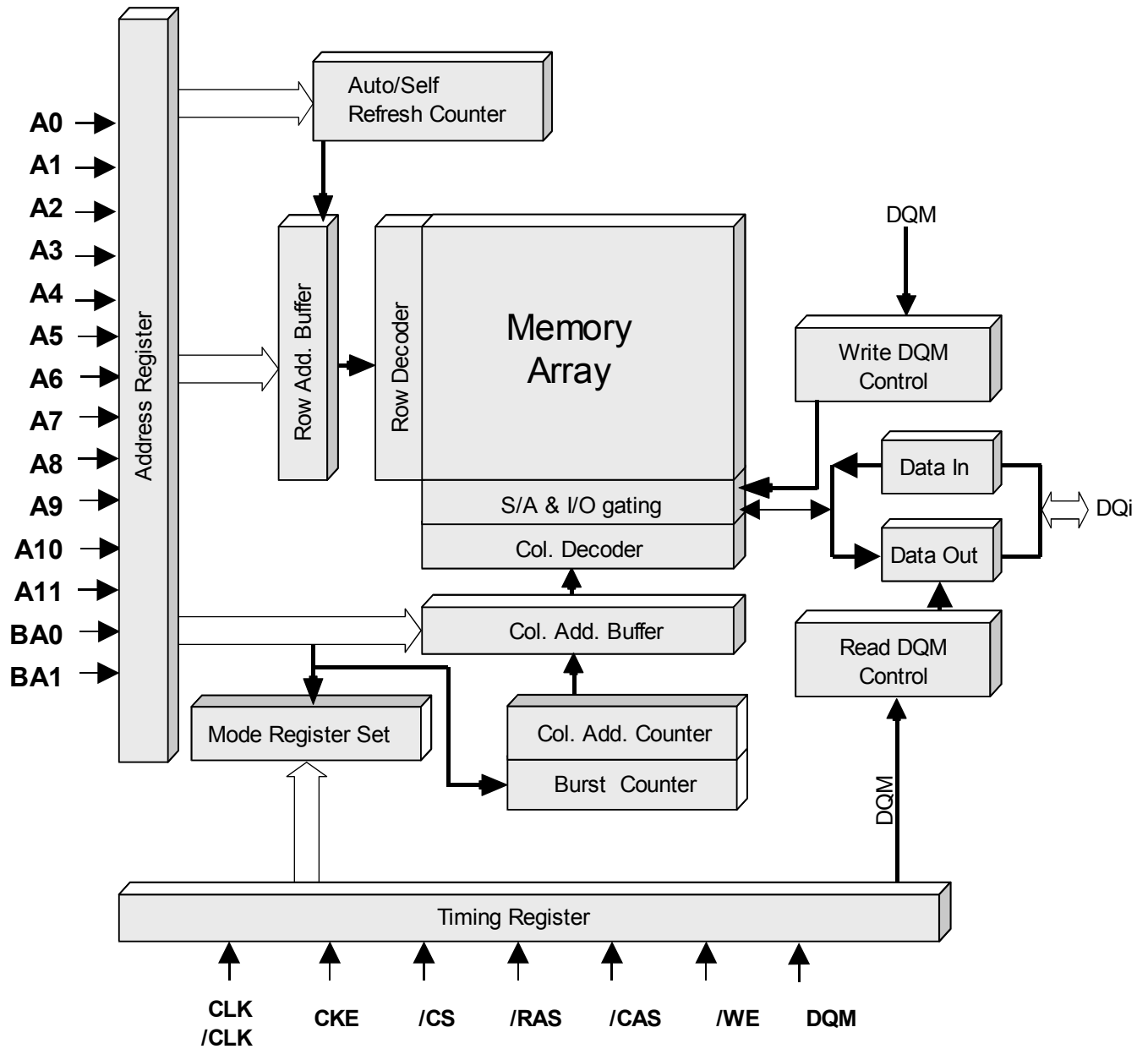
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|----------|------|------|------|---|---|---|------|------|------|
| A | O | O | O | | | | O | O | O |
| | DQ26 | DQ24 | VSS | | | | VDD | DQ23 | DQ21 |
| B | O | O | O | | | | O | O | O |
| | DQ28 | VDDQ | VSSQ | | | | VDDQ | VSSQ | DQ19 |
| C | O | O | O | | | | O | O | O |
| | VSSQ | DQ27 | DQ25 | | | | DQ22 | DQ20 | VDDQ |
| D | O | O | O | | | | O | O | O |
| | VSSQ | DQ29 | DQ30 | | | | DQ17 | DQ18 | VDDQ |
| E | O | O | O | | | | O | O | O |
| | VDDQ | DQ31 | NC | | | | NC | DQ16 | VSSQ |
| F | O | O | O | | | | O | O | O |
| | VSS | DQM3 | A3 | | | | A2 | DQM2 | VDD |
| G | O | O | O | | | | O | O | O |
| | A4 | A5 | A6 | | | | A10 | A0 | A1 |
| H | O | O | O | | | | O | O | O |
| | A7 | A8 | NC | | | | NC | BA1 | A11 |
| J | O | O | O | | | | O | O | O |
| | CLK | CKE | A9 | | | | BA0 | /CS | /RAS |
| K | O | O | O | | | | O | O | O |
| | DQM1 | NC | NC | | | | /CAS | /WE | DQM0 |
| L | O | O | O | | | | O | O | O |
| | VDDQ | DQ8 | VSS | | | | VDD | DQ7 | VSSQ |
| M | O | O | O | | | | O | O | O |
| | VSSQ | DQ10 | DQ9 | | | | DQ6 | DQ5 | VDDQ |
| N | O | O | O | | | | O | O | O |
| | VSSQ | DQ12 | DQ14 | | | | DQ1 | DQ3 | VDDQ |
| P | O | O | O | | | | O | O | O |
| | DQ11 | VDDQ | VSSQ | | | | VDDQ | VSSQ | DQ4 |
| R | O | O | O | | | | O | O | O |
| | DQ13 | DQ15 | VSS | | | | VDD | DQ0 | DQ2 |

(Top view)

Pin Descriptions (Simplified)

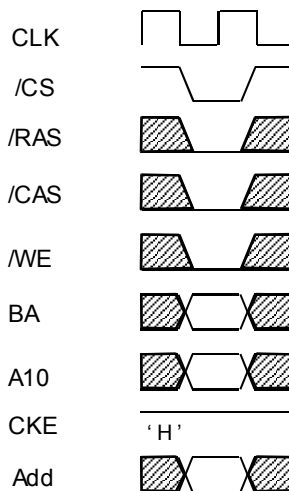
| Pin | Name | Pin Function |
|-------------|------------------------|---|
| CLK | System Clock | Master Clock Input(Active on the Positive rising edge) |
| /CS | Chip select | Selects chip when active |
| CKE | Clock Enable | Activates the CLK when "H" and deactivates when "L". CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. |
| A0 ~ A11 | Address | Row address (A0 to A11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. CA(CA0 to CA8) is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the pre-charge mode. When A10 = High at the pre-charge command cycle, all banks are pre-charged. But when A10 = Low at the pre-charge command cycle, only the bank that is selected by BA is pre-charged. |
| BA0~BA1 | Bank Address | Selects which bank is to be active. |
| /RAS | Row address strobe | Latches Row Addresses on the positive rising edge of the CLK with /RAS "L". Enables row access & pre-charge. |
| /CAS | Column address strobe | Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access. |
| /WE | Write Enable | Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access. |
| DQM0 ~ DQM3 | Data input/output Mask | DQM controls I/O buffers. |
| DQ0 ~ 31 | Data input/output | DQ pins have the same function as I/O pins on a conventional DRAM. |
| VDD/VSS | Power supply/Ground | VDD and VSS are power supply pins for internal circuits. |
| VDDQ/VSSQ | Power supply/Ground | VDDQ and VSSQ are power supply pins for the output buffers. |
| NC | No connection | This pin is recommended to be left No Connection on the device. |

Block Diagram



Commands

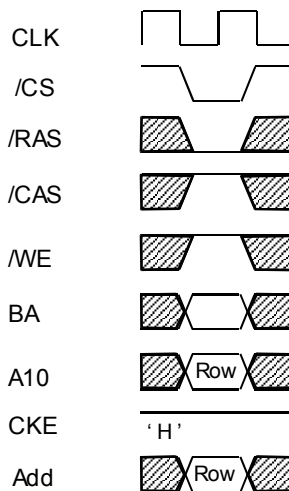
Mode register set command (/CS, /RAS, /CAS, /WE = Low)



The EM488M3244VBA have a mode register that defines how the device operates. In this command, A0 through BA are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. The EM488M3244VBA, cannot accept any other commands, only during 2CLK can following this command.

(Figure. 1 Mode register set command)

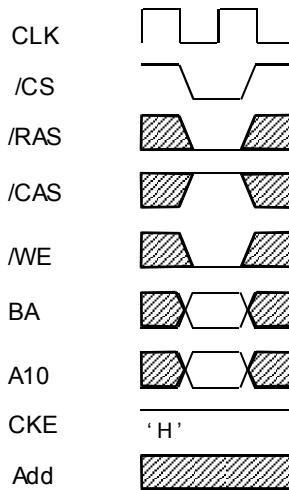
Active command (/CS, /RAS = Low , /CAS, /WE = High)



The EM488M3244VBA have 4 banks, each with 4,096 rows. This command activates the bank selected by BA and a row address selected by A0 through A11. This command corresponds to a conventional DRAM's /RAS falling.

(Figure. 2 Row address strobe and bank activate command)

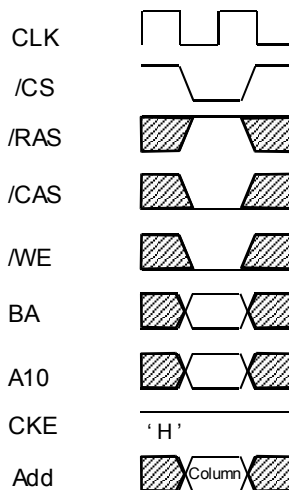
Precharge command (/CS, /RAS, /WE = Low , / CAS = High)



This command begins precharge operation of the bank selected by. When A10 is high,all banks are precharged, regardless of. When A10 is low,only the bank selected by BA is precharged.

(Figure. 3 Precharged command)

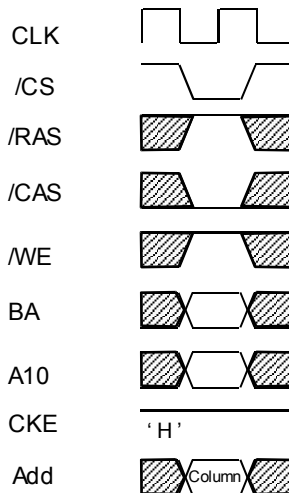
Write command (/CS, /CAS, /WE = Low, /RAS = High)



If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clicks.

(Figure. 4 Column address and write command)

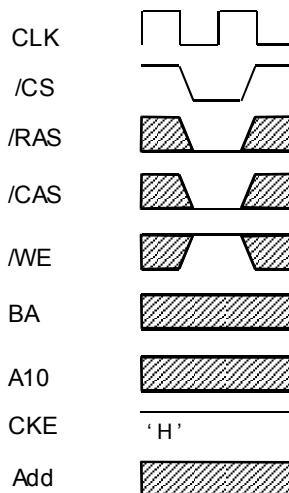
Read command (/CS, /CAS = Low , / RAS, /WE = High)



Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column.

(Figure. 5 Column address and read command)

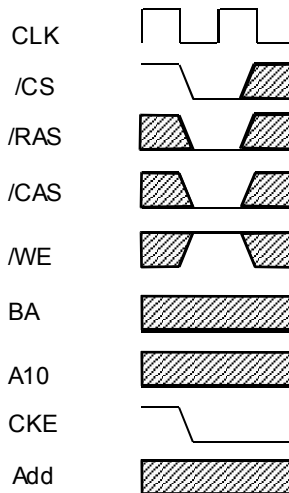
Auto refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)



This command is a request to begin the CBR refresh operation. The refresh address is generated internally. Before Executing CBR refresh, all banks must be precharged. After this cycle, all banks will be in the idle (Precharged) state and ready for a row activate command. During tRC period (from refresh command to refresh or activate command), the EM488M3244VBA cannot accept any other command.

(Figure. 6 Auto refresh command)

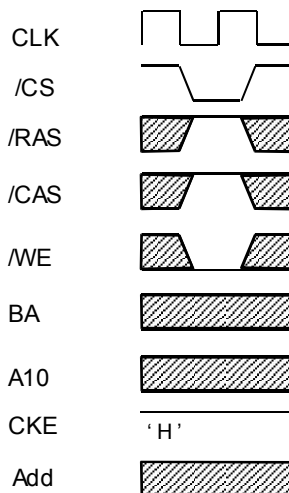
Self refresh entry command (/CS, /RAS , /CAS, CKE = Low , /WE = High)



After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the memory exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there before is no need for external control. Before executing self refresh, both banks must be precharged.

(Figure. 7 Self refresh entry command)

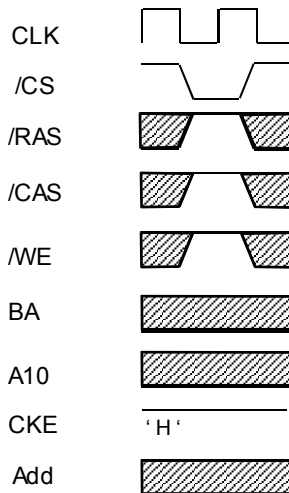
Burst stop command (/CS, /WE = Low, /RAS, /CAS = High)



This command can stop the current burst operation.

(Figure. 8 Burst stop command in full page mode)

No operation (/CS = Low, /RAS , /CAS, /WE = High)



This command is not execution command so there is no operations begin or terminate by this command.

(Figure. 9 No operation)

Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following:

1. CLK,CKE,/CS,DQM,DQ pin keep low till power stabilizes, and the CLK pin is stabilized whin 100us after power stabilizes before the following initialization sequence.
2. To stabilize internal circuits, when power is applied, a 200us or longer pause must precede any signal toggling.
3. After the pause, all banks must be precharged using the precharged command (The precharge all banks command is convenient).
4. Once the precharge is completed and the minimum tRP is satisfied, the mode register can be programmed.
5. Two or more Arto refresh must be performed.

- Remarks:**
1. The sequence of Mode register programming and Refresh above may be transposed.
 2. CKE and DQM must be held high until the precharge command is issued to ensure data-bus Hi-Z.

Programming the Mode Register

The mode register is programmed by the Mode register set command using address bits BA through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

| Options | /CAS Latency | Wrap type | Burst Length |
|---------------|---------------|-----------|---------------|
| BA through A7 | A6 through A4 | A3 | A2 through A0 |

Following mode register programming, no command can be issued before at least 2 CLK elapsed.

/CAS Latency

/CAS Latency is the most critical of the parameters begin set. It tells the device how many clocks must elapse before the data will be available.

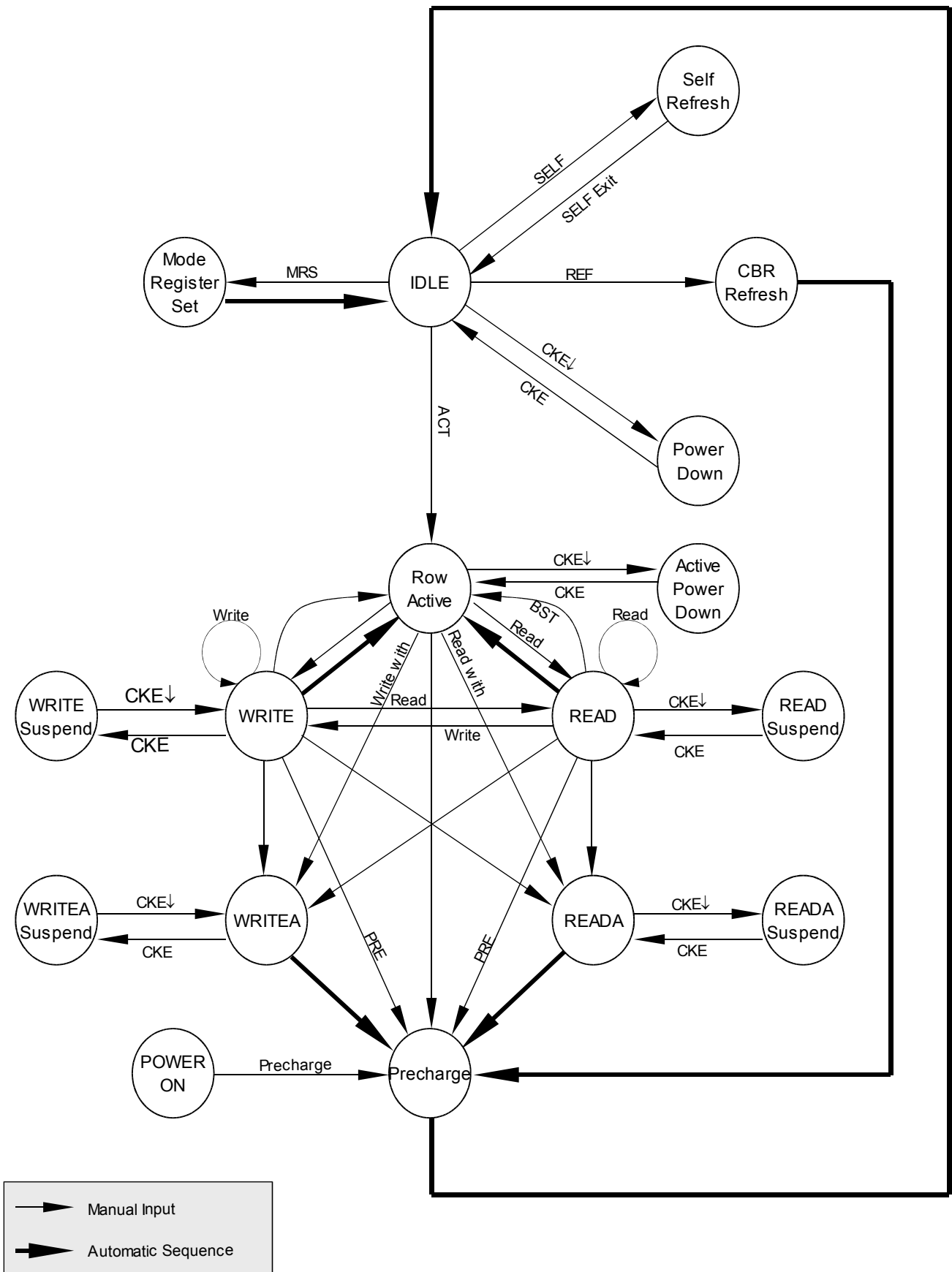
Burst Length

Burst length is the number of the words that will be output or input in a write cycle. After a read burst is completed, the output bus will become Hi-Z. The burst length is programmable as 1,2,4,8 or full page.

Wrap Type (Burst Sequence)

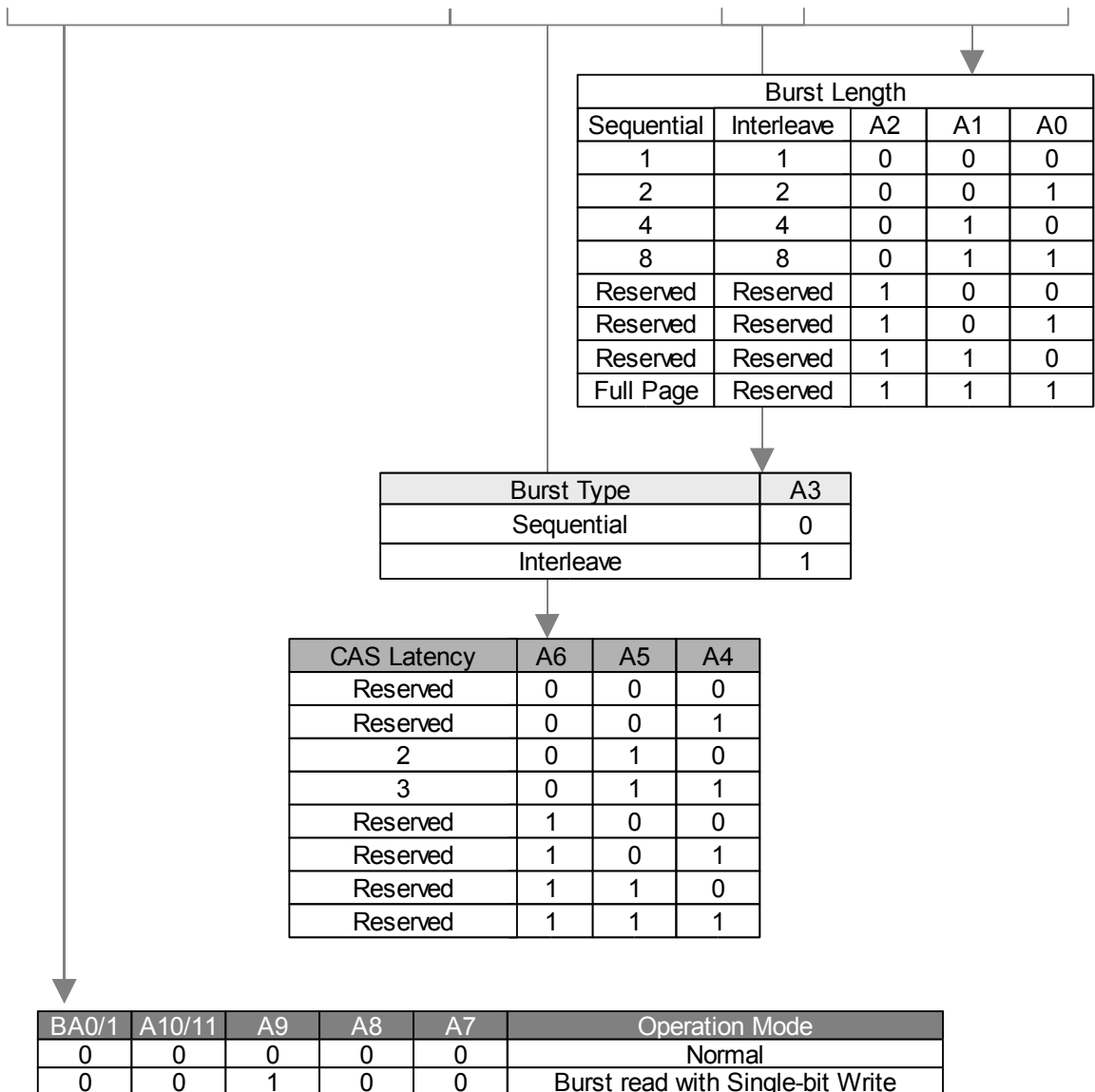
The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either Sequence or Interleave. The method chosen will depend on the type of CPU in the system. Some microprocessor cache systems are optimized for sequential addressing and others for interleaved.

Simplified State Diagram



Address Input for Mode Register Set

| | | | | | | | | | | | |
|----------------|--------|----|----|----|-------------|----|----|----|--------------|----|----|
| BA0/1 | A10/11 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| Operation Mode | | | | | CAS Latency | | | BT | Burst Length | | |



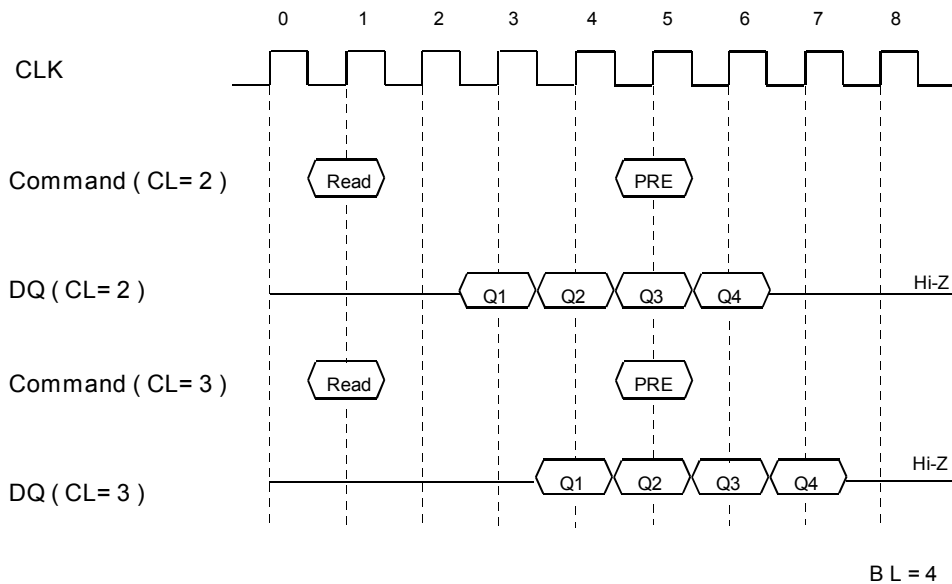
Burst Type (A3)

| Burst Length | A2 A1 A0 | Sequential Addressing | Interleave Addressing |
|--------------|----------|-----------------------|-----------------------|
| 2 | XX0 | 0 1 | 0 1 |
| | XX1 | 1 0 | 1 0 |
| 4 | X00 | 0 1 2 3 | 0 1 2 3 |
| | X01 | 1 2 3 0 | 1 0 3 2 |
| | X10 | 2 3 0 1 | 2 3 0 1 |
| | X11 | 3 0 1 2 | 3 2 1 0 |
| 8 | 000 | 0 1 2 3 4 5 6 7 | 0 1 2 3 4 5 6 7 |
| | 001 | 1 2 3 4 5 6 7 0 | 1 0 3 2 5 4 7 6 |
| | 010 | 2 3 4 5 6 7 0 1 | 2 3 0 1 6 7 4 5 |
| | 011 | 3 4 5 6 7 0 1 2 | 3 2 1 0 7 6 5 4 |
| | 100 | 4 5 6 7 0 1 2 3 | 4 5 6 7 0 1 2 3 |
| | 101 | 5 6 7 0 1 2 3 4 | 5 4 7 6 1 0 3 2 |
| | 110 | 6 7 0 1 2 3 4 5 | 6 7 4 5 2 3 0 1 |
| | 111 | 7 0 1 2 3 4 5 6 | 7 6 5 4 3 2 1 0 |
| Full Page * | n n n | Cn Cn+1 Cn+2 | - |

* Page length is a function of I/O organization and column addressing
 x32 (CA0 ~ CA8) : Full page = 512 bits

Precharge

The precharge command can be issued anytime after tRAS (min.) is satisfied. Soon After the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after tRP is satisfied. The parameter tRP is the time required to perform the precharge. The earliest timing in a read cycle that a precharege command can be issued without losing any data in the burst is as follows. It is depends on the /CAS latency and clock cycle time.



In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing tDPL(min.) with clock cycle time. In a word, the precharge command can be issued relative to reference clock that indicates the last data word is valid. The minus in the following table means clocks before the reference and the plus means time after the reference.

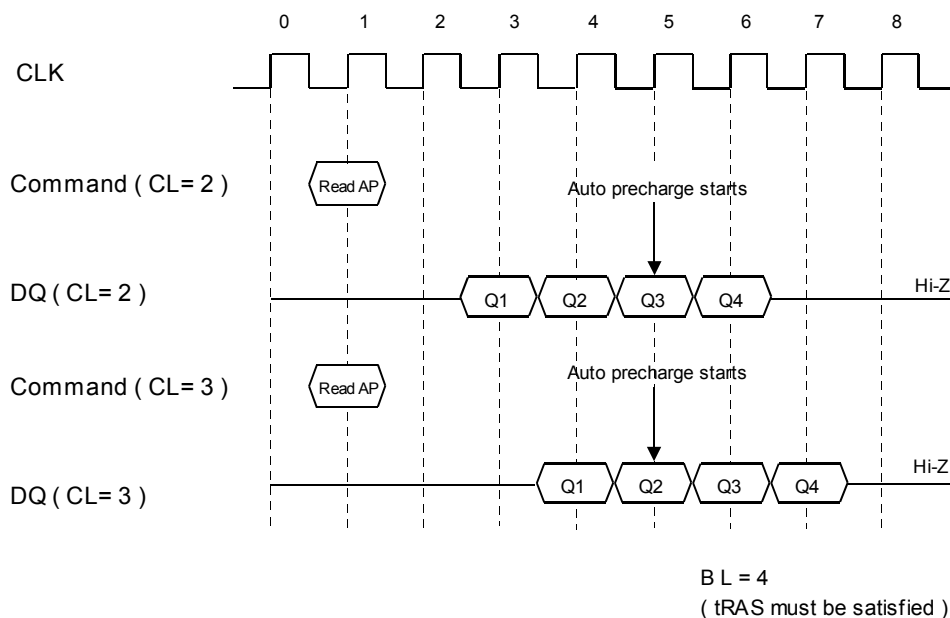
| /CAS latency | Read | Write |
|--------------|------|----------------|
| 2 | -1 | + tDPL(min.) |
| 3 | -2 | + tDPL (min.) |

Auto precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically. The t_{RAS} must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. In read cycle, once auto precharge has started , an activate command to the bank can be issued after t_{RP} has been satisfied

Read with Auto Precharge

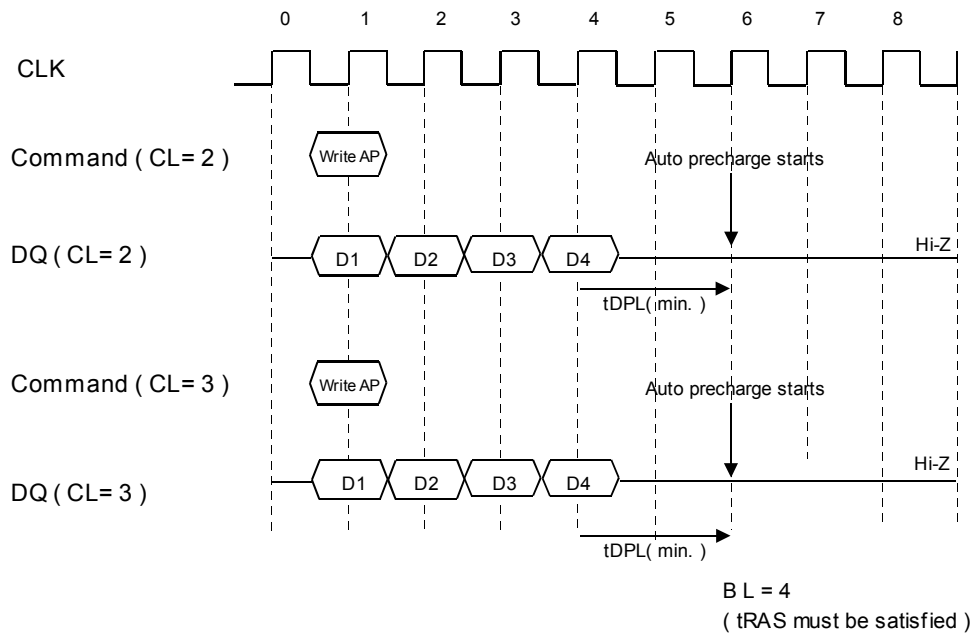
During a read cycle, the auto precharge begins same as (/CAS latency of 2) or one clock earlier (/CAS latency of 3) the last data word output.



Remarks: Read AP means Read with auto precharge

Write with Auto Precharge

During write cycle, the auto precharge starts at the timing that is equal to the value of the tDPL(min.) after the last dataword input to the device.



Remarks: Write AP means Write with auto precharge

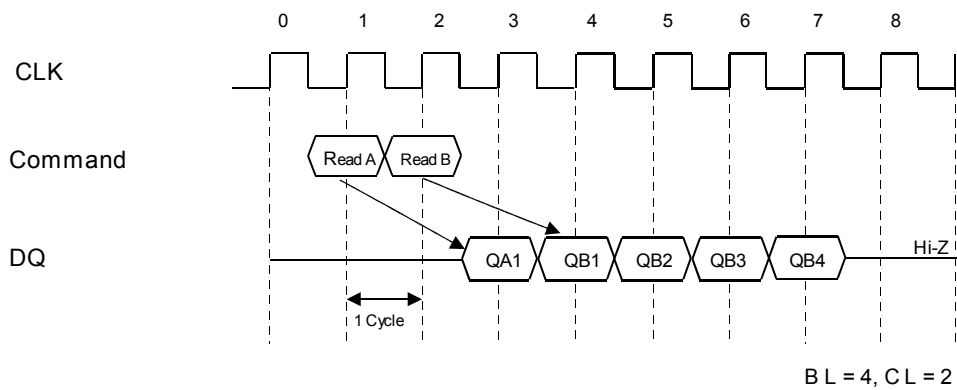
In summary, the auto precharge begins relative to a reference clock that indicates the last data word is valid. In the following table minus means clocks before the reference ,plus means after the reference.

| /CAS latency | Read | Write |
|--------------|------|----------------|
| 2 | -1 | + tDPL(min.) |
| 3 | -2 | + tDPL (min.) |

Read / Write command interval

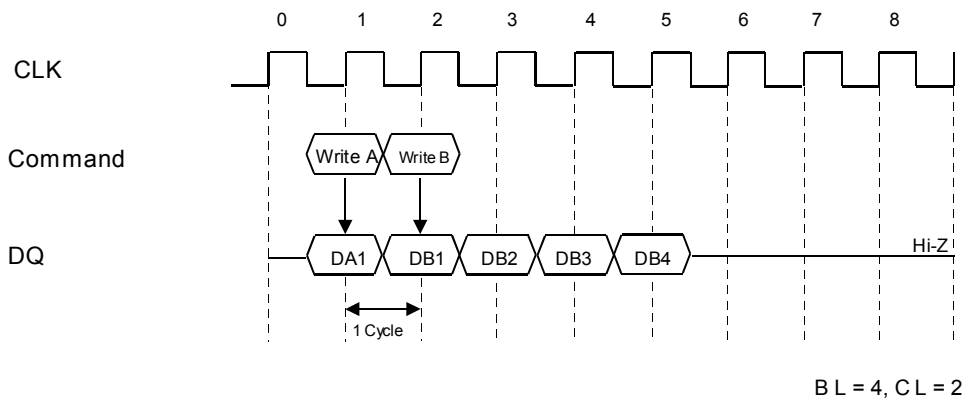
Read to read command interval

During a read cycle, when new Read command is issued, it will be effective after / CAS latency, even if the previous read operation does not completed. Read will be interrupted by another Read. The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



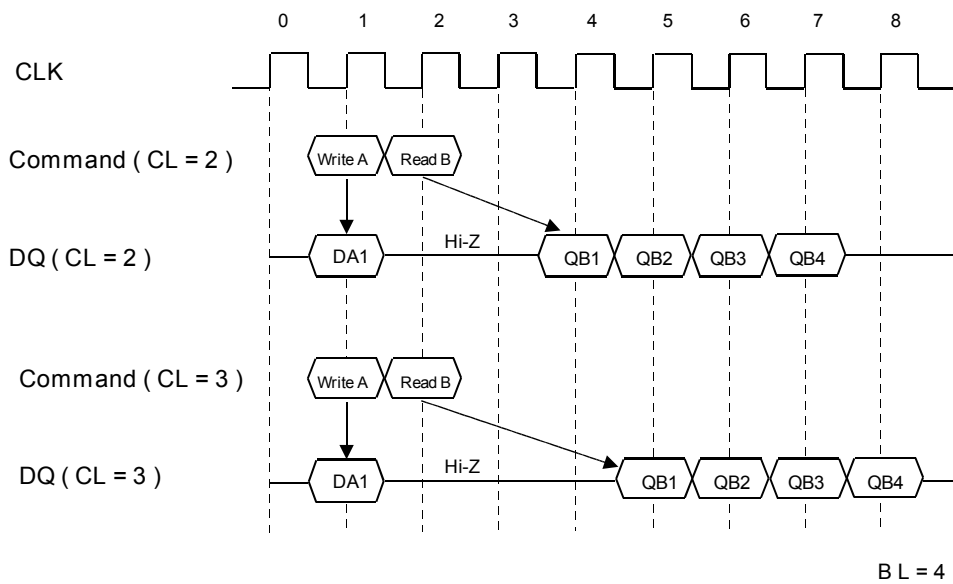
Write to write command interval

During a write cycle, when new write command is issued, the previous burst will terminate and the new burst will begin with a new write command. Write will be interrupted by another Write. The interval between the commands is minimum 1 cycle. Each write command can be issued in every clock without any restriction.



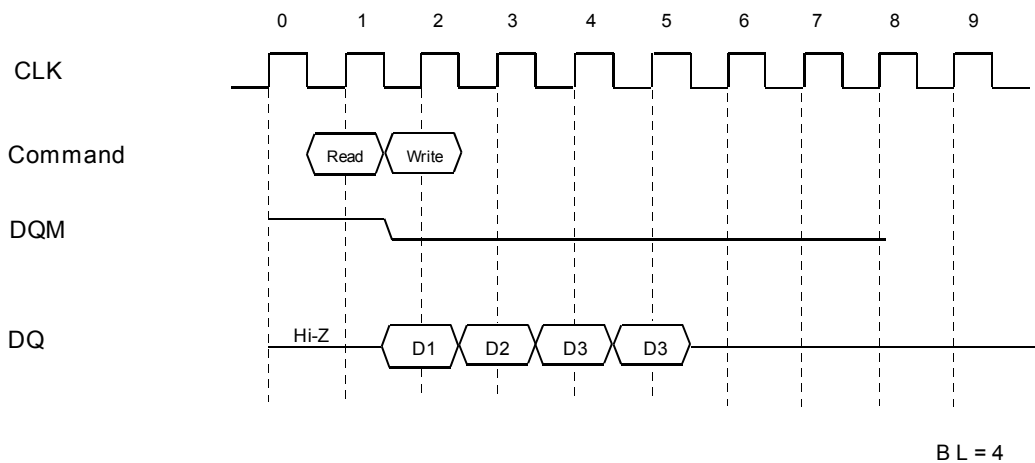
Write to read command interval

Write and Read command interval is also 1 cycle. Only the write data before read command will be written. The data bus must be Hi-Z at least one cycle prior to the first DOUT.

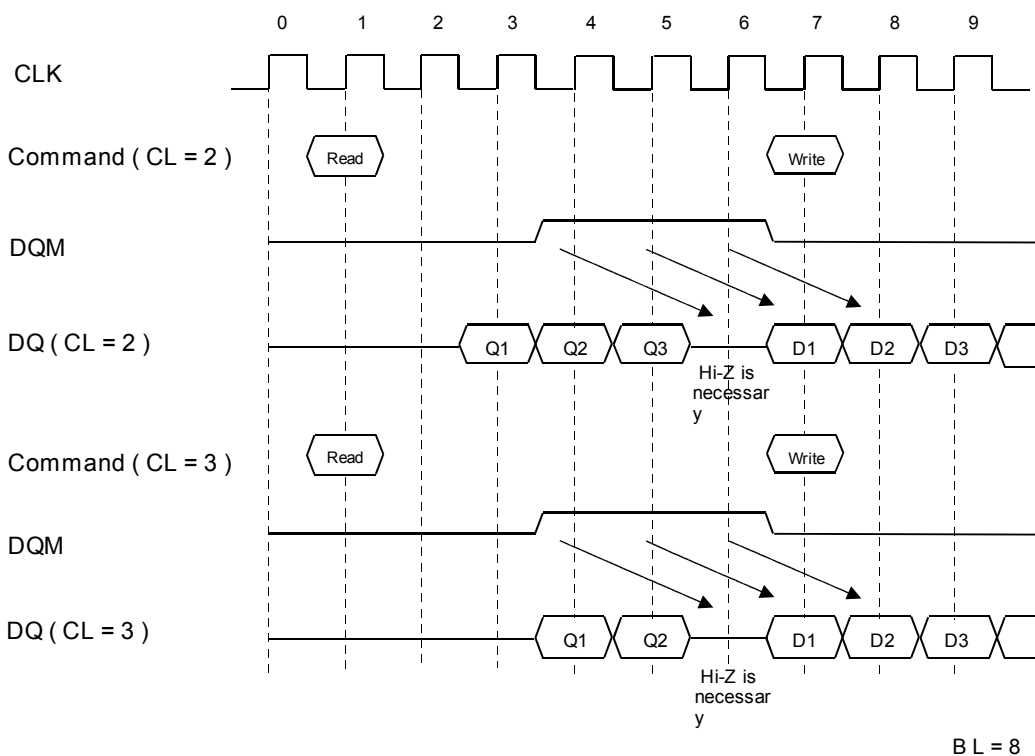


Read to write command interval

During a read cycle, Read can be interrupt by Write. The read and write command interval is 1 cycle minimum. There's a restriction to avoid data conflict. The data bus must be Hi-Z using DQM before write.



Read can be interrupted by Write. DQM must be high at least 3 clicks prior to the write command.

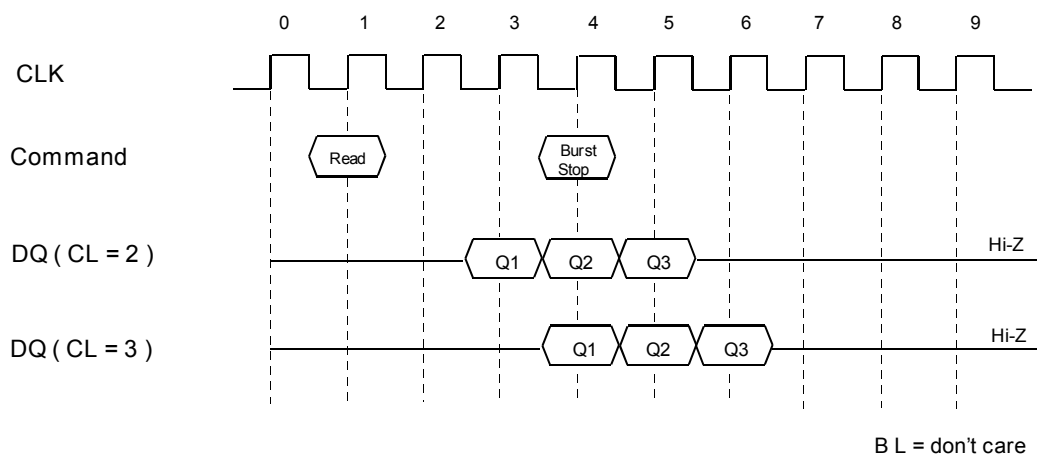


Burst terminate

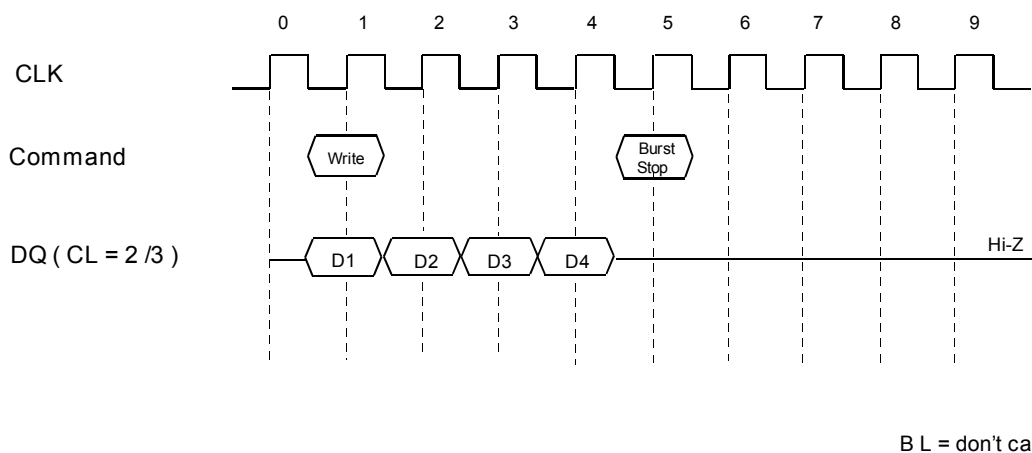
There are two ways to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

Burst stop command

During a read cycle,when the burst stop command is issued, the burst read are terminated and the data bus goes to Hi-Z after the /CAS latency from the burst stop command.



During a write cycle,when the burst stop command is issued, the burst write data are terminated and the data bus goes to Hi-Z at the same clock with the burst stop command.

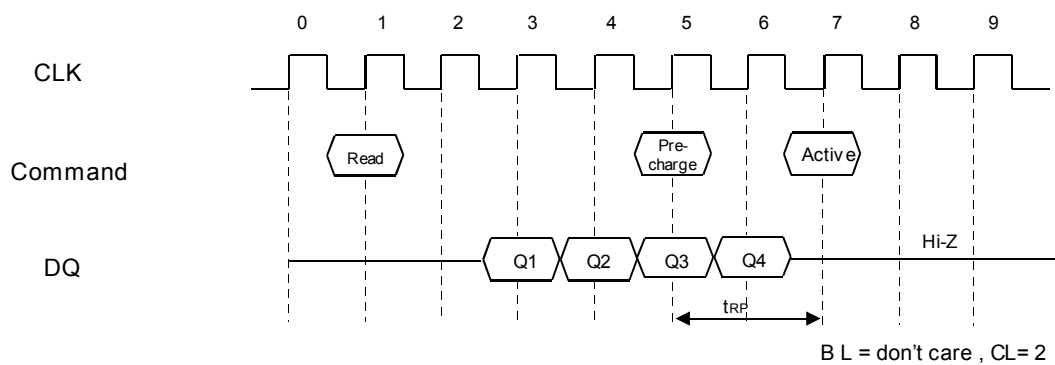


Precharge Termination

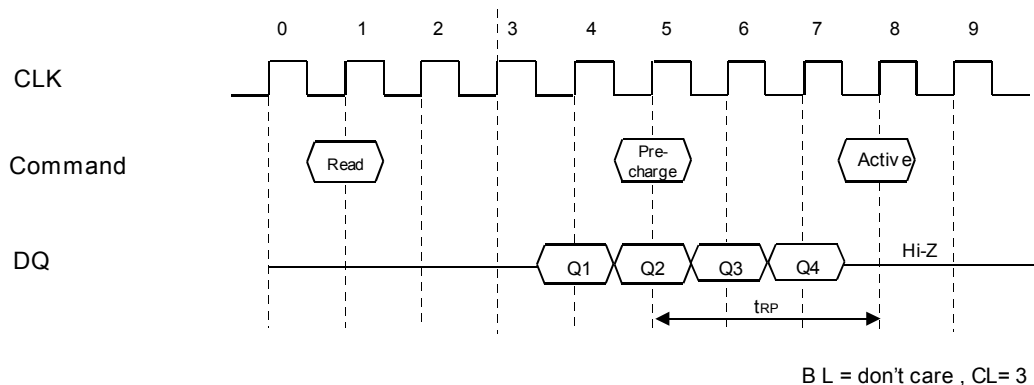
Precharge Termination in READ Cycle

During a read cycle, the burst read operation is terminated by a precharge command. When the precharge command is issued, the burst read operation is terminated and precharge starts. The same banks can be activated again after t_{RP} from the precharge command. To issue a precharge command, t_{RAS} must be satisfied.

When $/CAS$ Latency is 2, the read data will remain valid until two clocks after the precharge command.



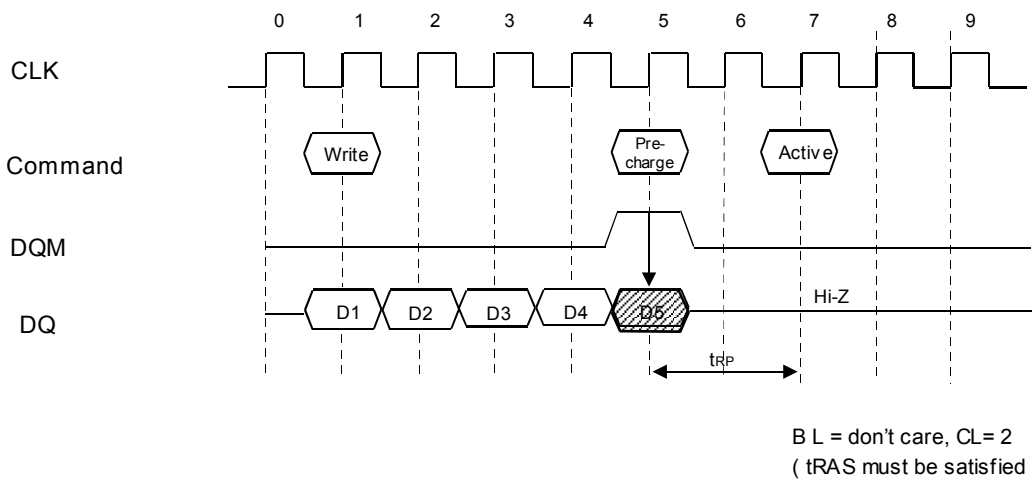
When $/CAS$ Latency is 3, the read data will remain valid until two clocks after the precharge command.



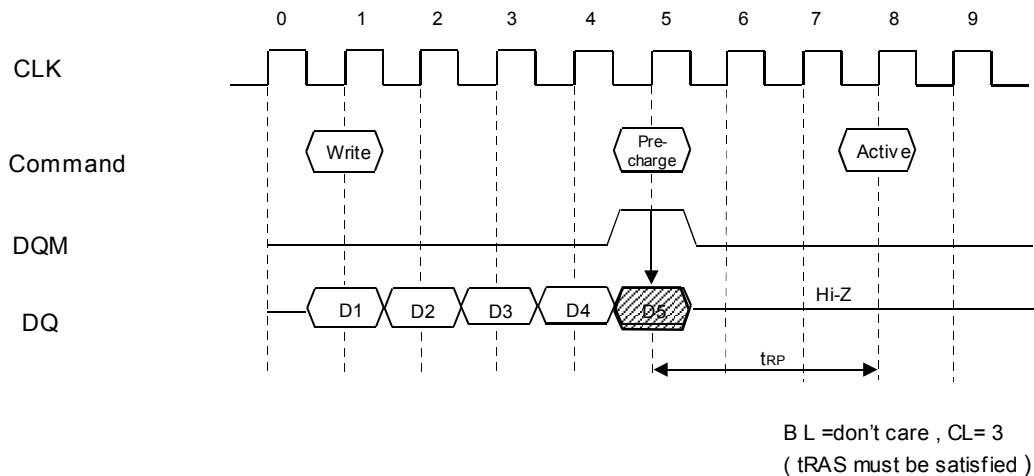
Precharge Termination in Write Cycle

During a write cycle, the burst write operation is terminated by a precharge command. When the precharge command is issued, the burst write operation is terminated and precharge starts. The same banks can be activated again after t_{RP} from the precharge command. To issue a precharge command, t_{RAS} must be satisfied.

When $/CAS$ Latency is 2, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. In order to avoid this situation, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



When $/CAS$ Latency is 3, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. In order to avoid this situation, DQM must be high at the same clock as the precharge command. This will mask the invalid data.



Truth Table

1. Command Truth Table (EM488M3244VBA)

| Command | Symbol | CKE | | /CS | /RAS | /CAS | /WE | BA | A10 | A9~A0 |
|----------------------------|--------|-----|---|-----|------|------|-----|----|-----|-------|
| | | n-1 | n | | | | | | | |
| Ignore Command | DESL | H | X | H | X | X | X | X | X | X |
| No operation | NOP | H | X | L | H | H | H | X | X | X |
| Burst stop | BSTH | H | X | L | H | H | L | X | X | X |
| Read | READ | H | X | L | H | L | H | V | L | V |
| Read with auto pre-charge | READA | H | X | L | H | L | H | V | H | V |
| Write | WRIT | H | X | L | H | L | L | V | L | V |
| Write with auto pre-charge | WRITA | H | X | L | L | H | H | V | H | V |
| Bank activate | ACT | H | X | L | L | H | H | V | V | V |
| Pre-charge select bank | PRE | H | X | L | L | H | L | V | L | X |
| Pre-charge all banks | PALL | H | X | L | L | H | L | X | H | X |
| Mode register set | MRS | H | X | L | L | L | L | L | L | V |

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. DQM Truth Table

| Command | Symbol | CKE | | /CS |
|---|--------|-----|---|-----|
| | | n-1 | n | |
| Data write / output enable | ENB | H | X | H |
| Data mask / output disable | MASK | H | X | L |
| Upper byte write enable / output enable | BSTH | H | X | L |
| Read | READ | H | X | L |
| Read with auto pre-charge | READA | H | X | L |
| Write | WRIT | H | X | L |
| Write with auto pre-charge | WRITA | H | X | L |
| Bank activate | ACT | H | X | L |
| Pre-charge select bank | PRE | H | X | L |
| Pre-charge all banks | PALL | H | X | L |
| Mode register set | MRS | H | X | L |

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

3. CKE Truth Table

| Command | Command | Symbol | CKE | | /CS | /RAS | /CAS | /WE | Addr. |
|---------------|--------------------------|--------|-----|---|-----|------|------|-----|-------|
| | | | n-1 | n | | | | | |
| Activating | Clock suspend mode entry | | H | L | X | X | X | X | X |
| Any | Clock suspend mode | | L | L | X | X | X | X | X |
| Clock suspend | Clock suspend mode exit | | L | H | X | X | X | X | X |
| Idle | CBR refresh command | REF | H | H | L | L | L | H | X |
| Idle | Self refresh entry | SELF | H | L | L | L | L | H | X |
| | | | L | H | L | H | H | H | X |
| Self refresh | Self refresh exit | | L | H | H | X | X | X | X |
| Idle | Power down entry | | H | L | X | X | X | X | X |
| Power down | Power down exit | | L | H | X | X | X | X | X |

Remark H = High level, L = Low level, X = High or Low level (Don't care)

4. Operative Command Table

| Current state | /CS | /R | /C | /W | Addr. | Command | Action | Notes |
|---------------|-----|----|----|---------|-----------|------------|---|-------|
| Idle | H | X | X | X | X | DESL | Nop or power down | 2 |
| | L | H | H | X | X | NOP or BST | Nop or power down | 2 |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA/RA | ACT | Row activating | |
| | L | L | H | L | BA, A10 | PRE/PALL | Nop | |
| | L | L | L | H | X | REF/SELF | Refresh or self refresh | 4 |
| | L | L | L | L | Op-Code | MRS | Mode register accessing | |
| Row active | H | X | X | X | X | DESL | Nop | |
| | L | H | H | X | X | NOP or BST | Nop | |
| | L | H | L | H | BA/CA/A10 | READ/READA | Begin read : Determine AP | 5 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | Begin write : Determine AP | 5 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PALL | Precharge | 6 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | 4 |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Read | H | X | X | X | X | DESL | Continue burst to end → Row active | |
| | L | H | H | H | X | NOP | Continue burst to end → Row active | |
| | L | H | H | L | X | BST | Burst stop → Row active | |
| | L | H | L | H | BA/CA/A10 | READ/READA | Terminate burst, new read : Determine AP | 7 |
| | L | L | L | L | BA/CA/A10 | WRIT/WRITA | Terminate burst, start write : Determine AP | 7, 8 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA/A10 | PRE/PALL | Terminate burst, pre-charging | 4 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| Write | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| | H | X | X | X | X | DESL | Continue burst to end → Write recovering | |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering | |
| | L | H | H | L | X | BST | Burst stop → Row active | |
| | L | H | L | H | BA/CA/A10 | READ/READA | Terminate burst, start read : Determine AP 7, 8 | 7, 8 |
| | L | L | L | L | BA/CA/A10 | WRIT/WRITA | Terminate burst, new write : Determine AP 7 | 7 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA/A10 | PRE/PALL | Terminate burst, pre-charging | 9 |
| L | L | L | H | X | REF/SELF | ILLEGAL | | |
| L | L | L | L | Op-Code | MRS | ILLEGAL | | |

Remark H = High level, L = Low level, X = High or Low level (Don't care)

| Current state | /CS | /R | /C | /W | Addr. | Command | Action | Notes |
|----------------|-----|----|----|----|-----------|------------|--|-------|
| Read with AP | H | X | X | X | X | DESL | Continue burst to end → Precharging | |
| | L | H | H | H | X | NOP | Continue burst to end → Precharging | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| Write with AP | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| | H | X | X | X | X | DESL | burst to end → Write recovering with auto precharge | |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering with auto precharge | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL | 3 |
| Precharging | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| | H | X | X | X | X | DESL | Nop → Enter idle after trp | |
| | L | H | H | H | X | NOP | Nop → Enter idle after trp | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| Row activating | L | L | H | L | BA, A10 | PRE/PALL | Nop → Enter idle after trp | |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| | H | X | X | X | X | DESL | Nop → Enter idle after trcd | |
| | L | H | H | H | X | NOP | Nop → Enter idle after trcd | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| Row activating | L | L | H | H | BA/RA | ACT | ILLEGAL | 3,10 |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Precharge

| Current state | /CS | /R | /C | /W | Addr. | Command | Action | Notes |
|--------------------------|-----|----|----|----|-----------|-------------------------------|-----------------------------------|-------|
| Write recovering | H | X | X | X | X | DESL | Nop → Enter row active after tDPL | |
| | L | H | H | H | X | NOP | Nop → Enter row active after tDPL | |
| | L | H | H | L | X | BST | Nop → Enter row active after tDPL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | Start read, Determine AP | |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | New write, Determine AP | 8 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Write recovering with AP | H | X | X | X | X | DESL | Nop → Enter precharge after tDPL | |
| | L | H | H | H | X | NOP | Nop → Enter precharge after tDPL | |
| | L | H | H | L | X | BST | Nop → Enter precharge after tDPL | |
| | L | H | L | H | BA/CA/A10 | READ/READA | ILLEGAL | 3,8 |
| | L | H | L | L | BA/CA/A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA/RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA, A10 | PRE/PALL | ILLEGAL | |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Refreshing | H | X | X | X | X | DESL | Nop → Enter idle after trc | |
| | L | H | H | X | X | NOP/ BST | Nop → Enter idle after trc | |
| | L | H | L | X | X | READ/WRIT | ILLEGAL | |
| | L | L | H | X | X | ACT/PRE/PALL | ILLEGAL | |
| | L | L | L | X | X | REF/SELF/MRS | ILLEGAL | |
| Mode Register Accessing | H | X | X | X | X | DESL | Nop | |
| | L | H | H | H | X | NOP | Nop | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | X | X | READ/WRIT | ILLEGAL | |
| | L | L | X | X | X | ACT/PRE/PALL/ REF/SELF/MRS | ILLEGAL | |

Remark H = High level, L = Low level, X = High or Low level (Don't care), AP = Auto Precharge

- Notes**
1. All entries assume that CKE was active (High level) during the preceding clock cycle.
 2. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Power down mode.
All input buffers except CKE will be disabled.
 3. Illegal to bank in specified states;
→ Function may be legal in the bank indicated by Bank Address (BA0/1), depending on the state of that bank.
 4. If all banks are idle, and CKE is inactive (Low level), SDRAM will enter Self refresh mode.
All input buffers except CKE will be disabled.
 5. Illegal if trCD is not satisfied.
 6. Illegal if trAS is not satisfied.
 7. Must satisfy burst interrupt condition.
 8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
 9. Must mask preceding data which don't satisfy tDPL.
 10. Illegal if trRD is not satisfied.

5. Command Truth Table for CKE

| Current state | CKE | | /CS | /R | /C | /W | Addr. | Action | Notes |
|-----------------------------------|-----|---|-----|----|----|----|---------|--|-------|
| | n-1 | n | | | | | | | |
| Self refresh | H | X | X | X | X | X | X | INVALID, CLK (n – 1) would exit self refresh | |
| | L | H | H | X | X | X | X | Self refresh recovery | |
| | L | H | L | H | H | X | X | Self refresh recovery | |
| | L | H | L | H | L | X | X | ILLEGAL | |
| | L | H | L | L | X | X | X | ILLEGAL | |
| | L | L | X | X | X | X | X | Maintain self refresh | |
| Self refresh recovery | H | H | H | X | X | X | X | Idle after trc | |
| | H | H | L | H | H | X | X | Idle after trc | |
| | H | H | L | H | L | X | X | ILLEGAL | |
| | H | H | L | L | X | X | X | ILLEGAL | |
| | H | L | H | X | X | X | X | ILLEGAL | |
| | H | L | L | H | H | X | X | ILLEGAL | |
| | H | L | L | H | L | X | X | ILLEGAL | |
| | H | L | L | L | X | X | X | ILLEGAL | |
| Power down | H | X | X | X | X | X | X | INVALID, CLK(n-1) would exit power down | |
| | L | H | X | X | X | X | X | Exit power down → Idle | |
| | L | L | X | X | X | X | X | Maintain power down mode | |
| Both banks idle | H | H | H | X | X | X | | Refer to operations in Operative Command Table | |
| | H | H | L | H | X | X | | Refer to operations in Operative Command Table | |
| | H | H | L | L | H | X | | Refer to operations in Operative Command Table | |
| | H | H | L | L | L | H | X | Refresh | |
| | H | H | L | L | L | L | Op-Code | Refer to operations in Operative Command Table | |
| | H | L | H | X | X | X | | Refer to operations in Operative Command Table | |
| | H | L | L | H | X | X | | Refer to operations in Operative Command Table | |
| | H | L | L | L | H | X | | Refer to operations in Operative Command Table | |
| | H | L | L | L | L | H | X | Self refresh | 1 |
| | H | L | L | L | L | L | Op-Code | Refer to operations in Operative Command Table | |
| | L | X | X | X | X | X | X | Power down | 1 |
| Row active | H | X | X | X | X | X | X | Refer to operations in Operative Command Table | |
| | L | X | X | X | X | X | X | Power down | 1 |
| Any state other than listed above | H | H | X | X | X | X | | Refer to operations in Operative Command Table | |
| | H | L | X | X | X | X | X | Begin clock suspend next cycle | 2 |
| | L | H | X | X | X | X | X | Exit clock suspend next cycle | |
| | L | L | X | X | X | X | X | Maintain clock suspend | |

Remark : H = High level, L = Low level, X = High or Low level (Don't care)

- Notes 1. Self refresh can be entered only from the both banks idle state.
 Power down can be entered only from both banks idle or row active state.
 2. Must be legal command as defined in Operative Command Table.

Absolute Maximum Ratings

| Symbol | Item | Rating | Units |
|------------------------------------|-----------------------|------------|-------|
| V _{IN} , V _{OUT} | Input, Output Voltage | -0.5 ~ 4.6 | V |
| V _{DD} , V _{DDQ} | Power Supply Voltage | -0.5 ~ 4.6 | V |
| T _{OP} | Operating Temperature | 0 ~ 70 | °C |
| T _{STG} | Storage Temperature | -55 ~ 125 | °C |
| P _D | Power Dissipation | 1 | W |
| I _{OS} | Short Circuit Current | 50 | mA |

Note : Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operation Conditions (Ta = 0 ~ 70°C)

| Symbol | Parameter | Min. | Typical | Max. | Units |
|------------------|---------------------------------------|------|---------|----------------------|-------|
| V _{DD} | Power Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{DDQ} | Power Supply Voltage (for I/O Buffer) | 3.0 | 3.3 | 3.6 | V |
| V _{IH} | Input logic high voltage | 2.0 | | V _{DD} +0.3 | V |
| V _{IL} | Input logic low voltage | -0.3 | | 0.8 | V |

- Note :**
- All voltage referred to V_{SS}.
 - V_{IH} (max) = V_{DD}+1.5V for pulse width ≤ 5ns
 - V_{IL} (min) = V_{SS}-1.5V for pulse width ≤ 5ns

Capacitance (V_{CC} = 3.3V, f = 1MHz, Ta = 25°C)

| Symbol | Parameter | Min. | Max. | Units |
|------------------|---|------|------|-------|
| C _{CLK} | Clock capacitance | 1.5 | 3.0 | pF |
| C _I | Input capacitance for CLK, CKE, Address, /CS, /RAS, /CAS, /WE, DQM0 ~ 3 | 1.5 | 3.0 | pF |
| C _O | Input/Output capacitance | 3.0 | 5.5 | pF |

Recommended DC Operating Conditions
 ($V_{DD} = 3.3V \pm 0.3V$, $T_a = 0 \sim 70^\circ C$, $T_a = -40$ to $85^\circ C$)

| Parameter | Symbol | Test condition | MAX | Units | Notes |
|--|--------|--|-----|-------|-------|
| Operating current | ICC1 | Burst length = 1, trc = trc (min), IOL = 0 mA, One bank active | 125 | mA | 1 |
| Precharge standby current in power down mode | ICC2P | CKE \leq VIL (max.), tck = tck(min) | 3 | mA | |
| | ICC2PS | CKE \leq VIL (max.), tck = ∞ | 2 | mA | |
| Precharge standby current in non-power down mode | ICC2N | CKE \geq VIL (min.), tck = tck(min), /CS \geq VIH (min.) Input signals are changed one time during 2clk | 20 | mA | |
| | ICC2NS | CKE,/CS \geq VIL (min.), tck = ∞ Input signals are stable | 9 | mA | |
| Active standby current in power down mode | ICC3P | CKE \leq VIL(max), tck = tck(min) | 4 | mA | |
| | ICC3PS | CKE \leq VIL(max), tck = ∞ | 3 | mA | |
| Active standby current in non-power down mode | ICC3N | CKE \geq VIL(min), tck = tck(min), /CS \geq VIH(min) Input signals are changed one time during 2clk | 45 | mA | |
| | ICC3NS | CKE \geq VIL(min), tck = ∞ Input signals are stable | 30 | mA | |
| operating current (Burst mode) | ICC4 | tCCD = 2CLKs , IOL = 0 mA | 150 | mA | 2 |
| Refresh current | ICC5 | trc = trc(min.) | 270 | mA | 3 |
| Self Refresh current | ICC6 | VIL \leq 0.2V , VIH \geq VDD- 0.2V | 3 | mA | 4 |

- Note :**
1. ICC1 depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during tCK(min)
 2. ICC4 depends on output loading and cycle rates.
Specified values are obtained with the output open.
Input signals are changed only one time during tCK(min)
 3. Input signals are changed only one time during tCK(min)
 4. Standard power version.

Recommended DC Operating Conditions (Continued)

| Parameter | Symbol | Test condition | Min. | Max. | Unit |
|---------------------------|-----------------|--|------|------|------|
| Input leakage current | I _{IL} | 0 ≤ V _I ≤ V _{DDQ} , V _{DDQ} =V _{DD} All other pins not under test=0 V | -1 | +1 | uA |
| Output leakage current | I _{OL} | 0 ≤ V _O ≤ V _{DDQ} , DOUT is disabled | -1.5 | +1.5 | uA |
| High level output voltage | V _{OH} | I _o = -2mA | 2.4 | | V |
| Low level output voltage | V _{OL} | I _o = +2mA | | 0.4 | V |

AC Operating Test Conditions**(V_{DD} = 3.3V +/- 0.3 V, T_a = 0 ~ 70°C)**

| | |
|----------------------------------|-------------|
| Output Reference Level | 1.4V / 1.4V |
| Output Load | CL=30pF |
| Input Signal Level | 2.4V / 0.4V |
| Transition Time of Input Signals | 2ns |
| Input Reference Level | 1.4V |

Operating AC Characteristics

(VDD = 3.3V +/- 0.3 V, Ta = 0 ~ 70°C, Ta = -40 to 85°C)

| Parameter | | Symbol | -8 | | Units | Notes |
|---|--------|------------------|------|------|-------|-------|
| | | | Min. | Max. | | |
| Clock cycle time | CL = 3 | t _{CK} | 8 | - | ns | |
| | CL = 2 | | 10 | - | ns | |
| Access time from CLK | | t _{AC} | - | 5.4 | ns | |
| | | | | | ns | |
| CLK high level width | | t _{CH} | 2.5 | - | ns | |
| CLK low level width | | t _{CL} | 2.5 | - | ns | |
| Data-out hold time | | t _{OH} | 2 | - | ns | 2 |
| | | | | | ns | |
| Data-out high impedance time | | t _{HZ} | - | 5.4 | ns | |
| | | | | | ns | |
| Data-out low impedance time | | t _{LZ} | 0 | - | ns | |
| Input hold time | | t _{IH} | 0.8 | | ns | |
| Input setup time | | t _{IS} | 1.5 | | ns | |
| ACTIVE to ACTIVE command period | | t _{RC} | 67.5 | | ns | 3 |
| ACTIVE to PRECHARGE command period | | t _{RAS} | 45 | 120k | ns | 3 |
| PRECHARGE to ACTIVE command period | | t _{RP} | 20 | | ns | 3 |
| ACTIVE to READ/WRITE delay time | | t _{RCD} | 20 | | ns | 3 |
| ACTIVE(one) to ACTIVE(another) command | | t _{RRD} | 15 | | ns | 3 |
| READ/WRITE command to READ/WRITE command | | t _{CCD} | 1 | | CLK | |
| Data-in to PRECHARGE command | | t _{DPL} | 2 | | CLK | |
| Data-in to BURST stop command | | t _{BDL} | 1 | | CLK | |
| Data-out to high impedance from PRECHARGE command | CL = 3 | t _{ROH} | 3 | | CLK | |
| | CL = 2 | | 2 | | CLK | |
| Refresh time(4,096 cycle) | | t _{REF} | | 64 | ms | |

Note :

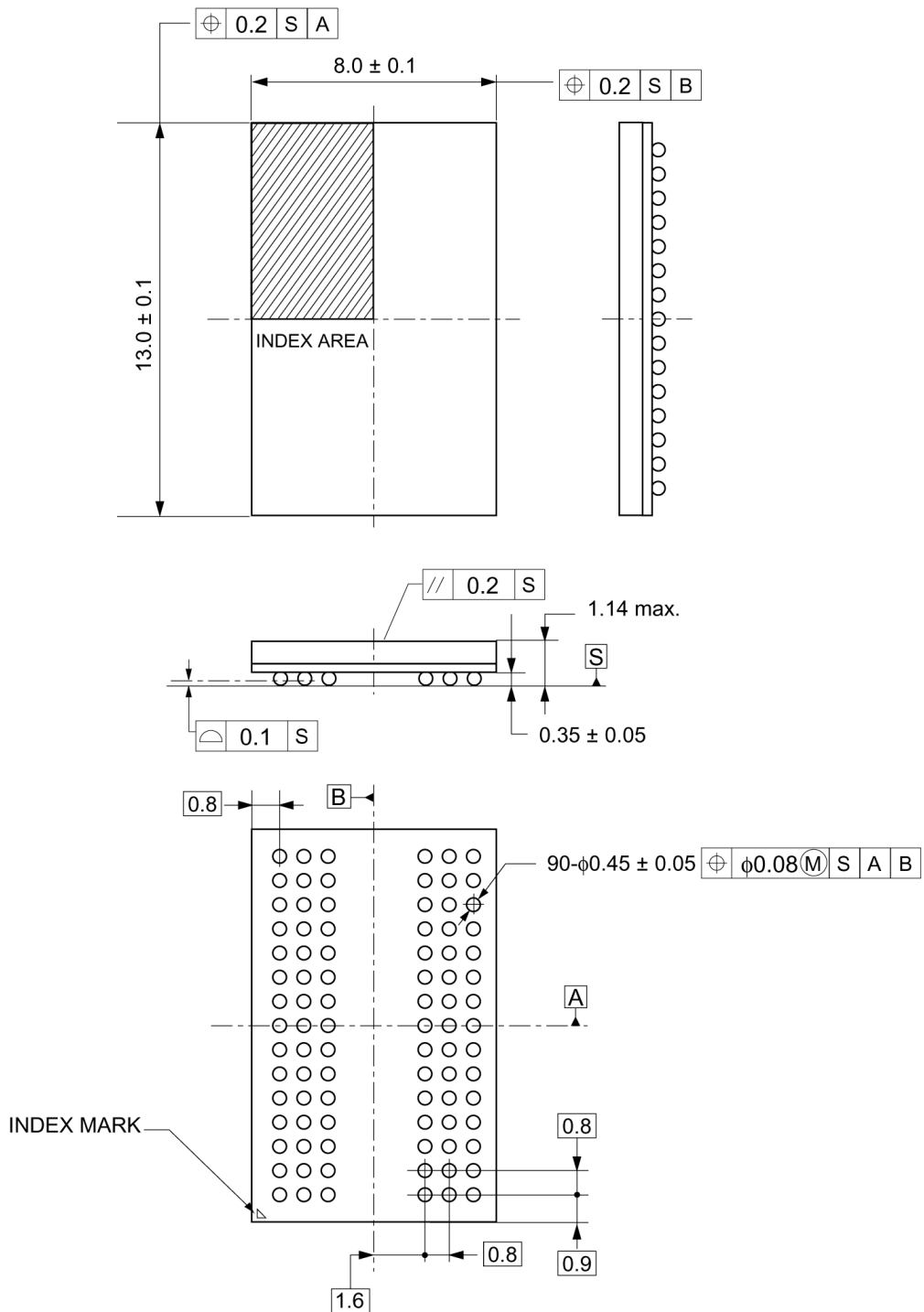
1. All voltages referenced to Vss.
2. t_{HZ} defines the time at which the output achieve the open circuit condition and is not referenced to output voltage levels.
3. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows :
The number of clock cycles = Specified value of timing/clock period
(Count fractions as a whole number)

Package Drawing

90-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



* EOREX reserves the right to change products or specification without notice.