

Data Sheet May 28, 2009 FN4898.2

Radiation Hardened 3.3V Quad Differential Line Driver

The Intersil HS-26CLV31RH is a radiation hardened 3.3V quad differential line driver designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV31RH accepts CMOS level inputs and converts them to differential outputs. Enable pins allow several devices to be connected to the same data source and addressed independently. The device has unique outputs that become high impedance when the driver is disabled or powered-down, maintaining signal integrity in multi-driver applications.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96663. A "hot-link" is provided on our homepage for downloading. www.intersil.com/military/

Features

- Electrically Screened to SMD # 5962-96663
- QML Qualified per MIL-PRF-38535 Requirements
- 1.2 Micron Radiation Hardened CMOS
 - Total Dose...... 300 krad(Si)(Max)
 - Single Event Upset LET 100MeV/mg/cm²)
 - Single Event Latch-up Immune
- Operating Supply Range 3.0V to 3.6V
- CMOS Level Inputs . . . $V_{IH} > (0.7)(V_{DD}); V_{IL} < (0.3)(V_{DD})$
- Differential Outputs...... V_{OH} > 1.8V; V_{OL} < 0.5V
- High Impedance Outputs when Disabled or Powered Down
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range
- Pb-Free (RoHS Compliant)

Applications

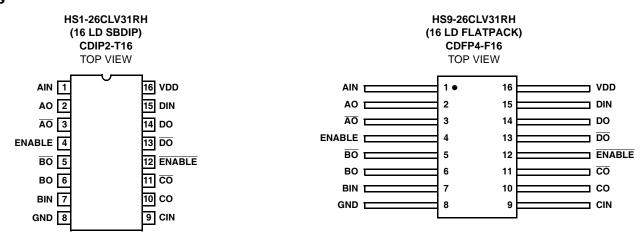
· Line Transmitter for MIL-STD-1553 Serial Data Bus

Ordering Information

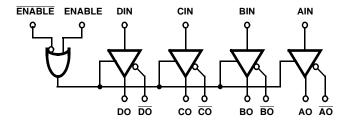
ORDERING NUMBER (Note)	INTERNAL MKT. NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
5962F9666302QEC	HS1-26CLV31RH-8	Q 5962F96 66302QEC	-55 to +125	16 LD SBDIP	D16.3
5962F9666302QXC	HS9-26CLV31RH-8	Q 5962F96 66302QXC	-55 to +125	16 LD FLATPACK	K16.A
5962F9666302VEC	HS1-26CLV31RH-Q	Q 5962F96 66302VEC	-55 to +125	16 LD SBDIP	D16.3
5962F9666302VXC	HS9-26CLV31RH-Q	Q 5962F96 66302VXC	-55 to +125	16 LD FLATPACK	K16.A
HS1-26CLV31RH/PROTO	HS1-26CLV31RH/PROTO	HS1- 26CLV31RH /PROTO	-55 to +125	16 LD SBDIP	D16.3
HS9-26CLV31RH/PROTO	HS9-26CLV31RH/PROTO	HS9- 26CLV31RH /PROTO	-55 to +125	16 LD FLATPACK	K16.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pinouts



Logic Diagram



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

Die Characteristics

DIE DIMENSIONS:

96.5 mil x 195 mils x 21 mils (2450 x 4950)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)

Thickness: 8kÅ ±1kÅ

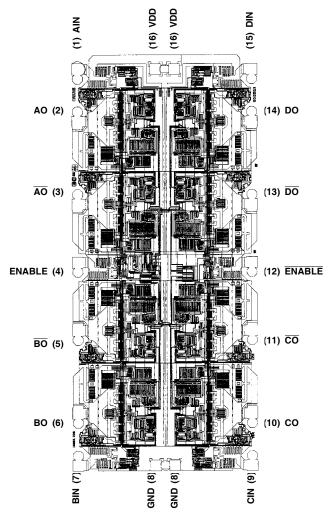
Metallization:

Bottom: Mo/TiW

Thickness: $5800\text{\AA} \pm 1\text{k}\text{\AA}$ Top: AlSiCu (Top) Thickness: $10\text{k}\text{Å} \pm 1\text{k}\text{Å}$

Metallization Mask Layout

HS-26CLV31RH



Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

 V_{DD}

ADDITIONAL INFORMATION:

Worst Case Current Density:

 $< 2.0 \times 10^5 \text{A/cm}^2$

Bond Pad Size:

110µm x 100µm

TABLE 1. HS26CLV31RH PAD COORDINATES

		RELATIVE TO PIN 1		
PIN NUMBER	PAD NAME	X COORDINATES	Y COORDINATES	
1	AIN	0	0	
2	A0	0	-570.7	
3	Ā0	0	-1483.5	
4	ENABLE	0	-2124.8	
5	B0	0	-2873.5	
6	В0	0	-3786.3	
7	BIN	0	-4357	
8	GND	852.4	-4357	
8	GND	1062.4	-4357	
9	CIN	1912.8	-4357	
10	C0	1912.8	-3786.3	
11	C0	1912.8	-2873.5	
12	ENABLE	1912.8	-2124.8	
13	D0	1912.8	-1483.5	
14	D0	1912.8	-570.7	
15	DIN	1912.8	0	
16	VIN	1062.4	0	
16	VIN	852.4	0	

NOTE: Dimensions in microns