K20 Sub-Family Data Sheet

Supports the following:
MK20X256VMC100,
MK20N512VMC100

K20P121M100SF2

Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C

- Performance
  - Up to 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

- Memories and memory interfaces
  - Up to 512 KB program flash memory on non-FlexMemory devices
  - Up to 256 KB program flash memory on FlexMemory devices
  - Up to 256 KB FlexNVM on FlexMemory devices
  - 4 KB FlexRAM on FlexMemory devices
  - Up to 128 KB RAM
  - Serial programming interface (EzPort)
  - FlexBus external bus interface

- Clocks
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator

- System peripherals
  - 10 low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 16-channel DMA controller, supporting up to 64 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit

- Security and integrity modules
  - Hardware CRC module to support fast cyclic redundancy checks
  - 128-bit unique identification (ID) number per chip

- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output

- Analog modules
  - Two 16-bit SAR ADCs
  - Programmable gain amplifier (up to x64) integrated into each ADC
  - 12-bit DAC
  - Three analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference

- Timers
  - Programmable delay block
  - Eight-channel motor control/general purpose/PWM timer
  - Two 2-channel quadrature decoder/general purpose timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock

- Communication interfaces
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - I2S module

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers: PK20 and MK20.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## M FFF T PP CCC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K20
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory

Table continues on the next page...

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • EX = 64 QFN (9 mm x 9 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (12 mm x 12 mm) • MB = 81 MAPBGA (8 mm x 8 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MF = 196 MAPBGA (15 mm x 15 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CCC	Maximum CPU frequency (MHz)	• 50 = 50 MHz • 72 = 72 MHz • 100 = 100 MHz • 120 = 120 MHz • 150 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK20N512VMD100

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

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3.4   Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1   Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5   Result of exceeding a rating

The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

K20 Sub-Family Data Sheet Data Sheet, Rev. 4, 3/2011.
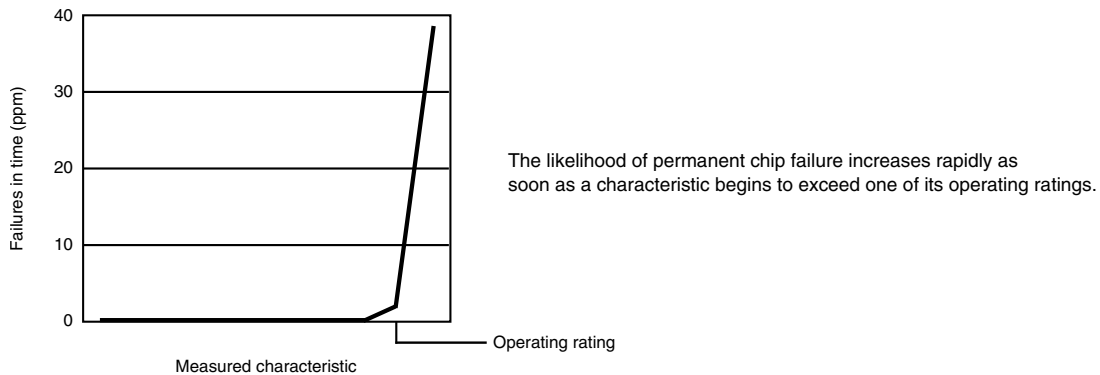
3.6 Relationship between ratings and operating requirements

Fatal range	Limited operating range	Normal operating range	Limited operating range	Fatal range
- Probable permanent failure	- No permanent failure - Possible decreased life - Possible incorrect operation	- No permanent failure - Correct operation	- No permanent failure - Possible decreased life - Possible incorrect operation	- Probable permanent failure

Handling range

- No permanent failure

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3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:
- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I$_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:
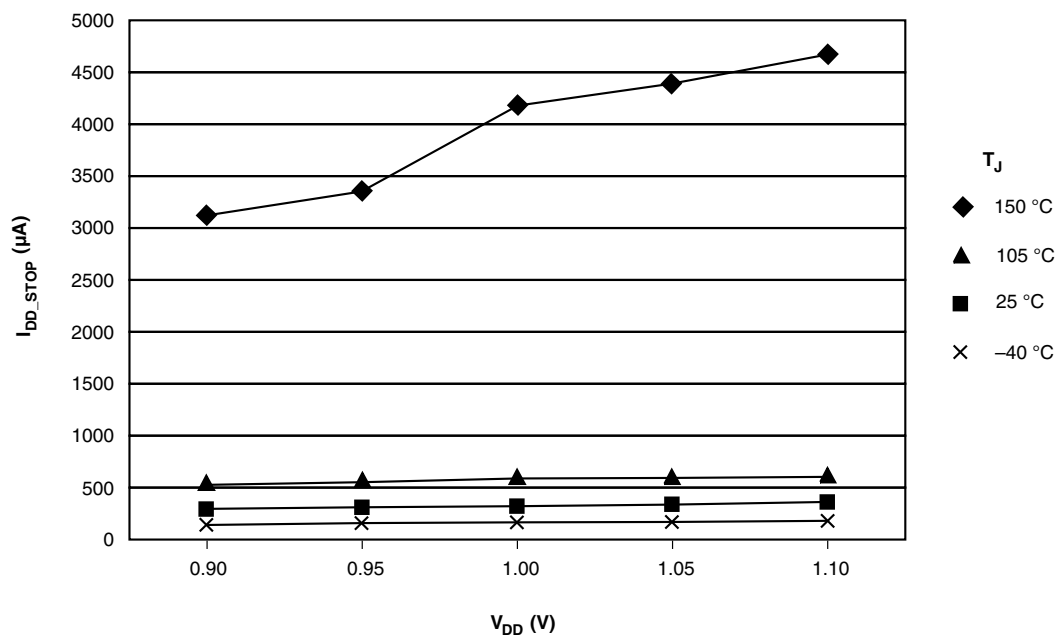
3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T$_A$	Ambient temperature	25	°C
V$_{DD}$	3.3 V supply voltage	3.3	V

4 Ratings

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4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	−55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 85°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	−0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	−0.3	5.5	V

Table continues on the next page...

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Symbol	Description	Min.	Max.	Unit
V_{AIO}	Analog, $\overline{RESET}$, EXTAL, and XTAL input voltage	−0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	−25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} − 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	−0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	−0.3	3.63	V
VREGIN	USB regulator input	−0.3	6.0	V
V_{BAT}	RTC battery supply voltage	−0.3	3.8	V

5 General

5.1 Nonswitching electrical specifications

5.1.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	−0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	−0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	

Table continues on the next page...

Table 1. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
I_{IC}	DC injection current — single pin • $V_{IN} < V_{SS}$	 0	 −0.2	 mA	1
	DC injection current — total MCU limit, includes sum of all stressed pins • $V_{IN} < V_{SS}$	 0	 −5	 mA	1
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	TBD	—	V	

1. All functional non-supply pins are internally clamped to V_{SS}, and induce an injection current when V_{IN} is less than V_{SS}. The I_{IC} maximum operating requirement should not be exceeded. If this requirement cannot be met, the input must be current limited to the value specified.

5.1.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	TBD	1.1	TBD	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	TBD	2.56	TBD	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	TBD	2.70	TBD	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	TBD	2.80	TBD	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	TBD	2.90	TBD	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	TBD	3.00	TBD	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range		60		mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	TBD	1.60	TBD	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	TBD	1.80	TBD	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	TBD	1.90	TBD	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	TBD	2.00	TBD	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	TBD	2.10	TBD	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range		40		mV	
V_{BG}	Bandgap voltage reference	TBD	1.00	TBD	V	
t_{LPO}	Internal low power oscillator period factory trimmed	TBD	1000	TBD	µs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3.   VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	TBD	1.1	TBD	V	

5.1.3   Voltage and current operating behaviors

Table 4.   Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	 $V_{DD} - 0.5$ $V_{DD} - 0.5$	 — —	 V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	 $V_{DD} - 0.5$ $V_{DD} - 0.5$	 — —	 V V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3mA	 — —	 0.5 0.5	 V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)	—	1	µA	1
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	30	50	kΩ	2
R_{PD}	Internal pulldown resistors	30	50	kΩ	3

1. Measured at VDD=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

5.1.4   Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

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- CPU and system clocks = 100 MHz
- Bus and FlexBus clocks = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8V to execution of the first instruction across the operating temperature range of the chip.	—	300	µs	1
	RUN → VLLS1 → RUN				
	• RUN → VLLS1	—	4.1	µs	
	• VLLS1 → RUN	—	123.8	µs	
	RUN → VLLS2 → RUN				
	• RUN → VLLS2	—	4.1	µs	
	• VLLS2 → RUN	—	49.3	µs	
	RUN → VLLS3 → RUN				
	• RUN → VLLS3	—	4.1	µs	
	• VLLS3 → RUN	—	49.2	µs	
	RUN → LLS → RUN				
	• RUN → LLS	—	4.1	µs	
	• LLS → RUN	—	5.9	µs	
	RUN → STOP → RUN				
	• RUN → STOP	—	4.1	µs	
	• STOP → RUN	—	4.2	µs	
	RUN → VLPS → RUN				
	• RUN → VLPS	—	4.1	µs	
	• VLPS → RUN	—	5.8	µs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.1.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	TBD	mA	1

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8V • @ 3.0V	— —	 40 42	 TBD TBD	 mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 1.8V • @ 3.0V	— —	 55 56	 TBD TBD	 mA mA	3
$I_{DD\_RUN\_MAX}$	Run mode current — all peripheral clocks enabled and peripherals active, code executing from flash • @ 1.8V • @ 3.0V	— —	 85 85	 TBD TBD	 mA mA	4
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	35	TBD	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	15	TBD	mA	5
I_{DD_STOP}	Stop mode current at 3.0 V	—	0.4	TBD	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.25	TBD	mA	6
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	TBD	TBD	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	1.05	TBD	mA	8
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V	—	50	TBD	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V	—	12	TBD	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • 128KB RAM devices	—	 8	 TBD	 µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V	—	4	TBD	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V	—	2	TBD	µA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V	—	550	TBD	nA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, but peripherals are not in active operation.
4. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled. Code executing from flash.

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7. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for fast IRCLK mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

5.1.5.1   Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

*   MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)
*   All peripheral clocks disabled except FTFL
*   LVD disabled, USB regulator disabled
*   No GPIOs toggled
*   Code execution from flash
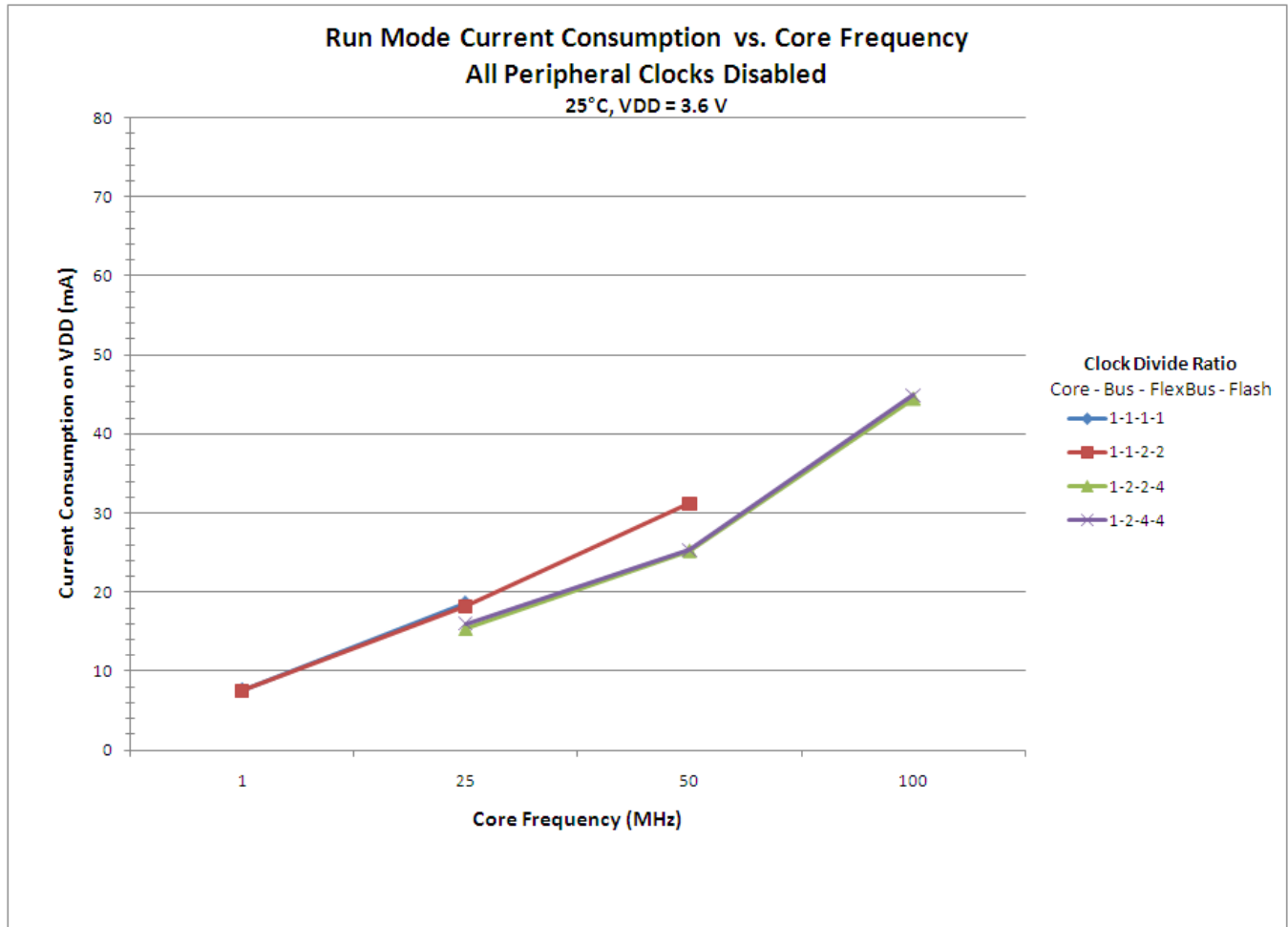
Figure 1. Run mode supply current vs. core frequency — all peripheral clocks disabled

The following data was measured under these conditions:

*   MCG in FEI mode (39.0625 kHz IRC), except for 1 MHz core (FBE)

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- All peripheral clocks enabled but peripherals are not in active operation
- LVD disabled, USB regulator disabled
- No GPIOs toggled
- Code execution from flash
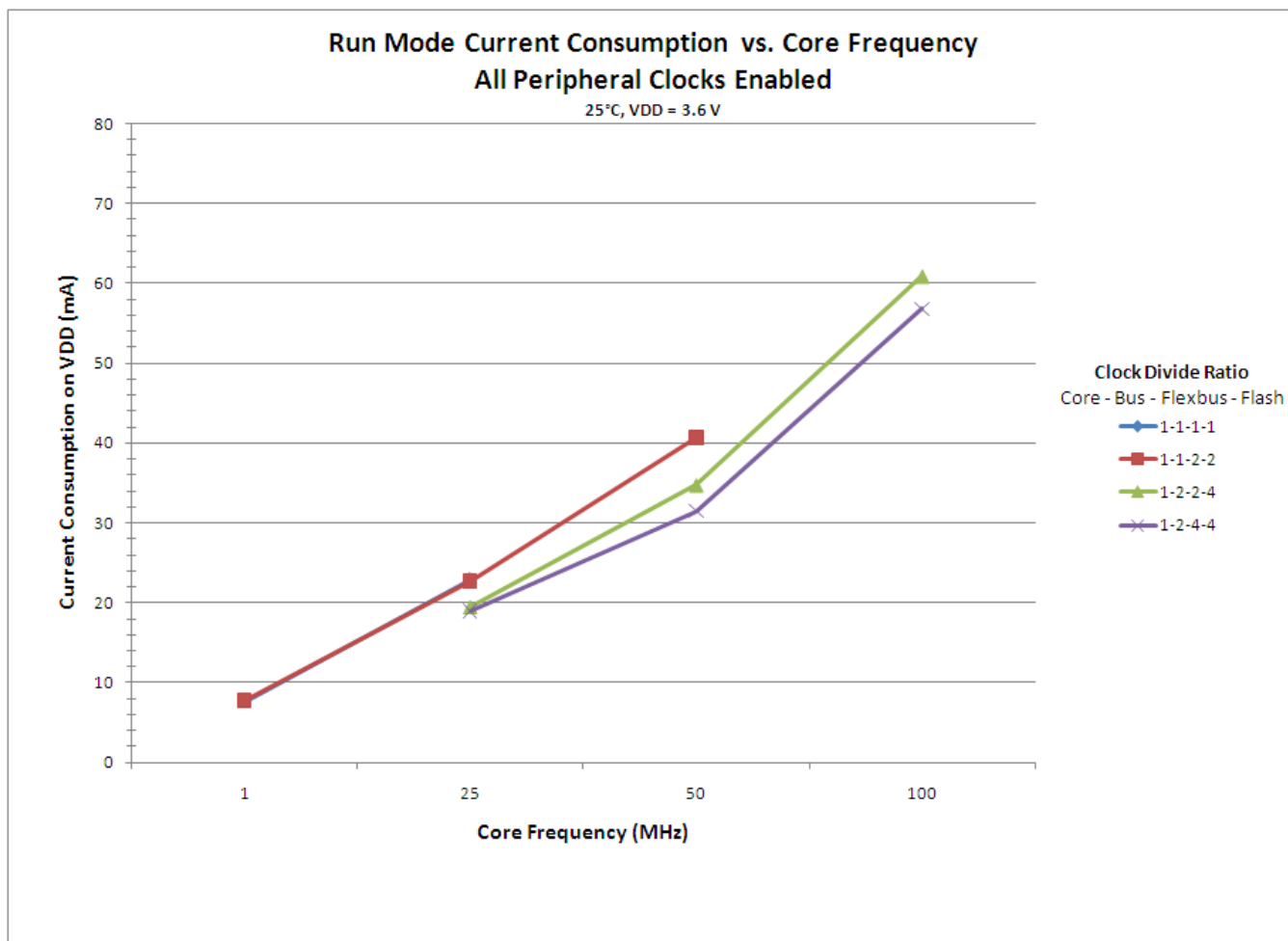
Figure 2. Run mode supply current vs. core frequency — all peripheral clocks enabled

5.1.6   EMC radiated emissions operating behaviors

Table 7.   EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	TBD		
V_{RE3}	Radiated emissions voltage, band 3	150–500	TBD		
V_{RE4}	Radiated emissions voltage, band 4	500–1000	TBD		
$V_{RE\_IEC\_SAE}$	IEC and SAE level	0.15–1000	TBD	—	2, 3

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1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions*, IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.
2. V_{DD} = 3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 96 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*, and Appendix D of SAE Standard J1752-3, *Measurement of Radiated Emissions from Integrated Circuits—TEM/Wideband TEM (GTEM) Cell Method*.

5.1.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:
1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

5.1.8 Capacitance attributes

Table 8.   Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.2 Switching specifications

5.2.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Normal run mode				
f_{SYS}	System and core clock	—	100	MHz	
f_{SYS_USB}	System and core clock when USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
	VLPR mode				
f_{SYS}	System and core clock	—	2	MHz	

Table continues on the next page...

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Symbol	Description	Min.	Max.	Unit	Notes
f_{BUS}	Bus clock	—	2	MHz	
FB_CLK	FlexBus clock	—	2	MHz	
f_{FLASH}	Flash clock	—	1	MHz	

5.2.2   General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I^{2}C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	TBD	—		
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength)				3
	• Slew disabled	—	12	ns	
	• Slew enabled	—	36	ns	
	Port rise and fall time (low drive strength)				4
	• Slew disabled	—	32	ns	
	• Slew enabled	—	36	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75pF load
4. 15pF load

5.3   Thermal specifications

5.3.1 Thermal operating requirements

Table 9. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40		°C

5.3.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	TBD	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	TBD	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	TBD	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	TBD	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	TBD	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

6 Peripheral operating requirements and behaviors

All digital I/O switching characteristics assume:

1. output pins
   - have C_L=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)

2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 10. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns
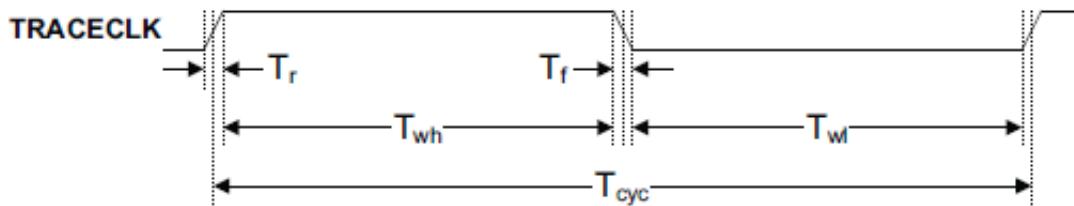
Figure 3. TRACE_CLKOUT specifications
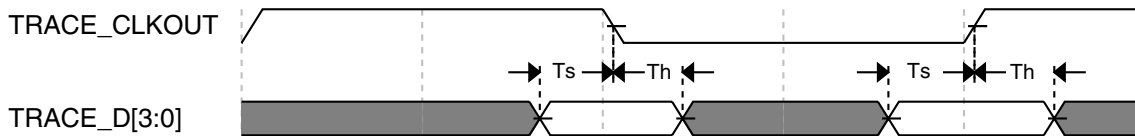
Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 11. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	

Table continues on the next page...

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Table 11. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	• Boundary Scan	50	—	
	• JTAG and CJTAG	20	—	
	• Serial Wire Debug	10		
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{TRST}$ assert time	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	8	—	ns

Table 12. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	• Boundary Scan	50	—	
	• JTAG and CJTAG	25	—	
	• Serial Wire Debug	12.5		
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns

Table continues on the next page...

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Table 12.   JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns
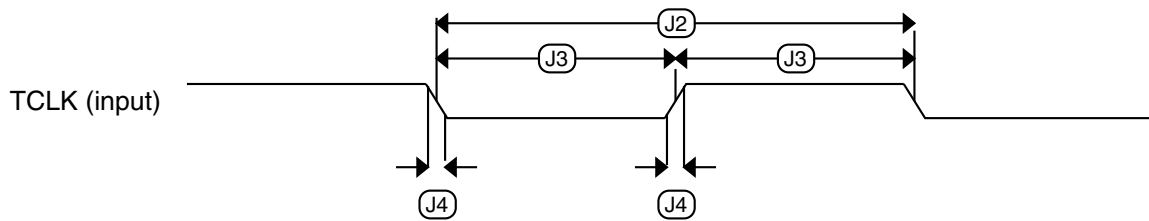
Figure 5. Test clock input timing
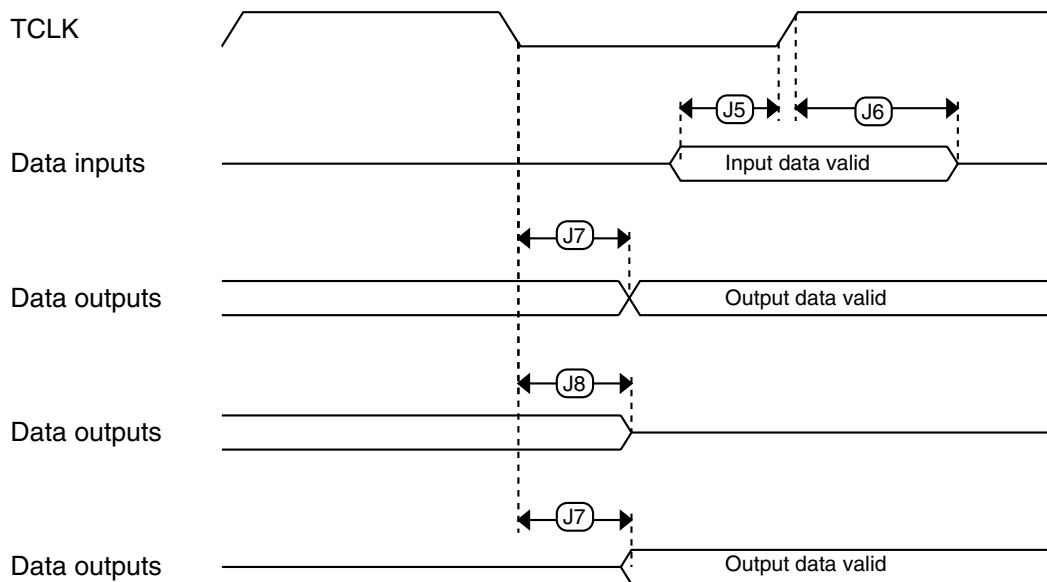
Figure 6. Boundary scan (JTAG) timing

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Figure 7. Test Access Port timing

Figure 8. $\overline{\text{TRST}}$ timing

6.2   System modules

There are no specifications necessary for the device's system modules.

6.3   Clock modules

6.3.1   MCG specifications

Table 13.   MCG specifications

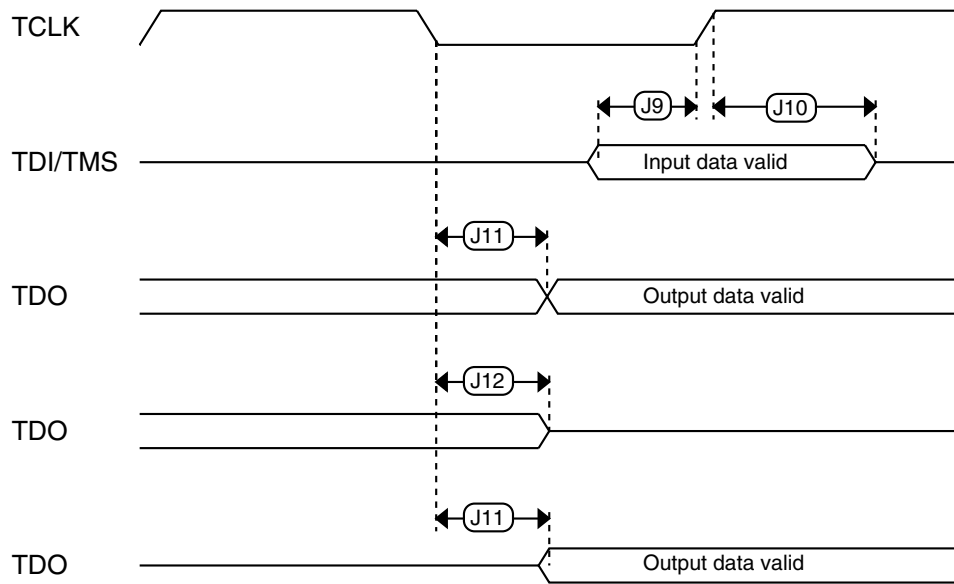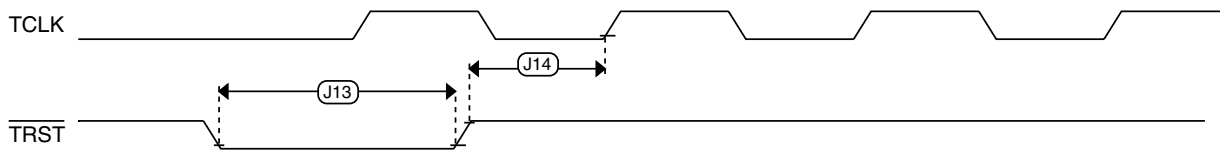| Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25°C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
I_{ints}	Internal reference (slow clock) current		—	TBD	—	µA	
$t_{irefsts}$	Internal reference (slow clock) startup time		—	TBD	4	µs	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.1	± 0.3	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+ 0.5 - 1.0	± 3.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.5	± TBD	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		3.4	—	4	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed		3	—	5	MHz	
I_{intf}	Internal reference (fast clock) current		—	TBD	—	µA	
$t_{irefstf}$	Internal reference startup time (fast clock)		—	TBD	TBD	µs	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	

Table continues on the next page...

Table 13.   MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	TBD	TBD	ps	6
J_{acc_fll}	FLL accumulated jitter of DCO output over a 1µs time window		—	TBD	TBD	ps	6
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	7
PLL							
f_{vco}	VCO operating frequency		48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$=8MHz, f_{pll_ref}=2MHz, VDIV multiplier=48)		—	950	—	µA	8
f_{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter		—	400	—	ps	9, 10
J_{acc_pll}	PLL accumulated jitter over 1µs window		—	TBD	—	ps	9, 10
D_{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time		—	—	0.15 + 1075(1/ f_{pll_ref})	ms	11

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification was obtained at TBD frequency.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification was obtained at internal frequency of TBD.
11. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 14. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	700	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz	—	800	—	µA	
	• 16 MHz	—	1.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 14. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 15. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	

Table continues on the next page...

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Table 15. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	TBD	—	ms	2, 3
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	800	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	4	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	3	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL
2. Proper PC board layout procedures must be followed to achieve specifications.
3. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.3   32kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1   32kHz oscillator DC electrical specifications

Table 16. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	2.5	—	pF
C_{load}	Internal load capacitance (programmable)	—	15	—	pF
V_{pp}	Peak-to-peak amplitude of oscillation	—	0.6	—	V

6.3.3.2   32kHz oscillator frequency specifications

Table 17. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1

1. Proper PC board layout procedures must be followed to achieve specifications.

6.4   Memories and memory interfaces

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6.4.1   Flash (FTFL) electrical specifications

This section describes the electrical characteristics of the FTFL module.

6.4.1.1   Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 18.   NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	20	TBD	µs	
$t_{hvrsscr}$	Sector Erase high-voltage time	—	20	100	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	160	800	ms	1

1.   Maximum time based on expectations at cycling end-of-life.

6.4.1.2   Flash timing specifications — commands
Table 19.   Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk256k}$	Read 1s Block execution time • 256 KB data flash	—	—	1.4	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	40	µs	1
t_{pgmchk}	Program Check execution time	—	—	35	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	35	µs	1
t_{pgm4}	Program Longword execution time	—	50	TBD	µs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB data flash	—	160	800	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	20	100	ms	2
$t_{pgmsec512}$ $t_{pgmsec1k}$ $t_{pgmsec2k}$	Program Section execution time • 512 B flash • 1 KB flash • 2 KB flash	— — —	TBD TBD TBD	TBD TBD TBD	ms ms ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.8	ms	
t_{rdonce}	Read Once execution time	—	—	35	µs	1
$t_{pgmonce}$	Program Once execution time	—	50	TBD	µs	

Table continues on the next page...

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Table 19. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{ersall}	Erase All Blocks execution time	—	320	1600	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	µs	1
$t_{pgmpart256k}$	Program Partition for EEPROM execution time • 256 KB FlexNVM	—	175	TBD	ms	
$t_{setram32k}$ $t_{setram256k}$	Set FlexRAM Function execution time: • 32 KB EEPROM backup • 256 KB EEPROM backup	— —	TBD TBD	TBD TBD	ms ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	100	TBD	µs	3
$t_{eewr8b32k}$ $t_{eewr8b64k}$ $t_{eewr8b128k}$ $t_{eewr8b256k}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup • 64 KB EEPROM backup • 128 KB EEPROM backup • 256 KB EEPROM backup	— — — —	TBD TBD TBD TBD	TBD 1.5 TBD 2.5	ms ms ms ms	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	100	TBD	µs	
$t_{eewr16b32k}$ $t_{eewr16b64k}$ $t_{eewr16b128k}$ $t_{eewr16b256k}$	Word-write to FlexRAM execution time: • 32 KB EEPROM backup • 64 KB EEPROM backup • 128 KB EEPROM backup • 256 KB EEPROM backup	— — — —	TBD TBD TBD TBD	TBD 1.5 TBD 2.5	ms ms ms ms	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	200	TBD	µs	
$t_{eewr32b32k}$ $t_{eewr32b64k}$ $t_{eewr32b128k}$ $t_{eewr32b256k}$	Longword-write to FlexRAM execution time: • 32 KB EEPROM backup • 64 KB EEPROM backup • 128 KB EEPROM backup • 256 KB EEPROM backup	— — — —	TBD TBD TBD TBD	TBD 2.7 TBD 3.7	ms ms ms ms	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

6.4.1.3 Flash (FTFL) current and power specfications

Table 20. Flash (FTFL) current and power specfications

Symbol	Description	Typ.	Unit
I_{DD_PGM}	Worst case programming current in program flash	10	mA

6.4.1.4 Reliability specifications

Table 21. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	TBD	—	years	2
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	10	TBD	—	years	2
$t_{nvmretp100}$	Data retention after up to 100 cycles	15	TBD	—	years	2
$n_{nvmcycp}$	Cycling endurance	10 K	TBD	—	cycles	3
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	TBD	—	years	2
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	10	TBD	—	years	2
$t_{nvmretd100}$	Data retention after up to 100 cycles	15	TBD	—	years	2
$n_{nvmcycd}$	Cycling endurance	10 K	TBD	—	cycles	3
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	TBD	—	years	2
$t_{nvmretee10}$	Data retention up to 10% of write endurance	10	TBD	—	years	2
$t_{nvmretee1}$	Data retention up to 1% of write endurance	15	TBD	—	years	2
	Write endurance					4
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	TBD	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	TBD	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	TBD	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	TBD	—	writes	
$n_{nvmwree32k}$	• EEPROM backup to FlexRAM ratio = 32,768	80 M	TBD	—	writes	

1. Typical data retention values are based on intrinsic capability of the technology measured at high temperature derated to 25°C. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618.
2. Data retention is based on T_{javg} = 55°C (temperature profile over the lifetime of the application).
3. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
4. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum value assumes all byte-writes to FlexRAM.

6.4.1.5   Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFL to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with Program Partition command
- Write_efficiency —
    - 0.25 for 8-bit writes to FlexRAM
    - 0.50 for 16-bit or 32-bit writes to FlexRAM

- $n_{nvmcycd}$ — data flash cycling endurance
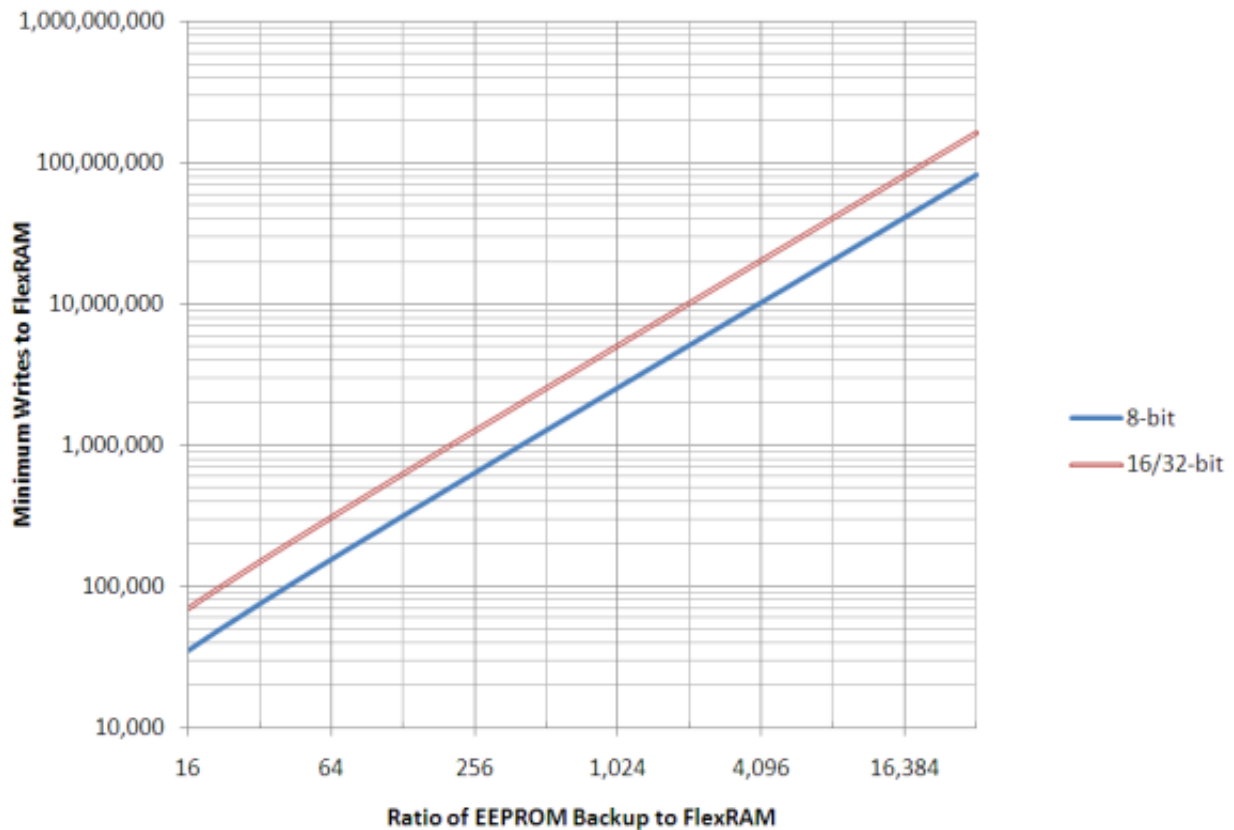
Figure 9. EEPROM backup writes to FlexRAM

6.4.2 EzPort Switching Specifications

Table 22. EzPort switching specifications

| Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{EZP\_CS}$ negation to next $\overline{EZP\_CS}$ assertion	$2 \times t_{EZP\_CK}$	—	ns
EP3	$\overline{EZP\_CS}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{EZP\_CS}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid (setup)	—	12	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{EZP\_CS}$ negation to EZP_Q tri-state	—	12	ns
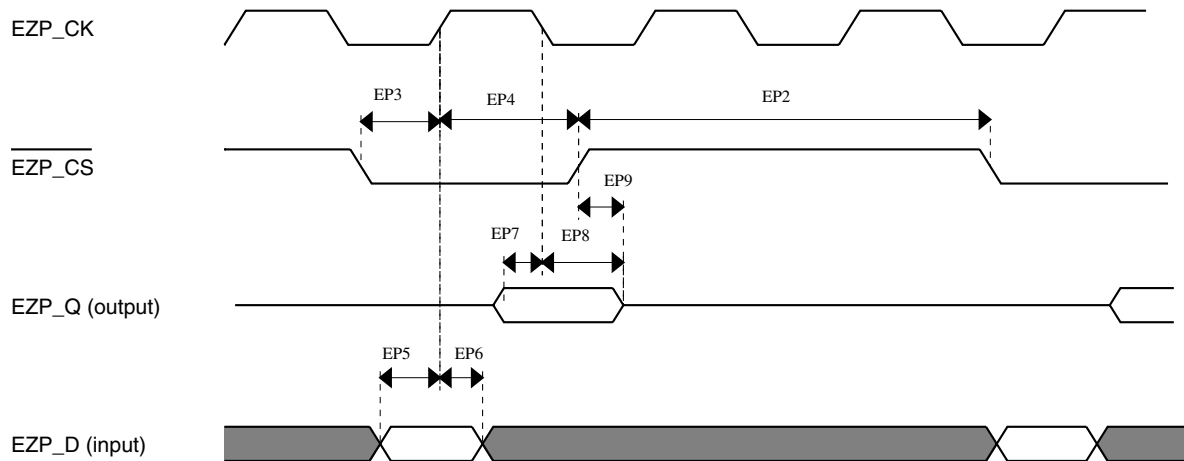
Figure 10. EzPort Timing Diagram

6.4.3 Flexbus Switching Specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 23. Flexbus switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	50	Mhz	
FB1	Clock period	20	—	ns	
FB2	Address, data, and control output valid	TBD	11.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and $\overline{FB\_TA}$ input setup	8.5	—	ns	2
FB5	Data and $\overline{FB\_TA}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{FB\_BE}/\overline{BWEn}$, $\overline{FB\_CSn}$, $\overline{FB\_OE}$, FB_R/$\overline{W}$,$\overline{FB\_TBST}$, FB_TSIZ[1:0], FB_ALE, and $\overline{FB\_TS}$.
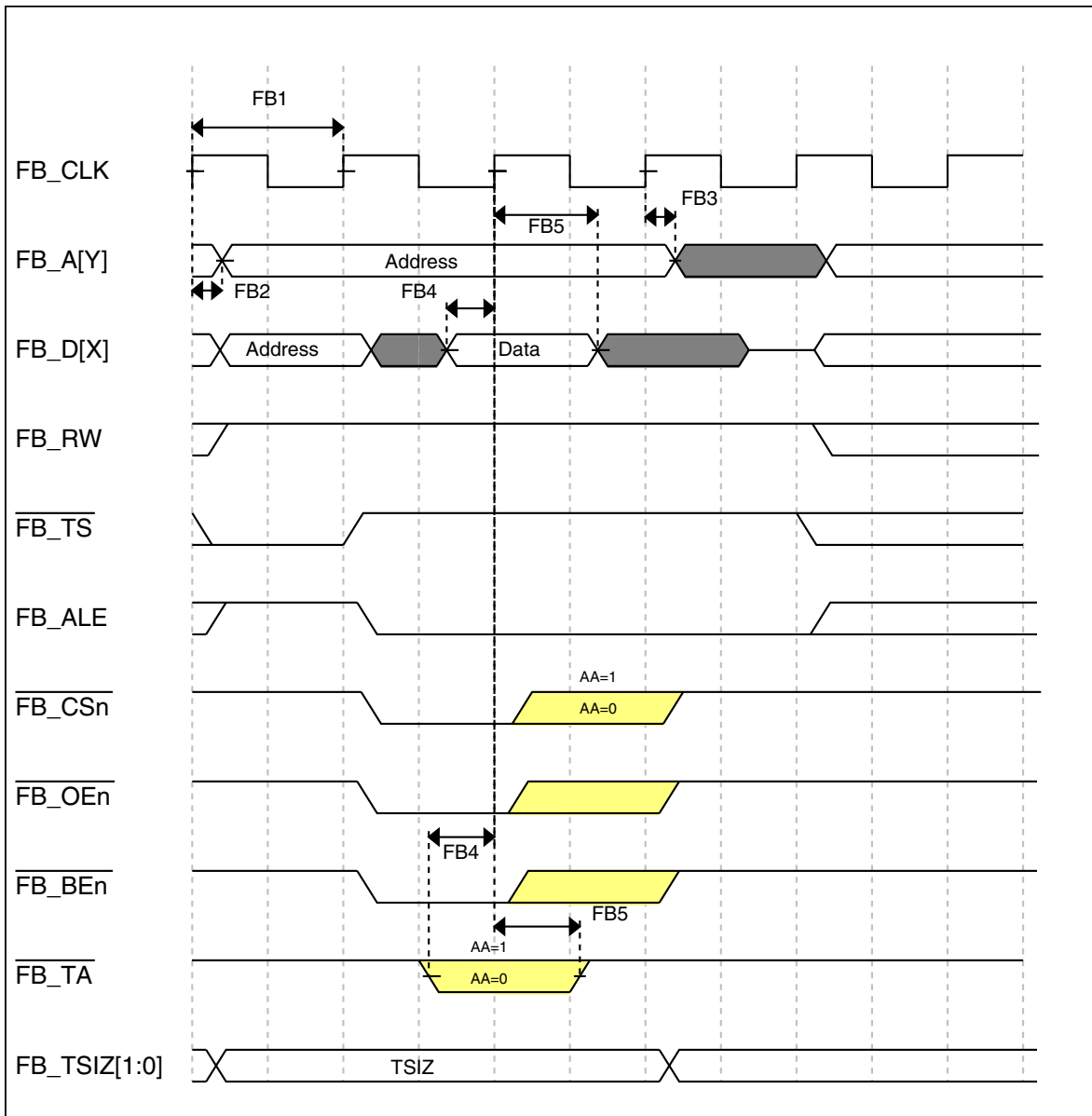2. Specification is valid for all FB_AD[31:0] and $\overline{FB\_TA}$.

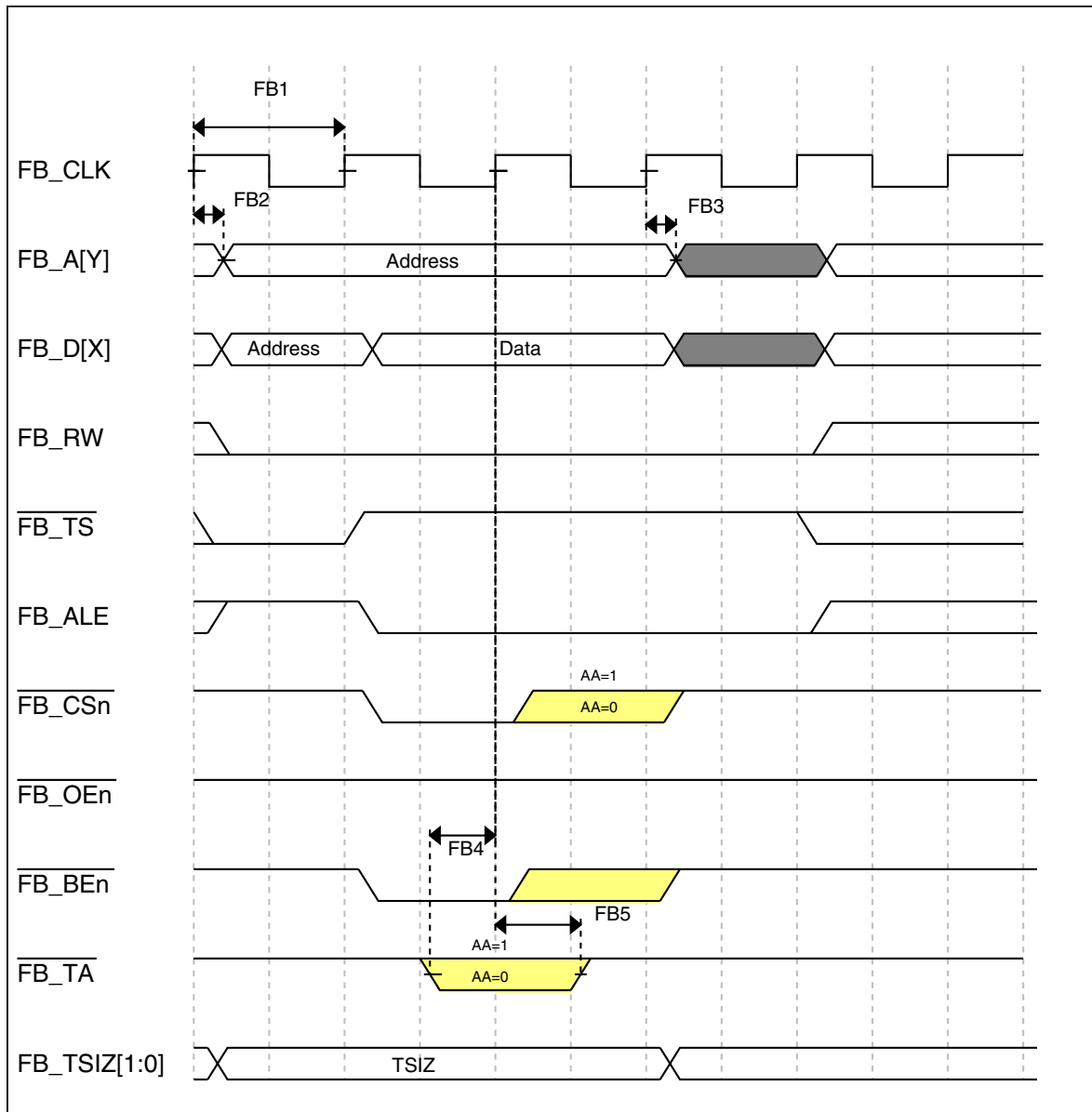**Figure 11. FlexBus read timing diagram**

Figure 12. FlexBus write timing diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 24 and Table 25 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DP3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are used as the PGA inputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 26 and Table 27.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 24.   16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	Reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16 bit modes	—	8	10	pF	
		• 8/10/12 bit modes	—	4	5		
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13/12 bit modes $f_{ADCK} < 4MHz$	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤13 bit modes	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	5

Table continues on the next page...

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Table 24.   16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	≤13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50MHz	18.484	—	818.330	Ksps	6
C_{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50MHz	37.037	—	361.402	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1ns.
4. In order to use the maximum ADC conversion clock frequency ADHSC bit should be set and the ADLPC should be clear.
5. In order to use the maximum ADC conversion clock frequency ADHSC bit should be set and the ADLPC should be clear.
6. For guidelines and examples of conversion rate calculation please download the ADC calculator tool http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1
7. For guidelines and examples of conversion rate calculation please download the ADC calculator tool http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1
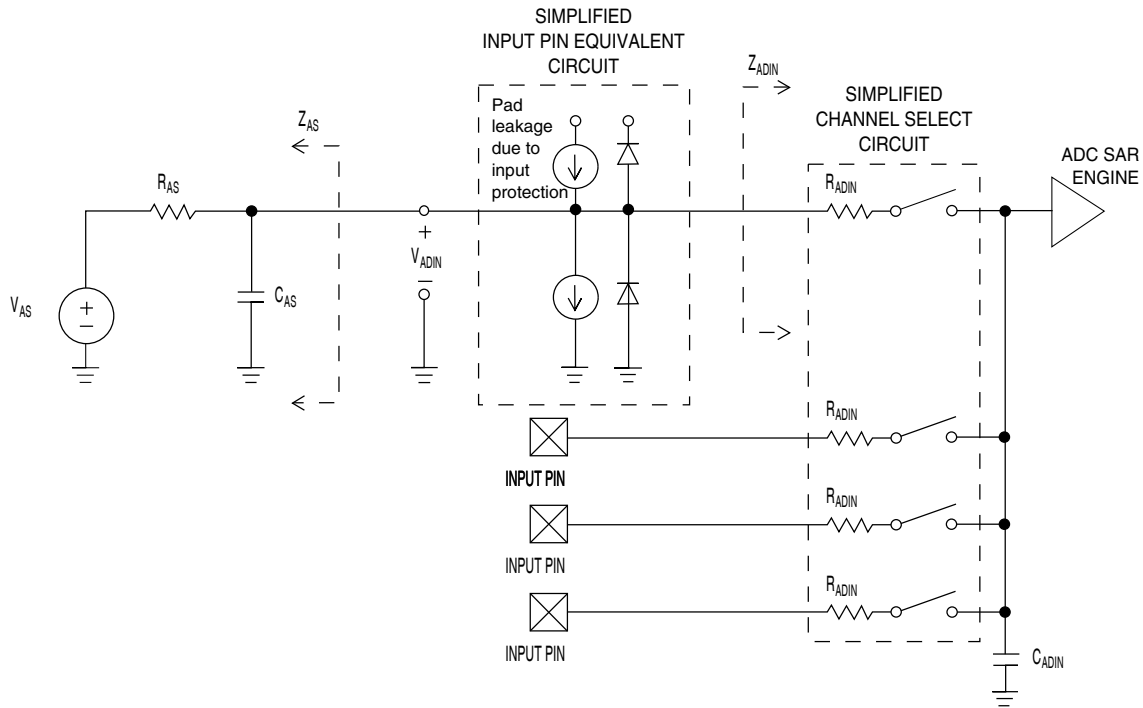
Figure 13. ADC input impedance equivalency diagram

6.6.1.2   16-bit ADC electrical characteristics

Table 25.   16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0	—	2.4	—	MHz	$t_{ADACK} = 1/ f_{ADACK}$
		• ADLPC=1, ADHSC=1	—	4.0	—	MHz	
		• ADLPC=0, ADHSC=0	—	5.2	—	MHz	
		• ADLPC=0, ADHSC=1	—	6.2	—	MHz	
	Sample Time	See Reference Manual chapter for sample times					
	Conversion Time	The ADC calculator tool can be used to determine ADC conversion times for different ADC configurations: http://cache.freescale.com/files/soft_dev_tools/software/app_software/ converters/ADC_CALCULATOR_CNV.zip?fpsp=1					
TUE	Total unadjusted error	• ≤13 bit modes		±0.8	±TBD	LSB[4]	ADC conversion clock <12MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
		• <12 bit modes		±0.5	±1		

Table continues on the next page...

Table 25.   16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
DNL	Differential non-linearity	• ≤13 bit modes • <12 bit modes		±0.7 ±0.2	±TBD ±0.5	LSB[4]	ADC conversion clock <12MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
INL	Integral non-linearity	• ≤13 bit modes • <12 bit modes	— —	±1.0 ±0.5	±TBD ±TBD	LSB[4]	Max averaging
E$_{FS}$	Full-scale error	• ≤13 bit modes • <12 bit modes	— —	±0.4 ±1.0	±TBD ±TBD	LSB[4]	V_{ADIN} = V_{DDA}
E$_Q$	Quantization error	• 16 bit modes • ≤13 bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16 bit differential mode • Avg=32 • Avg=1 16 bit single-ended mode • Avg=32 • Avg=1	 TBD TBD TBD TBD	 13.6 13.2 TBD TBD	 TBD TBD TBD TBD	 bits bits bits bits	5
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit differential mode • Avg=32 16 bit single-ended mode • Avg=32	 — —	 -94 TBD	 TBD TBD	 dB dB	5
SFDR	Spurious free dynamic range	16 bit differential mode • Avg=32 16 bit single-ended mode • Avg=32	 TBD TBD	 95 TBD	 — —	 dB dB	5

Table continues on the next page...

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Table 25. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_{IL}	Input leakage error			$I_{In} \times R_{AS}$		mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	• −40°C to 25°C	—	TBD	—	mV/°C	
		• 25°C to 105°C	—	TBD	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	TBD	—	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. Input data is 1 kHz sine wave.

FIGURE TBD

Figure 14. Typical TUE vs. ADC conversion rate 12-bit single-ended mode

FIGURE TBD

Figure 15. Typical ENOB vs. Averaging for 16-bit differential and 16-bit single-ended modes

6.6.1.3 16-bit ADC with PGA operating conditions
Table 26. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V_{REFPGA}	PGA ref voltage		VREFOUT	VREFOUT	VREFOUT	V	2, 3
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
V_{CM}	Input Common Mode range		V_{SSA}	—	V_{DDA}	V	

Table continues on the next page...

Table 26. 16-bit ADC with PGA operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
R_{PGAD}	Differntial input impedance	Gain = 1, 2, 4, 8	—	128	—	kΩ	IN+ to IN-[4]
		Gain = 16, 32	—	64	—		
		Gain = 64	—	32	—		
R_{AS}	Analog source resistance		—	100	—	Ω	5
T_S	ADC sampling time		1.25	—	—	µs	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREFOUT)
3. PGA reference connected to the VREFOUT pin. If the user wishes to drive VREFOUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedence of the driven input is 1/2.
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.

6.6.1.4 16-bit ADC with PGA characteristics
Table 27. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA_PGA}	Supply current		—	590	TBD	µA	
I_{DC_PGA}	Input DC current		$\dfrac{2}{R_{PGAD}}\left(\dfrac{\left(V_{REFPGA}\times0.583\right)-V_{CM}}{(Gain+1)}\right)$			A	2
I_{ILKG}	Input Leakage current	PGA disabled	—	TBD	TBD	µA	3
G	Gain[4]	• PGAG=0	TBD	0.98	TBD		$R_{AS} < 100\Omega$
		• PGAG=1	TBD	1.99	TBD		
		• PGAG=2	TBD	3.97	TBD		
		• PGAG=3	TBD	7.95	TBD		
		• PGAG=4	TBD	15.8	TBD		
		• PGAG=5	TBD	31.4	TBD		
		• PGAG=6	TBD	61.2	TBD		
BW	Input signal bandwidth	• 16-bit modes	—	—	4	kHz	
		• < 16-bit modes	—	—	40	kHz	
PSRR	Power supply rejection ration	Gain=1	TBD	TBD	—	dB	V_{DDA}= 3V ±100mV, f_{VDDA}= 50Hz, 60Hz

Table continues on the next page...

Table 27.   16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
CMRR	Common mode rejection ratio	• Gain=1	TBD	TBD	—	dB	V_{CM}= 500mVpp, f_{VCM}= 50Hz, 100Hz
		• Gain=64	TBD	TBD	—	dB	
V_{OFS}	Input offset voltage		—	0.2	TBD	mV	Gain=1, ADC Averaging=32
T_{GSW}	Gain switching settling time		—	—	10	µs	5
dG/dT	Gain drift over temperature	• Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C
		• Gain=64	—	TBD	TBD	ppm/°C	
dV_{OFS}/dT	Offset drift over temperature	Gain=1	—	TBD	TBD	ppm/°C	0 to 50°C, ADC Averaging=32
dG/dV_{DDA}	Gain drift over supply voltage	• Gain=1	—	TBD	TBD	%/V	V_{DDA} from 1.71 to 3.6V
		• Gain=64	—	TBD	TBD	%/V	
E_{IL}	Input leakage error	All modes	$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
$V_{PP,DIFF}$	Maximum differential input signal swing		$\left(\dfrac{\left(\min\!\left(V_X, V_{DDA}-V_X\right)-0.2\right)\times 4}{\text{Gain}}\right)$ where $V_X = V_{REFPGA} \times 0.583$			V	6
SNR	Signal-to-noise ratio	• Gain=1	TBD	83.0	—	dB	16-bit differential mode, Average=32
		• Gain=64	TBD	57.5	—	dB	
THD	Total harmonic distortion	• Gain=1	TBD	89.4	—	dB	16-bit differential mode, Average=32, f_{in}=500Hz
		• Gain=64	TBD	90.0	—	dB	
SFDR	Spurious free dynamic range	• Gain=1	TBD	90.9	—	dB	16-bit differential mode, Average=32, f_{in}=500Hz
		• Gain=64	TBD	77.0	—	dB	

Table continues on the next page...

Table 27. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
ENOB	Effective number of bits	• Gain=1, Average=4	TBD	12.3	—	bits	16-bit differential mode, f_{in}=500Hz
		• Gain=1, Average=8	TBD	12.7	—	bits	
		• Gain=64, Average=4	TBD	8.4	—	bits	
		• Gain=64, Average=8	TBD	8.7	—	bits	
		• Gain=1, Average=32	TBD	13.3	—	bits	
		• Gain=2, Average=32	TBD	13.1	—	bits	
		• Gain=4, Average=32	TBD	12.5	—	bits	
		• Gain=8, Average=32	TBD	11.8	—	bits	
		• Gain=16, Average=32	TBD	11.1	—	bits	
		• Gain=32, Average=32	TBD	10.2	—	bits	
		• Gain=64, Average=32	TBD	9.3	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	\multicolumn{3}{c}{$6.02 \times$ ENOB + 1.76}	dB	

1. Typical values assume V_{DDA} =3.0V, Temp=25°C, f_{ADCK}=6MHz unless otherwise stated.
2. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function if input common mode voltage (V_{CM}) and the PGA gain.
3. This is the input leakage current of the module in addition to the PAD leakage current.
4. Gain = 2^{PGAG}
5. When the PGA gain is changed, it takes some time to settle the output for the ADC to work properly. During a gain switching, a few ADC outputs should be discarded (minimum two data samples, may be more depending on ADC sampling rate and time of the switching).
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2   CMP and 6-bit DAC electrical specifications

Table 28.   Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV

Table continues on the next page...

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Table 28. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	120	250	600	ns
	Analog comparator initialization delay[2]	—	—	TBD	ns
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	−0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	−0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
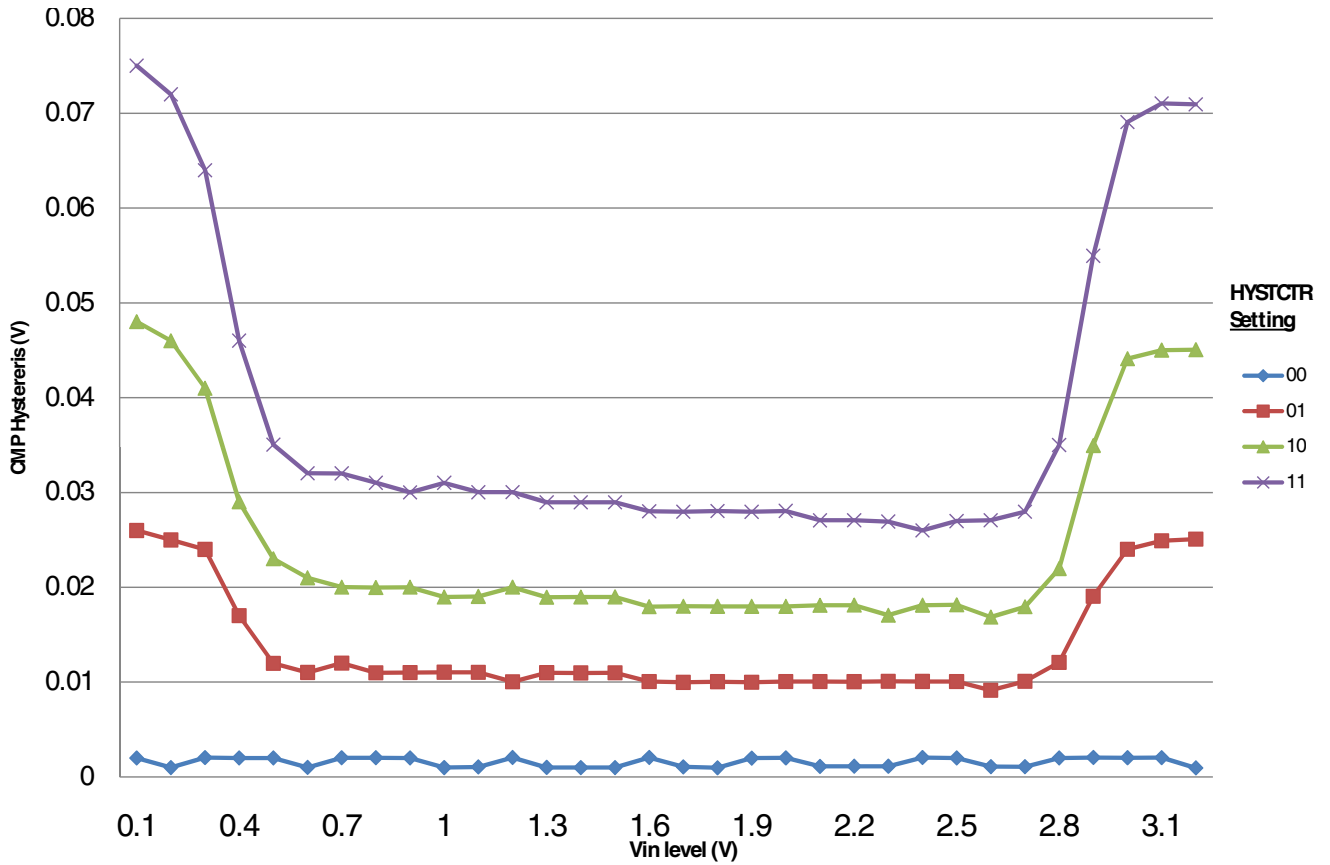3. 1 LSB = $V_{reference}/64$

Figure 16. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)
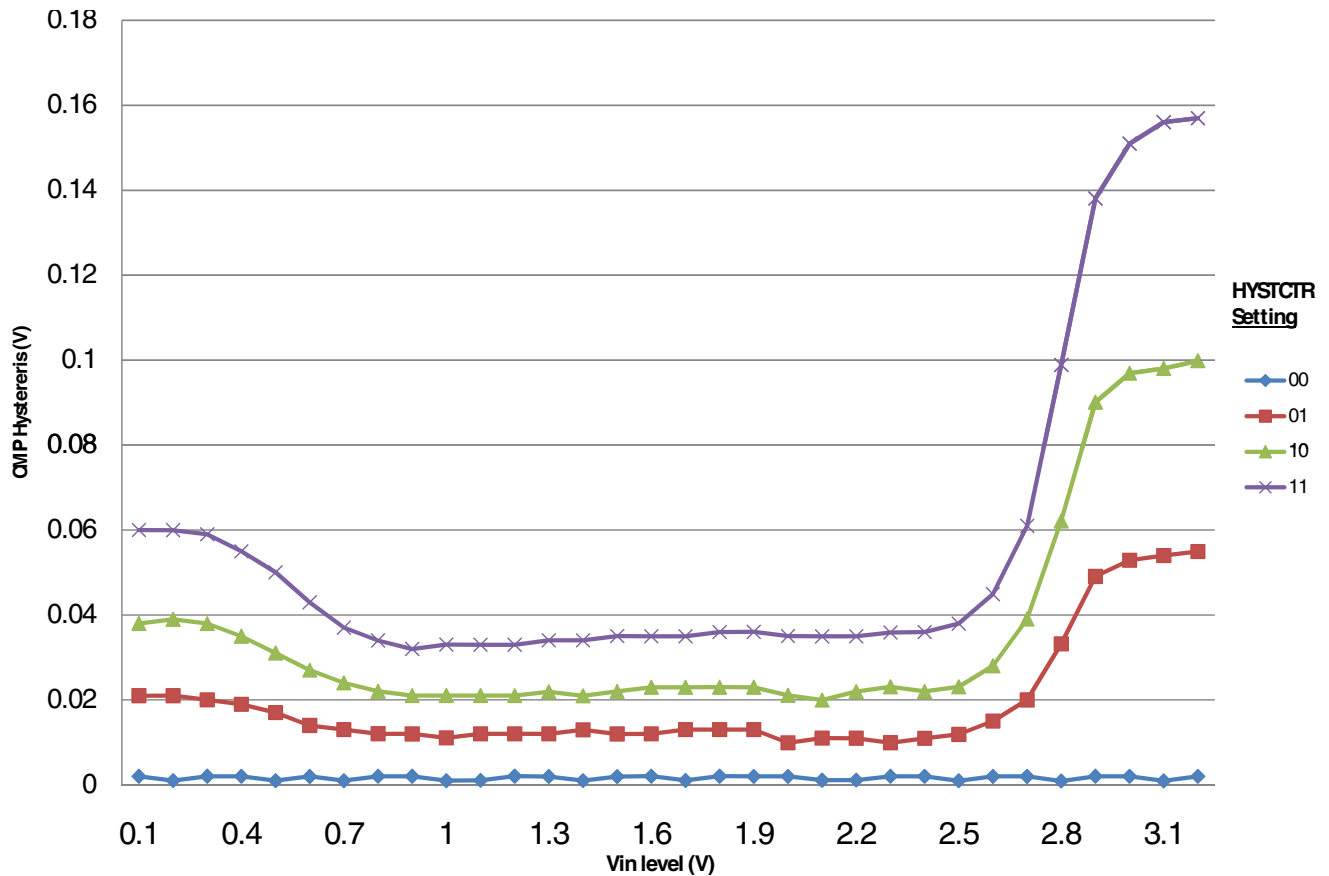
Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3   12-bit DAC electrical characteristics

6.6.3.1   12-bit DAC operating requirements
Table 29.   12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	−40	105	°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREFO)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2   12-bit DAC operating behaviors
Table 30.   12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode	—	—	5	µs	1
$t_{CCDACHP}$	Code-to-code settling time (0xBF8 to 0xC08) — high-speed mode	1	TBD	—	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	100	TBD	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREFO (1.15 V)	—	—	±1	LSB	4
V_{OFFSET}	Offset error	±0.4	—	±0.8	%FSR	5
E_G	Gain error	±0.1	—	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} > = 2.4 V	60		90	dB	
T_{CO}	Temperature coefficient offset voltage	—	TBD	—	µV/C	
T_{GE}	Temperature coefficient gain error	—	TBD	—	ppm of FSR/C	
A_C	Offset aging coefficient	—	—	TBD	µV/yr	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100 mV to V_{DACR}−100 mV
4. The DNL is measured for 0+100mV to V_{DACR}−100 mV with V_{DDA} > 2.4V

5. Calculated by a best fit curve from V_{SS}+100 mV to VREF−100 mV
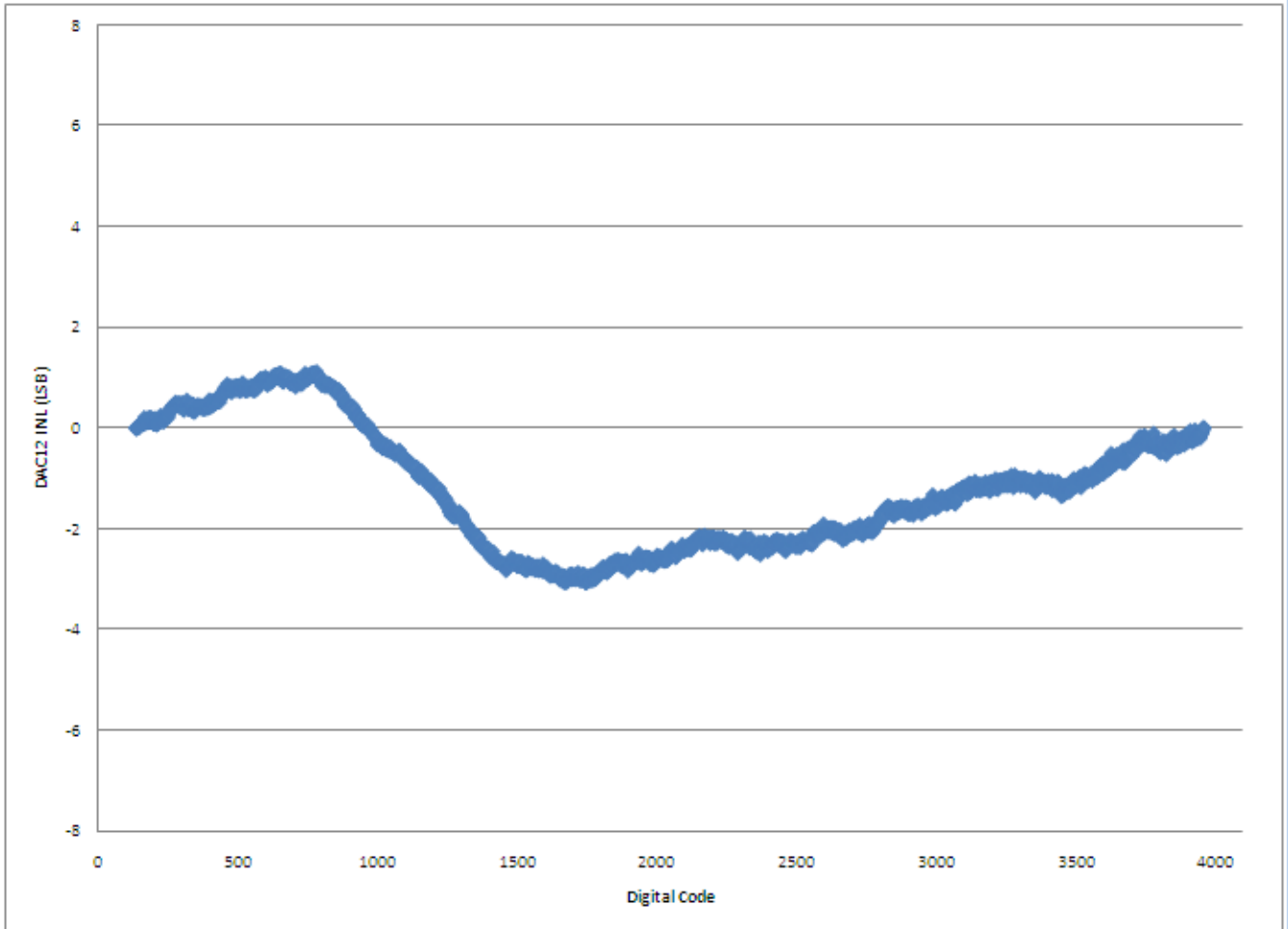
Figure 18. Typical INL error vs. digital code
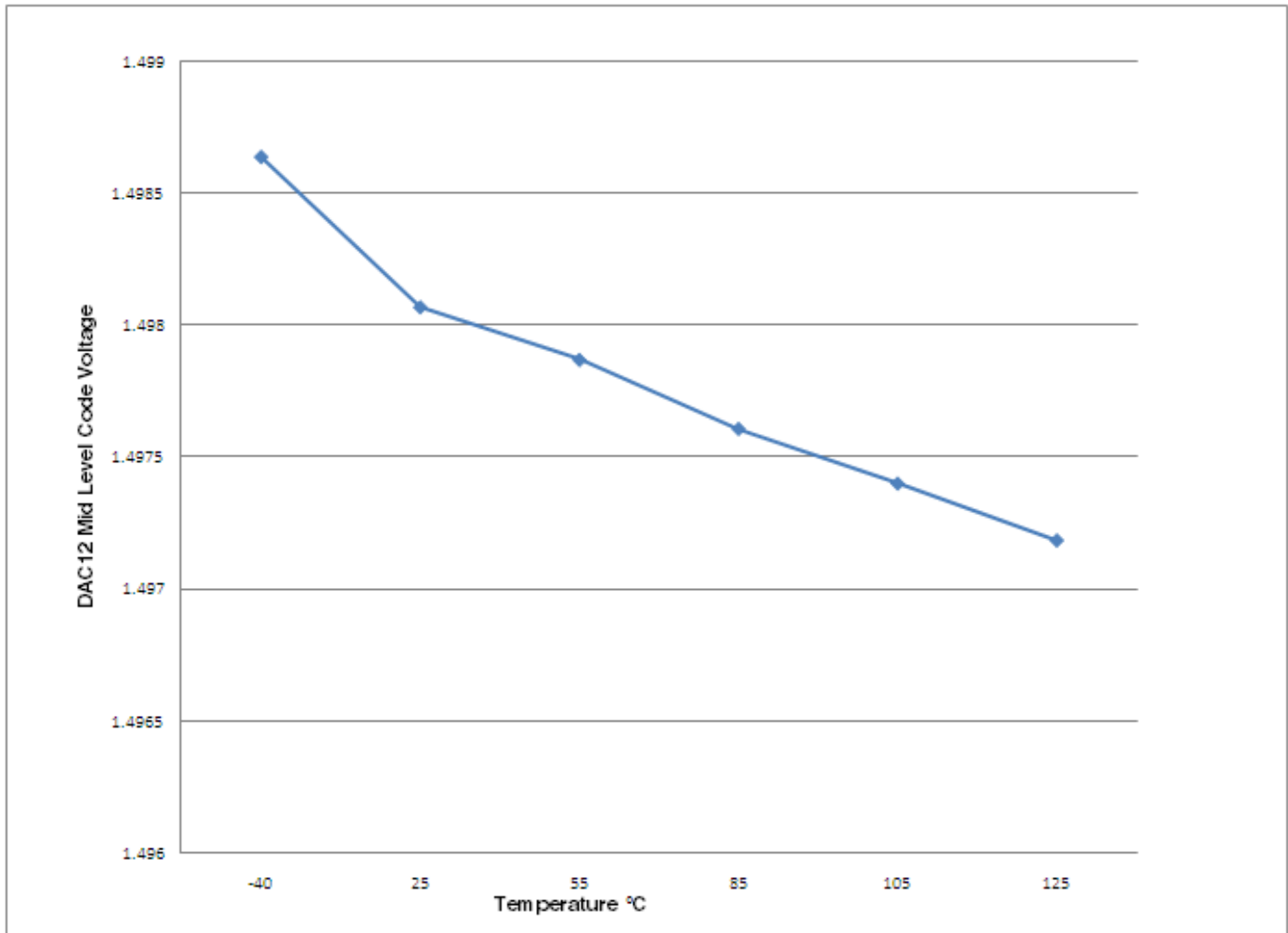
Figure 19. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 31. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	−40	105	°C	
C_L	Output load capacitance	—	100	nF	

Table 32. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	TBD	1.2	TBD	V	

Table continues on the next page...

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Table 32.   VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	TBD	—	TBD	V	
V_{out}	Voltage reference output user trim	1.198	—	1.202	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{drift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	20	mV	See Figure 20
Ac	Aging coefficient	—	—	TBD	ppm/year	
I_{bg}	Bandgap only (MODE_LV = 00) current	—	—	TBD	µA	
I_{tr}	Tight-regulation buffer (MODE_LV =10) current	—	—	1.1	mA	
	Load regulation (MODE_LV = 10) current = ±1.0mA	—	—	TBD	V	
T_{stup}	Buffer startup time	—	—	100	µs	
DC	Line regulation (power supply rejection)	—	—	TBD	mV	
		–60	—	TBD	dB	

Table 33.   VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 34.   VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	TBD	TBD	V	

TBD

Figure 20. Typical output vs.temperature

TBD

Figure 21. Typical output vs. VDD

6.7 Timers

See General switching specifications.

6.8   Communication interfaces

6.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

6.8.2 USB DCD electrical specifications

Table 35.   USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	TBD	TBD	TBD	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	TBD	0.4	V

6.8.3 USB VREG electrical specifications

Table 36.   USB VREG electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	TBD	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1	TBD	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25C • Across operating voltage and temperature	— —	500 —	— TBD	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.5	 3.3 2.8	 3.6 3.6	 V V	

Table continues on the next page...

Table 36. USB VREG electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.3	—	3.6	V	1
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Current limitation threshold	185	290	395	mA	

1. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.4 CAN switching specifications

See General switching specifications.

6.8.5 DSPI switching specifications (low-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 37. Master mode DSPI timing (low-speed mode)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BCLK}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCSn to DSPI_SCK output valid	$(t_{SCK}/2) - 4$	—	ns	
DS4	DSPI_SCK to DSPI_PCSn output hold	$(t_{SCK}/2) - 4$	—	ns	
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
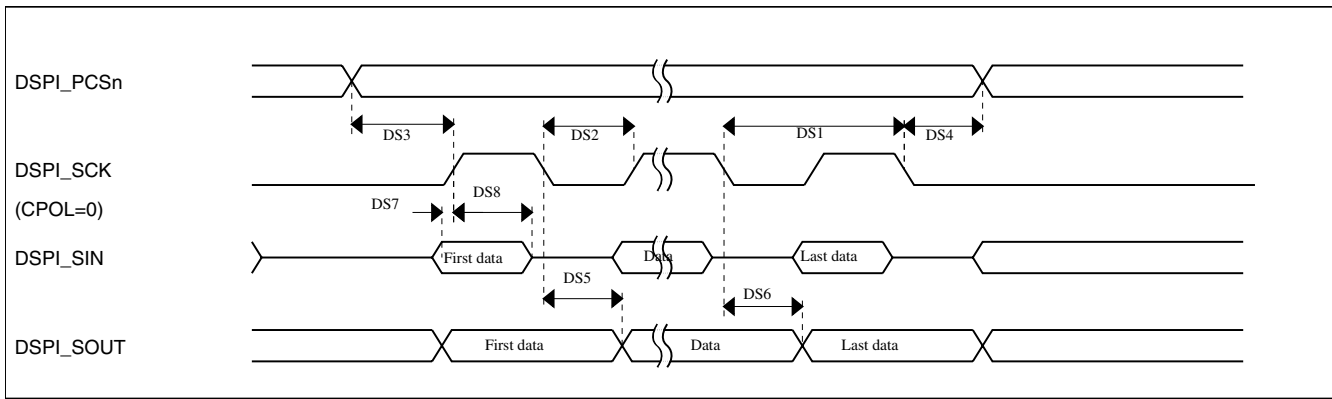
Figure 22. DSPI classic SPI timing — master mode

Table 38. Slave mode DSPI timing (low-speed mode)

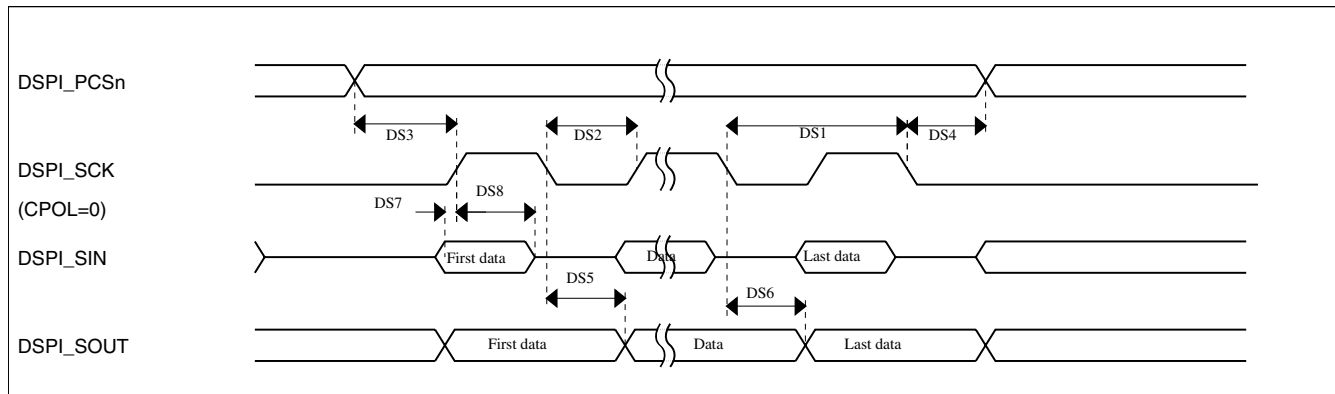| Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BCLK}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	5	—	ns
DS14	DSPI_SCK to DSIP_SIN input hold	15	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	15	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	15	ns
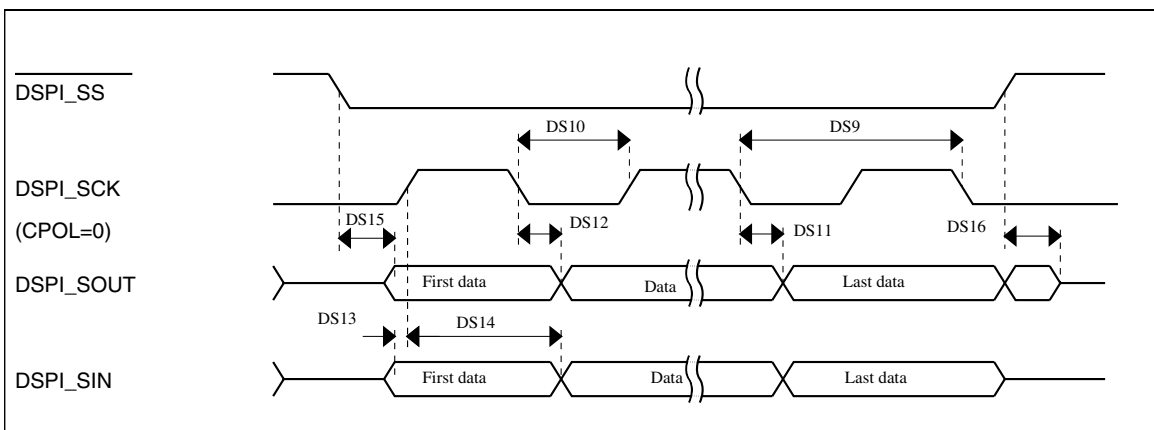
Figure 23. DSPI classic SPI timing — slave mode

6.8.6 DSPI switching specifications (high-speed mode)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 39. Master mode DSPI timing (high-speed mode)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation	—	25	MHz
DS1	DSPI_SCK output cycle time	$2 \times t_{BCLK}$	—	ns
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS3	DSPI_PCSn to DSPI_SCK output valid	$(t_{SCK}/2) - 2$	—	ns
DS4	DSPI_SCK to DSPI_PCSn output hold	$(t_{SCK}/2) - 2$	—	ns
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns
DS7	DSPI_SIN to DSPI_SCK input setup	TBD	—	ns
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns

Figure 24. DSPI classic SPI timing — master mode

**Table 40. Slave mode DSPI timing (high-speed mode)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BCLK}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2 + 2$	ns

Table continues on the next page...

Table 40. Slave mode DSPI timing (high-speed mode) (continued)

Num	Description	Min.	Max.	Unit
DS11	DSPI_SCK to DSPI_SOUT valid	—	TBD	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSIP_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	14	ns
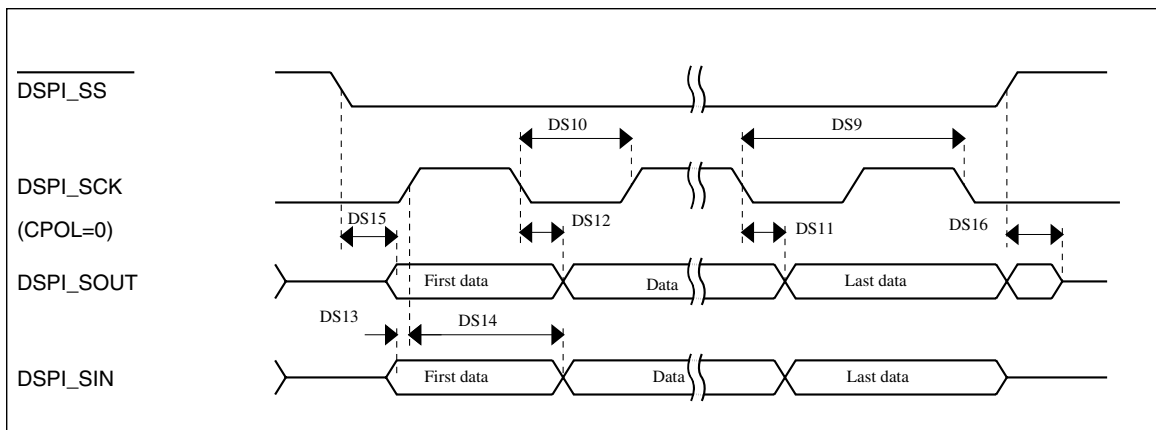
Figure 25. DSPI classic SPI timing — slave mode

6.8.7   I²C switching specifications

See General switching specifications.

6.8.8   UART switching specifications

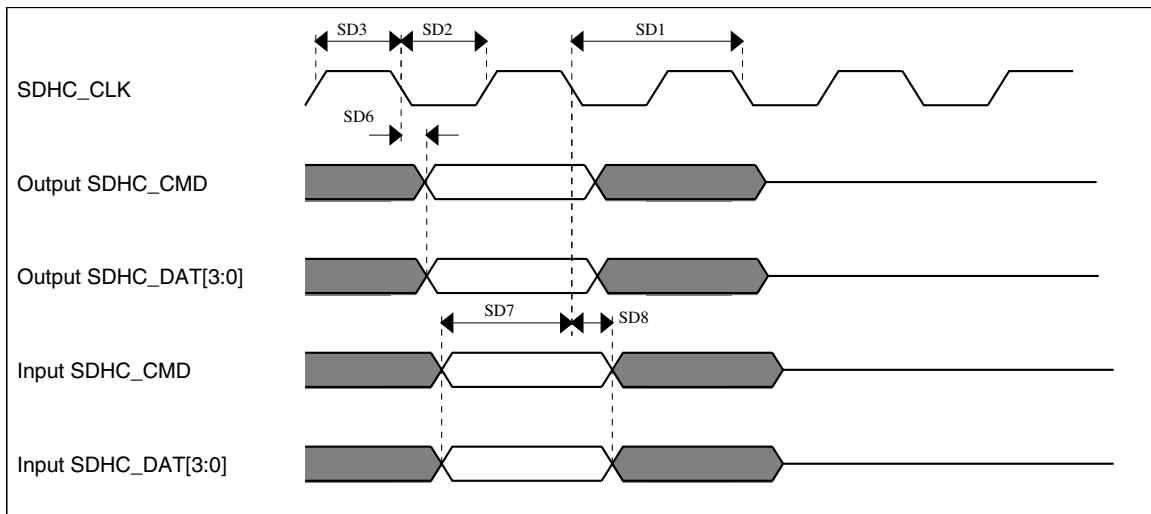See General switching specifications.

6.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 41. SDHC switching specifications

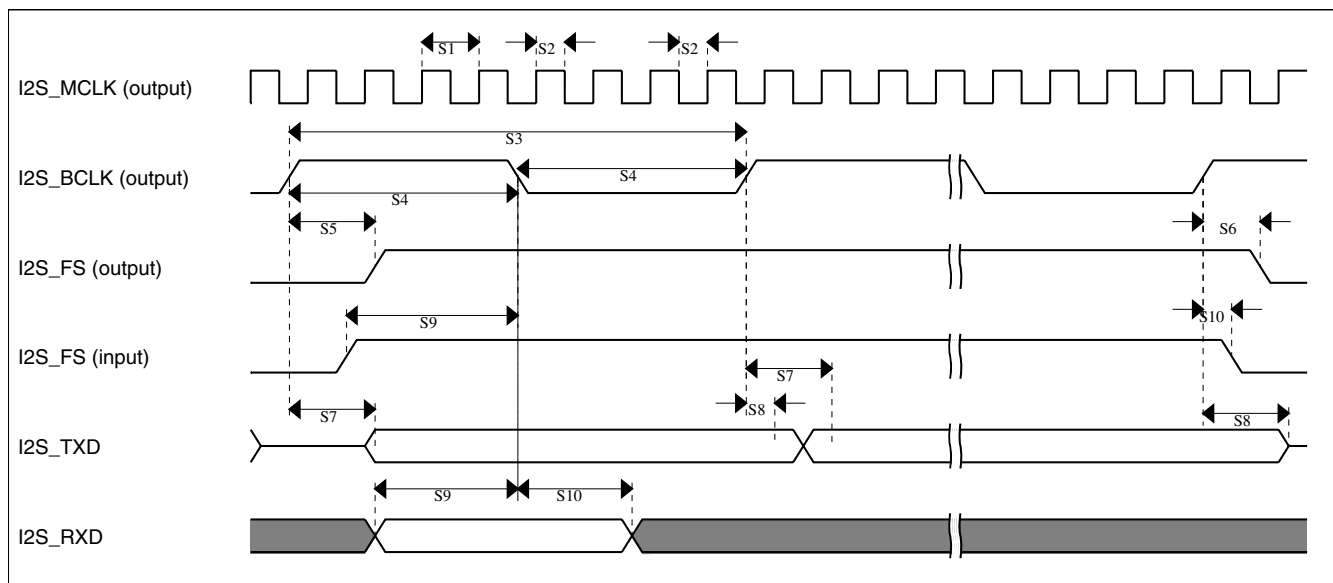| Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
Card input clock					
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t_{OD}	SDHC output delay (output valid)	-5	6.5	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t_{THL}	SDHC input setup time	5	—	ns
SD8	t_{THL}	SDHC input hold time	0	—	ns

Figure 26. SDHC timing

6.8.10   I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 42.   I²S master mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t$_{SYS}$		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t$_{SYS}$	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Figure 27. I²S timing — master mode

Table 43. I²S slave mode timing

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t_{SYS}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
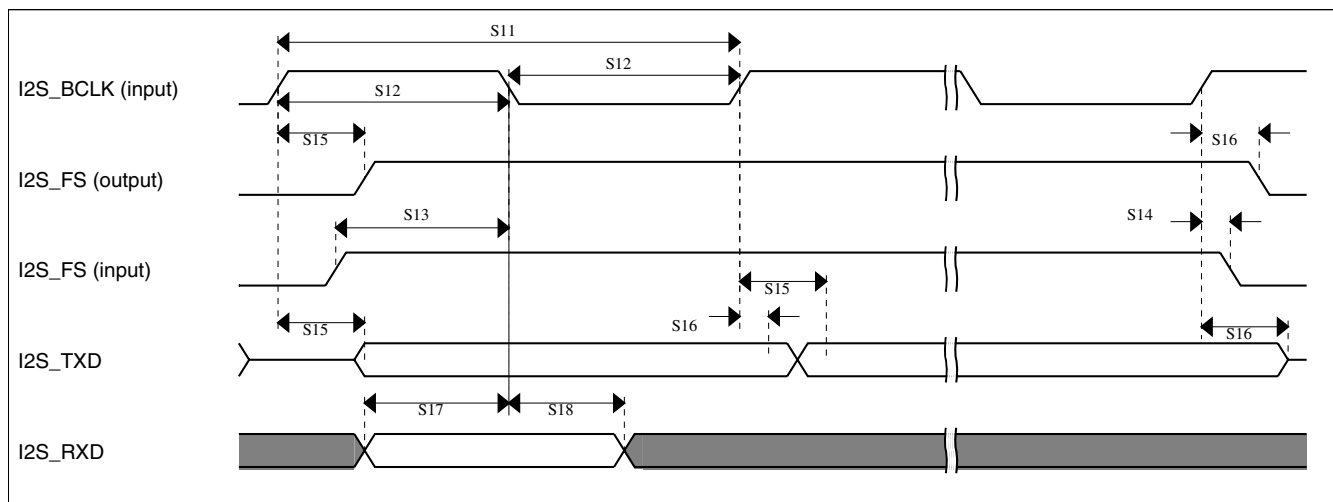
Figure 28. I²S timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 44. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	5.5	TBD	MHz	
f_{ELEmax}	Electrode oscillator frequency	—	0.5	TBD	MHz	

Table continues on the next page...

Table 44. TSI electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
C_{REF}	Internal reference capacitor	TBD	1	TBD	pF	
V_{DELTA}	Oscillator delta voltage	TBD	600	TBD	mV	
I_{REF}	Reference oscillator current source base current	TBD	1	TBD	µA	2
I_{ELE}	Electrode oscillator current source base current	TBD	1	TBD	µA	2
Pres5	Electrode capacitance measurement precision	—	TBD	TBD	%	3
Pres20	Electrode capacitance measurement precision	—	TBD	TBD	%	4
Pres100	Electrode capacitance measurement precision	—	TBD	TBD	%	5
MaxSens20	Maximum sensitivity @ 20 pF electrode	0.003	0.25	—	fF/count	6
MaxSens	Maximum sensitivity	0.003	—	—	fF/count	7
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	8
I_{TSI_RUN}	Current added in run mode	—	TBD	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1	TBD	µA	

1.   The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2.   The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
3.   Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; Iext = 16.
4.   Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; Iext = 16.
5.   Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; Iext = 16.
6.   Measured with a 20 pF electrode, reference oscillator frequency of ~5 MHz ($I_{REF} = 5$ µA, REFCHRG = 4), PS = 128, NSCN = 2; Iext = 16 (EXTCHRG = 15).
7.   Typical value depends on the configuration used.
8.   Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.

7   Dimensions

7.1   Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
121-pin MAPBGA	TBD

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8 Pinout

8.1 K20 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
•	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
•	PTE1	ADC1_SE5a	ADC1_SE5a	PTE1	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
•	PTE2	ADC1_SE6a	ADC1_SE6a	PTE2	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
•	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD				
•	PTE4	DISABLED		PTE4	SPI1_PCS0	UART3_TX	SDHC0_D3				
•	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
•	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		I2S0_CLKIN		
•	VDD	VDD	VDD								
•	VSS	VSS	VSS								
•	USB0_DP	USB0_DP	USB0_DP								
•	USB0_DM	USB0_DM	USB0_DM								
•	VOUT33	VOUT33	VOUT33								
•	VREGIN	VREGIN	VREGIN								
•	ADC0_DP1	ADC0_DP1	ADC0_DP1								
•	ADC0_DM1	ADC0_DM1	ADC0_DM1								
•	ADC1_DP1	ADC1_DP1	ADC1_DP1								
•	ADC1_DM1	ADC1_DM1	ADC1_DM1								
•	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
•	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
•	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
•	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
•	VDDA	VDDA	VDDA								

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
•	VREFH	VREFH	VREFH								
•	VREFL	VREFL	VREFL								
•	VSSA	VSSA	VSSA								
•	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
•	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
•	/CMP2_IN3/ ADC1_SE23		/CMP2_IN3/ ADC1_SE23								
•	XTAL32	XTAL32	XTAL32								
•	EXTAL32	EXTAL32	EXTAL32								
•	VBAT	VBAT	VBAT								
•	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_ b		
•	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX			EWM_IN		
•	PTE26	DISABLED		PTE26		UART4_CTS _b			RTC_CLKO UT	USB_CLKIN	
•	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS _b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
•	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
•	PTA2	JTAG_TDO/ TRACE_SW O/EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SW O	EZP_DO
•	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS _b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
•	PTA4	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4		FTM0_CH1				NMI_b	EZP_CS_b
•	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_BC LK	JTAG_TRST	
•	PTA10	DISABLED		PTA10		FTM2_CH0			FTM2_QD_P HA	TRACE_D0	
•	PTA11	DISABLED		PTA11		FTM2_CH1			FTM2_QD_P HB		
•	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD	FTM1_QD_P HA	
•	PTA13	CMP2_IN1	CMP2_IN1	PTA13	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_P HB	
•	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_TX_BC LK		
•	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD		
•	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS _b			I2S0_RX_FS		

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Pinout

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
•	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS _b			I2S0_MCLK	I2S0_CLKIN	
•	VDD	VDD	VDD								
•	VSS	VSS	VSS								
•	PTA18	EXTAL	EXTAL	PTA18		FTM0_FLT2	FTM_CLKIN 0				
•	PTA19	XTAL	XTAL	PTA19		FTM1_FLT0	FTM_CLKIN 1		LPT0_ALT1		
•	RESET_b	RESET_b	RESET_b								
•	PTA24	DISABLED		PTA24					FB_A29		
•	PTA25	DISABLED		PTA25					FB_A28		
•	PTA26	DISABLED		PTA26					FB_A27		
•	PTA27	DISABLED		PTA27					FB_A26		
•	PTA28	DISABLED		PTA28					FB_A25		
•	PTA29	DISABLED		PTA29					FB_A24		
•	PTB0	/ADC0_SE8/ ADC1_SE8/ TSI0_CH0	/ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0	I2C0_SCL	FTM1_CH0			FTM1_QD_P HA		
•	PTB1	/ADC0_SE9/ ADC1_SE9/ TSI0_CH6	/ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_P HB		
•	PTB2	/ ADC0_SE12/ TSI0_CH7	/ ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS _b			FTM0_FLT3		
•	PTB3	/ ADC0_SE13/ TSI0_CH8	/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS _b			FTM0_FLT0		
•	PTB6	/ADC1_SE12	/ADC1_SE12	PTB6				FB_AD23			
•	PTB7	/ADC1_SE13	/ADC1_SE13	PTB7				FB_AD22			
•	PTB8			PTB8		UART3_RTS _b		FB_AD21			
•	PTB9			PTB9	SPI1_PCS1	UART3_CTS _b		FB_AD20			
•	PTB10	/ADC1_SE14	/ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
•	PTB11	/ADC1_SE15	/ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
•	VSS	VSS	VSS								
•	VDD	VDD	VDD								
•	PTB16	/TSI0_CH9	/TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
•	PTB17	/TSI0_CH10	/TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_ b		
•	PTB18	/TSI0_CH11	/TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_BC LK	FB_AD15	FTM2_QD_P HA		
•	PTB19	/TSI0_CH12	/TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_P HB		
•	PTB20			PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
•	PTB21			PTB21	SPI2_SCK			FB_AD30	CMP1_OUT		
•	PTB22			PTB22	SPI2_SOUT			FB_AD29	CMP2_OUT		
•	PTB23			PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28			
•	PTC0	/ ADC0_SE14/ TSI0_CH13	/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD	FB_AD14			
•	PTC1	/ ADC0_SE15/ TSI0_CH14	/ ADC0_SE15/ TSI0_CH14	PTC1	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13			
•	PTC2	/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12			
•	PTC3	/CMP1_IN1	/CMP1_IN1	PTC3	SPI0_PCS1	UART1_RX	FTM0_CH2	FB_CLKOUT			
•	VSS	VSS	VSS								
•	VDD	VDD	VDD								
•	NC										
•	PTC4			PTC4	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
•	PTC5			PTC5	SPI0_SCK		LPT0_ALT2	FB_AD10	CMP0_OUT		
•	PTC6	/CMP0_IN0	/CMP0_IN0	PTC6	SPI0_SOUT	PDB0_EXTRG		FB_AD9			
•	PTC7	/CMP0_IN1	/CMP0_IN1	PTC7	SPI0_SIN			FB_AD8			
•	PTC8	/ ADC1_SE4b/ CMP0_IN2	/ ADC1_SE4b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN	FB_AD7			
•	PTC9	/ ADC1_SE5b/ CMP0_IN3	/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
•	PTC10	/ ADC1_SE6b/ CMP0_IN4	/ ADC1_SE6b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
•	PTC11	/ADC1_SE7b	/ADC1_SE7b	PTC11	I2C1_SDA		I2S0_RXD	FB_RW_b			
•	PTC12			PTC12		UART4_RTS_b		FB_AD27			
•	PTC13			PTC13		UART4_CTS_b		FB_AD26			
•	PTC14			PTC14		UART4_RX		FB_AD25			
•	PTC15			PTC15		UART4_TX		FB_AD24			
•	VSS	VSS	VSS								
•	VDD	VDD	VDD								
•	PTC16			PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_BLS15_8_b			
•	PTC17			PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/			

121 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
								FB_BE31_24_BLS7_0_b			
•	PTC18			PTC18		UART3_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_BLS23_16_b			
•	PTC19			PTC19		UART3_CTS_b		FB_CS3_b/ FB_BE7_0_BLS31_24_b	FB_TA_b		
•	PTD0			PTD0	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b			
•	PTD1	/ADC0_SE5b	/ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b			
•	PTD2			PTD2	SPI0_SOUT	UART2_RX		FB_AD4			
•	PTD3			PTD3	SPI0_SIN	UART2_TX		FB_AD3			
•	PTD4			PTD4	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
•	PTD5	/ADC0_SE6b	/ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
•	PTD6	/ADC0_SE7b	/ADC0_SE7b	PTD6	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
•	VSS	VSS	VSS								
•	PTD7			PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
•	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16		
•	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17		
•	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18		
•	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_CLKIN		FB_A19		
•	PTD12	DISABLED		PTD12	SPI2_SCK		SDHC0_D4		FB_A20		
•	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		
•	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
•	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		

8.2   K20 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

NOTE
The 121 MAPBGA ballmap assignments are currently being developed.

9 Revision History

The following table provides a revision history for this document.

Table 45. Revision History

Rev. No.	Date	Substantial Changes
1	11/2010	Initial public revision
2	3/2011	Many updates throughout
3	3/2011	Added sections that were inadvertently removed in previous revision
4	3/2011	Reworded I_{IC} footnote in "Voltage and Current Operating Requirements" table. Added paragraph to "Peripheral operating requirements and behaviors" section. Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.

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